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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Dual Input, Power Path, 3A Switching Mode Charger with FG

General Description

The MAX77818 is a high-performance companion PMIC for the latest smartphones and tablet computers. The PMIC includes a dual input, smart power path 3.0A switch mode charger with reverse boost capability and adapter input protection up to $16V_{DC}$ withstand, proprietary ModelGaugeTM (m5) fuel gauge technology.

The switch mode battery charger's operating frequency is 4MHz and includes integrated, low-loss switches to provide the industry's smallest L/C size, lowest heat, and fastest battery charging programmable up to 3.0A. The charger has two inputs that accept adapter/USB (CHIN) and/or wireless type inputs (WCIN). The wireless input can simultaneously charge the battery while powering USB-OTG type accessories. The USB-OTG output provides true-load disconnect and is protected by an adjustable output current limit.

The battery charger includes smart power path and I²C adjustable settings to accommodate a wide range of battery sizes and system loads. When external power is applied from either input, battery charging is enabled. With a valid input power source (adapter or wireless charger), the BYP pin voltage is equal to the input voltage minus resistive voltage drop. During battery-only reverse boost operation, the BYP output can be regulated with the reverse boost feature and provides up to 5V at 1.5A and requires no additional inductor, allowing the MAX77818 to power USB OTG accessories.

The switching charger is designed with a special CC, CV, and die temperature regulation algorithm. ModelGauge (m5) provides accurate battery fuel gauging without calibration and operates with extremely low battery current.

The safeout LDO drive system USB interface devices.

The MAX77818 features a $I^{2}C$ revision 3.0-compatible serial interface that comprises a bidirectional serial data line (SDA) and a serial clock line (SCL).

Applications

- Smartphones and Tablets
- Other Handheld Devices

Benefits and Features

- Dual Input Switchmode Battery Charger
 Adapter/USB Input
 - Up to 13.4V Adapter Charging
 - Up to 4.0A rated, Input Current Protection (Programmable)
 - · Wireless Charging Input
 - Up to 5.9V Wireless Charging
 - Up to 1.26A, Input Current Protection (Programmable)
 - Support USB-OTG Accessories
 - Battery Charge Current, Up to 3.0A
 - No Sense Resistor
 - CC, CV, and Die Temperature Control
 - Integrated Battery True-Disconnect FET
 - $R_{DS}(ON) = 12.8m\Omega$
 - Rated Up to 4.5A_{RMS}, Discharge Current Limit (Programmable)
 - Reverse Boost Capability
 - Supports USB-OTG Accessories
 - Up to 5.1V/1.5A
 - · Adjustable OCP
- ModelGauge (m5) Battery Fuel Gauge
 - + \pm 1% SOC Accuracy, No Calibration Cycles, Very Low I_Q
 - Time-to-Empty and Time-to-Full Prediction
- Two Safeout LDOs
- I²C Serial Interface
- 72-Bump. 3.867mm x 3.608mm WLP with 0.4mm Pitch

Ordering Information appears at end of data sheet.

ModelGauge is a trademark of Maxim Integrated Products, Inc.



Dual Input, Power Path, 3A Switching Mode Charger with FG

Absolute Maximum Ratings

Switching Charger

| CHGIN to GND | 0.3V to +16V |
|------------------------------------|----------------------------------|
| BYP to GND | 0.3V to +16V |
| WCIN, PVL, AVL, BAT_SP, BATT, SYS, | |
| DETBATB to GND | 0.3V to +6V |
| BST to PVL | 0.3V to +16V |
| BST to CHGLX | 0.3V to +6V |
| WCINOKB, INOKB to GND | 0.3V to SYS+0.3V |
| BAT_SN, CHGPG to GND | 0.3V to +0.3V |
| CHGLX, CHGPG Continuous Current | 3.5A _{RMS} |
| SYS, BATT Continuous Current | 4.5A _{RMS} |
| CHGIN, BYP Continuous Current | 4.0A _{RMS} |
| WCIN Continuous Current | 1.5A _{RMS} |
| Fuel Gauge | |
| V _{BFG} , to GND | 0.3V to +2.2V |
| THMB, THM to GND | -0.3V to V _{AVL} + 0.3V |

| Safeout LDOs | |
|--|-------------------------------|
| SAFEOUT1, SAFEOUT2 to GND | 0.3V to 6V |
| SAFEOUT1, SAFEOUT2 Continuous Curre | ent100mA |
| I ² C and Interface Logic | |
| V _{IO} to GND | 0.3V to +6V |
| SDA, SCL to GND | 0.3V to V _{IO} +0.3V |
| INTB to GND0.3 | $3V$ to V_{SYS} A + 0.3V |
| TEST_, V _{CCTEST} , SYS_ to GND | 0.3V to +6V |
| GND_ to GND | 0.3V to +0.3V |
| Thermal Ratings | |
| Operating Temperature Range | 40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | 65°C to +150°C |
| Soldering Temperature (reflow) | +260°C |
| Continuous Power Dissipation (T _A = +70°C | 2) |
| (derate 28.9mW/°C with 4L board, above | e 70°C)2.31W |
| | |

CHGLX has internal clamp diodes to CHGPG and BYP. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Package Thermal Characteristics (Note 1)

WLP

Junction-to-Ambient Thermal Resistance (θ_{JA})34.6°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

General Electrical Characteristics

 $(V_{SYS} = +3.7V, C_{HGIN} = 0V, V_{IO} = 1.8V, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------------|--------|---|------|------|------|-------|
| Shutdown Supply Current (DATT) | | All circuits off | | 22 | 50 | |
| Shuldown Supply Current (BATT) | | V _{BATT} = 3.6V | | 23 | 50 | μΑ |
| No Lood Supply Current (DATT) | | Fuel gauge is on | | 50 | 100 | |
| No Load Supply Culterit (BATT) | | All other circuits off, V_{BATT} = 3.6V | | 50 | 100 | μΑ |
| SYS INPUT RANGE | | | | | | |
| SYS Operating Voltage | | Guaranteed by V _{SYSUVLO} and V _{SYSOVLO} | 2.8 | | 5 | V |
| SYS Undervoltage Lockout Threshold | | V _{SYS} falling, 200mV hysteresis | 2.45 | 2.5 | 2.55 | V |
| SYS Overvoltage Lockout Threshold | | V _{SYS} rising, 200mV hysteresis | 5.2 | 5.36 | 5.52 | V |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Electrical Characteristics (continued)

General Electrical Characteristics

 $(V_{SYS} = +3.7V, C_{HGIN} = 0V, V_{IO} = 1.8V, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | ТҮР | MAX | UNITS |
|--|---------------------|---------------------------------|--------------------------|---------------------------|--------------------------|-------|
| LOGIC AND CONTROL INPUT | | | | | | |
| SCL, SDA Input Low Level | | T _A = +25°C | | | 0.3 x V _{IO} | V |
| SCL, SDA Input High Level | | T _A = +25°C | 0.7 x V _{IO} | | | V |
| SCL, SDA Input Hysteresis | | T _A = +25°C | | 0.05 x V _{IO} | | V |
| SCL, SDA Logic Input Current | | V _{IO} = 3.6V | -10 | | +10 | μA |
| SCL, SDA Input capacitance | | | | 10 | | pF |
| SDA Output Low Voltage | | Sinking 20mA | | | 0.4 | V |
| Output Low Voltage INTB | | I _{SINK} = 1mA | | | 0.4 | V |
| I ² C-COMPATIBLE INTERFACE TIM | MING FOR STA | NDARD, FAST, AND FAST-MODE PLUS | (Note 2) | | | |
| Clock Frequency | f _{SCL} | | | | 1000 | kHz |
| Hold Time (Repeated) START Condition | ^t HD;STA | | 0.26 | | | μs |
| CLK Low Period | t _{LOW} | | 0.5 | | | μs |
| CLK High Period | thigh | | 0.26 | | | μs |
| Setup Time Repeated START Condition | ^t SU;STA | | 0.26 | | | μs |
| DATA Hold Time | t _{HD:DAT} | | 0 | | | μs |
| DATA Valid Time | t _{VD:DAT} | | | | 0.45 | μs |
| DATA Valid Acknowledge Time | t _{VD:ACK} | | | | 0.45 | μs |
| DATA Setup Time | t _{SU;DAT} | | 50 | | | ns |
| Setup Time for STOP Condition | t _{SU;STO} | | 0.26 | | | μs |
| Bus Free Time Between STOP and START | ^t BUF | | 0.5 | | | μs |
| Pulse Width of Spikes that Must Be Suppressed by the Input Filter | | (Note 3) | | 50 | | ns |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Electrical Characteristics (continued)

General Electrical Characteristics

 $(V_{SYS} = +3.7V, C_{HGIN} = 0V, V_{IO} = 1.8V, T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| DADAMETED | SYMBOL | CONDITIONS | C _B = 100pF | | | |
|---|---------------------|------------------------|------------------------|-----|-----|-------|
| PARAMETER | STMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
| I ² C-COMPATIBLE INTERFACE TIN | IING FOR HS MOI | DE (Note 2) | | | | |
| Clock Frequency | f _{SCL} | | | | 3.4 | MHz |
| Setup Time Repeated START Condition | ^t SU;STA | | 160 | | | ns |
| Hold Time (Repeated) START Condition | ^t HD;STA | | 160 | | | ns |
| CLK Low Period | tLOW | | 160 | | | ns |
| CLK High Period | t _{HIGH} | | 60 | | | ns |
| DATA Setup time | t _{SU;DAT} | | 10 | | | ns |
| DATA Hold Time | t _{HD:DAT} | | 0 | | | ns |
| SCL Rise Time | t _{RCL} | T _A = +25°C | 10 | | 40 | ns |
| Rise Time of SCL Signal After a Repeated START condition and After an Acknowledge Bit | ^t RCL1 | T _A = +25°C | 10 | | 80 | ns |
| SCL Fall Time | t _{FCL} | T _A = +25°C | 10 | | 40 | ns |
| SDA Rise Time | t _{RDA} | T _A = +25°C | 10 | | 80 | ns |
| SDA Fall Time | t _{FDA} | T _A = +25°C | | | 80 | ns |
| Setup Time for STOP Condition | tsu;sто | | 160 | | | ns |
| Pulse Width of Spikes that Must be Suppressed by the Input Filter | | | | 10 | | ns |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------------------------|---|----------------------------|----------------------------|----------------------------|-------|
| CHGIN INPUT | | | | | | |
| CHGIN Operating Voltage Range | | Operating voltage | 3.2 | | V _{OVLO} | V |
| WCIN Operating Voltage Range | | Operating voltage | 3.2 | | V _{OVLO} | V |
| CHGIN Overvoltage Threshold (Note 4) | V _{CHGIN-OVLO} | V _{CHGIN} rising | 13.4 | 13.7 | 14 | V |
| WCIN Overvoltage Threshold (Note 4) | Vwcin-ovlo | V _{WCIN} rising | 5.9 | | 6 | V |
| WCIN Overvoltage Threshold Hysteresis | VWCINH-OVLO | V _{WCIN} falling | | 100 | | mV |
| CHGIN Overvoltage Threshold Hysteresis | V _{CHGINH-OVLO} | V _{CHGIN} falling | | 300 | | mV |
| | Ŧ | VWCIN/BUS_DET rising, 100mV overdrive, not production tested | | 10 | | us |
| | ^I D-OVLO | V _{WCIN/BUS_DET} falling, 100mV overdrive, not production tested | | 20 | | us |
| WCIN/CHGIN to GND Minimum Turn-On Threshold Range (Note 4) | Vwcin/chgin_ uvlo | V _{CHGIN} rising, 100mV hysteresis, programmable at 4.5V, 4.9V, 5.0V, 5.1V, WCIN input is disabled when valid CHGIN input is detected | 4.5 | | 5.1 | V |
| WCIN/CHGIN to GND Minimum Turn-On Threshold Accuracy | V _{WCIN/CHGIN} _ UVLO | V _{WCIN/CHGIN} rising, 4.5V setting | 4.4 | 4.5 | 4.6 | V |
| WCIN/CHGIN to SYS Minimum Turn-On Threshold (Note 4) | V _{WCIN/} CHGIN2SYS | V _{CHGIN} rising, 50mV hysteresis, WCIN input is disabled when valid CHGIN input is detected | V _{SYS} + 0.12 | V _{SYS} + 0.20 | V _{SYS} + 0.28 | V |
| WCIN/CHGIN Turn-On Threshold Delay | T _{D-UVLO} | Not production tested | | 10 | | us |
| WCIN/CHGIN Adaptive Current Regulation Threshold Range (Note 5) | V _{WCIN/} CHGIN_REG | Programmable at 4.3V, 4.7V, 4.8V, 4.9V | 4.3 | | 4.9 | V |
| WCIN/CHGIN Adaptive Voltage Regulation Threshold Accuracy | V _{WCIN} / CHGIN_REG | 4.9V setting | 4.8 | 4.9 | 5 | V |
| CHGIN Current-Limit Range | | Programmable, 500mA default, factory programmable option of 100mA, production tested at 100mA, 500mA, 1000mA, 1800mA, 4000mA settings only | 0.1 | | 4 | A |
| WCIN Current-Limit Range | | Programmable, 500mA default, factory programmable option of 100mA, production tested at 100mA, 250mA, 500mA, 1000mA settings only | 0.06 | | 1.26 | A |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---------------------|--|--|-------|------|-------|
| | | V _{WCIN/CHGIN} = 2.4V, the input is undervoltage and R _{INSD} is the only loading | | 0.075 | | |
| WCIN or CHGIN Supply Current | I _{IN} | V _{WCIN/CHGIN} = 5.0V, charger disabled 0.17 0.5 | | 0.5 | mA | |
| | | $V_{WCIN/CHGIN}$ = 5.0V, charger enabled, V_{SYS} = V_{BATT} = 4.5V, (no switching, battery charged) | | 2.7 | 4 | |
| VWCIN or VCHGIN Input Current Limit | | V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 100mA input current setting, T_A = +25°C | 90 | 102 | 108 | |
| | luu uu . | V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 500mA Input current setting, T_A = +25°C | 462.5 | 487.5 | 500 | m۸ |
| | INLIMIT | V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1000mA Input current setting, T_A = +25°C | 950 | 975 | 1000 | |
| | | V_{WCIN} or V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1000mA input current setting, T_A = 0°C to +85°C | 926 | 975 | 1024 | |
| | | V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = +25°C | 1710 | 1755 | 1800 | |
| | | V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 1800mA input current setting, T_A = 0°C to +85°C | 1667 | 1755 | 1843 | |
| | INLIMIT | V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = +25°C | 3800 | 3900 | 4000 | mA |
| | | V_{CHGIN} = 5.0V, charger enabled, V_{BATT} = 3.8V, 4000mA input current setting, T_A = 0°C to +85°C | H_{GIN} = 5.0V, charger enabled, ATT = 3.8V, 4000mA input current 3705 3900 40 ting, T _A = 0°C to +85°C | | 4095 |)95 |
| WCIN, CHGIN Self-Discharge Down to UVLO Time | t _{INSD} | Time required for the charger input to cause a 10μ F input capacitor to decay from 6.0V to 4.3V. | | 100 | | ms |
| WCIN, CHGIN Input Self-Discharge Resistance | R _{INSD} | For CHGIN, this resistor is disconnected from the CHGIN pin during MUIC microphone mode | | 35 | | kΩ |
| WCINOK/CHGINOK to Start Switching | ^t START | | | 150 | | ms |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | CONDITIO | NS | MIN | TYP | MAX | UNITS |
|--------------------------------|--|---|------------------------|-----|--------|------|-------|
| SWITCH IMPEDANCES AND LEA | KAGE CURRENTS | · | | | | | |
| CHGIN to BYP Resistance | R _{IN2BYP} | Bidirectional | | | 0.0144 | 0.04 | Ω |
| WCIN to BYP Resistance | R _{WCIN2BYP} | | | | 0.093 | 0.26 | Ω |
| CHGLX High-Side Resistance | R _{HS} | | | | 0.0327 | 0.1 | Ω |
| CHGLX Low-Side Resistance | R _{LS} | | | | 0.0543 | 0.14 | Ω |
| BATT to SYS Dropout Resistance | R _{BAT2SYS} | | | | 0.0128 | 0.04 | Ω |
| CHGIN to BATT Dropout | 5 | Calculation estimates a resistance (R _L) | 0.04Ω inductor | | 0.0000 | | _ |
| Resistance | RIN2BAT | RIN2BAT RIN2BAT = RIN2BYP + RHS + RL + RBAT2SYS | | | 0.0999 | | Ω |
| | | CHGLX = CHGPG or | T _A = +25°C | | 0.01 | 10 | μA |
| | | BYP | T _A = +85°C | | 1 | | μA |
| PST Lookage Current | | $\lambda = $ | T _A = +25°C | | 0.01 | 10 | μA |
| DST Leakage Current | | v _{BST} – 5.5v | T _A = +85°C | | 1 | | μA |
| BYD Lookago Current | | $V_{BYP} = 5.5V, V_{CHGIN}$ | T _A = +25°C | | 0.01 | 10 | μA |
| DTP Leakage Current | | charger disabled | T _A = +85°C | | 1 | | μA |
| WCIN Leakage Current | | $V_{BYP} = 0V,$ | T _A = +25°C | | 0.01 | | μA |
| | $V_{CHGIN} = 0.00, T_{A} = -100, T_{A} = -1$ | | T _A = +85°C | | 1 | | μA |
| SYS Leakage Current | | $V_{SYS} = 0V,$ $V_{DATT} = 4.2V$ | T _A = +25°C | | 0.01 | 10 | μA |
| | | charger disabled | T _A = +85°C | | 1 | | μA |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | CONDITIO | NS | MIN | ТҮР | MAX | UNITS |
|---|--|--|--------------------------------------|------|------|------|-------|
| | | $V_{CHGIN} = 0V,$ $V_{SYS} = 0V,$ | T _A = +25°C | | 20 | 30 | μA |
| | | QBAT is off | T _A = +85°C | | 20 | | μA |
| | Имват | V _{CHGIN} = 0V, V _{BATT} = 4.2V, QBAT is on main-battery | T _A = +25°C | | 15.3 | | μA |
| | | overcurrent protection disabled | T _A = +85°C | | 15.3 | | μA |
| BATT Quiescent Current (I _{SYS} = 0A, I _{BYP} = 0A) | | V _{CHGIN} = 0V, V _{BATT} = 4.2V, QBAT is on, main-battery overcurrent protection enabled | T _A = +25°C | | 20 | | μA |
| | | | T _A = +85°C | | 20 | | μA |
| | | V _{SYS} = 4.2V, | T _A = +25°C | | 0.01 | 10 | μA |
| | | disabled | T _A = +85°C | | 1 | | μA |
| | V _{CHGIN} = 5V, V _{BATT} = 4.2V, QBA is off, main-battery overcurrent protection disabled, Charger is enabled but in its do mode | $V_{CHGIN} = 5V,$ $V_{BATT} = 4.2V, QBAT$ is off, main-battery | T _A = +25°C | | 3 | 10 | μA |
| | | disabled, Charger is enabled but in its done mode | T _A = +85°C | | 3 | | μA |
| CHARGER DC-DC BUCK | 1 | 1 | 1 | | | | 1 |
| Minimum On-Time | t _{ON-MIN} | | | | 75 | | ns |
| Minimum Off-Time | toff | | | | 75 | | ns |
| | | T _A = 0°C to +85°C | I _{LIM} = 00 (3.00A out) | 4.15 | 5.05 | 5.95 | |
| | | $I_{ND} = 0 (0.47 \mu H)$ inductor option) | I _{LIM} = 01 (2.75A out) | | 4.75 | | Δ |
| | | Production tested at $I_{LIM} = 00$ setting | I _{LIM} = 10 (2.50A out) | | 4.45 | | |
| Current Limit | | (Note 7) | I _{LIM} = 11 (2.25A out) | | 4.15 | | |
| (Note 6) | 'LIM | $T_{A} = 0^{\circ}C \text{ to } +85^{\circ}C$ | I _{LIM} = 00 (3.00A out) | | 4.60 | | |
| | | $I_{ND} = 1$ (1.0µH inductor option) | I _{LIM} = 01 (2.75A out) | | 4.30 | | |
| | | Production tested at I _{LIM} = 11 setting (Note 7) | I _{LIM} = 10 (2.50A out) | | 4.00 | | |
| | | | I _{LIM} = 11 (2.25A out) | 3.00 | 3.70 | 4.40 | |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | CONDI | TIONS | MIN | ТҮР | MAX | UNITS |
|--|------------------------|---|--|-------|------|-------|-------|
| REVERSE BOOST | | • | | | | | |
| BYP Voltage Adjustment Range | | 2.5V < V _{BATT} < 4.5V 3V to 5.75V, product 5.0V and 5.75V setti | /. Adjustable from ion tested at 3V, ngs | 3 | | 5.75 | V |
| Reverse Boost Quiescent Current | I _{BYP} | Not switching: output forced 200mV above its target regulation voltage | | | 1150 | | μA |
| Reverse Boost BYP Voltage in OTG Mode | V _{BYP.OTG} | 5.1V setting | | 4.94 | 5.1 | 5.26 | V |
| CHGIN Voltage in OTG Mode | V _{CHGIN.OTG} | Mode = 0x05 or 0x0F, WCIN switch is on, VCHGIN_REG = 4.9V, RIN2WCIN + RDSCHGIN < 300mI, OTG load current ≤ 450mA | | 4.75 | | | V |
| | | | OTG_ILIM = 00 | 500 | | 550 | mA |
| | | 3.4V < V _{BATT} OTG_ILI < 4.5V, T _A = +25°C OTG_ILI | OTG_ILIM = 01 | 900 | | 990 | mA |
| CHGIN Output Current Limit | ICHGIN.OTG.LIM | | OTG_ILIM = 10 | 1200 | | 1320 | mA |
| | | | OTG_ILIM=11 | 1500 | | 1650 | mA |
| Reverse Boost Output Voltage | | Discontinuous inductor current (i.e., skip mode) Continuous inductor current | | | ±150 | | mV |
| Кірріе | | | | | ±150 | | mV |
| CHARGER | | | | | | | |
| BATT Regulation Voltage Range | V _{BATTREG} | Programmable in 25 production tested at only. | mV steps (4 bits), 3.65V and 4.4V | 3.65 | | 4.7 | V |
| | | 2.05) (and 4.7) (| T _A = +25°C | -0.75 | | +0.75 | % |
| Accuracy | | settings | T _A = 0°C to +85°C | -1 | | +1 | % |
| Fast-Charge Current Program Range | | 0A to 3.0A in 50mA s tested at 500,1000, 2 settings | teps, production 2000 and 3000mA | 0 | | 3 | A |
| | | Programmed currents ≥ 500mA, V _{BATT} > V _{SYSMIN} (short mode), | T _A = +25°C | -2.5 | | +2.5 | % |
| Fast-Charge Current Accuracy | | production tested at 500mA, 800mA, 1000mA, 2000mA, 3000mA settings | T _A = 0°C to +85°C | -5 | | +5 | % |
| | | Programmed currents ≥ 500mA, V _{BATT} < V _{SYSMIN} (LDO mode), production test at 800mA | | -10 | | +10 | % |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | cc | NDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|---|------------------------------------|-------|------|-------|-------|
| | | | Programmed for 3.0A | 2925 | 3000 | 3075 | mA |
| East Charge Currents | | T _A = +25°C, P | Programmed for 2.0A | 1950 | 2000 | 2050 | mA |
| Fast-Gharge Guirents | 'FC | | Programmed for 1.0A | 975 | 1000 | 1025 | mA |
| | | | Programmed for 0.5A | 487.5 | 500 | 512.5 | mA |
| Low-Battery Prequalification Threshold | V _{PQLB} | V_{BATT} rising | | 2.8 | 2.9 | 3 | V |
| Dead-Battery Prequalification Threshold | V _{PQDB} | V_{BATT} rising | | 1.9 | 2 | 2.1 | V |
| Prequalification Threshold Hysteresis | V _{PQ-H} | Applies to both $V_{\mbox{PQLB}}$ and $V_{\mbox{PQDB}}$ | | | 100 | | mV |
| Low-Battery Prequalification Charge Current | I _{PQLB} | Default setting = disabled | | 75 | 100 | 140 | mA |
| Dead-Battery Prequalification Charge Current | I _{PQDB} | | | 40 | 55 | 80 | mA |
| Charger Restart Threshold Range | V _{RSTRT} | Adjustable, 100 also be disabled | , 150, and 200; it can I | 100 | 150 | 200 | mV |
| Charger Restart Deglitch Time | | 10mV overdrive | , 100ns rise time | | 130 | | ms |
| Top-Off Current Program Range | | Programmable 1 8 steps. | from 100 to 350mA in | 100 | | 350 | mA |
| Top-Off Current Accuracy | | Gain | | | | 5 | % |
| (Note 8) | | Offset | | | | 20 | mA |
| Charge Termination Deglitch Time | t _{TERM} | 2mV overdrive, 100ns rise/fall time | | | 30 | | ms |
| Charger State Change Interrupt Deglitch Time | tSCIDG | Excludes transit watchdog timer | ion to timer fault state, state | | 30 | | ms |
| Charger Soft-Start Time | tss | | | | 1.5 | | ms |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | CON | IDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------|---|--|-----|-------|------|-------|
| SMART POWER SELECTOR | | · | | | | | |
| | | I _{BATT} = 10mA | | | 30 | | mV |
| BATT to SYS Reverse Regulation | Vacazo | I _{BATT} = 1A | I _{BATT} = 1A | | 60 | | mV |
| Voltage | *BSREG | Load regulation d regulation mode | uring the reverse | | 30 | | mV/A |
| Minimum SYS Voltage Accuracy | V _{SYSMIN} | Programmable fro 100mV steps, V _B 3.4V and 3.7V se | om 3.4V to 3.7V in _{ATT} = 2.8V, tested at ttings | -3 | | 3 | % |
| Maximum SYS Voltage | V | The maximum system voltage: VsysMAX = VBATREG + RBAT2SYS X IBATT | V _{BATREG} = 4.2V, I _{BATT} = 3.0A | | 4.245 | 4.32 | V |
| | V SYSMAX | The maximum system voltage: V _{SYSMAX} = V _{BATREG} + R _{BAT2SYS} x I _{BATT} . | V _{BATREG} = 4.7V, I _{BATT} = 3.0A | | 4.745 | 4.82 | V |
| WATCHDOG TIMER | | | | | | | |
| Watchdog Timer Period | t _{WD} | | | 80 | | | S |
| Watchdog Timer Accuracy | | | | -20 | 0 | +20 | % |
| CHARGE TIMER | | | | | | | |
| Prequalification Time | tPQ | Applies to both lo prequalification an prequalification m | w-battery nd dead-battery lodes | | 35 | | min |
| Fast-Charge Constant Current + Fast-Charge Constant Voltage Time | t _{FC} | Adjustable from 4hrs to 16hrs in 2 hour steps including a disable setting | | | 8 | | hrs |
| Top-Off Time | t _{TO} | Adjustable from 0min to 70min in 10min steps | | | 30 | | min |
| Timer Accuracy | | | | -20 | | +20 | % |
| AVL FILTER | | | | | | | |
| Internal AVL Filter Resistance | | | | | 12.5 | | Ω |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | | |
|---|--------------------|---|-----|------------------------------------|-----|-------|--|--|
| THERMAL FOLDBACK | | | | | | | | |
| Junction Temperature Thermal Regulation Loop Setpoint Program Range | T _{JREG} | Junction temperature when charge current is reduced. Programmable from +85°C to +130°C in 15°C steps, default value is +100°C | 85 | | 130 | °C | | |
| Thermal Regulation Gain | Atjreg | The charge current is decreased 6.7% of the fast charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.0A is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 500mA, this slope is valid for charge current reductions down to 100mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is 20°C above the programmed loop set point. | | -150 | | mA/°C | | |
| BATTERY OVERCURRENT PRO | TECTION | | | | | | | |
| Battery Overcurrent Threshold Range | IBOVCR | Programmable from 3.0A to 4.5A in 0.25A steps, can be disabled | 3 | | 4.5 | А | | |
| Battery Overcurrent Debounce Time | ^t BOVRC | This is the response time for generating the overcurrent interrupt flag | 3 | 6 | 10 | ms | | |
| Battery Overcurrent Protection Quiescent Current | IBOVRC | | | 3 + I _{BATT} /22000 | | μΑ | | |
| System Power-Up Current | ISYSPU | | 35 | 50 | 80 | mA | | |
| System Power-Up Voltage | V _{SYSPU} | V _{SYS} rising, 100mV hysteresis | 2 | 2.1 | 2.2 | V | | |
| System Power-Up Response Time | ^t syspu | Time required for circuit to activate from an unpowered state (i.e., main-battery hot insertion) | | 1 | | μs | | |
| SYSTEM SELF DISCHARGE WIT | H NO POWER | | | | | | | |
| BATT Self-Discharge Resistor | | | | 600 | | Ω | | |
| SYS Self-Discharge Resistor | | | | 600 | | Ω | | |
| Self-Discharge Latch Time | | | | 300 | | ms | | |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Switching Charger Electrical Characteristics (continued)

 $(V_{CHGIN} = 5V, V_{BATT} = 4.2V, T_A = -40^{\circ}C$ to +85°C, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$. Fast-charge current is set for 1.5A, done current is set for 150mA. Limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------|-------------------------|------------------------|-----|--------------------------|-----|-------|
| DETBATB, INOKB, WCINOKB | | | | | | | |
| DETBATB Logic Threshold | VIH | 4% hysterisis | | | 0.8 x V _{IO} | | V |
| Logic Input Leakage Current | IDETBATB | | | | 0.1 | 1 | μA |
| Output Low Voltage INOKB, WCINOKB | | I _{SINK} = 1mA | | | | 0.4 | V |
| Output High Leakage INOKB, | | | T _A = +25°C | -1 | 0 | +1 | μA |
| WCINOKB | | vSYS - 5.5V | T _A = +85°C | | 0.1 | | μA |

Safeout LDOs Electrical Characteristics

 $(V_{SYS} = 2.8V \text{ to } 4.5V, T_A = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$, typical values are at $T_A = +25^{\circ}\text{C}$, unless otherwise noted. Limits are 100% production tested at $T_A = +25^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------|---|-----|------|-----|-------|
| SAFEOUT1 | | | | | | |
| | | 5V < V _{CHGIN} < 5.5V, I _{OUT} = 10mA, SAFEOUT1 = 01 (default) | 4.8 | 4.9 | 5 | V |
| Output Voltage (Default On) | | SAFEOUT1 = 00 | | 4.85 | | V |
| | | SAFEOUT1 = 10 | | 4.95 | | V |
| | | SAFEOUT1 = 11 | | 3.3 | | V |
| Maximum Output Current | | | 60 | | | mA |
| Output Current Limit | | | 60 | 150 | 320 | mA |
| Dropout Voltage | | V _{CHGIN} = 5V, I _{OUT} = 60mA | | 120 | | mV |
| Load Regulation | | V _{CHGIN} = 5.5V, 30µA < I _{OUT} < 30mA | | 50 | | mV |
| Quiescent Supply Current | | Not production tested | | 72 | | μA |
| Output Capacitor for Stable Operation (Note 9) | | 0μA < I _{OUT} < 30mA, MAX ESR = 50mΩ | | 1 | | μF |
| Minimum Output Capacitor for Stable Operation (Note 9) | | $0\mu A < I_{OUT} < 30mA$, MAX ESR = 50m Ω | | 0.7 | | μF |
| Internal Off-Discharge Resistance | | | | 1200 | | Ω |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Safeout LDOs Electrical Characteristics (continued)

 $(V_{SYS} = 2.8V \text{ to } 4.5V, T_A = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$, typical values are at $T_A = +25^{\circ}\text{C}$, unless otherwise noted. Limits are 100% production tested at $T_A = +25^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------|---|-----|------|-----|-------|
| SAFEOUT2 | | | | | | |
| | | 5V < V _{CHGIN} < 5.5V, I _{OUT} = 10mA, SAFEOUT2 = 01 (default) | 4.8 | 4.9 | 5 | V |
| Output Voltage (Default Off) | | SAFEOUT2 = 00 | | 4.85 | | V |
| | | SAFEOUT2 = 10 | | 4.95 | | V |
| | | SAFEOUT2 = 11 | | 3.3 | | V |
| Maximum Output Current | | | 60 | | | mA |
| Output Current Limit | | | 60 | 150 | 320 | mA |
| Dropout Voltage | | V _{CHGIN} = 5V, I _{OUT} = 60mA | | 120 | | mV |
| Load Regulation | | V _{CHGIN} = 5.5V, 30µA < I _{OUT} < 30mA | | 50 | | mV |
| Quiescent Supply Current | | Not production tested | | 72 | | μA |
| Output Capacitor for Stable Operation (Note 9) | | 0μA < I _{OUT} < 30mA, MAX ESR = 50mΩ | | 1 | | μF |
| Minimum Output Capacitor for Stable Operation (Note 9) | | 0FA < I _{OUT} < 30mA, MAX ESR = 50mΩ | | 0.7 | | μF |
| Internal Off-Discharge Resistance | | | | 1200 | | Ω |

Fuel Gauge Electrical Characteristics

 $(V_{SYS} = 2.8V \text{ to } 4.5V, T_A = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}$, typical values are at $T_A = +25^{\circ}\text{C}$, unless otherwise noted. Limits are 100% production tested at $T_A = +25^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------------|---|------|--------|------|-------|
| | I _{DD0} | Fuel gauge shut down (Note 10) | | 0.5 | | μA |
| Supply Current | I _{DD1} | Fuel gauge active, average with 7.5% ADC duty cycle (Note 10) | | 35 | 70 | μA |
| ADC Duty Cycle | Duty | | | 7.5 | | % |
| Parameter Capture Rate | t _{ACQ} | Period of ADC activation loop | | 0.1758 | | s |
| Regulator Output | V _{BFG} | | 1.5 | 1.8 | 1.98 | V |
| VOLTAGE CHANNEL | | | | | | |
| V _{BATT} Measurement Error | V _{GERR} | V_{BATT} = 2.8V to 4.5V, T_A = +25°C | -7.5 | | +7.5 | mV |
| | | $T_{A} = -40^{\circ}C \text{ to } +85^{\circ}C$ | -20 | | +20 | mV |
| V _{BATT} Measurement Resolution | V _{LSB} | | | 1.25 | | mV |
| V _{BATT} Measurement Range | V _{RANGE} | | 2.8 | | 4.98 | V |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Fuel Gauge Electrical Characteristics (continued)

 $(V_{SYS} = 2.8V \text{ to } 4.5V, T_A = -40^{\circ}\text{C} \text{ to } 85^{\circ}\text{C}, \text{ typical values are at } T_A = +25^{\circ}\text{C}, \text{ unless otherwise noted. Limits are 100% production tested at } T_A = +25^{\circ}\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | ТҮР | MAX | UNITS |
|--|-----------------------|---|---------------------|---------------------------|--------|------------------|-----------------------|
| CURRENT CHANNEL | | | | | | | |
| Current Measurement Resolution | I _{LSB} | | | | 1.25 | | mA |
| Current Measurement Range | IRANGE | | | -3.6 | | +3.6 | Α |
| Current Measurement Offset | IOERR | Long term ave current | erage at zero input | | ±0.25 | | mA |
| Current Measurement Symmetrical Error | I _{SERR} | (Notes 11, 12, | 13) | | 2% | | % |
| | | ±3000mA | | -150 | | +150 | |
| Current Measurement | I _{AERR} | ±1000mA | (Notes 12, 13, 14) | -20 | | +20 | mA |
| | | ±300mA | | -9.5 | | +9.5 | |
| Linear Regulator Mode Current Measurement Error | I _{LRERR} | +1500mA | (Note 15) | -225 | | +225 | mA |
| | | +100mA | | -40 | | +40 | |
| Time-Base Accuracy | t _{ERR} | V _{SYS} = 3.7V at T _A = +25°C | | | ±1 | | 0/ |
| | | $T_A = -40^{\circ}C$ to | +85°C | -3.5 | | +3.5 | /0 |
| THERMAL CHANNEL | | | | | | | |
| Ratiometric Measurement Accuracy, THM | T _{GERR} | (Note 13) | | -0.5 | | +0.5 | % of full scale |
| Ratiometric Measurement Resolution, THM | T _{LSB} | | | | 0.0244 | | % of full scale |
| THMB Output Drive | V _{OH_THMB} | IOH_THMB = - | 0.5mA | V _{AVL} - 0.1 | | | V |
| THMB Precharge Time | ^t PRE_THMB | | | | 12.7 | | ms |
| THMB Operating Range | V _{THMB} | | | 2.8 | | V _{AVL} | V |
| THMB Input Leakage | IIN_THMB | V _{THMB} = 5V | | -1 | | +1 | μA |
| THM Input leakage | I _{IN_THM} | | | -1 | | +1 | μA |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Electrical Characteristics (continued)

- Note 2: Design guidance only, not tested during final test.
- Note 3: Input filters on the SDA and SCL inputs suppress noise spikes of less than 50ns.
- **Note 4:** The CHGIN input must be less than V_{OVLO} and greater than both V_{CHGIN_UVLO} and $V_{CHGIN2SYS}$ for the charger to turn-on. **Note 5:** The input voltage regulation loop decreases the input current to regulate the input voltage at V_{CHGIN_REG} . If the input
- current is decreased to I_{CHGIN_REG_OFF} and the input voltage is below V_{CHGIN_REG}, then the charger input is turned off. **Note 6:** Production tested to ¼ of the threshold with LPM bit = 1 (¼ FET configuration).
- **Note 7:** Production tested in charger DC-DC low-power mode.
- Note 8: Not production tested.
- Note 9: Not production tested.
- Note 10: The total chip supply current includes the charger supply current in addition to the supply current for the fuel gauge.
- **Note 11:** Symmetrical error is the sum of odd order errors in the measured values at two inputs symmetrical around zero; for example, ISERR_0.3A = (Error 0.3A Error -0.3A)/2/0.3A x 100.
- Note 12: Total current measurement error is the sum of the symmetrical and asymmetrical errors. Fuel gauge accuracy is sensitive to asymmetrical error but insensitive to symmetrical error.
- Note 13:Current and ratiometric measurement errors are production tested at V_{SYS} = 3.7V and guaranteed by design at V_{SYS} = 2.8V and 4.5V.
- Note 14:Asymmetrical error is the sum of even order errors in the measured values at two inputs symmetrical around zero; for example IAERR_0.3A = (Error 0.3A + Error -0.3A)/2.
- Note 15: Total linear regulator mode current measurement error is simply the total error with respect to the input. This mode exists for a short duration when charging an empty battery, hence this error has limited consequence.

Dual Input, Power Path, 3A Switching Mode Charger with FG

Pin Configuration



Dual Input, Power Path, 3A Switching Mode Charger with FG

Pin Description

| PIN | NAME | FUNCTION |
|---|---------------------|---|
| A1, A9, C4, C6, E2, E4, E6, F3, F4, G2, H1 | N.C. | No Connection |
| A2 | TEST4 | Test I/O Pin. Ground this pin in the application. |
| A3 | SDA | I ² C Serial Data. Add an external 2.2k Ω pullup resistor to V _{IO} . |
| A4 | SCL | I ² C Serial Clock. Add an external 2.2k Ω pullup resistor to V _{IO} . |
| A5 | WCINOKB | Wireless Charger Input Valid, Active-Low Logic Output Flag. Open-drain, active-low output that indicates when valid voltage is present at WCIN and SYS. |
| A6 | GND_Q | Quiet Ground. Short to GND_A and GND_D. |
| A7, A8 | WCIN | Wireless Charger Input. $6V_{DC}$ protected input pin connected to Wireless charger power source. The wireless charger may be active during OTG mode, or disabled using the WCINSEL bit. Connect a 4.7µF/10V ceramic capacitor from WCIN to GND plane |
| B1 | V _{CCTEST} | Test Mux Supply. Ground this pin in the application. |
| B2 | TEST3 | Test I/O. Ground this pin in the application. |
| B3 | TEST5 | Test I/O. Ground this pin in the application. |
| B4 | TEST6 | Test I/O. Ground this pin in the application. |
| B5 | V _{IO} | Digital I/O Supply Input for I ² C Interface. |
| B6 | DETBATB | Battery Detection Active-Low Input. Connect this pin to the ID pin on the battery pack. If DETBATB is pulled below 80% of the externally applied V_{IO} voltage, this is an indication that the battery is present and the charger starts when valid CHGIN and/or WCIN power is present. If DETBATB is driven high to VIO voltage or left unconnected, this is an indication that the battery is not present and the charger does not start. DETBATB is pulled high to V _{IO} pin through an off-chip pullup resistor. |
| B7 | SAFEOUT2 | Safeout LDO2 Output. Default off. Bypass with a 1µF ceramic capacitor to GND. |
| B8, C7, D7, E8, E9 | BYP | CHGIN Bypass. This pin can see up to OVP limit. Output of adapter Input current Limit block and input to switching charger. BYP is also the boost converter output when the charger is operating in reverse boost mode. Bypass with $2x10\mu$ F/16V ceramic capacitors from BYP to CHGPG ground plane. |
| В9 | SAFEOUT1 | Safeout LDO1 Output. Default 4.9V and on when CHGIN power is valid. Bypass with a $1\mu F$ ceramic capacitor to GND. |
| C1 | TEST1 | Test I/O. Ground this pin in the application. |
| C2 | TEST2 | Test I/O. Ground this pin in the application. |
| C3 | INTB | Interrupt Output. Active-low, open-drain output. Add a 200k Ω pullup resistor to V _{IO} . |
| C5 | INOKB | Charger Input Valid, Active-Low Logic Output Flag. Open-drain output indicates when valid voltage is present at both CHGIN and SYS or WCIN and SYS. |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Pin Description (continued)

| PIN | NAME | FUNCTION |
|-----------------------|------------------|--|
| C8, C9, D8, D9 | CHGIN | Charger Input. The adapter/USB charger input may be active, or disabled using the CHGINSEL bit. Connect a 2.2μ F/16V ceramic capacitor from CHGIN to GND plane. |
| D1–D5 | GND_A | Analog Ground. Short to GND_D and GND_Q. |
| E3 | GND_D | Digital Ground. Short to GND_A and GND_Q. |
| D6 | AVL | Analog Voltage Level. Output of on-chip 5V LDO used to power on-chip, low-noise circuits. Bypass with a 2.2µF/10V ceramic capacitor to GND. Powering external loads from AVL is not recommended, other than pulldown resistors. |
| E1, F2 | SYS_A | Analog SYS Input |
| E5, F5, G5, H5, H6 | SYS | System Power Connection. Connect system loads to this node. Bypass with $2x10\mu$ F ceramic capacitors from SYS to CHGPG ground plane. |
| E7 | PVL | Internal Bias Regulator High-Current Output Bypass. Supports internal noisy and high-current gate drive loads. Bypass to GND with a minimum 10µF/10V ceramic capacitor. |
| F1 | V _{BFG} | 1.8V power supply output for Fuel Gauge. Bypass V_{BFG} with a 0.1µF ceramic capacitor, V_{BFG} is not intended to power external circuitry. |
| F6 | BAT_SN | Battery Negative Differential Sense Connection. Connect to the negative or ground terminal close to the battery. |
| F7 | BST | High-Side FET Driver Supply. Bypass BST to LX with a 0.1µF ceramic capacitor. |
| F8, F9, G8, G9 | CHGLX | Charger Switching Node. Connect the inductor between CHGLX and SYS. |
| G1 | THMB | Pullup Voltage for THM Pin Pullup Resistor. Can be switched to save power. |
| G3, G4, H3, H4 | BATT | Battery Power Connection. Connect to the positive terminal of a single-cell (or parallel cell) Li Ion battery. Bypass BATT to CHGPG ground plane with a 10μ F ceramic capacitor. |
| G6 | BAT_SP | Battery Positive Differential Sense Connection. Connect to the positive terminal close to the battery. |
| G7 | CHGRGSUB | Substrate Charger Ground Connection. Connect with GND_A. |
| H2 | THM | Thermistor Connection. Determines battery temperature using ratiometric measurement. |
| H7–H9 | CHGPG | Charger Power Ground Connection |

Dual Input, Power Path, 3A Switching Mode Charger with FG

Block Diagram



Detailed Description

System Faults

MAX77818 monitors the system for the following faults:

V_{SYS} undervoltage lockout

V_{SYS} overvoltage lockout

V_{SYS} Fault

The system monitors the V_{SYS} node for undervoltage and overvoltage. The following describes the IC behavior if any of these events is to occur.

V_{SYS} Undervoltage Lockout (VSYSUVLO)

When charger input is valid and SYS node falls below SYS UVLO, all charger and fuel gauge O type registers are reset and following happen:

when DEADBAT < SYS < UVLO (= 2.5V), QBAT is on and SYS is shorted to BAT.

when 0 < SYS < DEADBAT (= 2.0V), QBAT is off, but the charger pulls up SYS from BAT with a constant current of 50mA.

When charger input is invalid and battery is present:

when DEADBAT < SYS < UVLO (= 2.5V), QBAT is on and SYS is shorted to BAT.

when 0 < SYS < DEADBAT (= 2.0V), QBAT is off.

V_{SYS} Overvoltage Lockout (VSYSOVLO)

The absolute maximum ratings state that the SYS node withstands up to 6V. The SYS OVLO threshold is set to 5.36V (typ). Ideally, V_{SYS} should not exceed the battery charge termination threshold. Systems must be designed so that V_{SYS} never exceeds 4.8V (transient and stead-state). If the V_{SYS} should exceed $V_{SYSOVLO}$ during a fault, the MAX77818 resets the charger and fuel gauge O type registers.

Dual Input, Power Path, 3A Switching Mode Charger with FG

INTB

The MAX77818 uses one interrupt pin: INTB. The interrupt is meant to indicate to the application processor that the status of MAX77818 has changed. The INTB signal is asserted whenever one or more interrupts are toggled, and those interrupts are not masked. The application processor reads the interrupts in two steps. First, the AP reads the INTSRC register. This is a read-only register that indicates which functional block is generating the interrupt (i.e., charger and FG). Depending on the result of the read, the next step is to read the actual interrupt registers pertaining to the functional block.

For example, if the application processor reads 0x02 from INTSRC register, it means the top-level MAX77818 block has an interrupt generated. The next step is to read the related interrupt register of the MAX77818 functional block.

The INTB pin becomes high (cleared) as soon as the read sequence of the last INT_ register that contains an active interrupt starts. FG interrupts are cleared by setting new threshold values. All interrupts can be masked to prevent the INTB from being asserted for masked interrupts. A mask bit in the INTM register implements masking. The INTSRC register can still provide the actual interrupt status of the masked interrupts, but the INTB pin is not asserted.

Safeout LDO

SAFEOUT1 is enabled by default once charger detection is complete and CHGIN is valid regardless of DETBATB. SAFEOUT2 can also be enabled once the same conditions are met, and the user sets the ENSAFEOUT2 register bit.

Switching Mode Charger

Features:

- Complete Li+/Li-poly battery charger
- Prequalification, constant current, constant voltage
- 55mA dead-battery prequalification
- 100mA low-battery prequalification current
- Adjustable constant current charge
 - OA to 3.0A in 50mA steps
 - ±5% accuracy
- Adjustable charge termination threshold
 - 100mA to 200mA in 25mA steps and 200mA to 350mA in 50mA steps
 - ±5% accuracy
- Adjustable battery regulation voltage
 - 3.625V to 4.700V in 25mV steps
 - ±0.5% accuracy at T = +25°C
 - ±1% accuracy
 - Remote differential sensing
- Synchronous switch-mode design
- Reverse boost mode with adjustable V_{BYP} from 3.0V to 5.8V
- Smart Power Selector™
 - Optimally distributes power between charge adapter, system, and main battery
 - When powered by a charge adapter, the main battery can provide supplemental current to the system
 - The charge adapter and can support the system without a main battery
- No external MOSFETs required
- Dual input
 - Reverse leakage protection prevents the battery leaking current to the inputs
 - 4.0A adapter input
 - 16V withstand, 14V operating
 - Adjustable input current limit (100mA to 4.0A in 33.3mA steps (CHGIN_ILIM), 500mA default)
 - · Support AC-to-DC wall warts and USB adapters
 - 1.26A wireless charger input
 - 6V fault tolerant
 - Adjustable input current limit (60mA to 1.26A in 20mA steps (WCIN_ILIM), 500mA default)

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

Dual Input, Power Path, 3A Switching Mode Charger with FG

- Charge safety timer
 - Selectable: 4hr to 16hr in 2hr steps plus a disable setting
- Die temperature monitor with thermal foldback loop
 - Selectable die temperature thresholds (°C): 70, 85,100, and 115
- Input voltage dropout control allows operation from high-impedance sources. Charge current is reduced so input is not pulled below 4.3V.
- BATT to SYS switch is 12.8mΩ (typ).
- Dead battery detection

- Short-circuit protection
 - Programmable BAT to SYS overcurrent threshold from 3.0A to 4.5A in 0.25A steps plus a disable setting
 - DISIBS bit allows the host to disable the battery to system discharge path to protect against a shortcircuit
 - · SYS short to ground
 - BUCK current is limited by by the ILIM current limit. BATT currents above the programmed by B2SOVRC threshold generate an interrupt. The host can then disable the battery to system discharge path by setting DISIBS.



Figure 1. Simplified Charger Functional Diagram

Dual Input, Power Path, 3A Switching Mode Charger with FG



Figure 2. Main Battery Charger Detailed Functional Diagram

Dual Input, Power Path, 3A Switching Mode Charger with FG

Detailed Description

The MAX77818 includes a full-featured switch-mode charger for a one-cell lithium ion (Li+) or lithium polymer (Li-poly) battery. As shown in Figure 2, the current limit for CHGIN input is independently programmable from 0 to 3.0A in 33.3mA steps allowing the flexibility for connection to either an AC-to-DC wall charger or a USB port. CHGIN current limit default is set between 100mA and 500mA with 500mA being the programmed default.

The synchronous switch-mode DC-DC converter utilizes a high 4.0MHz switching frequency which is ideal for portable devices because it allows the use of small components while eliminating excessive heat generation. The DC-DC has both a buck and a boost mode of operation. When charging the main battery the converter operation as a buck. The DC-DC buck operates from a 3.2V to 14V source and delivers up to 3.0A to the battery. Battery charge current is programmable from 0A to 3.0A. As a boost converter, the DC-DC uses energy from the main battery to boost the voltage at BYP. The boosted BYP voltage is useful to provide the supply the USB OTG voltage.

Maxim's Smart Power Selector architecture makes the best use of the limited adapter power and the battery's power at all times to supply up to 3.0A continuous (4A peak) from the buck to the system. Additionally, supplement mode provides additional current from the battery to the system up to $4.5A_{RMS}$. Adapter power that is not used for the system goes to charging the battery. All power switches for charging and switching the system load between battery and adapter power are included on chip. No external MOSFETs are required.

Maxim's proprietary process technology allows for low-R_{DSON} devices in a small solution size. The total dropout resistance from adapter power input to the battery is 0.0999 Ω (typ) assuming that the inductor has 0.04 Ω of ESR. This 0.0999 Ω typical dropout resistance allows for charging a battery up to 3.0A from a 5V supply. The resistance from the BATT to SYS node is 0.0128 Ω , allowing for low power dissipation and long battery life.

A multitude of safety features ensures reliable charging. Features include a charge timer, watchdog, junction thermal regulation, over/undervoltage protection, and shortcircuit protection.

The BATT to SYS switch has overcurrent protection. See the <u>Main battery Overcurrent Protection</u> section for more information.

Smart Power Selector

The Smart Power Selector architecture is a network of internal switches and control loops that distributes energy between an external power source CHGIN, BYP, SYS, and BATT.

<u>Figure 1</u> shows a simplified arrangement for the smart power selector's power steering switches. <u>Figure 2</u> shows a more detailed arrangement of the smart power selector switches and gives them the following names: Q_{CHGIN} , Q_{HS} , Q_{LS} , and Q_{BAT} .

Switch and Control Loop Descriptions

Input Switch: Q_{CHGIN} provides the input current limit. The input switch is completely on and does not provide forward blocking. As shown in Figure 2, there are SPS control loops that monitor the current through the input switches as well as the input voltage.

DC-DC Switches: Q_{HS} and Q_{LS} are the DC-DC switches that can operate as a buck (step-down) or a boost (step-up). When operating as a buck, energy is moved from BYP to SYS. When operating as a boost, energy is moved from SYS to BYP. SPS control loops monitor the DC-DC switch current, the SYS voltage, and the BYP voltage.

Battery-to-System Switch: Q_{BAT} controls the battery charging and discharging. Additionally Q_{BAT} allows the battery to be isolated from the system (SYS). An SPS control loop monitors the Q_{BAT} current.

Control Bits

MODE configures the Smart Power Selector.

MINVSYS sets the minimum system voltage.

VBYPSET sets the BYP regulation voltage target.

B2SOVRC configures the main battery overcurrent protection.

Energy Distribution Priority:

With a valid external power source:

The external power source is the primary source of energy.

The main battery is the secondary source of energy.

Energy delivery to BYP is the highest priority.

Energy delivery to SYS is the second priority.

Any energy that is not required by BYP or SYS is available to the main battery charger.

With no power source available at CHGIN:

The main battery is the primary source of energy.

Energy delivery to BYP is the highest priority.

BYP includes the CHGIN if they are asked to supply energy in a USB OTG type of application.

Energy delivery to SYS is the second priority.

BYP Regulation Voltage

When the DC-DC is enabled in boost only mode (MODE = 0x08), the voltage from BYP to ground (V_{BYP}) is regulated to VBYPSET.

When the DC-DC is enabled in one of its USB OTG modes (MODE = 0x09 or MODE = 0x0A), V_{BYP} is set for 5.1V (V_{BYP.ORG}).

When the DC-DC is off or in one of its buck modes (MODE = 0x00 or MODE = 0x04 or MODE = 0x05) and there is a valid power source at CHGIN, $V_{BYP} = V_{CHGIN} - I_{CHGIN} \times R_{QCHGIN}$ When the DC-DC is off and there is no valid power source at CHGIN, BYP is connected to SYS with an internal 200 Ω resistor. This 200 Ω resistor keeps BYP biased as SYS and allows for the system to draw very light loads from BYP. IF the system loading on BYP is more than 1.0mA then the DC-DC should be operated in boost mode. Note that the inductor and the high-side switch's body diode are in parallel with the 200 Ω from SYS to BYP.

SYS Regulation Voltage

When the DC-DC is enabled as a buck and the charger is disabled (MODE = 0x04), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and Q_{BAT} is off.

When the DC-DC is enabled as a buck and the charger enabled but in a non-charging state such as done, watch-dog suspend or timer fault (MODE = 0x05 and not charging), V_{SYS} is regulated to V_{BATREG} (CHG_CV_PRM) and Q_{BAT} is off.

When the DC-DC is enabled as a buck and charging in prequalification, fast-charge, or top-off modes (MODE = 0x05 and charging), V_{SYS} is regulated to V_{SYSMIN} when the $V_{BATT} < V_{SYSMIN}$; in this mode the Q_{BAT} switch acts like a linear regulator and dissipates power [P = ($V_{SYSMIN} - V_{BATT}$) x I_{BATT}]. When $V_{BATT} > V_{SYSMIN}$, then $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$; in this mode the Q_{BAT} switch is closed.

In all of the above modes, if the combined SYS and BYP loading exceed the input current limit, then V_{SYS} drops to V_{BATT} - V_{BSREG} and the battery provides supplemental current. If the fuel gauge requests main battery information (voltage and current) during this supplement mode, then the Q_{BAT} switch is closed (V_{SYS} = V_{BATT} - I_{BATT} x R_{BAT2SYS}) during the fuel gauge sample. If the fuel

Dual Input, Power Path, 3A Switching Mode Charger with FG

gauge wants requests continuous samples from the main battery during supplement mode, then the Q_{BAT} switch eventually opens when I_{BATT} decreases below 40mA.

When the DC-DC is enabled as a boost (MODE = 0x08 or 0x09 or 0x0A), then the QBAT switch is closed and V_{SYS} = $V_{BATT} - I_{BATT} \times R_{BAT2SYS}$

Battery Detect Input Pin (DETBATB)

DETBATB is tied to the ID pin of the battery pack. If DETBATB is pulled below 80% of V_{IO} pin voltage, this is an indication that the main battery is present and the battery charger starts upon valid CHGIN. If DETBATB is left unconnected or equal to V_{IO} voltage, this indicates that the battery is not present and the charger does not start upon valid CHGIN, see Figure 3. The DETBATB is internally pulled to BATT through an external resistor.

DETBATB status bit is valid when BATT is not present.

Input Validation

As shown in <u>Figure 4</u>, the charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following three characteristics to be valid:

CHGIN must be above V_{CHGIN UVLO} to be valid.

CHGIN must be below its overvoltage lockout threshold (V_{OVLO}) .

CHGIN must be above the system voltage by V_{CHGIN2SYS}.

CHGIN input generates a CHGIN_I interrupt when its status changes. The input status can be read with CHGIN_OK and CHGIN_DTLS. Interrupts can be masked with CHGIN_M.



Figure 3. DETBATB Internal Circuitry and System Diagram