Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX77826

Power Management IC

General Description

The MAX77826 is a subpower management IC for the latest 3G/4G smartphones and tablets. The MAX77826 contains a high-efficiency BUCK regulator, a BUCK BOOST regulator and 15 LDOs to power up peripherals. The MAX77826 also provides power on/off control logic and an I²C serial interface to program individual regulator output voltages and on/off control for complete flexibility.

The linear regulators support a remote cap feature and provide greater than 70dB PSRR and less than 45μV_{RMS} noise.

The MAX77826 features I²C-compatible, 2-wire serial interface that comprises a bidirectional serial data line (SDA) and a serial clock line (SCL). The MAX77826 supports SCL clock rates up to 3.4MHz.

Applications

- GSM, GPRS, EDGE, CDMA WCDMA, and LTE Smartphones and Tablets

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Compact Total Solution Size Allows More Peripheral Devices in Smartphones and Tablets
  - 3A High-Efficiency BUCK Regulator
    - DVS (Dynamic Voltage Scaling) Through HS I²C
    - ±1% (typ) Output Voltage DC Accuracy
    - Low Power Mode
  - 2A BUCK BOOST Regulator
  - 15 Linear Regulators with Remote Cap
    - 3 NMOS LDOs (V_{OUT} Range: 0.6V to 2.1875V with 12.5mV Step)
    - 1 x 150mA
    - 1 x 450mA
    - 1 x 600mA
  - 6 PMOSLV LDOs (V_{OUT} Range: 0.8V to 3.975V with 25mV Step)
    - 3 x 150mA
    - 3 x 300mA
  - 6 PMOSLS LDOs (V_{OUT} Range: 0.8V to 3.975V with 25mV Step)
    - 3 x 150mA
    - 3 x 300mA
  - ±1.5% Typical Output Voltage DC Accuracy
  - 70dB PSRR at 1kHz
  - Low Power Mode with 2µA (typ) for all LDOs
- Simple Management of Power-Up/Down Sequence, Output Voltage Setting, and Fault Detection
  - High-Speed (Up to 3.4MHz) I²C Serial Interface

19-6893; Rev 0; 6/15

maxim integrated™

Absolute Maximum Ratings

SYS, V_{IO}, INL1, INL2, INL3, INL4, INL5 to GND ..... -0.3V to +6.0V
INB to PGNDB ..... -0.3V to +6.0V
INBB, OUTBB to PGNDBB ..... -0.3V to +6.0V
PGNDB, PGNDBB to GND ..... -0.3V to +0.3V
IRQB, CE, SDA, SCL to GND ..... -0.3V to (V_{IO} + 0.3V)
FB_B, ENBB, ENB, ENL12, REFBYP to GND ..... -0.3V to (V_{SYS} + 0.3V)
FB_BB to PGNDBB ..... -0.3V to (V_{OUTBB} + 0.3V)
LXB to PGNDB ..... -0.3V to (V_{INB} + 0.3V)
LXBB1 to PGNDBB ..... -0.3V to (V_{INBB} + 0.3V)
LXBB2 to PGNDBB ..... -0.3V to (V_{OUTBB} + 0.3V)
LDO1, LDO2 to GND ..... -0.3V to (V_{INL1} + 0.3V)
LDO3 to GND ..... -0.3V to (V_{INL2} + 0.3V)
LDO4, LDO5, LDO6, LDO7, LDO8, LDO9 to GND ..... -0.3V to (V_{INL3} + 0.3V)
LDO10, LDO11 to GND ..... -0.3V to (V_{INL4} + 0.3V)
LDO12, LDO13, LDO14, LDO15 to GND ..... -0.3V to (V_{INL5} + 0.3V)
LXB Continuous RMS Current (Note 1) 3A
LXBB1/LXBB2 Continuous RMS Current (Note 1) 3.3A
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +260°C

Note 1: LX_ node has internal clamp diodes to PGND_ and INB_. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed IC's package power dissipation limits.

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

General Electrical Characteristics

(V_{SYS} = $V_{IN\_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current	I_{SHDN_SYS}	CE = low		2.5	10	µA
Standby Current	I_{Q_SYS}	CE = high and all regulators are off		35		µA
Shutdown V_{IO} Current	I_{SHDN_VIO}	All regulators are off		0		µA
No Load Supply Current 1	I_{NO_LOAD1}	BUCK is on in normal mode (no switching)		60		µA
No Load Supply Current 2	I_{NO_LOAD2}	BUCK and BUCK BOOST are on in normal mode (no switching)		120		µA
No Load Supply Current 3	I_{NO_LOAD3}	All regulators are on in normal mode (no switching)		400	700	µA
V_{SYS} UNDERVOLTAGE LOCKOUT						
V_{SYS} Undervoltage Lockout Threshold	V_{UVLO_R}	V_{SYS} rising	2.375	2.50	2.625	V
	V_{UVLO_F}	V_{SYS} falling (default)		2.05		
REFERENCE						
REFBYP Output Voltage			0.786	0.80	0.814	V
REFBYP Supply Rejection		2.7V ≤ V_{SYS} ≤ 5.5V		0.2		mV/V

General Electrical Characteristics (continued)

(V_{SYS} = $V_{IN\_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL SHUTDOWN							
Thermal Shutdown Threshold	T_{SHDN}	T_J rising, 15°C hysteresis			+165		°C
Thermal Interrupt at +120°C	T_{120}	T_J rising, 15°C hysteresis			+120		°C
Thermal Interrupt at +140°C	T_{140}	T_J rising, 15°C hysteresis			+140		°C
LOGIC AND CONTROL INPUTS							
Input Low Level	V_{IL}	ENB, ENBB, ENL12	V_{SYS} ≤ 4.5V T_A = +25°C			0.4	V
		CE	T_A = +25°C			0.3 x V_{IO}	
Input High Level	V_{IH}	ENB, ENBB, ENL12	V_{SYS} ≤ 4.5V T_A = 25°C	1.2			V
		CE	T_A = +25°C	0.7 x V_{IO}			
Logic Input Leakage Current	I_{LEAK}	CE (0V < V_{IO} < 1.8V)	T_A = +25°C	-1		+1	µA
			T_A = +85°C		0.1		
IRQB Output Low Voltage	V_{OL}	I_{SINK} = 1mA				0.4	V
IRQB Output High Leakage	I_{OZH}	V_{IO} = 5.5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		0.1		
INTERNAL PULLDOWN RESISTANCE							
ENB, ENBB, ENL12	R_{PD}	Pulldown resistor to GND		400	800	1600	kΩ

I²C Electrical Characteristics

(V_{SYS} = $V_{IN\_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{IO} Voltage	V_{IO}		1.7		3.6	V
SDA AND SCL I/O STAGES						
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{IO}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{IO}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{IO}		V
SCL, SDA Input Current	I_I	V_{IO} = 3.7V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 20mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IO} to 0.3 x V_{IO}	t_{OF}				120	ns
I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST, AND FAST MODE PLUS) (Note 3)						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time REPEATED START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Capacitive Load for Each Bus Line	C_B				550	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				50		ns

I²C Electrical Characteristics (continued)

(V_{SYS} = $V_{IN\_}$ = +3.7V, V_{IO} = 1.8V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF			C_B = 400pF			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I²C-COMPATIBLE INTERFACE TIMING (HS MODE)									
Clock Frequency	f_{SCL}				3.4			1.7	MHz
Set-Up Time REPEATED START Condition	$t_{SU;STA}$		160			160			ns
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		160			160			ns
CLK Low Period	t_{LOW}		160			320			ns
CLK High Period	t_{HIGH}		60			120			ns
DATA Setup time	$t_{SU:DAT}$		10			10			ns
DATA Hold Time	$t_{HD:DAT}$			35			75		ns
SCL Rise Time (Note 3)	t_{RCL}	T_A = +25°C	10		40	20		80	ns
Rise Time of SCL Signal After a REPEATED START Condition and After an Acknowledge Bit (Note 3)	t_{rCL1}	T_A = +25°C	10		80	20		160	ns
SCL Fall Time (Note 3)	t_{fCL}	T_A = +25°C	10		40	20		80	ns
SDA Rise Time (Note 3)	t_{rDA}	T_A = +25°C			80			160	ns
SDA Fall Time (Note 3)	t_{fDA}	T_A = +25°C			80			160	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160			160			ns
Capacitive Load for Each Bus Line	C_B				100			400	pF
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter				10			10		ns

BUCK Electrical Characteristics

(V_{SYS} = V_{INB} = +3.7V, V_{FB_B} = V_{OUT} = 1.25V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	Parametric		2.6		5.5	V
Shutdown Supply Current (Note 3)				0.1		µA
Supply Quiescent Current (Note 3)	No switching, No load	Normal mode		22		µA
		Low power mode		8		
Output Voltage Range	I^2C-programmable 6.25mV step		0.5		1.8	V
Output Voltage Accuracy	V_{INB} = 2.6V to 4.5V, V_{OUT} = 1.25V, no load	PWM mode, T_A = +25°C	-1.0		+1.0	%
		Low power mode	-3.0		+4.0	
Line Regulation	V_{INB} = 2.6V to 4.5V			0.200		%/V
Load Regulation (Note 3)	V_{OUT} = 1.25V			0.125		%/A
Transient Load Response, VDROOP (Note 3)	V_{OUT} = 1.25V, IOUT changes from 0A to 1.5A in 6µs, C_{OUT_ACTUAL} = 22µF, L = 0.47µH			-50		mV
Soft-Start Slew Rate				14		mV/µs
Output Voltage Ramp-Up Slew Rate	RAMP[1:0] = 00b (default)			12.5		mV/µs
	RAMP[1:0] = 01b			25		
	RAMP[1:0] = 10b			50		
	RAMP[1:0] = 11b			100		
Maximum Output Current	Normal mode		3000			mA
	Low power mode			10		
Peak Current Limit			3.30	4.25	5.50	A
Valley Current Limit				3.825		A
Negative Current Limit				1.000		A
N-FET Zero-Crossing Threshold	Skip mode			20		mA
Switching Frequency			1.8	2	2.2	MHz
Turn-On Delay Time	EN signal to LX switching with bias ON			30		µs
HS PMOS RDSON	V_{INB} = 3.7V, INB to LX, I_{LX} = 200mA			60		mΩ
LS NMOS RDSON	V_{INB} = 3.7V, LX to PGNDB, I_{LX} = 200mA			35		mΩ
Output Active Discharge Resistance	Output disabled, resistance from FB_B to PGNDB			100		Ω
LX Leakage	V_{LXB} = 5.5V or 0V	T_A = +25°C	-1	0.1	+1	µA
		T_A = +85°C		1		
POWER-OK COMPARATOR						
Output POK Trip Level	V_{OUT} POK rising threshold			90		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

BUCK BOOST Electrical Characteristics

(V_{INBB} = +3.7V, V_{OUTBB} = +3.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL						
Operating Input Voltage Range	Supplied from V_{SYS}		2.6		5.5	V
Shutdown Supply Current	V_{INBB} = 5.5V, V_{OUTBB} = 0V	T_A = +25°C		0.01		µA
		T_A = +85°C		1		
Input Supply Current	Enabled, no load	HSKIP mode (no switching)		60		µA
		FPWM mode (switching)		9		mA
Active Discharge Resistance				100		Ω
Thermal Shutdown	T_A rising, 20°C hysteresis			+165		°C
H-BRIDGE						
Maximum Output Current (Note 6)	V_{INBB} = 3.0V, V_{OUTBB} = 3.5V		2000			mA
	V_{INBB} = 2.6V, V_{OUTBB} = 3.5V		1500			
Default Output Voltage	No load, BB_VOUT[6:0] = 0x48			3.5		V
Output Voltage Accuracy	BB_VOUT[6:0] = 0x48, no load	PWM mode	-1.0		+1.0	%
		HSKIP mode T_A = +25°C	-1.0		+4.0	
Output Voltage Range	I^2C programmable (12.5mV step)		2.6		4.1875	V
Line Regulation	V_{INBB} = 2.6V to 5.5V			0.200		%/V
Load Regulation (Note 6)	V_{OUTBB} = 3.5V			0.125		%/A
Transient Load Response, V_{DROOP} (Note 6)	V_{INBB} = 3.8V, V_{OUTBB} = 3.5V, I_{OUT} changes from 10mA to 1A in 10µs, C_{OUT_ACTUAL} = 47µF, L = 1µH			-100		mV
Output Overvoltage Threshold	With respect to V_{OUTBB}	BB_OVP_TH[1:0] = 01b		110		%
		BB_OVP_TH[1:0] = 10b		115		
		BB_OVP_TH[1:0] = 11b (default)		120		
Switching Frequency	2-phase BUCK or BOOST mode		1.6	1.8	2.0	MHz
	3-phase mode			0.9		
LXBB1, LXBB2 Leakage Current	$V_{LXBB1/2}$ = 0V or 5.5V, V_{OUTBB} = 5.5V, V_{SYS} = V_{INBB} = 5.5V	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.2		
LXBB1/2 Current Limit			3.5	4.5	5.5	A
PMOS On-Resistance	I_{LXBB} = 100mA, per switch			65		mΩ
NMOS On-Resistance	I_{LXBB} = 100mA, per switch			55		mΩ

BUCK BOOST Electrical Characteristics (continued)

(V_{INBB} = +3.7V, V_{OUTBB} = +3.5V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Effective Output Capacitance	0µA < I_{OUT} < 2000mA		16		µF
Turn-On Delay Time	From ENBB asserting to LXBB Switching with bias on		6		µs
Soft-Start Time	V_{OUTBB} = 3.5V, I_{OUT} = 10mA		40		µs
POWER-OK COMPARATOR					
Output POK Trip Level	$V_{OUTBB\ POK}$ rising threshold		80		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches		5		%

LDO Electrical Characteristics

LDO NO.	TYPE	V_{OUT} RANGE (V)	STEP SIZE (mV)	I_{OUT} (max, mA)	DEFAULT V_{OUT} (V)	DEFAULT ON/OFF	INPUT PIN	C_{OUT} (µF)
1	NMOS	0.6–2.1875	12.5	600	1.0	Off	INL1	4.7
2	NMOS	0.6–2.1875	12.5	150	1.0	Off	INL1	1
3	NMOS	0.6–2.1875	12.5	450	1.0	Off	INL2	4.7
4	PMOSLV	0.8–3.975	25	300	1.5	Off	INL3	4.7
5	PMOSLV	0.8–3.975	25	300	1.8	Off	INL3	4.7
6	PMOSLV	0.8–3.975	25	150	1.8	Off	INL3	2.2
7	PMOSLV	0.8–3.975	25	300	1.8	Off	INL3	4.7
8	PMOSLV	0.8–3.975	25	150	1.8	Off	INL3	2.2
9	PMOSLV	0.8–3.975	25	150	1.8	Off	INL3	2.2
10	PMOSLS	0.8–3.975	25	300	2.8	Off	INL4	2.2
11	PMOSLS	0.8–3.975	25	150	2.8	Off	INL4	2.2
12	PMOSLS	0.8–3.975	25	300	3.3	Off	INL5	2.2
13	PMOSLS	0.8–3.975	25	300	3.3	Off	INL5	2.2
14	PMOSLS	0.8–3.975	25	150	3.3	Off	INL5	2.2
15	PMOSLS	0.8–3.975	25	150	3.3	Off	INL5	2.2

Note: *LDO12 can also be enabled/disabled by external logic inputs, ENL12.*

LDO1 (600mA NMOS)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		V_{OUT}		V_{SYS}	V
	V_{SYS}		2.6		5.5	
	(Note 7)		1.5			
Input Supply Current	Normal mode, no load			2		µA
	Low power mode, no load			2		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			30		µA
	Low power mode, no load			4		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.6		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			2.1875		
	Least significant step size			0.0125		
Output Voltage Accuracy	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		600			mA
	Low power mode		5			
Load Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V)	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{SYS} - V_{OUT} = 2.5V		60	150	mV
		V_{SYS} - V_{OUT} = 1.5V		100		
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		900	1800	mA
		Low power mode		10		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		2.35	4.7		µF

LDO1 (600mA NMOS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = 2.7V, V_{INLx} = 1.2V, V_{OUT} = V_{OUTMIN}		30		μV_{RMS}
		V_{SYS} = 2.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = 3.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 4.7µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.0V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 1.8V to 1.5V to 1.8V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled.			5		µs
Output Overshoot during Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

LDO2 (150mA NMOS)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 1.0µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		V_{OUT}		V_{SYS}	V
	V_{SYS}		2.6		5.5	
	(Note 7)		1.5			
Input Supply Current	Normal mode, no load			2		µA
	Low power mode, no load			2		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			25		µA
	Low power mode, no load			3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.6		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			2.1875		
	Least significant step size			0.0125		
Output Voltage Accuracy	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		150			mA
	Low power mode		5			
Load Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V)	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{SYS} - V_{OUT} = 2.5V		60	150	mV
		V_{SYS} - V_{OUT} = 1.5V		100		
Output Current Limit	V_{OUT} = 90% of V_{OUT} (TARGET)	Normal mode		225	450	mA
		Low power mode		10		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		0.5	1.0		µF

LDO2 (150mA NMOS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 1.0µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = 2.7V, V_{INLx} = 1.2V, V_{OUT} = V_{OUTMIN}		30		μV_{RMS}
		V_{SYS} = 2.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = 3.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 1.0µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.0V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 1.8V to 1.5V to 1.8V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled.			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

LDO3 (450mA NMOS)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		V_{OUT}		V_{SYS}	V
	V_{SYS}		2.6		5.5	
	(Note 7)		1.5			
Input Supply Current	Normal mode, no load			2		µA
	Low power mode, no load			2		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			25		µA
	Low power mode, no load			3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.6		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			2.1875		
	Least significant step size			0.0125		
Output Voltage Accuracy	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		450			mA
	Low power mode		5			
Load Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V)	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{SYS} ≥ V_{OUT} + 1.5V (V_{SYSMIN} = 2.6V), I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal Mode, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{SYS} - V_{OUT} = 2.5V		60	150	mV
		V_{SYS} - V_{OUT} = 1.5V		100		
Output Current Limit	V_{OUT} = 90% of V_{OUT} (TARGET)	Normal mode		675	1350	mA
		Low power mode		10		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		2.35	4.7		µF

LDO3 (450mA NMOS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 1.0µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = 2.7V, V_{INLx} = 1.2V, V_{OUT} = V_{OUTMIN}		30		μV_{RMS}
		V_{SYS} = 2.7V, V_{INLx} = 1.8V, V_{OUT} = 1.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power-Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = 3.7V, V_{INLx} = 1.8V, V_{OUT} = 1.2V, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 4.7µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.2V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 1.8V to 1.5V to 1.8V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot during Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			5		%

LDO4, LDO5 and LDO7 (300mA PMOSLV)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		1.7		V_{SYS}	V
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			1.5		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3		µA
	Low power mode, no load			0.3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum VOUT, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		300			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{INLx} = 3.7V		60	150	mV
		V_{INLx} = 1.7V		100		
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		600	1120	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		2.35	4.7		µF

LDO4, LDO5 and LDO7 (300mA PMOSLV) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 4.7µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 4.7µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.2V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 2.0V to 1.7V to 2.0V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Over-shoot during Startup Over-shoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			+165		°C
	T_J falling			+150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

LDO6, LDO8, and LDO9 (150mA PMOSLV)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx} must be lower than or equal to V_{SYS}		1.7		V_{SYS}	V
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			1.5		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3		µA
	Low power mode, no load			0.3		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA,	-5		+5	
Maximum Output Current (Note 8)	Normal mode		150			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}	V_{INLx} = 3.7V		60	150	mV
		V_{INLx} = 1.7V		100		
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		300	560	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		1.1	2.2		µF

LDO6, LDO8, and LDO9 (150mA PMOSLV) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x IMAX to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 2.2µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{OUT} = 1.2V, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs	V_{SYS} = V_{INLx} = 3.7V to 3.2V to 3.7V		5		mV
		V_{SYS} = 3.7V, V_{INLx} = 2.0V to 1.7V to 2.0V		5		
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			+165		°C
	T_J falling			+150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

LDO11, LDO14 and LDO15 (150mA PMOSLS)

(V_{SYS} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx}		2.6		5.5	V
	V_{SYS}		2.6		5.5	
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			4		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3.25		µA
	Low power mode, no load			0.85		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		150			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = V_{INLx} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}			100	200	mV
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		300	560	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		0.6	2.2		µF

LDO11, LDO14 and LDO15 (150mA PMOSLS) (continued)

(V_{SYS} = V_{INLx} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x IMAX to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 2.2µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{INLx} = 3.7V to 3.2V to 3.7V, V_{OUT} = default, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs			5		mV
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			165		°C
	T_J falling			150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

LDO10, LDO12 and LDO13 (300mA PMOSLS)

(V_{SYS} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLx}		2.6		5.5	V
	V_{SYS}		2.6		5.5	
Input Supply Current	Normal mode, no load			15		µA
	Low power mode, no load			4		
	Shutdown			< 0.1		
System Supply Current	Normal mode, no load			3.25		µA
	Low power mode, no load			0.85		
	Shutdown			< 0.1		
Output Voltage Programming	Minimum V_{OUT}, Lx_VOUT[6:0] = 7'h00			0.8		V
	Maximum V_{OUT}, Lx_VOUT[6:0] = 7'h7F			3.975		
	Least significant step size			0.025		
Output Voltage Accuracy	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}	Normal mode I_{OUT} = 0.1mA to I_{MAX}	-2		+2	%
		Low power mode I_{OUT} = 0.1mA to 5mA	-5		+5	
Maximum Output Current (Note 8)	Normal mode		300			mA
	Low power mode		5			
Load Regulation	V_{INLx} = V_{OUT} + 0.3V	Normal mode I_{OUT} = 0.1mA to I_{MAX}		0.5		%
		Low power mode I_{OUT} = 0.1mA to 5mA		0.5		
Line Regulation	V_{INLx} = V_{OUT} + 0.3V to V_{SYS}, I_{OUT} = 0.1mA	Normal mode		0.05		%/V
		Low power mode		0.05		
Dropout Voltage	Normal mode, V_{SYS} = V_{INLx} = 3.7V, I_{OUT} = I_{MAX}, V_{DO} = V_{INLx} - V_{OUT}			100	200	mV
Output Current Limit	V_{OUT} = 90% of $V_{OUT(TARGET)}$	Normal mode		600	1120	mA
		Low power mode		40		
Output Capacitance for Stability	DCR < 200mΩ, ESL < 20nH (Note 9)		0.6	2.2		µF

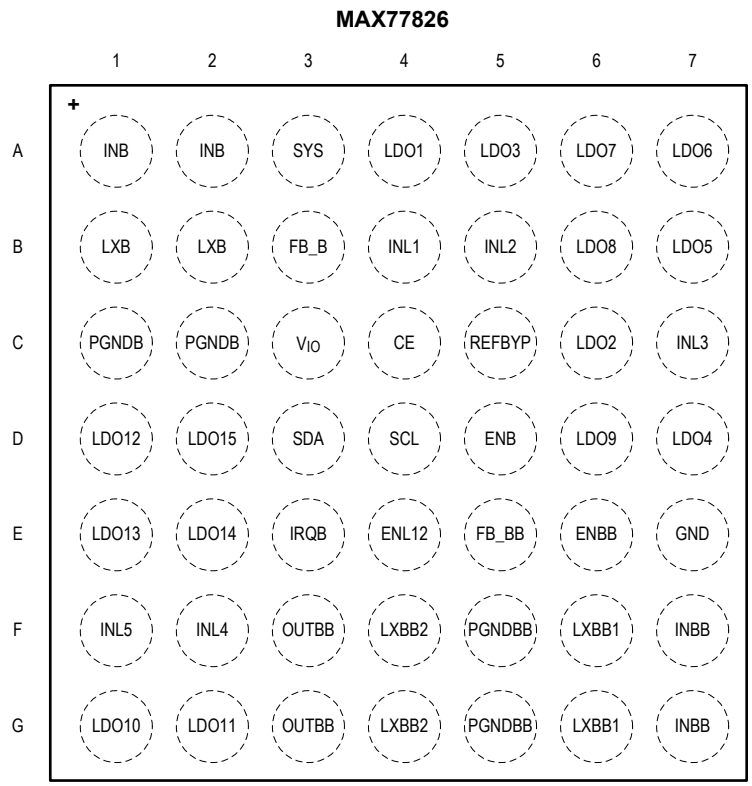
LDO10, LDO12 and LDO13 (300mA PMOSLS) (continued)

(V_{SYS} = +3.7V, C_{SYS} = 1.0µF, C_{OUT} = 2.2µF, C_{REFBYP} = 100nF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise	Normal mode, f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = V_{OUTMIN}		25		μV_{RMS}
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 1.0V		30		
		V_{SYS} = V_{INLx} = 2.7V, V_{OUT} = 2.0V		40		
		V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = 3.0V		60		
		V_{SYS} = V_{INLx} = 5.5V, V_{OUT} = V_{OUTMAX}		60		
Power Supply Rejection	Normal mode, f = 1kHz, I_{OUT} = 30mA			70		dB
Output Load Transient ($\Delta V/V_{OUT}$)	Normal mode, V_{SYS} = V_{INLx} = 3.7V, V_{OUT} = default, I_{OUT} = 1mA to ½ x I_{MAX} to 1mA, t_{RISE} = t_{FALL} = 1µs	C_{OUT} = 2.2µF		±5		%
		C_{OUT} = 10µF		±3		
Output Line Transient	Normal mode, V_{INLx} = 3.7V to 3.2V to 3.7V, V_{OUT} = default, I_{OUT} = 1mA, t_{RISE} = t_{FALL} = 5µs			5		mV
Output Startup Ramp Rate	10% to 90%			30		mV/µs
Turn-On Delay Time	From Lx_EN = 1 (or ENL12 = high) to output rising, REFBYP enabled > 300µs prior to LDO being enabled			5		µs
Output Overshoot During Startup Overshoot				50		mV
Output Active Discharge Resistance	(Note 10)			100		Ω
Thermal Shutdown	T_J rising			+165		°C
	T_J falling			+150		
POWER-OK COMPARATOR						
Output POK Trip Level	Rising edge, V_{OUT} when V_{POK} switches			87.5		%
Output POK Hysteresis	V_{OUT} when V_{POK} switches			3		%

Note 3: Guaranteed by design. Not production tested.
Note 4: 100% production tested at T_A = +25°C, limits over the operating range are guaranteed by design.
Note 5: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
Note 6: The maximum output current spec is not directly tested. Instead, it is guaranteed by LX NMOS current limit test.
Note 7: For NMOS LDOs, V_{SYS} must be at least 1.5V above V_{OUT} ($V_{SYS} \geq V_{OUT}$ + 1.5V).
Note 8: The maximum output current is guaranteed by the output voltage accuracy tests.
Note 9: For stability, guaranteed by design and not production tested.
Note 10: There is an n-channel MOSFET in series with the output active discharge resistance. This NMOS requires V_{SYS} > 1.2V to be enhanced.

Pin Configurations



Pin Description

PIN	NAME	FUNCTION
C4	CE	Active-High Chip Enable Input. When CE = high (standby), the I²C interface is enabled and regulators are ready to be turned on. When CE = low (shutdown), all regulators are turned off and all Type-O registers are reset to their POR default values.
D5	ENB	Active-High BUCK External Enable Input. An 800kΩ internal pull-down resistance to the GND. If this pin is not used, leave it floating.
E6	ENBB	Active-High BUCK BOOST External Enable Input. An 800kΩ internal pulldown resistance to the GND. If this pin is not used, leave it unconnected.
E4	ENL12	Active-High LDO12 External Enable Input. An 800kΩ internal pulldown resistance to the GND. If this pin is not used, leave it unconnected.
B3	FB_B	BUCK Output Voltage Feedback
E5	FB_BB	BUCK BOOST Output Voltage Feedback
E7	GND	Ground
A1, A2	INB	BUCK Input. Bypass to PGNDB with a 10µF capacitor.
F7, G7	INBB	BUCK BOOST Input

Pin Description (continued)

PIN	NAME	FUNCTION
B4	INL1	Input for LDO1 and 2. Bypass to GND with a 4.7µF capacitor.
B5	INL2	Input for LDO3. Bypass to GND with a 1µF capacitor.
C7	INL3	Input for LDO4, 5, 6, 7, 8, and 9. Bypass to GND with a 4.7µF capacitor.
F2	INL4	Input for LDO10 and 11. Bypass to GND with a 4.7µF capacitor.
F1	INL5	Input for LDO12, 13, 14, and 15. Bypass to GND with a 4.7µF capacitor.
E3	IRQB	Interrupt Output. A 100kΩ external pullup resistor to V_{IO} is required.
B1, B2	LXB	BUCK Switching Node
F6, G6	LXBB1	BUCK BOOST Switching Node 1
F4, G4	LXBB2	BUCK BOOST Switching Node 2
A4	LDO1	LDO1 (600mA NMOS) Output. Bypass to GND with a 4.7µF capacitor.
C6	LDO2	LDO2 (150mA NMOS) Output. Bypass to GND with a 1µF capacitor.
A5	LDO3	LDO3 (450mA NMOS) Output. Bypass to GND with a 4.7µF capacitor.
D7	LDO4	LDO4 (300mA PMOSLV) Output. Bypass to GND with a 4.7µF capacitor.
B7	LDO5	LDO5 (300mA PMOSLV) Output. Bypass to GND with a 4.7µF capacitor.
A7	LDO6	LDO6 (150mA PMOSLV) Output. Bypass to GND with a 2.2µF capacitor.
A6	LDO7	LDO7 (300mA PMOSLV) Output. Bypass to GND with a 4.7µF capacitor.
B6	LDO8	LDO8 (150mA PMOSLV) Output. Bypass to GND with a 2.2µF capacitor.
D6	LDO9	LDO9 (150mA PMOSLV) Output. Bypass to GND with a 2.2µF capacitor.
G1	LDO10	LDO10 (300mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
G2	LDO11	LDO11 (150mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
D1	LDO12	LDO12 (300mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
E1	LDO13	LDO13 (300mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
E2	LDO14	LDO14 (150mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
D2	LDO15	LDO15 (150mA PMOSLS) Output. Bypass to GND with a 2.2µF capacitor.
F3, G3	OUTBB	BUCK BOOST Output
C1, C2	PGNDB	BUCK Power GND
F5, G5	PGNDBB	BUCK BOOST Power GND
C5	REFBYP	LDO Reference Bypass Node. Connect a 0.1µF Cap to GND.
D4	SCL	I^2C Clock Input. High Impedance in Off State. A 1.5kΩ~2.2kΩ of pullup resistor to VIO is required.
D3	SDA	I^2C Data I/O. High Impedance in Off State. A 1.5kΩ–2.2kΩ of pullup resistor to V_{IO} is required.
A3	SYS	System (Battery) Voltage Input. Bypass to GND with a 1µF capacitor.
C3	V_{IO}	IO Supply Voltage Input. Bypass to GND with a 0.1µF capacitor.

Block Diagram