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MAX77950 WPC/PMA Dual Mode Wireless Power Receiver

General Description

The MAX77950 is an advanced wireless power receiver IC that meets the specification requirements for WPC low-power (v1.2) and PMA SR1 (v2.0) communication protocols. This device operates using near-field magnetic induction when coupled with a WPC or PMA transmitter and provides output power up to 12 watts.

The IC has precision output current and voltage-sensing scheme over the entire load range. It enables accurate received power packets, as defined in the WPC specifications for best foreign object detection (FOD). The IC supports FSK demodulation to receive PMA advertisement ID as well as WPC FSK packets.

The IC features the patent-pending PeerPower™ function. In PeerPower mode, the IC operates as a transmitter, enabling power transfer to another peer device through in-band ASK communications.

The MAX77950 communicates with an application processor through an I²C serial interface. The status of power transfer and alerts are read through this interface.

Applications

- Smartphones
- Tablets
- Smart Watches
- Headsets
- Wearable Devices
- Battery-Power Banks
- Wi-Fi Hotspots
- Digital Cameras
- Portable Medical Applications
- Portable Media Players
- Point-of-Sale Devices
- Handheld Devices

Benefits and Features

- WPC/PMA Dual Mode Wireless Power Receiver
- Compliant with WPC Low Power (v1.2) and PMA SR1 (v2.0)
- Peer-to-Peer Power Transmission with In-Band ASK Communications
- WPC ASK Demodulator/FSK Demodulator
- Output Programmable Range from 3.5V to 12.7V with 100mV Step
- Integrated High-Efficiency n-Channel Full-Bridge Synchronous Rectifier
- Programmable Foreign Object Detection
- Programmable Dynamic Rectifier-Voltage Scaling
- Overvoltage, Overcurrent, and Overtemperature Protection

Ordering Information *appears at end of data sheet.*

19-100003; Rev 0; 3/17

maxim integrated™

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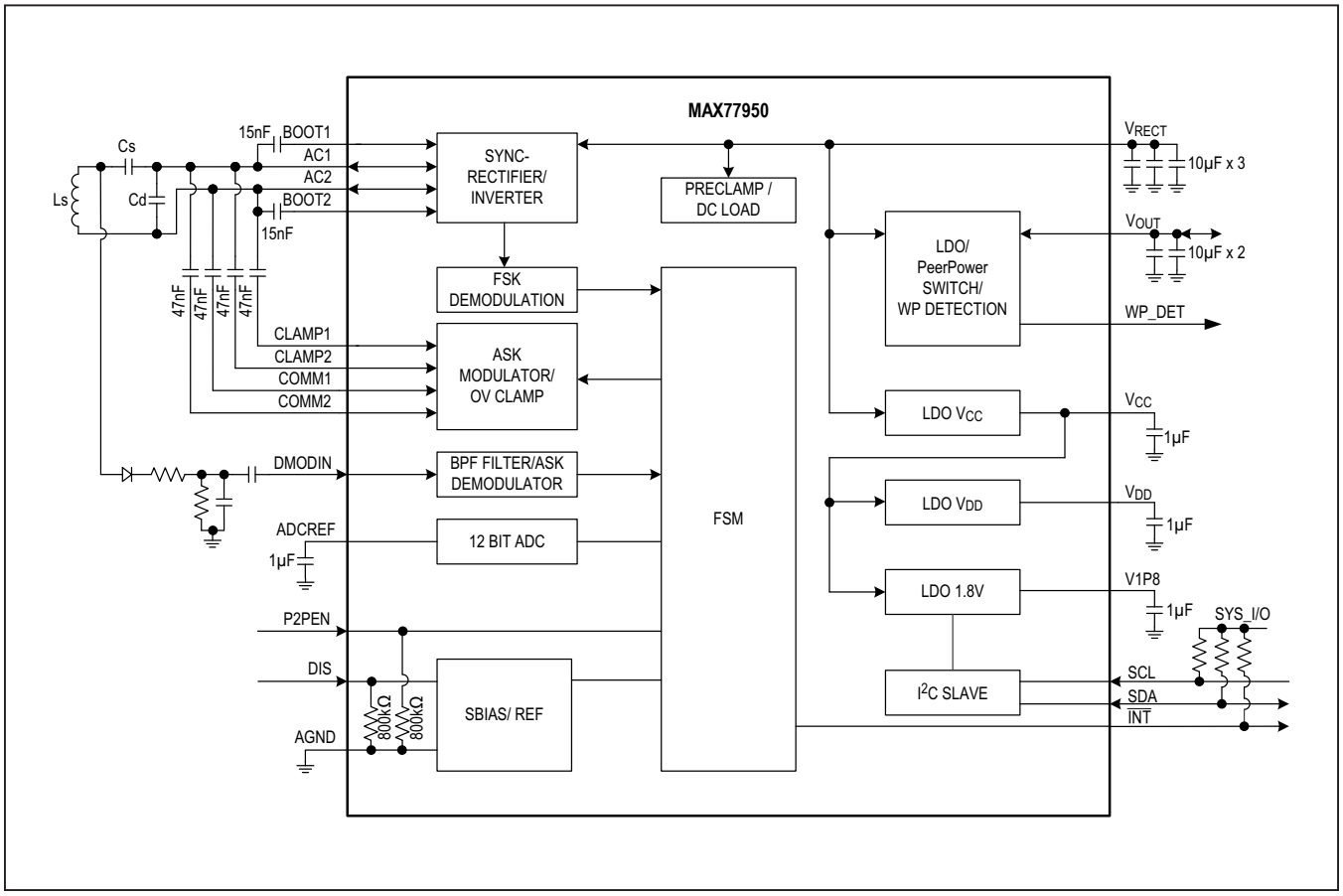
Simplified Block Diagram



Absolute Maximum Ratings

AC1, AC2 to PGND .....-0.3V to +20V
V_{RECT}, V_{OUT} to PGND.....-0.3V to +20V
COMM1, COMM2, CLAMP1, CLAMP2 to PGND .-0.3V to +20V
BST1, BST2 to PGND.....-0.3V to +25V
Differential ABS-MAX: BST1 to AC1, BST2 to AC2 .....+4.5V
V_{CC} to AGND .....-0.3V to +4.5V
V_{DD} to AGND .....-0.3V to +1.65V
V1P8 to AGND .....-0.3V to +4.5V
SCL, SDA, $\overline{INT}$ to AGND.....-0.3V to +4.5V
DIS to AGND .....-0.3V to V1P8 + 0.3V
WP_DET to AGND .....-0.3V to V1P8 + 0.3V
P2PEN to AGND .....-0.3V to V1P8 + 0.3V
DMODIN to AGND.....-0.3V to V_{CC} + 0.3V
ADCREF to AGND .....-0.3V to V_{DD} + 0.3V
DNC.....-0.3V to V_{CC} + 0.3V
AGND to PGND.....-0.3V to +0.3V
AC1, AC2 Current.....2.5A
V_{OUT} Current .....-1.5A to +1.5A
COMM1, COMM2.....1A
CLAMP1, CLAMP2.....1.5A
Operating Ambient Temperature Range..... -40°C to +85°C
Junction Temperature..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	W546A9+1 (6x9, 0.4mm pitch)
Outline Number	**21-100082**
Land Pattern Number	**Refer to Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	40°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{RECT} = 3V to 20V, T_A = -40°C to +85°C, unless otherwise noted, limits are 100% tested at T_A = +25°C; limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Current	I_{VRECT}	No load		5		mA
Disable Supply Current	I_{VRECT_SHDN}	DIS = 1, V_{RECT} = 5V		2.1		mA
Disable supply Current	I_{VRECT_SHDN}	DIS = 1, V_{RECT} = 20V		2.2		mA
Undervoltage Lockout Threshold	V_{UVLO}	V_{RECT} rising	2.4		2.9	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}			400		mV
Internal Pulldown Resistance for DIS and P2PEN	R_{PD}	Pulldown resistance to AGND	400	800	1600	kΩ
VOLTAGE REGULATORS						
Voltage Regulator for Internal Blocks	V_{CC}		4.06	4.275	4.49	V
	V_{DD}		1.496	1.575	1.65	
V1P8 Voltage Regulator	V1P8	I_{V1P8} = 20mA	1.71	1.8	1.89	V
LDO						
HV LDO Input Voltage Range	V_{RECT}		3		20	V
V_{OUT} Programmable Range Through I²C	V_{OUTPRG}	100mV step	3.5		12.7	V
HV LDO Startup Rate	$t_{LDOSTUP}$	I_{OUT} = 0mA		0.5		V/ms
HV LDO Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	LDO_VOUTSET[6:0] = 0x32, I_{OUT} = 1mA; V_{RECT} = 6V to 12V		0.1		%
HV LDO Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	LDO_VOUTSET[6:0] = 0x32, I_{OUT} = 1mA to 1A, V_{RECT} = 5.2V		0.5		%
HV LDO Load Transient		I_{OUT} = 1mA to 1A and 1A to 1mA within 20µs		±8		%
HV LDO Dropout Voltage	V_{DO}	LDO_VOUTSET[6:0] = 0x32, I_{OUT} = 1A, V_{DO} = V_{RECT}–V_{OUT}			100	mV
HV LDO Current Limit	I_{LIM}	LDO_ILIMSET[4:0] = 0x1A, LDO_VOUT-SET[6:0] = 0x32, V_{RECT} = +5.1V, V_{OUT} = +4.8V	1.1		1.5	A
Output Voltage Initial Accuracy	V_{OUT_ACC}	LDO_VOUTSET[6:0] = 0x32, I_{OUT} = 1mA, T_A = +25°C	-2		+2	%
COMM PINS						
COMMn On-Resistance	R_{COMM}			1		Ω
COMMn Leakage Current	I_{COMM}	V_{COMM1} = V_{COMM2} = 20V, T_A = +25°C			1	µA
CLAMP PINS						
CLAMPn On-Resistance	R_{CLAMP}			0.5		Ω
CLAMPn Leakage Current	I_{CLAMP}	V_{CLAMP1} = V_{CLAMP2} = 20V, T_A = +25°C			1	µA
OVP Preclamp Threshold	$OVLO_{PRECLAMP}$	V_{RECT} rising		16		V

Electrical Characteristics (continued)

(V_{RECT} = 3V to 20V, T_A = -40°C to +85°C, unless otherwise noted, limits are 100% tested at T_A = +25°C; limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNCHRONOUS RECTIFIER						
High-Side Switch On-Resistance	R_{ON_HS}			50		mΩ
Low-Side Switch On-Resistance	R_{ON_LS}			50		mΩ
ADC						
ADC Reference Voltage	V_{ADC_REF}	No load	1.237	1.25	1.262	V
Initial ADC Accumulated Error for V_{RECT}	ADC_ERR_VRECT	V_{RECT} = 3V to 15V, production tested at 3.5V, 7.5V, and 14.5V	-1		+1	%
Initial ADC Accumulated Error for V_{OUT}	ADC_ERR_VOUT	V_{OUT} = 3.6V to 10V, production tested at 3.5V, 6.5V, and 9.5V	-1		+1	%
Initial ADC Accumulated Error for ISNS	ADC_ERR_ISNS	Current range 0 to 1A, T_A = +25°C	-10		+10	mA
DEMODULATOR						
DMODIN Input Resistance				0.7		mΩ
DMODIN Minimum Detectable Input Voltage			200			mV
THERMAL PROTECTION						
Thermal Shutdown	T_{JOFF}	T_J rising		165		°C
Thermal-Shutdown Hysteresis	$T_{JOFFHYS}$	T_J falling		10		°C
Temperature-Warning Threshold	T_{JWARN}			120		°C
LOGIC OUTPUT						
WP_DET Output High Voltage		Source current 5mA	V1P8 - 0.4			V
WP_DET Output Low Voltage		Sink current 5mA			0.4	V
INTB Output Low Voltage	V_{OL}	Sink current 20mA			0.4	V
LOGIC INPUT						
P2PEN Input High Voltage			1.4			V
P2PEN Input Low Voltage					0.4	V
P2PEN Input Leakage Current					1	µA
DIS Input High Voltage			1.4			V
DIS Input Low Voltage					0.4	V
DIS Input Leakage Current					1	µA

Electrical Characteristics (continued)

(V_{RECT} = 3V to 20V, T_A = -40°C to +85°C, unless otherwise noted, limits are 100% tested at T_A = +25°C; limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.)

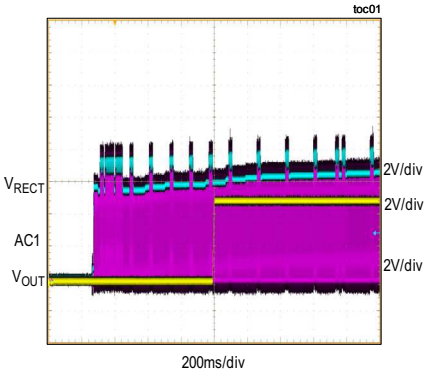
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C INTERFACE						
SCL, SDA Input High Voltage	V_{IH}		1.4			V
SCL, SDA Input Low Voltage	V_{IL}				0.4	V
SCL, SDA Input Hysteresis	V_{HYS}			0.2		V
SCL, SDA Input Leakage Current	I_I	0.1 x V_{DD} < SCL/SDA < 0.9 x V_{DD}	-1		+1	µA
SDA Output Low Voltage	V_{OL}	Sinking 10mA			0.4	V
SCL, SDA Pin Capacitance	C_I			10		pF
Output Fall Time from V_{IH} to V_{IL}	t_{OF}				300	ns
Clock Frequency	f_{SCL}		0		400	kHz
Hold Time Repeated Start Condition	$t_{HD;STA}$	Note 4	0.6			µs
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Setup Time Repeated Start Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}	Note 5	0		0.9	µs
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
Data Valid Time	$t_{VD:DAT}$				0.9	µs
Data Valid Acknowledge Time	$t_{VD:ACK}$				0.9	µs
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spikes	t_{SP}	Maximum pulse width of spikes that must be suppressed by the input filter		50		ns

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 2: All voltages are referenced to AGND.
Note 3: Test is performed on unmounted/unsoldered ports.
Note 4: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 5: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

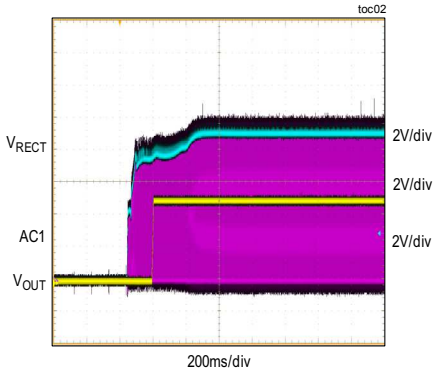
Typical Operating Characteristics

(Using WPC A11 and PMA 7 transmitters at T_A = +25°C, unless otherwise noted.)

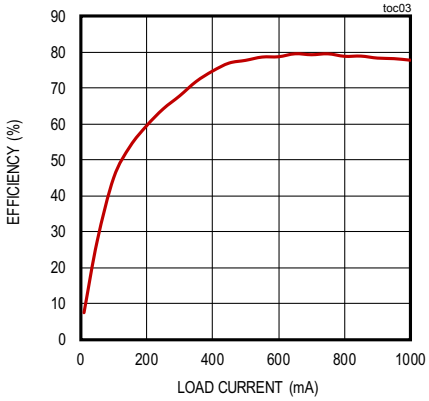
WPC MODE NO LOAD START-UP



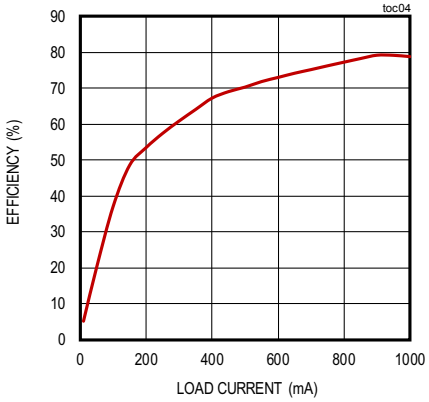
PMA MODE NO LOAD START-UP



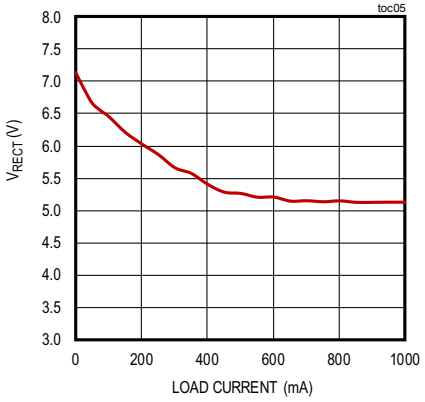
WPC MODE DC-DC EFFICIENCY



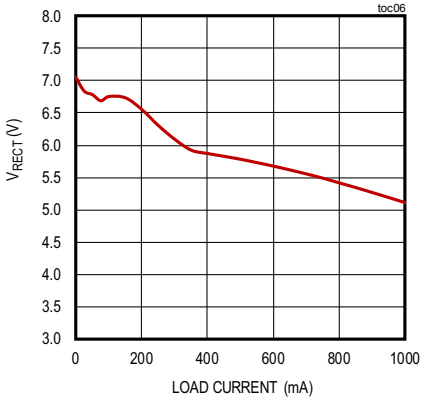
PMA MODE DC-DC EFFICIENCY



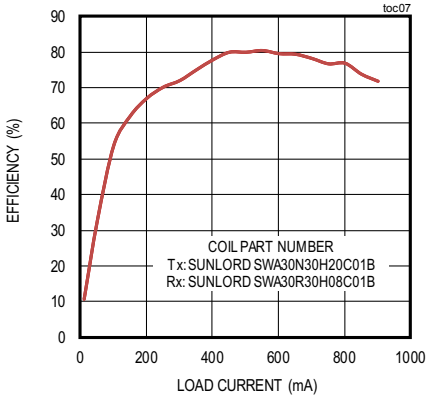
RECTIFIER VOLTAGE IN WPC MODE



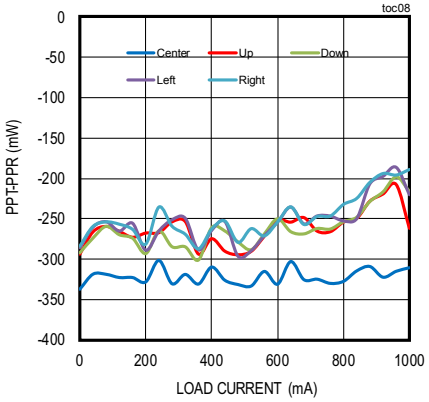
RECTIFIER VOLTAGE IN PMA MODE



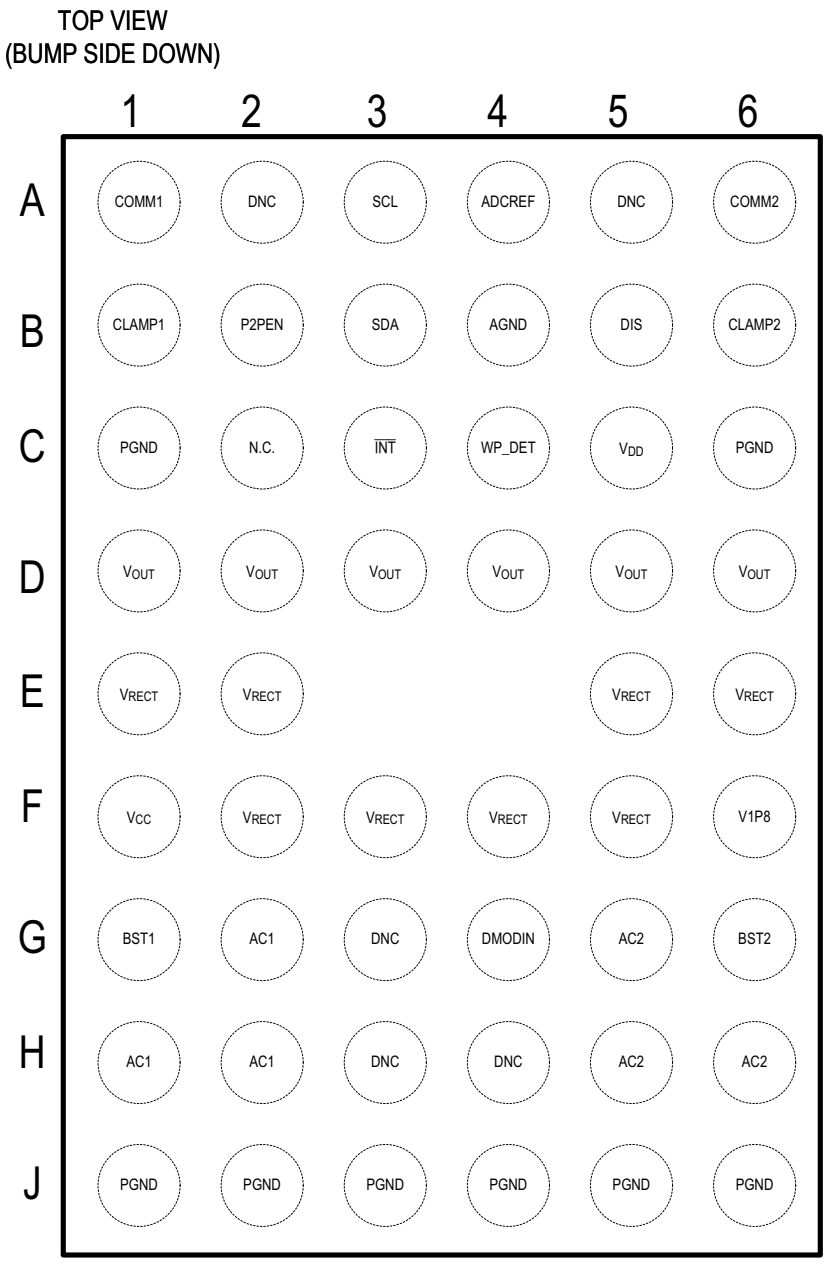
PeerPower MODE DC-DC EFFICIENCY



WPC FOREIGN OBJECT DETECTION



Bump Configuration

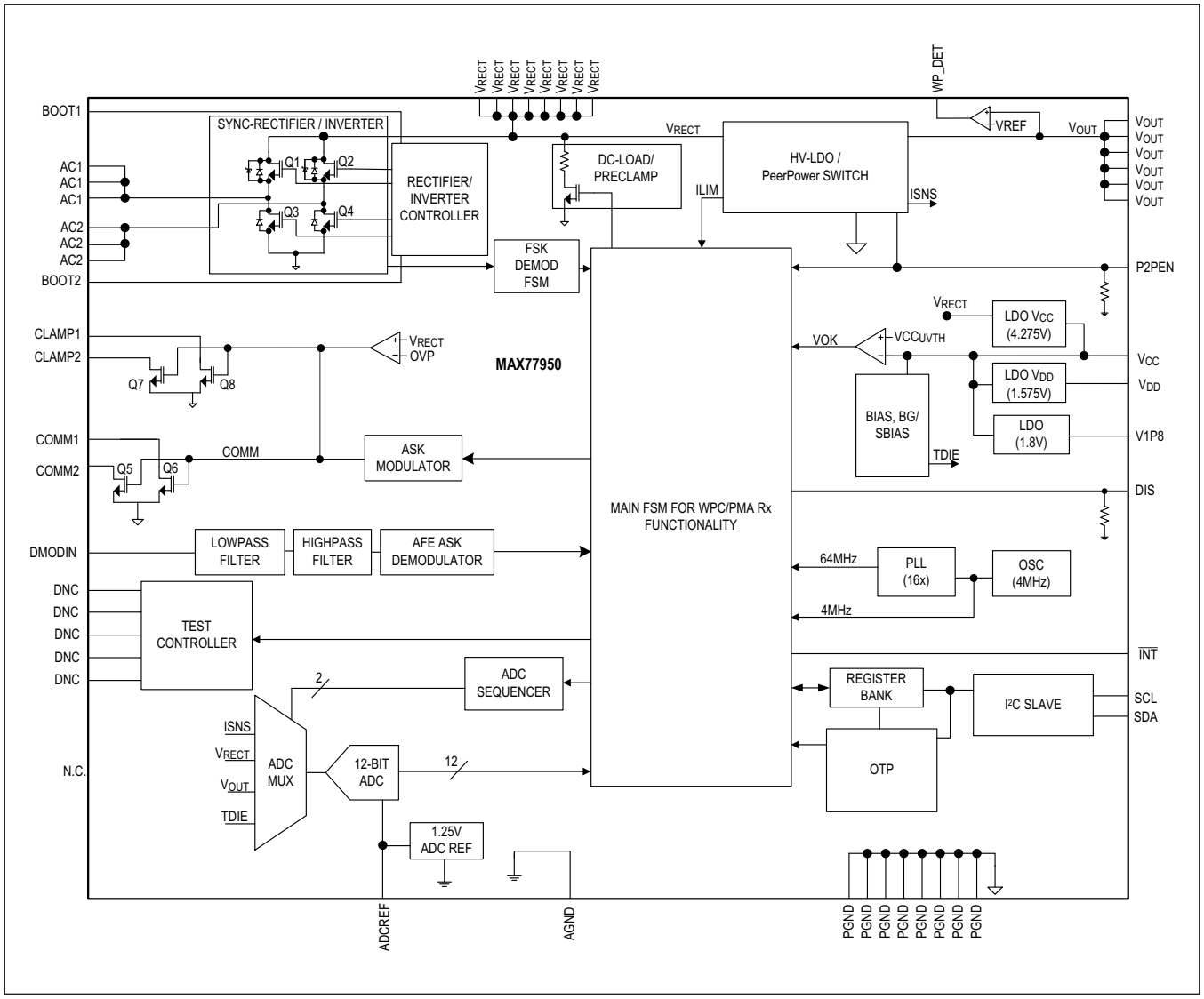


(52-Bump WLP, 0.4mm pitch)

Bump Description

PIN	NAME	FUNCTION	TYPE
A1	COMM1	Open-Drain Output. Achieves the AC modulation to communicate with the Tx.	Digital Output
A2, A5, G3, H3, H4	DNC	Do Not Connect. Leave open in system.	Analog I/O
A3	SCL	I^2C Clock Input	Digital Input
A4	ADCREF	ADC Reference Voltage. Bypass to ground with a 1µF ceramic capacitor.	Analog Output
A6	COMM2	Open-Drain Output. Achieves the AC modulation to communicate with the Tx.	Digital Output
B1	CLAMP1	Open-Drain Outputs. Switches to modulate ASK to communicate with Tx. Turns on when V_{RECT} overvoltage event occurs.	Digital Output
B2	P2PEN	PeerPower function active-high enable input.	Digital Input
B3	SDA	I^2C Data Input/Output	Digital I/O
B4	AGND	Analog Reference Ground. "Star-ground" connection to system GND.	Ground
B5	DIS	Disable Pin, Active-High	Digital Input
B6	CLAMP2	Open-Drain Outputs. Switches to modulate ASK to communicate with Tx. Turns on when V_{RECT} overvoltage event occurs.	Digital Output
C1, C6, J1– J6	PGND	Power Ground	Ground
C2	N.C.	Not Internally Connected. Can connect to power, ground, or leave open.	No Connect
C3	$\overline{INT}$	Open-Drain, Active-Low Interrupt Output	Digital Output
C4	WP_DET	Wireless Power Detected Output. Active-high	Digital Output
C5	V_{DD}	+1.575V linear regulator low ripple output for internal use. Bypass to ground with a 1µF ceramic capacitor.	Power Output
D1–D6	V_{OUT}	Linear Regulator Output. Bypass to ground with two 10µF capacitors.	Power I/O
E1, E2, F2–F5, E5, E6	V_{RECT}	Rectifier's Output. Bypass to ground with three 10µF and one 100nF ceramic capacitor.	Power I/O
F1	V_{CC}	+4.275V linear regulator low ripple output for internal use. Bypass to ground with a 1µF ceramic capacitor.	Power Output
F6	V1P8	+1.8V linear regulator low ripple output. Bypass to ground with a 1µF ceramic capacitor.	Power Output
G1	BST1	Bootstrap pin for rectifier's high side n-channel FET gate driver.	Analog Output
G2, H1, H2	AC1	Rectifier Input. Connect to receiver LC tank.	Power Input
G4	DMODIN	Amplitude Shift Keying Demodulator Input	Analog Input
G5, H5, H6	AC2	Rectifier Input. Connect to receiver LC tank.	Power Input
G6	BST2	Bootstrap pin for rectifier's high side n-channel FET gate driver	Analog Output

Functional Diagram



Detailed Description

Wireless Power Transfer System Overview

A wireless power system consists of a base station on the primary side and a power receiver on the secondary side, as shown in Figure 1. The base station (referred to as a power transmitter), comprises a power conversion unit, primary coil, communications demodulator, and control unit. The power receiver comprises a secondary coil, power pick-up unit, communications modulator, and controller.

When the receiver is placed on top of the transmitter's interface surface, the magnetic field that is generated by the primary coil induces a voltage on the secondary coil when the coils are magnetically coupled together. The output voltage of the receiver is regulated, and the received power is controlled through the communications and control unit in the receiver. The receiver communicates with the transmitter for requesting increased power, decreased power, no change in power transfer, or power-transfer termination. This communication is conducted in-band between the coils and is digitally overlaid on top of the power signal. The impedance on the secondary side is modulated as the receiver communicates, which is captured as load modulation by the primary coil. The transmitter changes frequency, duty cycle, or even voltage input of the power inverter to meet the demand of power that the receiver requests through the communication.

In WPC mode, the transmitter detects the modulation of the current and/or voltage across the primary coil and demodulates communication messages known as packets. A few examples of WPC packets are control error packet, received power packet, and end power transfer packet. The digital communication scheme, in the WPC protocol, utilizes differential bi-phase encoding as ONE and ZERO bits are transferred from the secondary to primary at a rate of 2kbps.

The PMA communication protocol operates continuously to transmit symbol messages that are encoded through frequency-based modulation. The receiver can send six different types of symbols to the transmitter using different frequency rates between 250Hz and 8kHz. They include decrement (DEC), increment (INC), no change (NoCh), end of charge (EOC), MsgBit, and a proprietary symbol intended for future use.

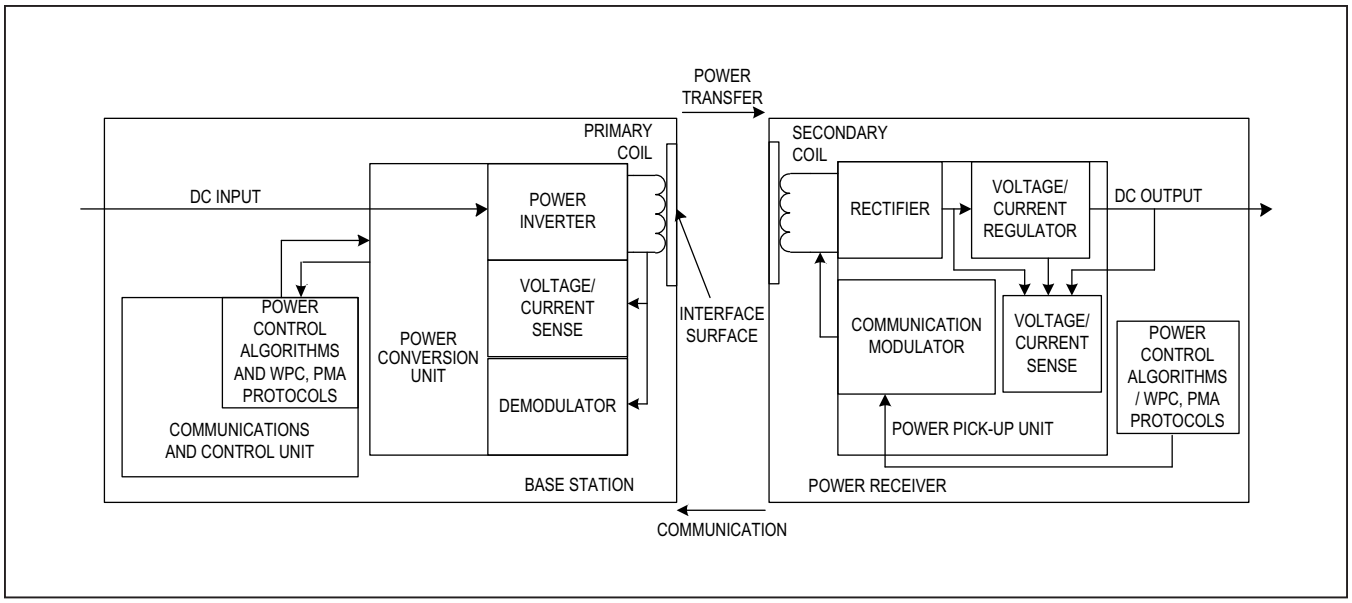


Figure 1. Wireless Power Transfer System Diagram

Rectified-Voltage Control Loop

The rectified voltage (V_{RECT}) is regulated by a closed control loop between the wireless power transmitter (base station) and the wireless power receiver (mobile device). To achieve the best compromise between optimal efficiency and output load transient response, the rectified voltage is regulated based on the output current. The V_{RECT} profile versus the load can be programmed in the following user registers, as shown in Figure 2.

The V_{RECT} target voltage is stored in eight 8-bit registers allocated for WPC mode (VRECT_TARGET_Y0 to VRECT_TARGET_Y7) and eight 8-bit registers allocated for PMA mode (VRECT_TARGET_PMA_Y0 to VRECT_TARGET_PMA_Y7). The output current is divided into eight thresholds which are stored in the registers VRECT_TARGET_X0 to VRECT_TARGET_X7. Different V_{RECT} target profiles are used for WPC and PMA due to the different power transfer profile characteristics.

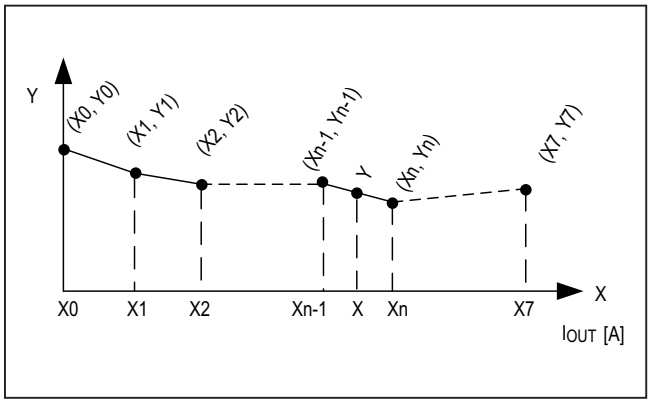


Figure 2. Rectified Voltage Profile vs. Output Current

The following equation calculates the V_{RECT} target based on linear interpolation between the adjacent coefficients:

$$y = y_{n-1} + \frac{(x - x_{n-1})(y_n - y_{n-1})}{x_n - x_{n-1}}$$

Where X is the actual output current reading:

$$VRECT\_TARGET\_X_n = \frac{X_n(A) \times 255 \times 0.73}{1.25}$$

$$VRECT\_TARGET\_Y_n = \frac{Y_n(V) \times 255}{1.25 \times 12}$$

$$VRECT\_TARGET\_PMA\_Y_n = \frac{Y_n(V) \times 255}{1.25 \times 12}$$

PeerPower Function

Overview

The PeerPower function enables one mobile device to charge another mobile device wirelessly. Figure 3 shows the main concept.

The MAX77950 is a highly configurable wireless power IC that allows the user to reconfigure the rectifier into a full-bridge inverter, achieving high-efficiency power transfer due to low $R_{DS(ON)}$ of the power MOSFETs.

Once P2PEN is pulled high, the switch located between V_{OUT} and V_{RECT} is turned on and the inverter generates a digital ping repeatedly. The IC continues power transfer once it receives the signal strength packet and also terminates power transfer after the end power transfer packet is received. A demodulated packet is stored in the registers (such as TX_WPC_HEADER, TX_WPC_DATA0/../7) until the next packet comes.

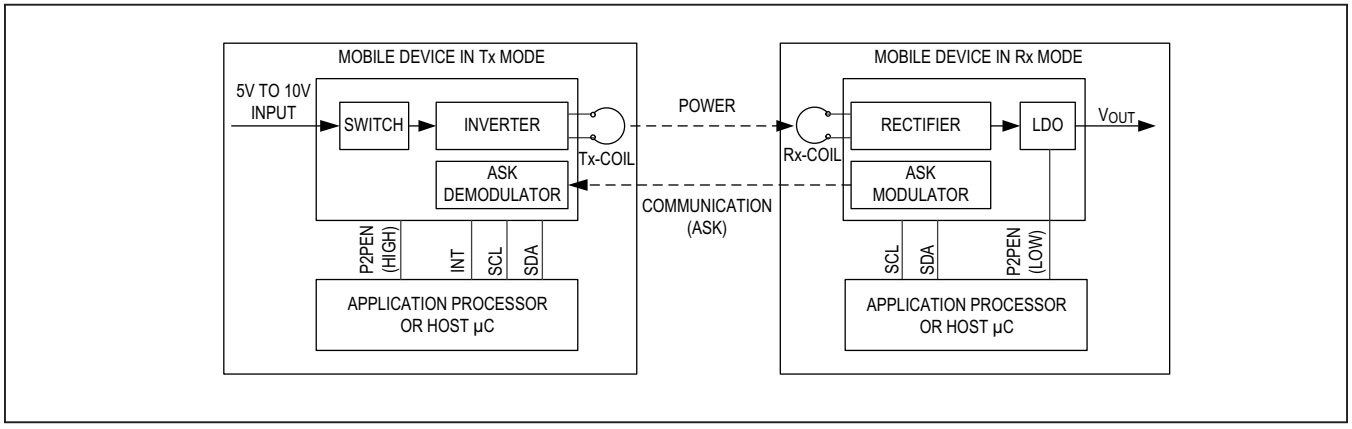


Figure 3. System-Level Block Diagram in PeerPower Mode

In PeerPower mode, the IC can generate interrupts in power transfer phase whenever it receives WPC packets that are non-zero CEP, RPP, CSP, EPT, and PPP so that an application processor or microcontroller notices it. To make this, a user needs to enable the ASK_DEMOD_PT_INT_EN bit. Then, $\overline{INT}$ goes low and the ASK_DEMOD_PT bit is set whenever the IC receives packets in power transfer phase.

To operate the IC in PeerPower mode, the following steps must be followed:

1) Supply an input voltage to the output of the LDO (V_{OUT} pin).
2) Program initial frequency into TX_FOP_SET_H/L; otherwise, the inverter will operate at 125kHz since it is the default frequency.
3) Pull P2PEN pin high to make LDO be a switch and run the inverter.

Wireless Power Detection Function

The IC offers a WP_DET output that is a power-good indicator that monitors the V_{OUT} level. The WP_DET output goes high once V_{OUT} exceeds the level programmed in WPDET_H_Threshold[1:0] and it goes low once V_{OUT} drops down to the level programmed in WPDET_L_Threshold[1:0].

Clamp Function

An overvoltage event may occur when the mobile device is moved over the transmitter's surface, or when partially removed from the mobile device and quickly placed on the power transmitter. In addition, it may occur during the ping stage in PMA mode. The IC has preclamp and clamp features to limit the rectifier-output voltage as an overvoltage protection. The preclamp pulls 250mA from V_{RECT} to PGND when the voltage on V_{RECT} exceeds 16V. If the rectifier-output voltage reaches 17V, even after the preclamp is activated, the IC turns on FETs between CLAMP1/2 and PGND as an additional protection. The preclamp and the clamp thresholds are both programmable through I^2C.

ASK/FSK Demodulation

The IC contains an ASK demodulation block that demodulates WPC ASK in PeerPower mode. In WPC, transmitted power is coupled to the receiver coil. When the receiver is powered up, it communicates with the transmitter at 2kHz by modulating the impedance of the receiver coil with communication capacitors. The function of the IC's ASK demodulator is to detect the 2kHz communication signal from the power signal.

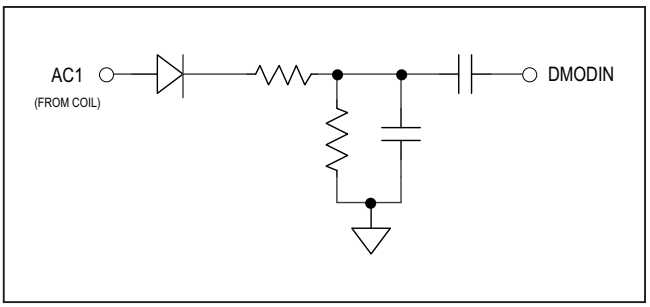


Figure 4. External Circuits for Envelope Detection, Level Shifting, and AC Coupling

The external circuits, shown in Figure 4, are required for the ASK demodulation in PeerPower mode. If the user application does not require PeerPower mode, the circuit is not necessary, so connect the DMODIN pin to GND.

The IC can demodulate the PMA advertising packet and WPC FSK with the FSK demodulation block.

The IC demodulates WPC FSK by using positive (+) polarity with modulation depth 0 following WPC Power Class 0 specification, version 1.2.1.

Foreign Object Detection (FOD)

As stated in the WPC specifications, a foreign object is defined as any object positioned on the interface surface of a base station but not part of the mobile device, such as coins, keys, or other metals. If the foreign object is within the active area, it may heat up during the power transfer, due to eddy currents, resulting from the oscillating magnetic field. Power loss is the key to detecting foreign objects and limiting the power loss on a wireless power system actually limits the heat. To start a power-transfer cycle during the selection phase, the transmitter detects and locates objects that are placed on the interface surface and attempts to differentiate between the foreign objects and a possible power receiver device. Once the wireless power receiver is discovered and the power transmitter completes the identification and the configuration phase, the power receiver reports to the power transmitter its received power in a received power packet ($P_{RECEIVED}$).

The received power (P_{PR}) equals the power available from the output of the power receiver, plus any power lost in producing that output power. For example, the power loss includes, but is not limited to:

- Power loss in the secondary coil and series resonant capacitor
- Power loss in the shielding of the power receiver
- Power loss in the rectifier
- Power loss in any post-regulation stage
- Eddy current loss in metal components or contacts within the power receiver

The IC complies with the WPC low-power (v1.2) requirement:

$$P_{RECEIVED} - 350mW \le P_{PR} \le P_{RECEIVED}$$

This means that the reported received power is an over-estimate of the actual received power, by 350mW, where P_{PR} is the actual received power determined by the mobile device by measuring its load power and adding the estimated parasitic power losses.

The IC has high-precision output current-sensing capabilities and accurate V_{RECT} control over the operating load, ensuring they are sufficient to estimate the received power and comply with WPC (v1.2) FOD requirements.

The IC provides registers that are FOD_Xn and FOD_Yn as part of the received power look-up table (LUT). Based on this LUT, the state machine sends a received power packet that is specified in the WPC requirements.

FOD_Xn stores 16 X-coordinates for output current values and FOD_Yn stores 16 Y-coordinates of received power values so it makes 16 pairs of coordinates, as shown in Figure 5.

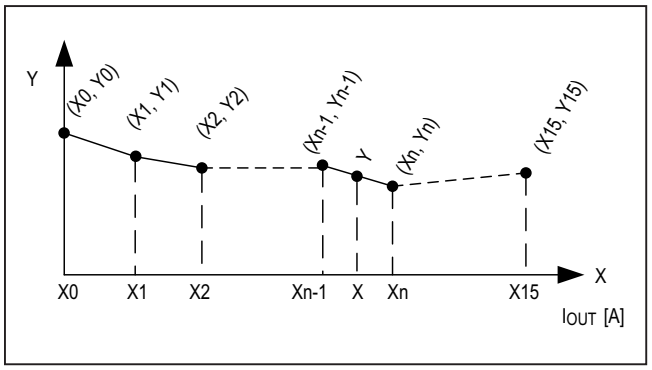


Figure 5. FOD Coefficients vs. Load Current

Between each coordinate, the values are interpolated linearly, as shown in the following equation:

$$y = y_{n-1} + \frac{(x - x_{n-1})(y_n - y_{n-1})}{x_n - x_{n-1}}$$

Equations for the FOD register are:

$$FOD\_X_n = \frac{X_n(A) \times 255 \times 0.73}{1.25}$$

$$FOD\_Y_n = \frac{Y_n(W) \times 128 \times 2}{10}$$

Watchdog Function

The IC supports a watchdog function that disables the main LDO output in case the watchdog timer expires. When the WDOG_INT_EN bit is set, it enables the watchdog function as well as the associated interrupt (WDOG_INT). The default timer is 41.5s. To keep the main LDO outputs after setting the WDOG_INT_EN bit, an application processor must periodically set the WDOG_INT_CLR bit before the timer expires. If the WDOG_INT_CLR bit is set, the timer is reset, and the WDOG_INT bit cleared. This feature prevents the IC from supplying power to a charger when the application processor freezes. To turn the main LDO back on, the application processor needs to set the WDOG_INT_CLR and Toggle_LDO bits. The timer options are programmable by OTP.

Sending End Power Transfer (EPT)/End of Charge (EOC)

The WPC EPT packet and the PMA EOC symbol is sent to a transmitter only by setting SEND_EPT bit 1 in RX_COM register (address : 0x20) or pulling the DIS pin high. The IC state machine does not send EPT or EOC by itself.

Sending Proprietary Packets (PPP)

The IC supports PPP, that is defined in the WPC specifications. The maximum length of a PPP is 5 bytes of messages. An example procedure for sending a PPP (3 bytes of messages) is as follows:

1. Write 0x38 in PPP_HEADER[7:0]
2. Write the first message in RX_DATA_VALUE0[7:0]
3. Write the second message in RX_DATA_VALUE1[7:0]
4. Write the third message in RX_DATA_VALUE2[7:0]
5. Set SEND_RX_DATA bit in RX_COM[7:0]

Register Map

ADDRESS	NAME	MSB							LSB
FUNCTIONAL									
0x00	CHIP_ID[7:0]	CHIP_ID[7:0]							
0x05	OTP_REV[7:0]	OTP_REV[7:0]							
0x06	STATUS_L[7:0]	STAT_VOUT	STAT_VRECT	STAT_WDOG	FSK_RCVD	RESERVED	RESERVED	OVER_VOLTAGE	OVER_CURRENT
0x07	STATUS_H[7:0]	OVER_TEMP	TX_OVER_CURRENT	TX_OVER_TEMP	RESERVED	TX_CONN	ASK_DEMOD_PING	ASK_DEMOD_IDCF	ASK_DEMOD_PT
0x08	INT_L[7:0]	VOUT_INT	VRECT_INT	WDOG_INT	FSK_RCVD_INT	RESERVED	RESERVED	OV_INT	OC_INT
0x09	INT_H[7:0]	OT_INT	TX_OC_INT	TX_OT_INT	RESERVED	TX_CONN_INT	ASK_DEMOD_PING_INT	ASK_DEMOD_IDCF_INT	ASK_DEMOD_PT_INT
0x0A	INT_ENABLE_L[7:0]	VOUT_INT_EN	VRECT_INT_EN	WDOG_INT_EN	FSK_RCVD_INT_EN	RESERVED	RESERVED	OV_INT_EN	OC_INT_EN
0x0B	INT_ENABLE_H[7:0]	OT_INT_EN	TX_OC_INT_EN	TX_OT_INT_EN	RESERVED	TX_CONN_INT_EN	ASK_DEMOD_PING_INT_EN	ASK_DEMOD_IDCF_INT_EN	ASK_DEMOD_PT_INT_EN
0x0C	INT_CLEAR_L[7:0]	VOUT_INT_CLR	VRECT_INT_CLR	WDOG_INT_CLR	FSK_RCVD_INT_CLR	RESERVED	RESERVED	OV_INT_CLR	OC_INT_CLR
0x0D	INT_CLEAR_H[7:0]	OT_INT_CLR	TX_OC_INT_CLR	TX_OT_INT_CLR	RESERVED	TX_CONN_INT_CLR	ASK_DEMOD_PING_INT_CLR	ASK_DEMOD_IDCF_INT_CLR	ASK_DEMOD_PT_INT_CLR
0x0E	CHARGE_STATUS[7:0]	CHARGE_STATUS[7:0]							
0x0F	EPT_REASON[7:0]	EPT_REASON[7:0]							
0x10	VOUTVAL_H[7:0]	VOUTVAL[11:4]							
0x11	VOUTVAL_L[7:0]	RESERVED[3:0]				VOUTVAL[3:0]			
0x12	VOUTSET[7:0]	RESERVED	VOUTSET[6:0]						
0x13	VRECT_ADJ[7:0]	VRECT_ADJ[7:0]							
0x14	VRECTVAL_H[7:0]	VRECTVAL[11:4]							
0x15	VRECTVAL_L[7:0]	RESERVED[3:0]				VRECTVAL[3:0]			
0x16	ISENSEVAL_H[7:0]	ISENSEVAL[11:4]							
0x17	ISENSEVAL_L[7:0]	RESERVED[3:0]				ISENSEVAL[3:0]			
0x18	TDIE_VALUE[7:0]	TDIE_VALUE[7:0]							
0x19	OP_FREQ_L[7:0]	OP_FREQ[7:0]							
0x1A	OP_FREQ_H[7:0]	OP_FREQ[15:8]							
0x1B	PING_OP_FREQ_L[7:0]	PING_OP_FREQ[7:0]							

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0x1C	PING_OP_FREQ_H[7:0]	PING_OP_FREQ[15:8]							
0x1D	LDO_ILIMSET[7:0]	RESERVED[2:0]			LDO_ILIMSET[4:0]				
0x1E	TX_ILIMSET[7:0]	RESERVED[2:0]			TX_ILIMSET[4:0]				
0x1F	SYS_OP_MODE[7:0]	SYS_OP_MODE[7:0]							
0x20	RX_COM[7:0]	RESERVED	RESERVED	CLEAR_INTERRUPT	SEND_CHARGE_STATUS	SEND_EPT	RESERVED	TOGGLE_LDO	SEND_RX_DATA
0x21	PPP_HEADER[7:0]	PPP_HEADER[7:0]							
0x22	RX_DATA_VALUE0[7:0]	RX_DATA_VALUE0[7:0]							
0x23	RX_DATA_VALUE1[7:0]	RX_DATA_VALUE1[7:0]							
0x24	RX_DATA_VALUE2[7:0]	RX_DATA_VALUE2[7:0]							
0x25	RX_DATA_VALUE3[7:0]	RX_DATA_VALUE3[7:0]							
0x26	RX_DATA_VALUE4[7:0]	RX_DATA_VALUE4[7:0]							
0x27	FSK_DATA_VALUE0[7:0]	FSK_DATA_VALUE0[7:0]							
0x28	FSK_DATA_VALUE1[7:0]	FSK_DATA_VALUE1[7:0]							
0x29	FSK_DATA_VALUE2[7:0]	FSK_DATA_VALUE2[7:0]							
0x2A	TX_FOP_SET_L[7:0]	TX_FOP_SET[7:0]							
0x2B	TX_FOP_SET_H[7:0]	RESERVED[6:0]							TX_FOP_SET[8]
0x2C	TX_FOP_TON_SET_L[7:0]	TX_FOP_TON_SET[7:0]							
0x2D	TX_FOP_TON_SET_H[7:0]	RESERVED[6:0]							TX_FOP_TON_SET[8]
0x34	TX_WPC_HEADER[7:0]	TX_WPC_HEADER[7:0]							
0x35	TX_WPC_DATA0[7:0]	TX_WPC_DATA0[7:0]							
0x36	TX_WPC_DATA1[7:0]	TX_WPC_DATA1[7:0]							
0x37	TX_WPC_DATA2[7:0]	TX_WPC_DATA2[7:0]							
0x38	TX_WPC_DATA3[7:0]	TX_WPC_DATA3[7:0]							
0x39	TX_WPC_DATA4[7:0]	TX_WPC_DATA4[7:0]							
0x3A	TX_WPC_DATA5[7:0]	TX_WPC_DATA5[7:0]							
0x3B	TX_WPC_DATA6[7:0]	TX_WPC_DATA6[7:0]							

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0x3C	TX_WPC_DATA7[7:0]	TX_WPC_DATA7[7:0]							
0x3D	TX_WPC_CHECK-SUM[7:0]	TX_WPC_CHECKSUM[7:0]							
0x3E	FOD_X0[7:0]	FOD_X0[7:0]							
0x3F	FOD_Y0[7:0]	FOD_Y0[7:0]							
0x40	FOD_X1[7:0]	FOD_X1[7:0]							
0x41	FOD_Y1[7:0]	FOD_Y1[7:0]							
0x42	FOD_X2[7:0]	FOD_X2[7:0]							
0x43	FOD_Y2[7:0]	FOD_Y2[7:0]							
0x44	FOD_X3[7:0]	FOD_X3[7:0]							
0x45	FOD_Y3[7:0]	FOD_Y3[7:0]							
0x46	FOD_X4[7:0]	FOD_X4[7:0]							
0x47	FOD_Y4[7:0]	FOD_Y4[7:0]							
0x48	FOD_X5[7:0]	FOD_X5[7:0]							
0x49	FOD_Y5[7:0]	FOD_Y5[7:0]							
0x4A	FOD_X6[7:0]	FOD_X6[7:0]							
0x4B	FOD_Y6[7:0]	FOD_Y6[7:0]							
0x4C	FOD_X7[7:0]	FOD_X7[7:0]							
0x4D	FOD_Y7[7:0]	FOD_Y7[7:0]							
0x4E	FOD_X8[7:0]	FOD_X8[7:0]							
0x4F	FOD_Y8[7:0]	FOD_Y8[7:0]							
0x50	FOD_X9[7:0]	FOD_X9[7:0]							
0x51	FOD_Y9[7:0]	FOD_Y9[7:0]							
0x52	FOD_X10[7:0]	FOD_X10[7:0]							
0x53	FOD_Y10[7:0]	FOD_Y10[7:0]							
0x54	FOD_X11[7:0]	FOD_X11[7:0]							
0x55	FOD_Y11[7:0]	FOD_Y11[7:0]							
0x56	FOD_X12[7:0]	FOD_X12[7:0]							
0x57	FOD_Y12[7:0]	FOD_Y12[7:0]							
0x58	FOD_X13[7:0]	FOD_X13[7:0]							
0x59	FOD_Y13[7:0]	FOD_Y13[7:0]							
0x5A	FOD_X14[7:0]	FOD_X14[7:0]							
0x5B	FOD_Y14[7:0]	FOD_Y14[7:0]							
0x5C	FOD_X15[7:0]	FOD_X15[7:0]							
0x5D	FOD_Y15[7:0]	FOD_Y15[7:0]							
0x62	OV_CLAMP_VOLT-AGE[7:0]	RESERVED[2:0]			POV_ CLAMP_ VOLTAGE	RESERVED[1:0]		OV_CLAMP_VOLT-AGE[1:0]	
0x63	TX_LAST_CEP[7:0]	TX_LAST_CEP[7:0]							

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0x64	TX_LAST_RPP[7:0]	TX_LAST_RPP[7:0]							
0x65	TX_LAST_PCHP[7:0]	TX_LAST_PCHP[7:0]							
LDO									
0x70	LDO_WPDET_CNFG[7:0]	WPDET_H_DEBOUNCE[1:0]		WPDET_L_DEBOUNCE[1:0]		WPDET_H_THRESHOLD[1:0]		WPDET_L_THRESHOLD[1:0]	
VRECT_TARGET									
0xBA	VRECT_TARGET_X0[7:0]	VRECT_TARGET_X0[7:0]							
0xBB	VRECT_TARGET_Y0[7:0]	VRECT_TARGET_Y0[7:0]							
0xBC	VRECT_TARGET_PMA_Y0[7:0]	VRECT_TARGET_PMA_Y0[7:0]							
0xBD	VRECT_TARGET_X1[7:0]	VRECT_TARGET_X1[7:0]							
0xBE	VRECT_TARGET_Y1[7:0]	VRECT_TARGET_Y1[7:0]							
0xBF	VRECT_TARGET_PMA_Y1[7:0]	VRECT_TARGET_PMA_Y1[7:0]							
0xC0	VRECT_TARGET_X2[7:0]	VRECT_TARGET_X2[7:0]							
0xC1	VRECT_TARGET_Y2[7:0]	VRECT_TARGET_Y2[7:0]							
0xC2	VRECT_TARGET_PMA_Y2[7:0]	VRECT_TARGET_PMA_Y2[7:0]							
0xC3	VRECT_TARGET_X3[7:0]	VRECT_TARGET_X3[7:0]							
0xC4	VRECT_TARGET_Y3[7:0]	VRECT_TARGET_Y3[7:0]							
0xC5	VRECT_TARGET_PMA_Y3[7:0]	VRECT_TARGET_PMA_Y3[7:0]							
0xC6	VRECT_TARGET_X4[7:0]	VRECT_TARGET_X4[7:0]							
0xC7	VRECT_TARGET_Y4[7:0]	VRECT_TARGET_Y4[7:0]							
0xC8	VRECT_TARGET_PMA_Y4[7:0]	VRECT_TARGET_PMA_Y4[7:0]							
0xC9	VRECT_TARGET_X5[7:0]	VRECT_TARGET_X5[7:0]							
0xCA	VRECT_TARGET_Y5[7:0]	VRECT_TARGET_Y5[7:0]							
0xCB	VRECT_TARGET_PMA_Y5[7:0]	VRECT_TARGET_PMA_Y5[7:0]							

Register Map (continued)

ADDRESS	NAME	MSB							LSB
0xCC	VRECT_TARGET_X6[7:0]	VRECT_TARGET_X6[7:0]							
0xCD	VRECT_TARGET_Y6[7:0]	VRECT_TARGET_Y6[7:0]							
0xCE	VRECT_TARGET_PMA_Y6[7:0]	VRECT_TARGET_PMA_Y6[7:0]							
0xCF	VRECT_TARGET_X7[7:0]	VRECT_TARGET_X7[7:0]							
0xD0	VRECT_TARGET_Y7[7:0]	VRECT_TARGET_Y7[7:0]							
0xD1	VRECT_TARGET_PMA_Y7[7:0]	VRECT_TARGET_PMA_Y7[7:0]							
DEMOD									
0xDB	PMA_ADV_DATA[7:0]	PMA_ADV_DATA[7:0]							
0xDC	PMA_ADV_CRC[7:0]	RESERVED[3:0]				PMA_ADV_CRC[3:0]			

CHIP_ID (0x00)

BIT	7	6	5	4	3	2	1	0
Field	CHIP_ID[7:0]							
Reset	0b0001_0010							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CHIP_ID	7:0	-

OTP_REV (0x05)

BIT	7	6	5	4	3	2	1	0
Field	OTP_REV[7:0]							
Reset	0b0000_0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
OTP_REV	7:0	OTP revision

STATUS_L (0x06)

BIT	7	6	5	4	3	2	1	0
Field	STAT_ VOUT	STAT_ VRECT	STAT_ WDOG	FSK_RCVD	RESERVED	RESERVED	OVER_ VOLTAGE	OVER_ CURRENT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
STAT_VOUT	7	1: LDO is ON 0: LDO is OFF (Rx ONLY)
STAT_VRECT	6	1: V_{RECT} is over UVLO (Rx ONLY)
STAT_WDOG	5	1: Watchdog timer expires 0: No watchdog timer expires
FSK_RCVD	4	1: FSK data sent by transmitter is received 0: No FSK data
RESERVED	3	RSVD
RESERVED	2	RSVD
OVER_VOLTAGE	1	1: Overvoltage (V_{RECT}) 0: Normal
OVER_CURRENT	0	1: Overcurrent (LDO output current) in Rx mode 0: Normal

STATUS_H (0x07)

BIT	7	6	5	4	3	2	1	0
Field	OVER_ TEMP	TX_OVER_ CURRENT	TX_OVER_ TEMP	RESERVED	TX_CONN	ASK_DE-MOD_PING	ASK_DE-MOD_IDCF	ASK_DE-MOD_PT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OVER_TEMP	7	1: Overtemperature in Rx mode 0: Normal
TX_OVER_CURRENT	6	1: Overcurrent in Tx mode 0: Normal
TX_OVER_TEMP	5	1: Overtemperature in Tx mode 0: Normal
RESERVED	4	RSVD
TX_CONN	3	1: Power transfer established in Tx mode 0: No power transfer established
ASK_DEMOD_PING	2	1: Packet received in PING phase 0: No packet
ASK_DEMOD_IDCF	1	1: Packet received in ID and configuration phase 0: No packet
ASK_DEMOD_PT	0	1: Packet received in power transfer phase (count CEP if that is non zero) 0: No packet

INT_L (0x08)

BIT	7	6	5	4	3	2	1	0
Field	VOUT_INT	VRECT_INT	WDOG_INT	FSK_ RCVD_INT	RESERVED	RESERVED	OV_INT	OC_INT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
VOUT_INT	7	1: V_{OUT} state change (off to on, on to off)
VRECT_INT	6	1: V_{RECT} is over UVLO (Rx ONLY)
WDOG_INT	5	1: Watchdog timer expired
FSK_RCVD_INT	4	1: FSK data sent by transmitter is received
RESERVED	3	RSVD
RESERVED	2	RSVD
OV_INT	1	1: Overvoltage (V_{RECT}) 0: Normal
OC_INT	0	1: Overcurrent (LDO output current) in Rx mode 0: Normal

INT_H (0x09)

BIT	7	6	5	4	3	2	1	0
Field	OT_INT	TX_OC_INT	TX_OT_INT	RESERVED	TX_CONN_ INT	ASK_DE-MOD_ PING_INT	ASK_DE-MOD_ IDCF_INT	ASK_DE-MOD_PT_ INT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
OT_INT	7	1: Overtemperature in Rx mode
TX_OC_INT	6	1: Overcurrent in Tx mode
TX_OT_INT	5	1: Overtemperature in Tx mode
RESERVED	4	RSVD
TX_CONN_INT	3	1: Power tranfer phase established in Tx mode
ASK_DEMOD_PING_ INT	2	1: Packet received in PING Phase
ASK_DEMOD_IDCF_ INT	1	1: Packet received in ID and configuration phase
ASK_DEMOD_PT_INT	0	1: Packet received in power transfer phase