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MAX78615+LMU

Isolated Energy Measurement Processor for Load Monitoring Units

GENERAL DESCRIPTION

The MAX78615+LMU is an isolated energy measurement processor (EMP) for load monitoring and control of any 2-wire single-phase or 3-wire split-phase (120/180°) AC circuit. It provides flexible sensor configuration of up to two MAX78700 (four analog inputs) and numerous host interface options for easy integration into any system architecture.

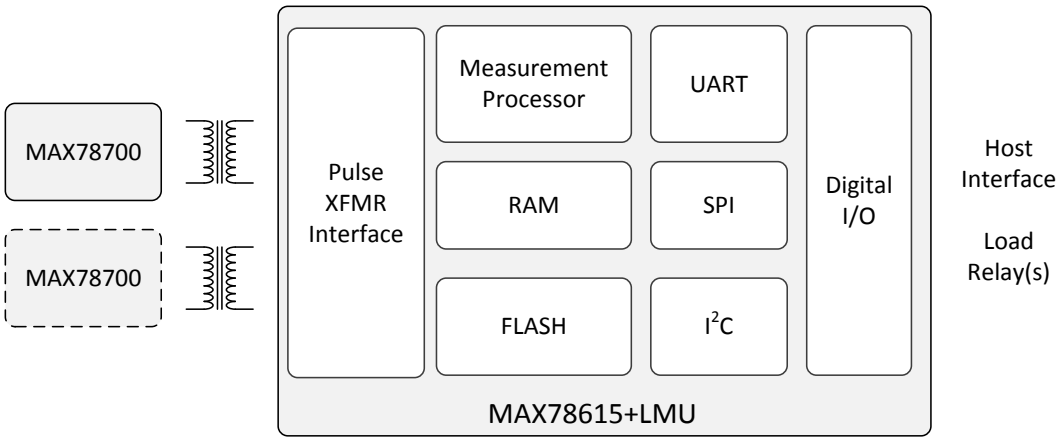
The internal 24-bit processor and field upgradeable firmware performs all the necessary signal processing, compensation, and data formatting for accurate real-time measurement. Energy accumulation, alarm monitoring, and fault detection schemes minimize the overhead requirements of the host interface and/or network. The integrated flash memory also provides for nonvolatile storage of input configurations and calibration coefficients.

APPLICATIONS

- Building Automation Systems (Commercial, Industrial)
- Inverters and Renewable Energy Systems
- Level 1 and 2 EV Charging Systems
- Grid-Friendly Appliances and Smart Plugs

BENEFITS AND FEATURES

- Best-in-Class Embedded Algorithms Support Highly Accurate Electricity Measurements
  - Voltage, Current and Frequency
  - Active, Reactive and Apparent Power/Energy
  - Power Quality Measurements including Peak Current and Harmonic Content
  - Digital Temperature Compensation
- Configurable Device Provides Design Flexibility
  - Nonvolatile Storage of Calibration and Configuration Parameters
  - SPI, I^2C, and UART Interface Options
  - Configurable I/O Pins for Alarm Signaling, Address Pins, or User Control
- Highly Integrated Features Support Compact Designs and Reduced Bill of Materials
  - Small 24-TQFN Package
  - Internal or External Oscillator Timing References
  - Remote ADC Interfaces Provide Cost-Effective and Reliable Isolation
  - Quick Calibration Routines Minimize Manufacturing (System) Cost
  - Digital Temperature Compensation



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6571; Rev 2; 1/15

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ABSOLUTE MAXIMUM RATINGS

(All voltages with respect to ground.)

Voltage Range
V_{CC} ..... -0.5V to +4.6V

Voltage Range
CH1N, CH1P, CH2N, CH2P, CH3N, CH3P ..... -0.5V to (V_{CC} + 0.5V)

Voltage Range
XIN, XOUT ..... -0.5V to +3.0V

Voltage Range
IFC0, IFC1, SSB/DIR/SCL, SDO/TX/SDAO, SDI/RX/SDAI, $\overline{\text{RESET}}$, SPCK/ADDR0 ..... -0.5V to +3.0V

Voltage Range, Any Digital Pin Configured as Input ..... -0.5V to +6.0V

Maximum Current
CH1N, CH1P, CH2N, CH2P, CH3N, CH3P ..... -50mA to +50mA

Maximum Current Range
XIN, XOUT ..... -10mA to +10mA

Maximum Current
IFC0, IFC1, SSB/DIR/SCL, SDO/TX/SDAO, SDI/RX/SDAI, $\overline{\text{RESET}}$, SPCK/ADDR0 ..... -30mA to +30mA

Maximum Current, Any Digital Pin Configured as Input ..... 10mA to +10mA

Operating Junction Temperature
Peak, 100ms ..... +140°C
Continuous ..... +125°C

Storage Temperature Range ..... -45°C to +165°C

Lead Temperature (soldering, 10s) ..... +260°C

Soldering Temperature (reflow) ..... +300°C

ESD Stress, All Pins ..... ±4kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED EXTERNAL COMPONENTS

NAME	FROM	TO	FUNCTION	VALUE	UNITS
XTAL	XIN	XOUT	20.000MHz	20.000	MHz
CXS	XIN	GND	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board)	18 ±10%	pF
CXL	XOUT	GND		18 ±10%	pF

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage (V_{3P3})	Normal operation	3.15	3.3	3.45	V
Operating Temperature		-40		+85	°C

PERFORMANCE SPECIFICATIONS

(Note that production tests are performed at room temperature.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT LOGIC LEVELS					
Digital High-Level Input Voltage (V_{IH})		2			V
Digital Low-Level Input Voltage (V_{IL})				0.8	V
OUTPUT LOGIC LEVELS					
Digital High-Level Output Voltage (V_{OH})	I_{LOAD} = 1mA	V_{CC} - 0.4			V
	I_{LOAD} = 10mA	V_{CC} - 0.6			
Digital Low-Level Output Voltage (V_{OL})	I_{LOAD} = 1mA	0		0.4	V
	I_{LOAD} = 10mA			0.5	
SUPPLY CURRENT					
V_{CC} Current	MAX78615+LMU only: V_{cc} = 3.3V		5.6		mA
	With one MAX78700: V_{cc} = 3.3V		7.8		
	With two MAX78700s: V_{cc} = 3.3V		10.0		
CRYSTAL OSCILLATOR					
XIN to XOUT Capacitance	(Note 1)		3		pF
Capacitance to GND (Note 1)	XIN		5		pF
	XOUT		5		
INTERNAL RC OSCILLATOR					
Nominal Frequency			20.000		MHz
Accuracy	At least one MAX78700 connected		±1.50		%
$\overline{\text{RESET}}$ **TIMING**					
Reset Pulse Fall Time	(Note 1)		1		µs
Reset Pulse Width	(Note 1)		5		µs
SPI SLAVE PORT					
SPCK Cycle Time (t_{SPIcyc})	(Note 1)	1			µs
Enable Lead Time ($t_{SPILead}$)	(Note 1)	15			ns
Enable Lag Time (t_{SPILag})	(Note 1)	0			ns
SPCK Pulse Width (t_{SPIW})	High (Note 1)	250			ns
	Low (Note 1)	250			
SSB to First SPCK Fall (t_{SPISCK})	Ignore if SPCK is low when SSB falls (Note 1)		2		ns
Disable Time (t_{SPIDIS})	(Note 1)		0		ns
SPCK to Data Out (SDO) (t_{SPIEV})	(Note 1)			25	ns
Data Input Setup Time (SDI) (t_{SPISU})	(Note 1)	10			ns
Data Input Hold Time (SDI) (t_{SPIH})	(Note 1)	5			ns

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I^2C SLAVE PORT					
Bus Idle (Free) Time Between Transmissions (STOP/START) (t_{BUF})	(Note 1)	1500			ns
I^2C Input Fall Time (t_{ICF})	(Notes 1, 2)	20		300	ns
I^2C Input Rise Time (t_{ICR})	(Notes 1, 2)	20		300	ns
I^2C START or Repeated START Condition Hold Time (t_{STH})	(Note 1)	500			ns
I^2C START or Repeated START Condition Setup Time (t_{STS})	(Note 1)	600			ns
I^2C Clock High Time (t_{SCH})	(Note 1)	600			ns
I^2C Clock Low Time (t_{SCL})	(Note 1)	1300			ns
I^2C Serial Data Setup Time (t_{SDS})	(Note 1)	100			ns
I^2C Serial Data Hold Time (t_{SDH})	(Note 1)	10			ns
I^2C Valid Data Time (t_{VDA}): SCL Low to SDA Output Valid ACK Signal from SCL Low to SDA (Out) Low	(Note 1)			900	ns

Note 1: Guaranteed by design, not subject to test.

Note 2: Dependent on bus capacitance.

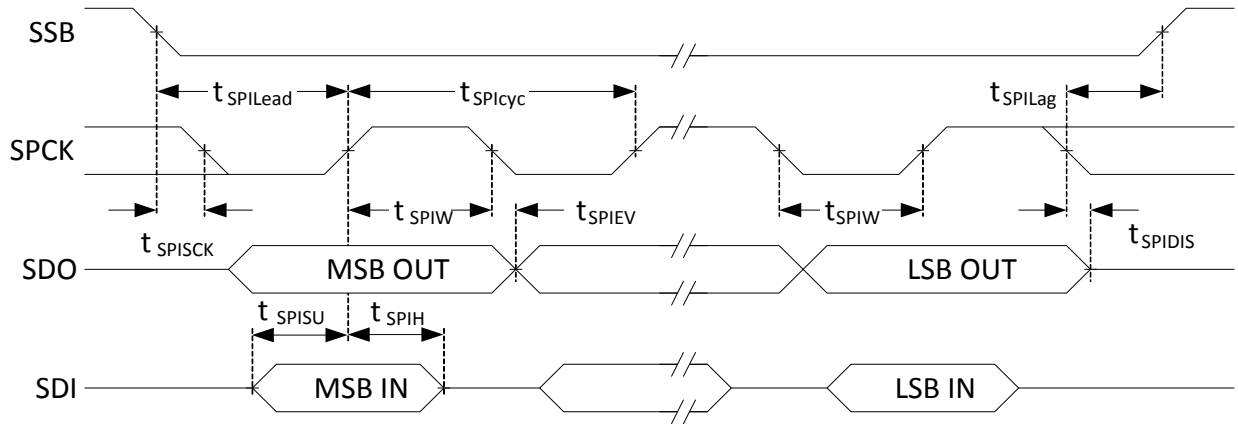


Figure 1. SPI Timing

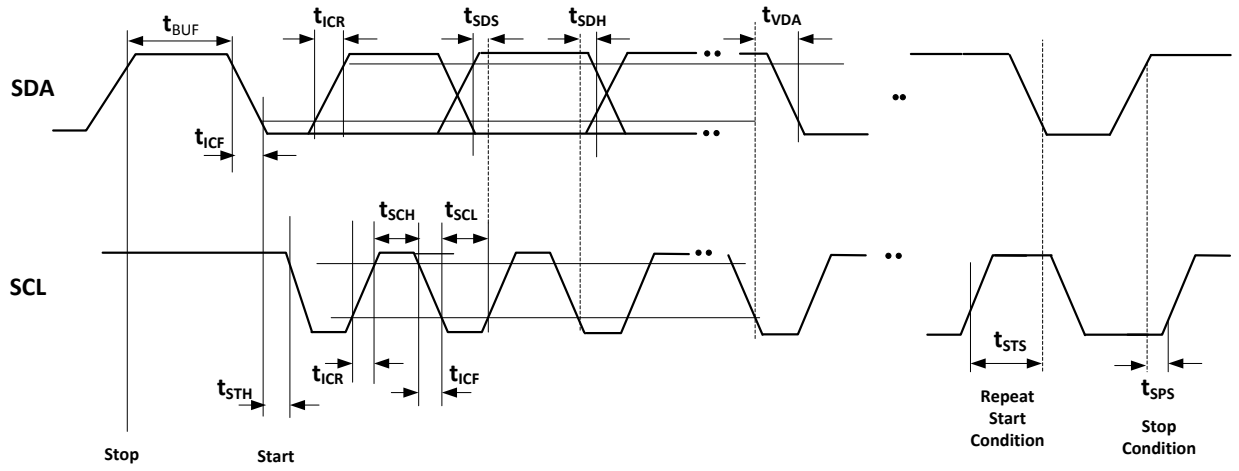


Figure 2. I^2C Timing

Pin Configuration

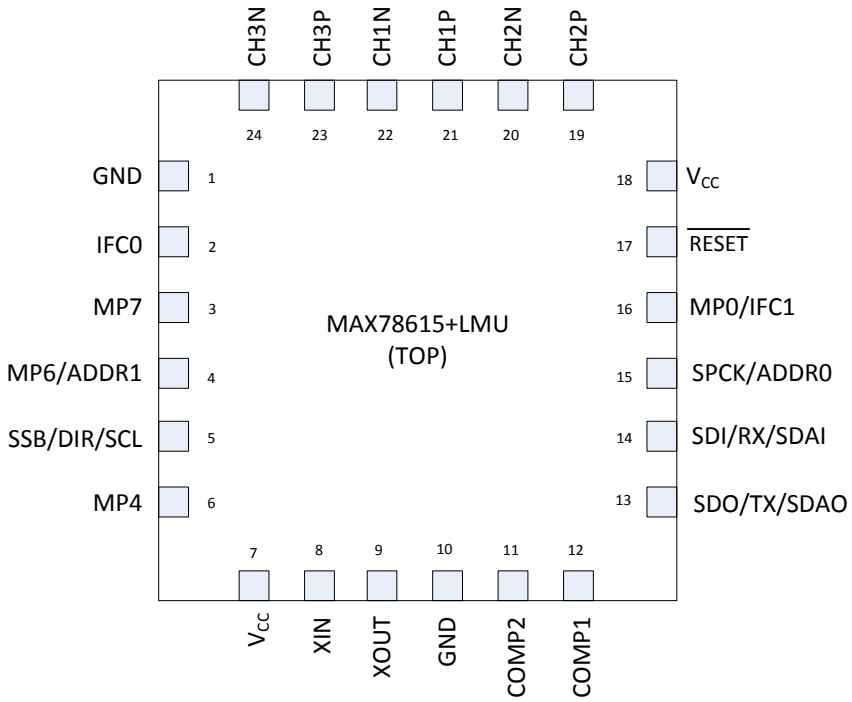


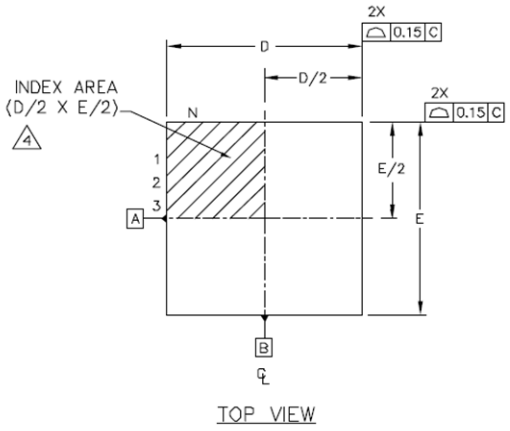
Figure 3. TQFN Package Pinout

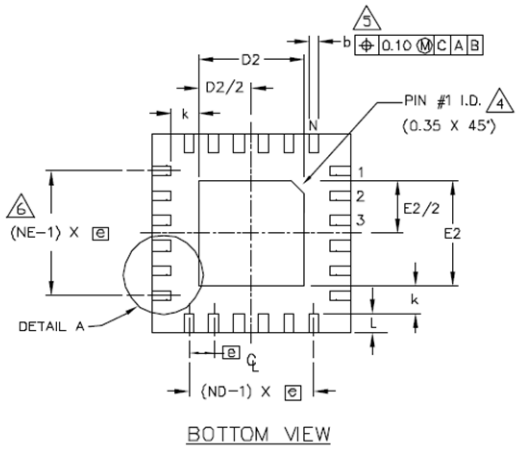
PIN	SIGNAL	FUNCTION	PIN	SIGNAL	FUNCTION
1	GND	Ground	13	SDO/TX/SDAO	SPI DATA OUT/UART Tx/ I^2C Data Out
2	IFC0	IFC1/SPI (1 = IFC1; 0 = SPI)	14	SDI/RX/SDAI	SPI DATA IN/UART Rx/ I^2C Data In
3	MP7	Multipurpose DIO	15	SPCK/ADDR0	SPI CLOCK / Address Pin
4	MP6/ADDR1	Multipurpose DIO / Address Pin	16	MP0/IFC1	I^2C/UART (1 = I^2C; 0 = UART)
5	SSB/DIR/SCL	Slave Select (SPI) / RS-485 TX-Rx / I^2C Serial Clock	17	$\overline{RESET}$	Active-Low Reset Input
6	MP4	Multipurpose DIO	18	V_{CC}	3.3V DC Supply
7	V_{CC}	3.3V DC Supply	19	CH2P	Channel 2 Input
8	XIN	Crystal Oscillator Driver Input	20	CH2N	Channel 2 Input
9	XOUT	Crystal Oscillator Driver Output	21	CH1P	Channel 1 Input
10	GND	Ground	22	CH1N	Channel 1 Input
11	COMP2	Reserved; No Connection	23	CH3P	Reserved; No Connection
12	COMP1	Reserved; No Connection	24	CH3N	Reserved; No Connection

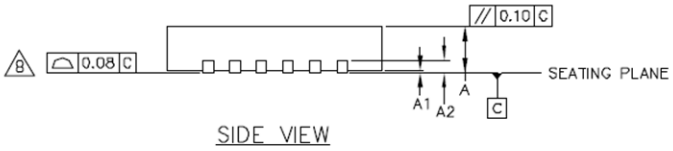
Package Information

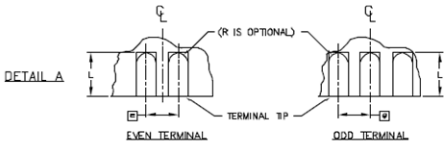
For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
24 TQFN	T2444+4	21-0139	90-0022









PKG	24L 4x4		
REF.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.0	0.02	0.05
A2		0.20 REF	
b	0.18	0.23	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e		0.50 BSC.	
k	0.25	-	-
L	0.30	0.40	0.50
N		24	
ND		6	
NE		6	
Jedec Var.		WGGD-2	

On-Chip Resources Overview

The MAX78615+LMU device, when connected with an isolated MAX78700, integrates all the hardware blocks required for accurate AC power and energy measurement. Included in the MAX78615 are:

- Oscillator circuits and clock management logic
- Power-on reset, watchdog timer, and reset circuitry
- 24-bit energy measurement processor (EMP) with RAM and flash memory
- Serial UART, SPI, I^2C interfaces and multipurpose digital I/O
- Pulse Transformer Interface (for connection to one or more MAX78700)

Block Diagram

The following is a block diagram of the hardware resources available on the MAX78615+LMU.

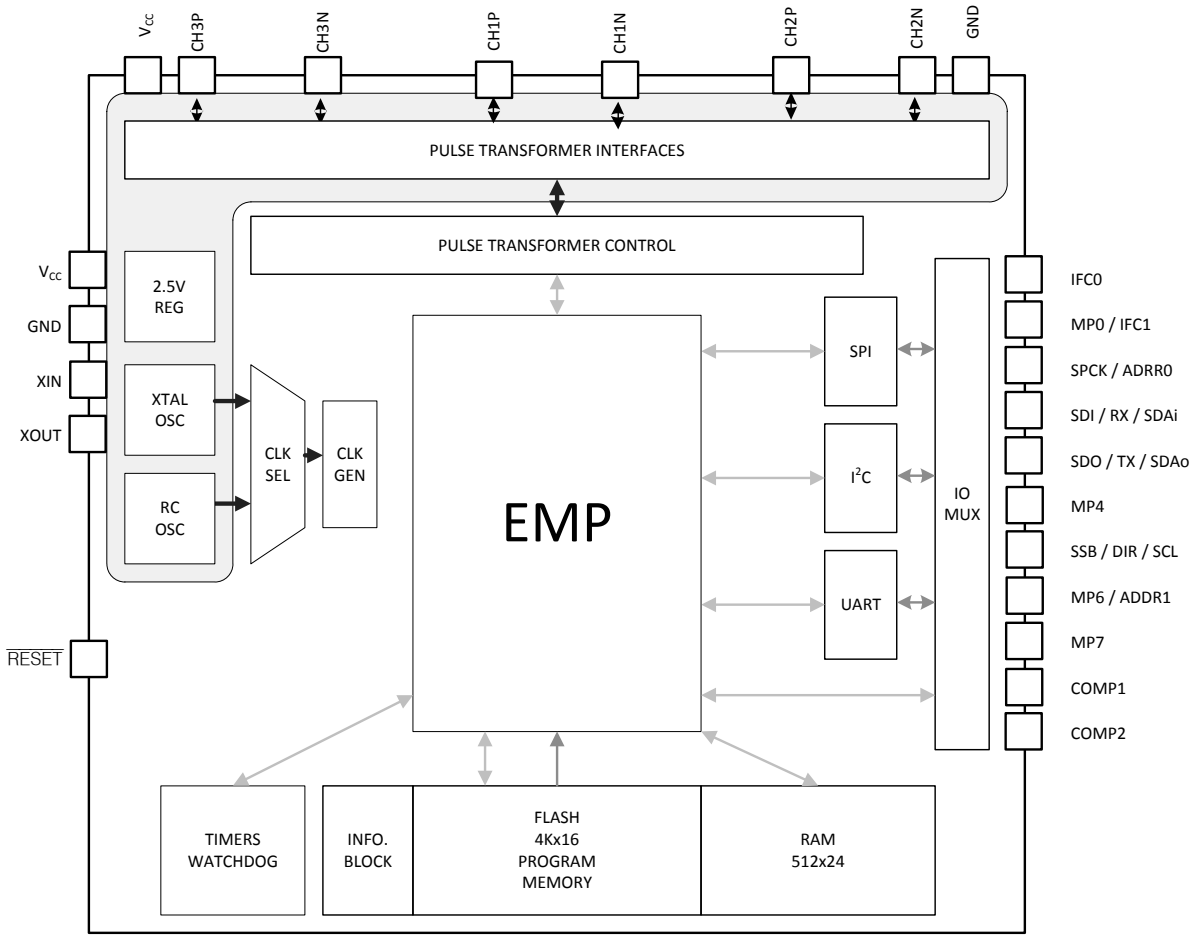


Figure 4. Block Diagram

Clock Management

The device can be clocked by either a trimmed internal RC oscillator or by oscillator circuitry that relies on an external crystal. The internal RC oscillator provides an accurate clock source for UART baud rate generation. Only time based calculations such as line frequency and watt-hour (energy) are affected by clock accuracy.

The chip hardware automatically handles the clock sources logic and distributes the clock to the rest of the device. Upon reset or power-on, the device will utilize the internal RC oscillator circuit for the first 1024 clock cycles, allowing the external crystal adequate time to start-up. The device will then automatically select the external clock, if available. It will also automatically switch back to the internal oscillator in the event of a failure with the external oscillator. This condition is also monitored by the processor and available to the user in the STATUS register.

The MAX78615+LMU external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. The figure below shows the typical connection of the external crystal. This oscillator is self biasing and therefore an external resistor should NOT be connected across the crystal.

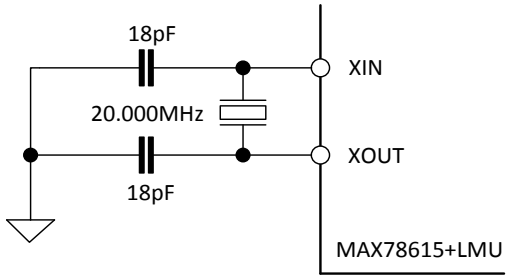


Figure 5. Crystal Connections

An external 20MHz system clock signal can also be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GND.

Alternatively, if no external crystal or clock is utilized, the XOUT pin should be connected to GND and the XIN pin left unconnected.

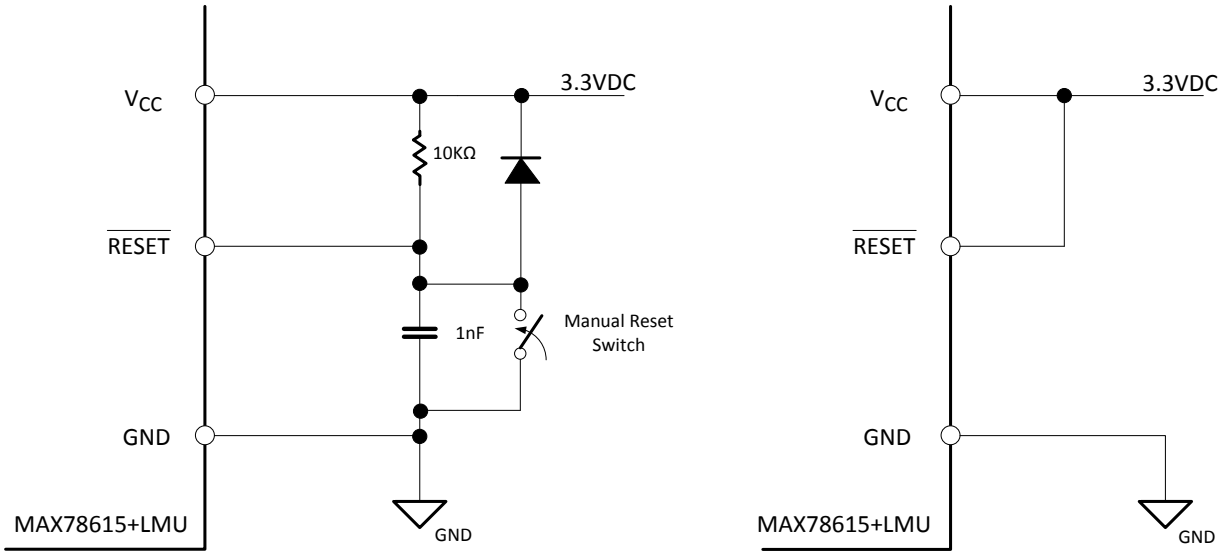
Power-On and Reset Circuitry

An on-chip power-on reset (POR) block monitors the supply voltage (V_{3P3D}) and initializes the internal digital circuitry at power-on. Once V_{3P3D} is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

In addition to the internal sources, a reset can be forced by applying a low level to the $\overline{\text{RESET}}$ pin. If the $\overline{\text{RESET}}$ pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until $\overline{\text{RESET}}$ has been held low for at least 1µs.

Once initiated, the reset mode persists until the $\overline{\text{RESET}}$ is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor (EMP) begins executing from address 0.

If not used, the $\overline{\text{RESET}}$ pin can be connected either directly or through a pullup resistor to V_{3P3D} supply. A simple connection diagram is shown below.



a) External $\overline{\text{RESET}}$ Connection Example

b) Unused $\overline{\text{RESET}}$ Connection Example

Figure 6. Connecting the $\overline{\text{RESET}}$ Pin

Watchdog Timer

A Watchdog Timer (WDT) block detects any software processing errors. The software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

Pulse Transformer Interface

Up to three isolation interfaces (channels) are provided to control, configure, and read measurement data from a MAX78700. Power pulses are spaced at 10.00MHz/6 (600ns period) with write and read pulses located in between. Within every power pulse cycle a write data pulse and a read data pulse is inserted. Power and write pulses come from the MAX78615+LMU, read pulses come from the MAX78700.

24-Bit Energy Measurement Processor (EMP)

The MAX78615+LMU integrates a dedicated 24-bit signal processor that performs the entire digital signal processing necessary for energy measurement, alarm generation, calibration, compensation, etc. for the following section provides a description of functionality and operations.

Flash and RAM

The MAX78615+LMU includes 8KB of on-chip flash memory. The flash memory primarily contains program code, but also stores calibration data and defaults for select nonvolatile configuration registers. The device also includes 1.5KB of on-chip RAM which contains the values of input and output registers and is utilized by the processor for its operations.

Multipurpose DIOs

There are a total of nine digital input/outputs (DIOs) on the MAX78615+LMU device. Some are dedicated to serial interface communications and configuration. Others are multipurpose I/O that can be used as simple push-pull outputs under user control or routed to special purpose internal signals like alarm signaling and relay control.

Communication Interface

The MAX78615+LMU includes three communication interfaces: UART, SPI, and I^2C. Since the I/O pins are shared, only one mode is supported at a time. Interface configuration and address pins are sampled at power-on or reset to determine which interface will be active and to set device addresses.

Functional Description and Operation

This section describes the operation and configuration of the MAX78615+LMU. It includes the flow of measurement data, relevant calculations, alarm monitoring, I/O control, and user configurations.

Measurement Interface

The MAX78615+LMU incorporates an isolated measurement interface for simplified integration into any single-phase system. This section describes the configuration and signal conditioning of the raw data received from the MAX78700.

Settings and calibration parameters described in this section can be saved to flash memory and automatically initialized upon power on or reset.

AFE Input Multiplexer

The MAX78615+LMU processes data from up to four (4) external sensors with an effective sample rate of 1.767kS/s for each multiplexer slot. Two differential sensor inputs are implemented on each MAX78700.

Sensor Slot	MAX78700 Analog Input	Input Type
S0	Channel 1- INAP/N	Voltage
S1	Channel 1- INBP/N	Current
S2	Channel 2- INAP/N	Voltage
S3	Channel 2- INBP/N	Current

High Pass Filters and Offset Removal

Offset registers for each analog input contain values to be subtracted from the raw ADC outputs for the purpose of removing inherent system DC offsets from any calculated power and RMS values. These registers are signed fixed point numbers with a possible range of -1.0 to 1 - LSB. They default to 0 and can be manually changed by the user or integrated offset calibration routines.

Register	Description
S1_OFFS	Current Input S1 Offset Calibration
S0_OFFS	Voltage Input S0 Offset Calibration
S3_OFFS	Current Input S3 Offset Calibration
S2_OFFS	Voltage Input S2 Offset Calibration

Alternatively, the user can enable an integrated High Pass Filter (HPF) to dynamically update the offset registers every accumulation interval. During each accumulation interval (or low-rate cycle) the HPF calculates the median or DC average of each input. Adjustable coefficients determine what portion of the measured offset is combined with the previous offset value.

HPF_COEF_x registers contain signed fixed point numbers with a usable range of 0 to 1 - LSB (0.99999), negative values are not supported. By default, they are initialized to 0.5 (0x400000) meaning the new offset value will come from one-half the measured offset and one-half will come from the previous offset value. Setting them to 1.0 (0x7FFFFF) causes the entire measured offset to be applied to the offset register enabling lump-sum offset removal. Setting them to zero disables any dynamic update of the offset registers by the HPF.

Register	Description
HPF_COEF_I	HPF coefficient for S1 and S3 current inputs
HPF_COEF_V	HPF coefficient for S0 and S2 voltage inputs

To allow the DC component of the load current to be included in the measurement (i.e. half-wave rectified current waveforms), the HPF_COEF_I coefficients must be set to zero.

Using the offset calibration routine will automatically set the filter coefficients to zero to disable the HPF.

Gain Correction

The system (sensors) and the MAX78615+LMU device inherently have gain errors that can be corrected by using the gain registers. These registers can be directly accessed and modified by an external processor or automatically updated by an integrated self calibration routine.

Input gain registers are signed fixed point numbers with the binary point to the left of bit 21. They are set to 1.0 by default and have a usable range of 0 to 4 - LSB, negative values are not supported. The gain equation for each input slot can be described as Sx = Sx * Sx_GAIN

Register	Description
S0_GAIN	Voltage Input S0 Gain Calibration.
S1_GAIN	Current Input S1 Gain Calibration
S2_GAIN	Voltage Input S2 Gain Calibration.
S3_GAIN	Current Input S3 Gain Calibration

Die Temperature Compensation

The MAX78615+LMU receives die temperature measurements from the isolated ADC devices (MAX78700). This data is used by the signal processor for correcting the voltage reference error (band gap curvature) and made available to the user in the TEMPC register.

Setting the Temperature Compensation (TC) bit in the Command Register allows the firmware to further adjust the system gain based on measured isolated die temperature. The isolated ADC die Temperature Offset is typically calibrated by the user during the calibration stage. Die temperature gain is set to a factory default value for most applications, but can be adjusted by the user. Note that temperature calibration cannot be combined with any gain or offset calibrations in the same command.

Register	Description
T_OFFS	Die Temperature Offset Calibration.
T_GAIN	Die Temperature Slope Calibration. Set by factory.

Voltage Reference Gain Adjustment

The isolated ADC on-chip precision bandgap voltage reference incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. It can be assumed that the part is trimmed at 22°C to produce a uniform voltage reference gain at that temperature. The voltage reference is digitally compensated over changes in measured die temperature using a quadratic equation.

Phase Compensation

Phase compensation registers are used to compensate for phase errors or time delays between the voltage input source and respective current source that are introduced by the off-chip sensor circuit. The user configurable registers are signed fixed point numbers with the binary point to the left of bit 21. Values are in units of high rate (1.767kHz) sample delays so each integer unit of delay is 566µs with a total possible delay of ±4 samples (roughly ±20° at 60Hz).

Register	Description
PHASECOMP1	Phase (delay) compensation for S1 input current
PHASECOMP3	Phase (delay) compensation for S3 input current

Example:

To compensate a phase error of 277.77µs (or 6° at 60Hz) introduced by a current transformer (CT) it is necessary to enter the following:

$$Phase\ Compensation = \frac{Phase\ Error}{\frac{1}{Sample\ Rate}}$$

$$Phase\ Compensation = \frac{277E^{-6}}{\frac{1}{1767}} = 0.48946$$

The value to be entered in the phase compensation register is therefore:

$$PComp = \ 0.48946 * 2^{21} = 1026470 = \ 0x0FA9A5$$

Voltage Input Configuration

The MAX78615+LMU supports multiple analog input configurations for determining the three potential voltage sources in a split-phase circuit. The device measures the voltage difference between any two references and uses this information to derive the voltages VA, VB, and VC as shown below.

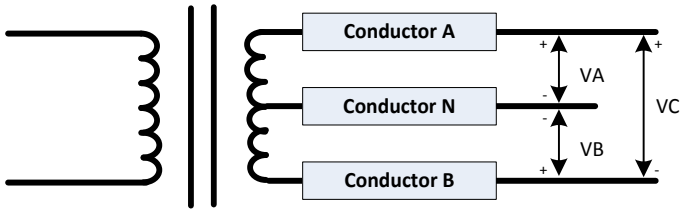


Figure 7. Defining Source Voltages

Each calculated voltage source (VA, VB, and VC) is derived from the following user configurable function of the voltage input multiplexer slots (S0, S2) and three pairs of multiplier values (M0, M2). This function derives source voltages VA, VB, and VC by summing S0 x M0 and S2 x M2.

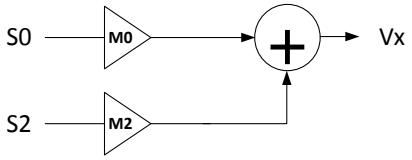


Figure 8. Computing Source Voltage

The user sets the multiplier values M0 and M2 for each voltage source in the CONFIG register using the model where a one (1) value adds the input, a two (2) value adds two of the input, a minus one (-1) value subtract the input, a zero (0) value does not include the input.

CONFIG Bits	**19:18**	**17:16**	**15:14**	**13:12**	**11:10**	**9:8**
Multiplier	M2	M0	M2	M0	M2	M0
Source	VC		VB		VA	

There are four choices for every M value as shown below.

Multiplier Bits	**00**	**01**	**10**	**11**
M (multiplier) Value	-1	0	1	2

The output registers VA, VB and VC are automatically scaled by a factor of 0.5 if M0 and M2 are both nonzero. For example, by setting the multiplier bits as follows:

$$Vc = +1 * S0 - 1 * S2$$

The effective content of the Vc register would result in:

$$Vc = \frac{(+1 * S0) + (-1 * S2)}{2}$$

This scaling is done to prevent the output register from overflowing.

Voltage Input Flowchart

The figure below illustrates the computational flowchart for VA, VB, and VC. The values for voltage input configuration register can be saved in flash memory and automatically restored at power-on or reset.

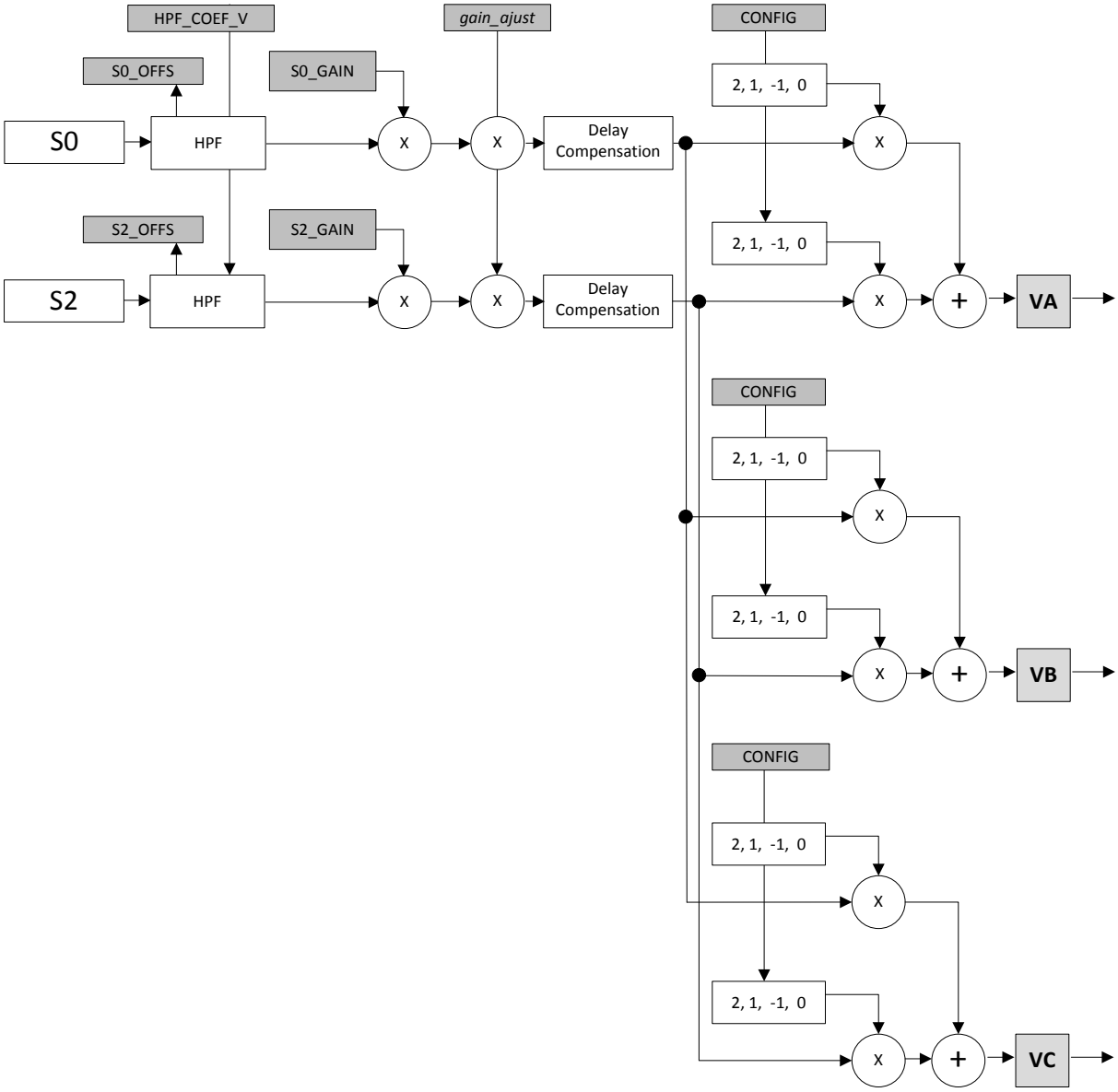


Figure 9. Voltage Input Flowchart

Current Input Configuration

The MAX78615+LMU supports multiple analog input configurations for determining the two load currents in a split-phase AC circuit. The device measures the current of any two conductors and uses this information to derive the load currents shown below.

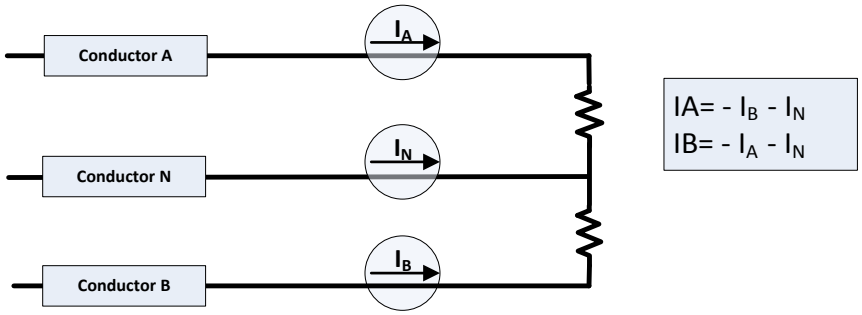


Figure 10. Current Input Configuration

Each calculated load current (IA and IB) is derived from the following function of the current input slots (S1 and S3) and 2 pairs of multiplier values (M1 and M3). This function derives source currents IA and IB by summing S1 x M1 and S3 x M3.

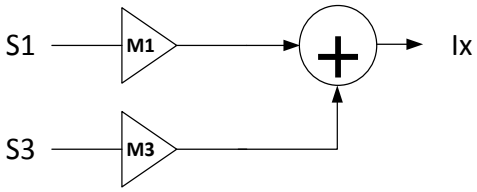


Figure 11. Computing Input Current

The user sets the multiplier values for each current source in the CONFIG register using the model where a one (1) value adds the input, a two (2) value adds two of the input, a minus one (-1) value subtract the input, a zero (0) value does not include the input.

CONFIG Bits	**7:6**	**5:4**	**3:2**	**1:0**
Multiplier	M3	M1	M3	M1
Source	IB		IA	

There are four choices for every M value as shown below.

Bit Values	**00**	**01**	**10**	**11**
M (multiplier) Value	-1	0	1	2

The output registers IA and IB are automatically scaled by a factor of 0.5 if M1 and M3 are both nonzero. For example, by setting the multiplier bits as follows:

$$IB = +1 * S1 - 1 * S3$$

The effective content of the Vc register would result in:

$$Vc = \frac{(+1 * S1) + (-1 * S3)}{2}$$

This scaling is done to prevent the output register from overflowing.

Current Input Flowchart

The figure below illustrates the computational flowchart for IA and IB. The values for current input configuration register can be saved in flash memory and automatically restored at power-on or reset.

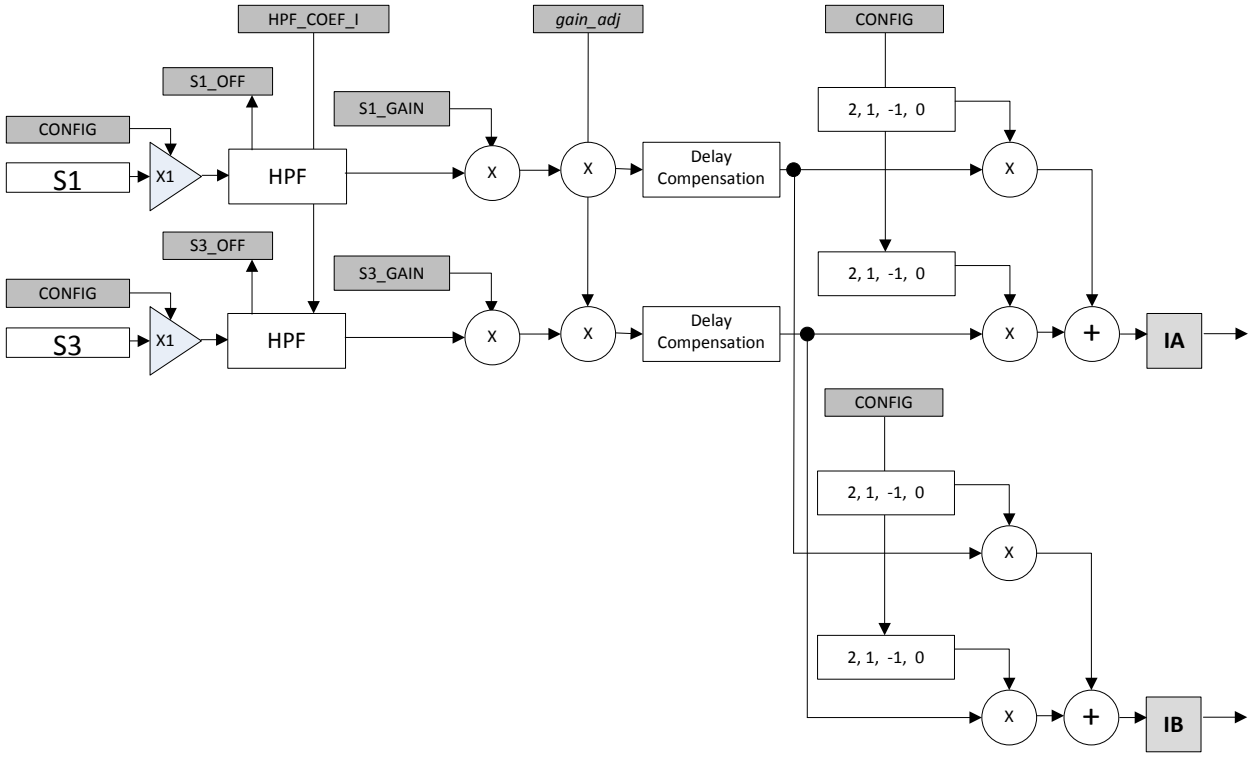


Figure 12. Current Input Flowchart

Data Refresh Rates

Instantaneous Voltage, Current, Power, and Quadrature measurement results are updated at the sample rate of 1.767kS/s and are generally not useful unless accessed with a high speed interface such as SPI. The CYCLE register is a 24-bit counter that increments every high-rate sample update and resets when low-rate results are updated.

Low-rate results, updated at a user configurable rate, are typically used and more suitable for most applications. The FRAME register is a counter that increments every accumulation interval. A data ready indicator in the STATUS register indicates when new data is available.

The high-rate samples are averaged to produce one low-rate result (known as an accumulation interval), increasing their accuracy and repeatability. Low-rate results include RMS voltages and currents, frequency, power, energy, and power factor. The accumulation interval can be based on a fixed number of ADC samples or locked to the incoming line voltage cycles.

If Line Lock is disabled, the accumulation interval defaults to a fixed time interval defined by the number of samples defined in the SAMPLES register (default of 400 samples or 226.4ms).

When the Line-Lock bit in the Command Register is set, and a valid AC voltage signal is present, the actual accumulation interval is stretched to the next positive zero crossing of the reference line voltage after the defined number of samples has been reached. If there is not a valid AC signal present and line lock is enabled, there is a 100 sample timeout implemented that would limit the accumulation interval to SAMPLES+100.

The DIVISOR register records the actual duration (number of high-rate samples) of the last low-rate interval whether or not Line-Lock is enabled.

Two bits in the CONFIG register allow the user to select the reference voltage slot for deriving zero-crossing detection and line frequency.

CONFIG[23:22]	**00**	**01**	**10**	**11**
Voltage reference	S0	S2	S0-S2	S0+S2

Scaling Registers

Most measurement data is reported in binary full-scale units with a value range of -1.0 to 1 - LSB. All full scale register readings correspond to the max analog input of 250mVpk (or 31.25mVpk with 8x gain). As an example, if 230V-peak at the input to the voltage divider gives 250mV-peak at the chip input, one would get a full scale register reading of 1 - LSB (0x7FFFFF) for instantaneous voltage. Similarly, if 30Apk at the sensor input provides 250mV-peak to the chip input, a full scale register value of 1 - LSB (0x7FFFFF) for instantaneous current would correspond to 30 amps. Full scale watts correspond to the result of full scale current and voltage so, in this example, full scale watts is 230 x 30 or 6900 watts.

Nonvolatile registers (IFSCALE and VFSCALE) are provided for storing the real-world current and voltage levels that apply to the full scale register readings for any given board design. Any host application can then format the measurement results to any data format as needed. The usage of these nonvolatile scratchpad registers is user defined and their content has no effect on the internal operations of the device.

Frequency data has a range of 0 to +32768Hz less one LSB (format S15.8). Temperature data has a fixed scaling with a range of -65536°C to +65536°C less one LSB (format S16.7). Energy data scaling is described in detail in the Energy Calculations section.

Calibration Routines

The MAX78615+LMU includes optional integrated calibration routines to modify gain and offset coefficients. The user can set up and initiate on-chip calibration routines through the Command Register. When in calibration mode, results are averaged over multiple accumulation intervals defined in the CALCYCS register.

The calibration routines will write the new coefficients to the relevant input registers. The user can then save the new coefficients into flash memory as defaults using the flash access command (ACC) in the Command Register.

See the Command Register section for more information on using calibration and flash access commands.

Voltage and Current Gain Calibration

In order to calibrate the gain parameters for voltage and current channels, a reference AC signal must be applied to the channel to be calibrated. The RMS value corresponding to the applied reference signal must be entered in the relevant target register (VTARGET, ITARGET). Considering calibration is done with low-rate RMS results, the value of the target register should never be set to a value above 70.7% of full-scale.

Initially, the value of the gain is set to unity for the selected channels. RMS values are then calculated on selected inputs and averaged over the number of measurement cycles set by the CALCYCS register. The new gain is calculated by dividing the appropriate Target register value by the averaged measured value. The new gain is then written to the select Gain registers unless an error occurred.

On a successful calibration, the command bits are cleared in the Command Register, leaving only the system setup bits. In case of a failed calibration, the bit in the Command Register corresponding to the failed calibration is left set.

Offset Calibration

To calibrate offsets, all signals should be removed from all analog inputs (although it is possible to do the calibration in the presence of AC signals). In the command, the user also specifies which channel(s) to calibrate. Target registers are not used for Offset calibration.

During the calibration process, each input is accumulated over the entire calibration interval as specified by the CALCYCS register. The result is divided by the total number of samples and written to the appropriate offset register if selected in the calibration command. Using the Offset Calibration command will set the respective HPF coefficients to zero thereby fixing the Sx_OFFS offset registers to their calibrated values. Upon completion of calibration, only the 0xCAxxxx bits of the Command Register are cleared.

Die Temperature Calibration

To re-calibrate the temperature sensor offsets of the MAX78700 devices, the user must first write the known chip temperature to the T_TARGET register. Next, the user initiates the Temperature Calibration Command in the Command Register. This will update the respective T_OFFSx offset parameters with a new offset based on the known temperature supplied by the user. The T_GAIN gain register is set by the factory and not updated with this routine. The range of the Die Temperature registers is -128 to +128 - LSB Degrees Celsius.

Voltage Channel Measurements

Instantaneous and quadrature voltage measurements are updated every sample while RMS Voltage and Peak Voltage are updated every accumulation interval (n samples). An AC voltage frequency measurement is also updated every low-rate interval.

Register	Description	Time Scale
VA VB VC	Instantaneous Voltage @ time t	1 sample
VQA VQB	Quadrature Voltage @ time t - 90°	
FREQ	AC Voltage Frequency	1 interval
VA_PEAK VB_PEAK	Peak Voltage in last interval	
VA_RMS VB_RMS VC_RMS	RMS Voltage of last interval	

Quadrature Voltage

The quadrature voltage is instantaneous voltage that is phase shifted (delayed) 90° from the respective input voltage.

Voltage Frequency

This output is a measurement of the fundamental frequency of the referenced AC voltage source with a range from 0Hz to 128Hz - LSB. This is a single reading per device.

Peak Voltage

This output is a capture of the largest magnitude instantaneous voltage source sample during the previous accumulation interval.

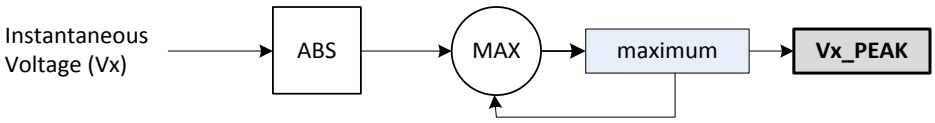


Figure 13. Peak Voltage Measurement