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### GENERAL DESCRIPTION

The MAX78630+PPM is an energy measurement processor (EMP) for polyphase power monitoring systems. It is designed for real-time monitoring for a variety of typical three-phase configurations in industrial applications. It is available in a 32-pin TQFN package.

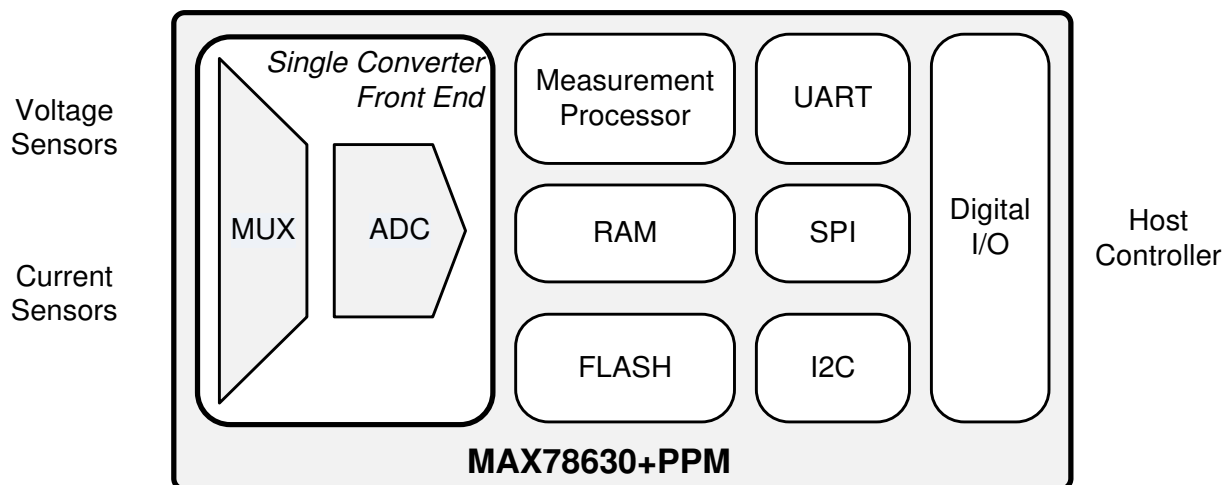
The MAX78630+PPM provides up to six analog inputs for interfacing to voltage and current sensors. Scaled voltages from the sensors are fed to the single converter front-end utilizing a high-resolution delta-sigma converter. Supported current sensors include current transformers (CT), Rogowski coils, and resistive shunts.

An embedded 24-bit measurement processor and firmware perform all necessary computations and data formatting for accurate reporting to the host. With integrated flash memory for storing nonvolatile calibration coefficients and device configuration settings, the MAX78630+PPM is capable of being a completely autonomous solution.

The MAX78630+PPM is designed to interface to the host processor via the UART interface. Alternatively, SPI or I<sup>2</sup>C may also be used.

### BENEFITS AND FEATURES

- Six Configurable Analog Inputs for Monitoring a Variety of Delta- and Wye-Connected Three-phase Topologies
- Supports Current Transformers (CT), Resistive Shunts, and Rogowski Coils
- Delta-Sigma ADC with Precision Voltage Reference and On-Chip Temperature Sensor
- Internal or External Oscillator Timing Reference
- SPI, I<sup>2</sup>C, or UART Interface Options with Configurable I/O pins for alarm Signaling, Address Pins, or User Control
- 24-Bit Measurement Processor with Integrated Firmware and Flash Memory for Nonvolatile Storage of Calibration and Configuration Parameters
- Supports Extraction of Individual Harmonics
- Small 32-TQFN Package and Reduced Bill of Materials



## Table of Contents

ABSOLUTE MAXIMUM RATINGS .....	4
Recommended External Components .....	4
Recommended Operating Conditions .....	4
Performance Specifications .....	5
Input Logic Levels .....	5
Output Logic Levels .....	5
Supply Current .....	5
Crystal Oscillator .....	5
Internal RC Oscillator .....	5
ADC Converter, $V_{3P3}$ Referenced .....	6
Timing Specifications .....	7
Reset .....	7
SPI Slave Port .....	7
I <sup>2</sup> C Slave Port (Note 1) .....	8
<b>Pin Configuration .....</b>	<b>9</b>
Package Information .....	11
<b>On-Chip Resources Overview .....</b>	<b>12</b>
IC Block Diagram .....	12
Clock Management .....	13
Power-On Reset, Watchdog-Timer, and Reset Circuitry .....	14
Analog Front-End and Conversion .....	15
24-Bit Measurement Processor .....	17
Flash and RAM .....	17
Digital I/O Pins .....	17
Communication Interfaces .....	17
<b>Functional Description and Operation .....</b>	<b>18</b>
Measurement Interface .....	18
AFE Input Multiplexer .....	18
High Pass Filters and Offset Removal .....	19
Enabling the software integrators for Rogowski Coil current sensors .....	19
Gain Correction .....	19
Die Temperature Compensation .....	20
Phase Compensation .....	20
Voltage Input Configuration .....	21
Current Input Configuration .....	23
Current Input Flowchart .....	24
Data Refresh Rates .....	25
Scaling Registers and Result Formats .....	25
Calibration .....	26
Voltage and Current Gain Calibration .....	26
Offset Calibration .....	26
Die Temperature Calibration .....	26
Voltage Channel Measurements .....	27
RMS Voltage .....	27
Line Frequency .....	27
Current Channel Measurements .....	28
Peak Current .....	28
RMS Current .....	28
Current and Voltage Imbalance .....	29
Power Calculations .....	30
Active Power (P) .....	30
Reactive Power (Q) .....	31
Apparent Power (S) .....	31
Power Factor (PF) .....	31

Totals of active power, reactive power, apparent power and power factor .....	31
Fundamental and Harmonic Calculations .....	33
Energy Calculations .....	34
Bucket Size for Energy Counters .....	35
Min/Max Tracking .....	36
Voltage Sag Detection .....	37
Voltage Sign Outputs .....	38
Alarm Monitoring .....	38
Status Registers .....	39
Digital IO Functionality .....	40
DIO Direction .....	41
DIO Polarity .....	41
Alarm Pins .....	41
Command Register .....	42
General Settings .....	42
No Action (0x00xxxx) .....	42
Save to Flash Command (0xACC2xx) .....	43
Clear Flash Storage 0 Command (0xACC0xx) .....	43
Clear Flash Storage 1 Command (0xACC1xx) .....	43
Calibration Command (0xCAxxxx/0xCBxxxx) .....	44
Configuration Register .....	45
<b>Application Examples .....</b>	<b>46</b>
Wye-connected source, wye-connected load (Y-Y) .....	47
Isolated configuration, 3 VT, 3 CT .....	47
Non-isolated configuration, 3 voltage-dividers, 3 CTs .....	48
Non-isolated, 3 voltage-dividers, 2 CTs, 1 Shunt .....	49
Non-isolated, 3 voltage-dividers, 3 shunts .....	50
Delta-connected source, delta-connected load ( $\Delta$ - $\Delta$ ) .....	51
Isolated configuration, 2 VTs, 2 CT, line current measurement .....	52
Non-isolated, 2 voltage-dividers referenced to line, 2 CTs, line current measurements .....	53
Non-isolated, 1 CT, 2 shunts and 2 voltage-dividers, all referenced to phase .....	56
Wye-connected source, delta-connected load (Y- $\Delta$ ) .....	57
<b>Register Access .....</b>	<b>58</b>
Data Types .....	58
Register Locations .....	59
<b>Serial Interfaces .....</b>	<b>64</b>
UART Interface .....	64
RS-485 Support .....	64
Device Address Configuration .....	65
SSI Protocol Description .....	65
SPI Interface .....	69
I <sup>2</sup> C Interface .....	72
Device Address Configuration .....	72
Bus Characteristics .....	73
Device Addressing .....	73
Write Operations .....	74
Read Operations .....	75
<b>Ordering Information .....</b>	<b>76</b>
<b>Contact Information .....</b>	<b>76</b>
<b>Revision History .....</b>	<b>77</b>

## Electrical Specifications

**ABSOLUTE MAXIMUM RATINGS**

(All voltages with respect to ground.)

<b>Supplies and Ground Pins:</b>	
$V_{3P3D}$ , $V_{3P3A}$	-0.5V to 4.6V
GNDD, GNDA	-0.5V to +0.5V
<b>Analog Input Pins:</b>	
AV1, AV2, AV3, AI1, AI2, AI3	-10mA to +10mA -0.5V to ( $V_{3P3} + 0.5V$ )
<b>Oscillator Pins:</b>	
XIN, XOUT	-10mA to +10mA -0.5V to 3.0V
<b>Digital Pins:</b>	
DIO0 through DIO15; <i>Digital Pins configured as outputs</i>	-30mA to +30mA, -0.5 to ( $V_{3P3D} + 0.5V$ )
DIO0 through DIO15, RESET; <i>Digital Pins configured as inputs</i>	-10mA to +10mA, -0.5V to +6V
<b>Temperatures:</b>	
Operating Junction Temperature	
Peak, 100ms	+140°C
Continuous	+125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C
Soldering Temperature (reflow)	+300°C
ESD Stress on All Pins	±4kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended External Components**

NAME	FROM	TO	FUNCTION	VALUE	UNITS
XTAL	XIN	XOUT	20.000MHz	20.000	MHz
CXS	XIN	GNDD	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board)	18 ±10%	pF
CXL	XOUT	GNDD		18 ±10%	pF

**Recommended Operating Conditions**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage ( $V_{3P3}$ )	Normal operation	3.0	3.3	3.6	V
Operating Temperature		-40		+85	°C

**Performance Specifications**

Note that production tests are performed at room temperature.

**Input Logic Levels**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital High-Level Input Voltage ( $V_{IH}$ )		2			V
Digital Low-Level Input Voltage ( $V_{IL}$ )				0.8	V

**Output Logic Levels**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Digital High-Level Output Voltage ( $V_{OH}$ )	$I_{LOAD} = 1\text{mA}$	$V_{3P3} - 0.4$			V
	$I_{LOAD} = 10\text{mA}$	$V_{3P3} - 0.6$			V
Digital Low-Level Output Voltage ( $V_{OL}$ )	$I_{LOAD} = 1\text{mA}$	0		0.4	V
	$I_{LOAD} = 10\text{mA}$			0.5	V

**Supply Current**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{3P3D}$ and $V_{3P3A}$ Current (Compounded)	Normal operation, $V_{3P3} = 3.3\text{V}$		8.1	10.3	mA

**Crystal Oscillator**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
XIN to XOUT Capacitance	(Note 1)		3		pF
Capacitance to GNDD (Note 1)	XIN		5		pF
	XOUT		5		

**Note 1:** Guaranteed by design; not subject to test.

**Internal RC Oscillator**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Nominal Frequency			20.000		MHz
Accuracy	$V_{3P3} = 3.0\text{V}, 3.6\text{V};$ temperature = $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		$\pm 1.5$	$\pm 1.75$	%

**ADC Converter,  $V_{3P3}$  Referenced**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Usable Input Range ( $V_{IN} - V_{3P3}$ )		-250		+250	mV peak
THD (First 10 Harmonics)	$V_{IN} = 65\text{Hz}$ , 64kpts FFT, Blackman-Harris window		-85		dB
Input Impedance	$V_{IN} = 65\text{Hz}$	30		90	k $\Omega$
Temperature Coefficient of Input Impedance	$V_{IN} = 65\text{Hz}$ (Note 1)		1.7		$\Omega/^{\circ}\text{C}$
ADC Gain Error vs. %Power Supply Variation $\frac{10^6 \Delta N_{out_{PK}} 357nV / V_{IN}}{100 \Delta V_{3P3} A / 3.3}$	$V_{IN} = 200\text{mVpk}$ , 65Hz; $V_{3P3} = 3.0\text{V}$ , 3.6V			50	ppm/%
Input Offset ( $V_{IN} - V_{3P3}$ )		-10		+10	mV

<sup>1</sup> Guaranteed by design; not subject to test.

## Timing Specifications

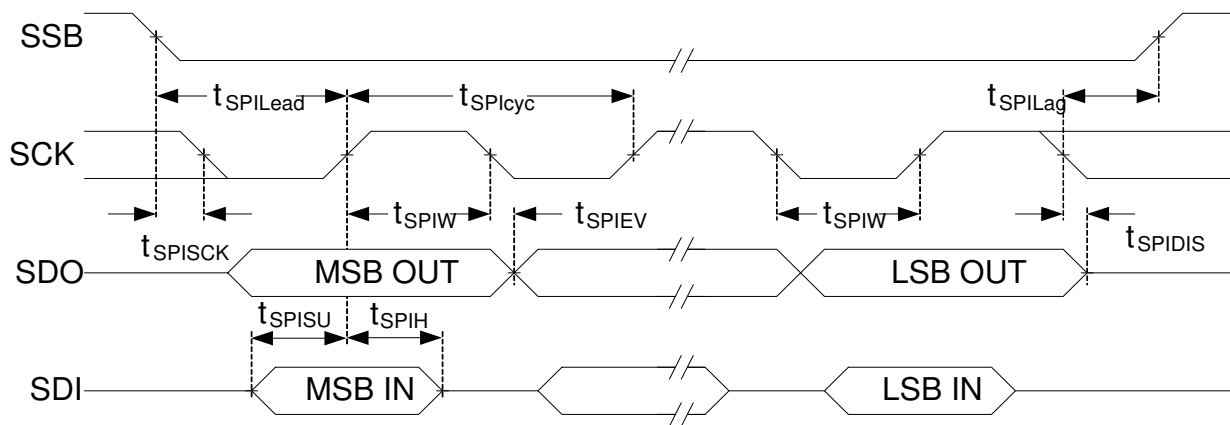
### Reset

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Reset Pulse Fall Time	(Note 1)		1		$\mu\text{s}$
Reset Pulse Width	(Note 1)		5		$\mu\text{s}$

### SPI Slave Port

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Cycle Time ( $t_{\text{SPICyc}}$ )		1			$\mu\text{s}$
Enable Lead Time ( $t_{\text{SPILeAd}}$ )		15			ns
Enable Lag Time ( $t_{\text{SPILag}}$ )		0			ns
SCK Pulse Width ( $t_{\text{SPIW}}$ )	High	250			ns
	Low	250			
SSB to First SCK Fall ( $t_{\text{SPISCK}}$ )	Ignore if SCK is low when SSB falls (Note 1)		2		ns
Disable Time ( $t_{\text{SPIDIS}}$ )	(Note 1)		0		ns
SCK to Data Out (SDO) ( $t_{\text{SPIEV}}$ )				25	ns
Data Input Setup Time (SDI) ( $t_{\text{SPISU}}$ )		10			ns
Data Input Hold Time (SDI) ( $t_{\text{SPIH}}$ )		5			ns

**Note 1:** Guaranteed by design, not subject to test.



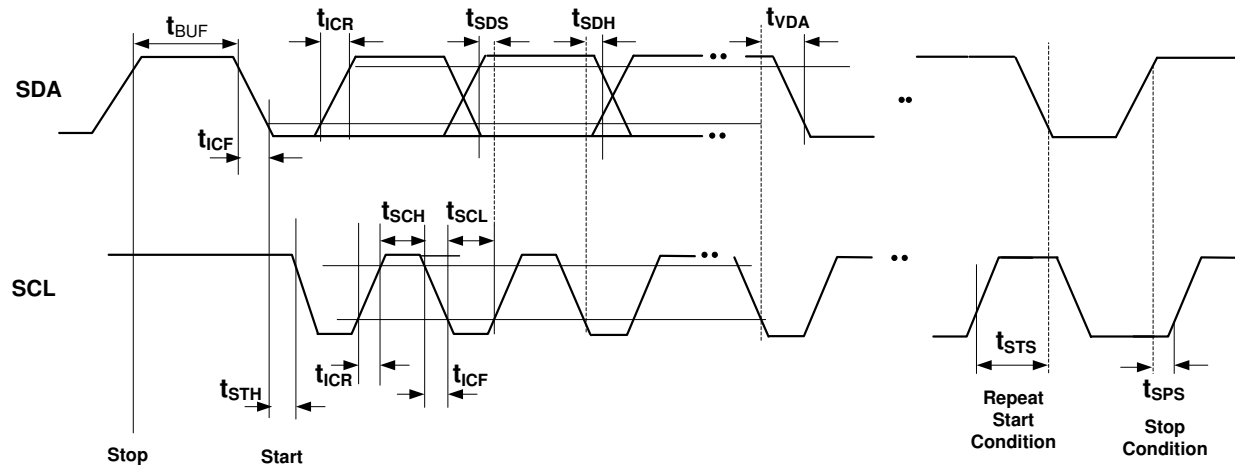


**I<sup>2</sup>C Slave Port (Note 1)**

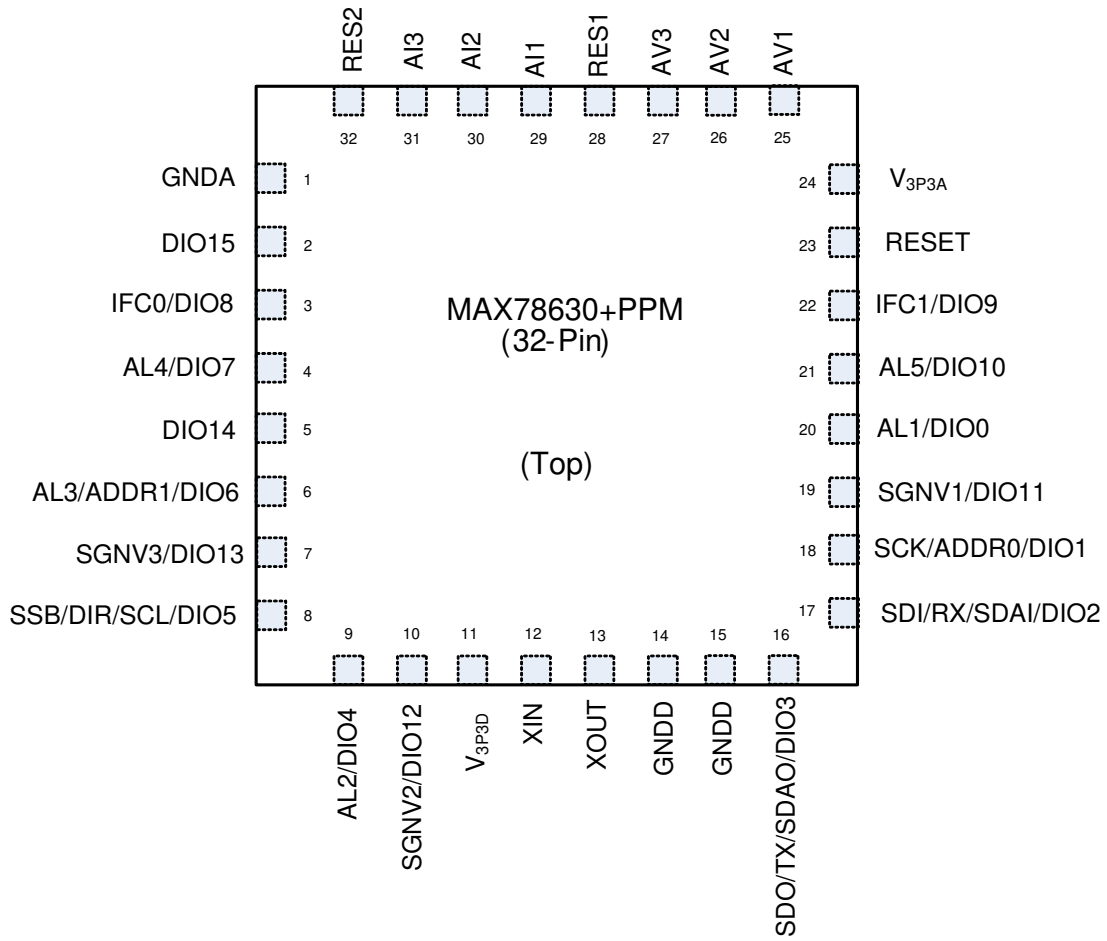
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Idle (Free) Time Between Transmissions (STOP/START) ( $t_{BUF}$ )		1500			ns
I <sup>2</sup> C Input Fall Time ( $t_{ICF}$ )	(Note 2)	20		300	ns
I <sup>2</sup> C Input Rise Time ( $t_{ICR}$ )	(Note 2)	20		300	ns
I <sup>2</sup> C START or Repeated START Condition Hold Time ( $t_{STH}$ )		500			ns
I <sup>2</sup> C START or Repeated START Condition Setup Time ( $t_{STS}$ )		600			ns
I <sup>2</sup> C Clock High Time ( $t_{SCH}$ )		600			ns
I <sup>2</sup> C Clock Low Time ( $t_{SCL}$ )		1300			ns
I <sup>2</sup> C Serial Data Setup Time ( $t_{SDS}$ )		100			ns
I <sup>2</sup> C Serial Data Hold Time ( $t_{SDH}$ )		10			ns
I <sup>2</sup> C Valid Data Time ( $t_{VDA}$ ): SCL Low to SDA Output Valid ACK Signal from SCL Low to SDA (Out) Low				900	ns

**Note 1:** Guaranteed by design, not subject to test

**Note 2:** Dependent on bus capacitance.



# Pin Configuration



Pin	Signal	Function	Pin	Signal	Function
1	GNDA	GROUND (Analog)	17	SDI/RX/SDAI/ DIO2	SPI DATA IN / UART RX/ I <sup>2</sup> C Data In / Digital I/O
2	DIO15	Digital I/O	18	SCK/ADDR0/ DIO1	SPI CLOCK IN / I <sup>2</sup> C/Multi- Point UART Address/ Digital I/O
3	IFC0/DIO8	IFC1/SPI (1=IFC1 pin; 0=SPI) <sup>(1)</sup> / Digital I/O	19	SGNV1 / DIO11	Sign of AV1 Output / Digital I/O
4	AL4/DIO7	Alarm Output / Digital I/O	20	AL1/DIO0	Alarm Output / Digital I/O
5	DIO14	Digital I/O	21	AL5/DIO10	Alarm Output / Digital I/O
6	AL3/ADDR1/ DIO6	I <sup>2</sup> C/ UART Address / Alarm Output / Digital I/O	22	IFC1//DIO9	I <sup>2</sup> C/UART (1=I <sup>2</sup> C;0=UART) <sup>(1)</sup> / Digital I/O
7	SGNV3 / DIO13	Sign of AV3 Output / Digital I/O	23	RESET	Reset Input
8	SSB/DIR/SCL/ DIO5	Slave Select (SPI) / RS485 TX-RX / I <sup>2</sup> C Serial Clock/ Digital I/O	24	V <sub>3P3A</sub>	3.3VDC Supply (Analog)
9	AL2/DIO4	Alarm Output / Digital I/O	25	AV1	Voltage Input (Phase 1)
10	SGNV2 / DIO12	Sign of AV2 Output / Digital I/O	26	AV2	Voltage Input (Phase 2)
11	V <sub>3P3D</sub>	3.3VDC Supply (Digital)	27	AV3	Voltage Input (Phase 3)
12	XIN	Crystal Oscillator Driver Input	28	RES1	Reserved for future use. Tie to V3P3A
13	XOUT	Crystal Oscillator Driver Output	29	AI1	Current Input (Phase 1)
14	GNDD	GROUND (Digital)	30	AI2	Current Input (Phase 2)
15	GNDD	GROUND (Digital)	31	AI3	Current Input (Phase 3)
16	SDO/TX/ SDAO/DIO3	SPI DATA OUT/ UART TX/ I <sup>2</sup> C Data Out / Digital I/O	32	RES2	Reserved for future use. Tie to V3P3A

## Notes:

- 1) **IFC0** and **IFC1** pins are sampled at power-on to select the communication peripheral as follows:  
**IFC0** = 0 to select SPI; **IFC1** = X (Don't Care)  
**IFC0** = 1, **IFC1** =0 to select UART/RS485; **IFC1** = 1 to select I<sup>2</sup>C

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN	T3255+4	<a href="#">21-0140</a>	<a href="#">90-0012</a>

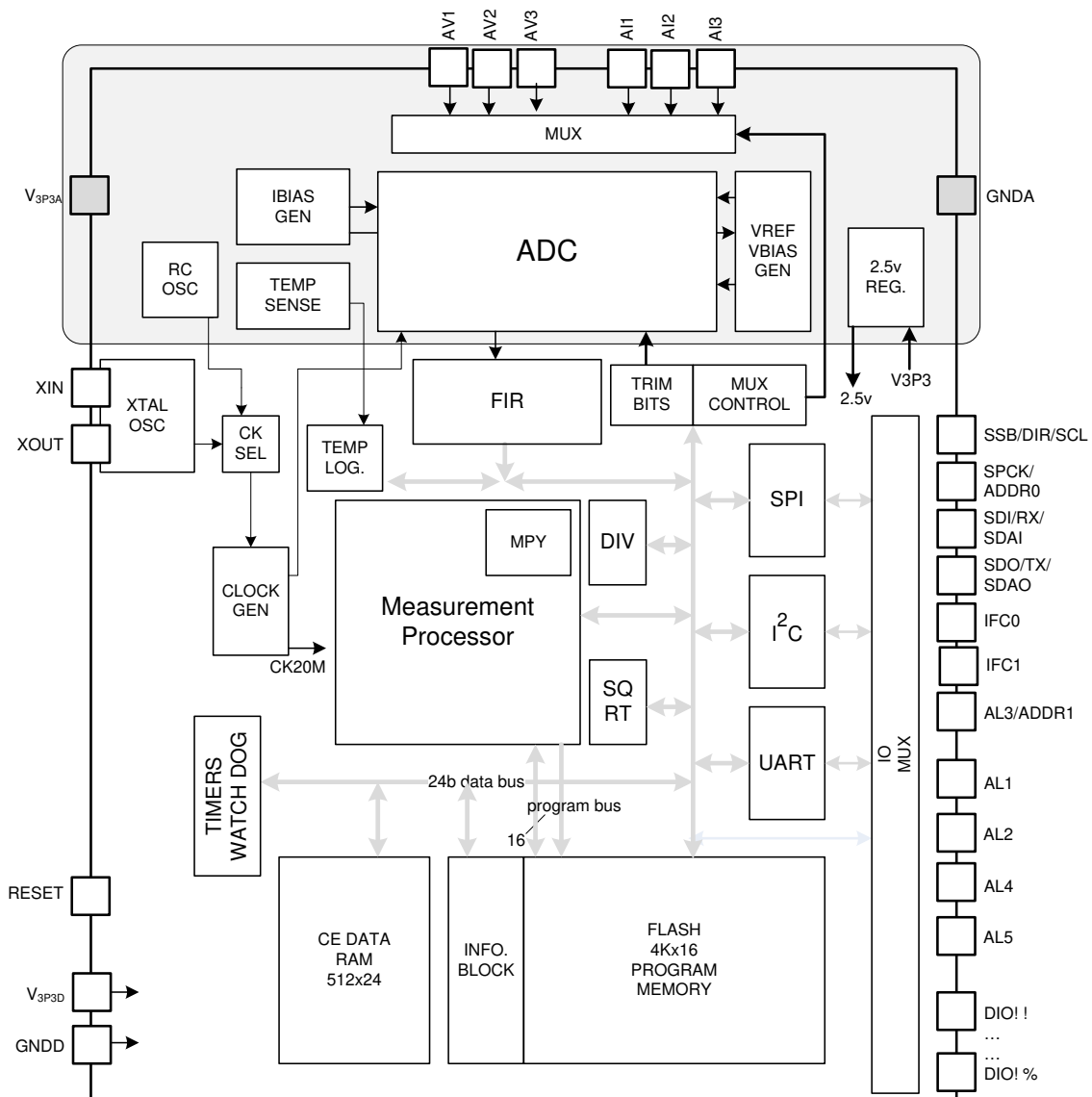
## On-Chip Resources Overview

The MAX78630+PPM device integrates all the hardware blocks required for accurate AC power and energy measurement. Included on the device are:

- Oscillator and clock management logic
- Power-on reset, watchdog timer, and reset circuitry
- High-accuracy Analog Front End (AFE) with trimmed voltage reference and temperature sensor
- 24-bit measurement processor with RAM and flash memory
- UART, SPI and I<sup>2</sup>C serial communication interfaces and multipurpose Digital I/O

## IC Block Diagram

The following is a block diagram of the hardware resources available on the MAX78630+PPM.

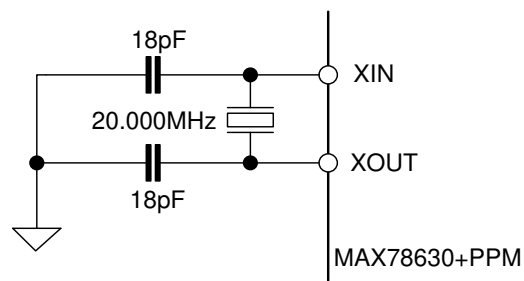


## Clock Management

The device can be clocked by oscillator circuitry that relies on an external crystal or, as a backup source, by a trimmed internal RC oscillator. The internal RC oscillator provides an accurate clock source for UART baud rate generation.

The chip hardware automatically handles the clock sources logic and distributes the clock to the rest of the device. Upon reset or power-on, the device will utilize the internal RC oscillator circuit for the first 1024 clock cycles, allowing the external crystal adequate time to start-up. The device will then automatically select the external clock, if available. It will also automatically switch back to the internal oscillator in the event of a failure with the external oscillator. This condition is also monitored by the processor and available to the user in the STATUS register.

The MAX78630+PPM external clock circuitry requires a 20.000MHz crystal. The circuitry includes two 18pF ceramic capacitors. The figure below shows the typical connection of the external crystal. This oscillator is self biasing and therefore an external resistor should NOT be connected across the crystal.



An external 20MHz system clock signal can also be utilized instead of the crystal. In this case, the external clock should be connected to the XOUT pin while the XIN pin should be connected to GNDD.

Alternatively, if no external crystal or clock is utilized, the XOUT pin should be connected to GNDD and the XIN pin left unconnected.

## Power-On Reset, Watchdog-Timer, and Reset Circuitry

### Power-On RESET (POR)

An on-chip Power-On Reset (POR) block monitors the supply voltage (V3P3D) and initializes the internal digital circuitry at power-on. Once V3P3D is above the minimum operating threshold, the POR circuit triggers and initiates a reset sequence. It will also issue a reset to the digital circuitry if the supply voltage falls below the minimum operating level.

### Watchdog Timer (WDT)

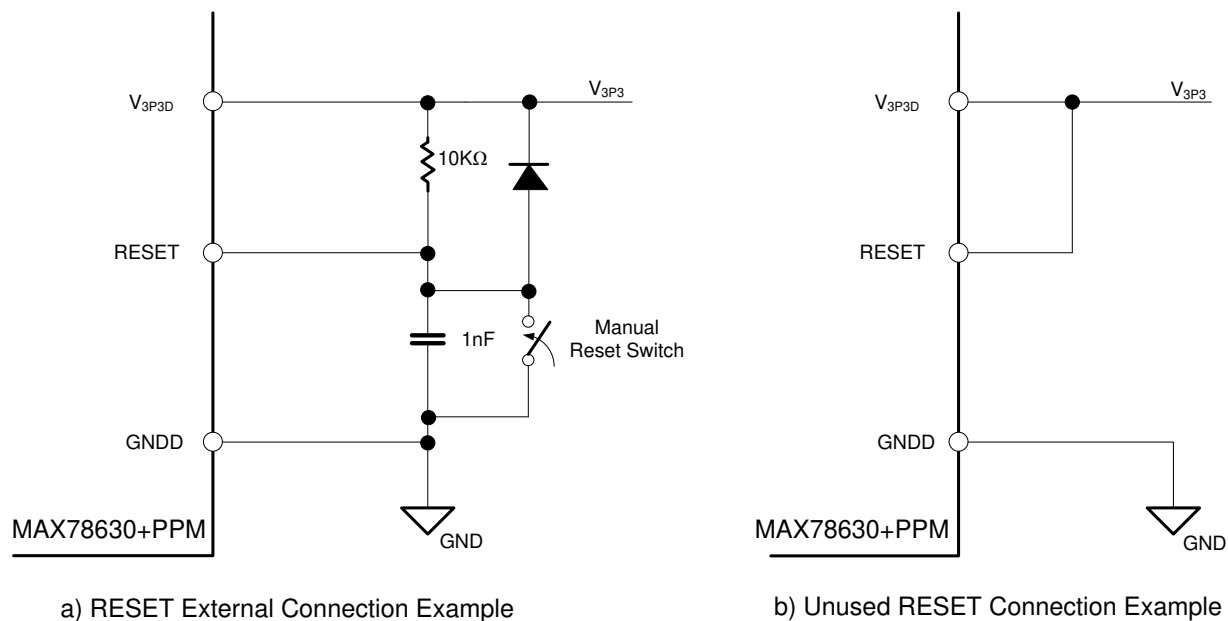
A Watchdog Timer (WDT) block detects any software processing errors. The embedded software periodically refreshes the free-running watchdog timer to prevent it from timing out. If the WDT times out, it is an indication that software is no longer being executed in the intended sequence; thus, a system reset is initiated.

### External Reset Pin (RESET Pin)

In addition to the internal sources, a reset can be forced by applying a low level to the RESET pin. If the RESET pin is pulled low, all digital activities in the device stop, except the clock management circuitry and oscillators, which continue to run. The external reset input is filtered to prevent spurious reset events in noisy environments. The reset does not occur until RESET has been held low for at least 1  $\mu$ s.

Once initiated, the reset mode persists until the RESET is set high and the reset timer times out (4096 clock cycles). At the completion of the reset sequence, the internal reset is released and the processor begins executing from address 0.

If not used, the RESET pin can be connected either directly or through a pull-up resistor to V3P3D supply. A simple connection diagram is shown below.



## Analog Front-End and Conversion

The Analog Front-End (AFE) of the MAX78630+PPM includes an input multiplexer, optional pre-amplifier gain stage, Delta-Sigma A/D Converter, bias current references, voltage references, temperature sensor, and several voltage fault comparators.

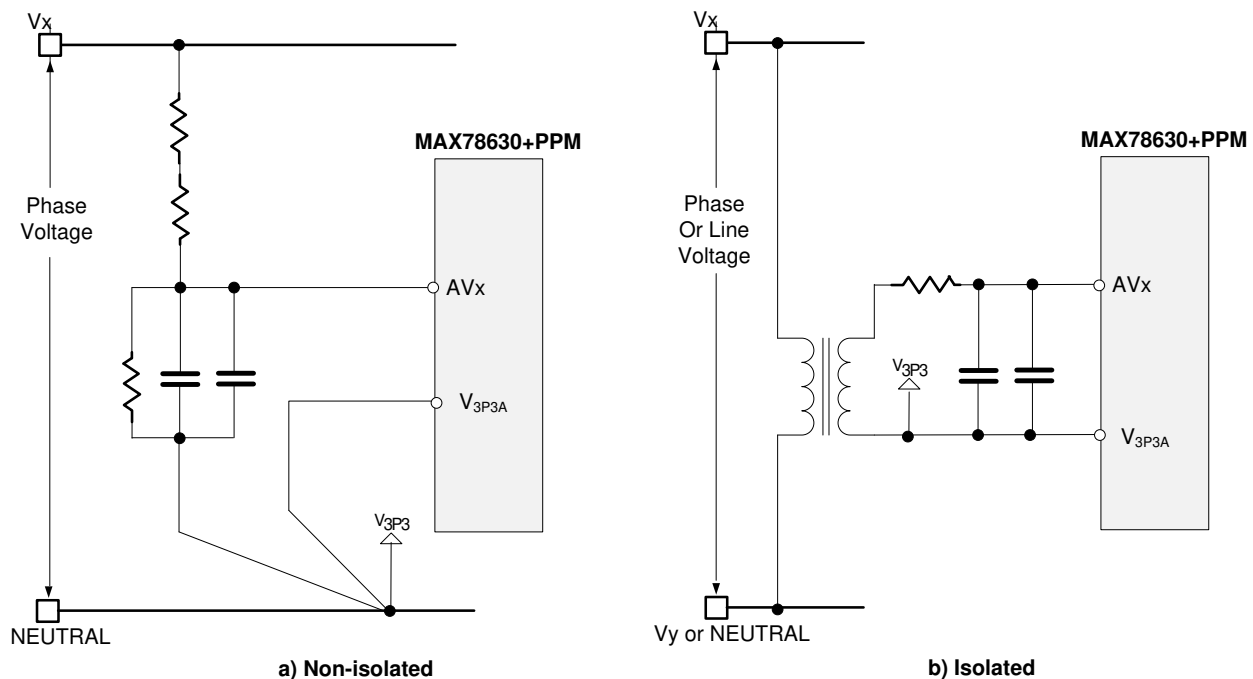
### Analog Inputs

Up to six external sensors can be connected to the MAX78630+PPM. The full-scale signal level that can be applied to any analog input pin with respect to  $V_{3P3A}$  is  $\pm 250$  mVpk. Considering a sinusoidal AC waveform, the maximum RMS voltage applied to the inputs pins is:

$$\text{rmsMAX} = \frac{250\text{mVpk}}{\sqrt{2}} = 176.78\text{mVrms}$$

### Voltage Inputs

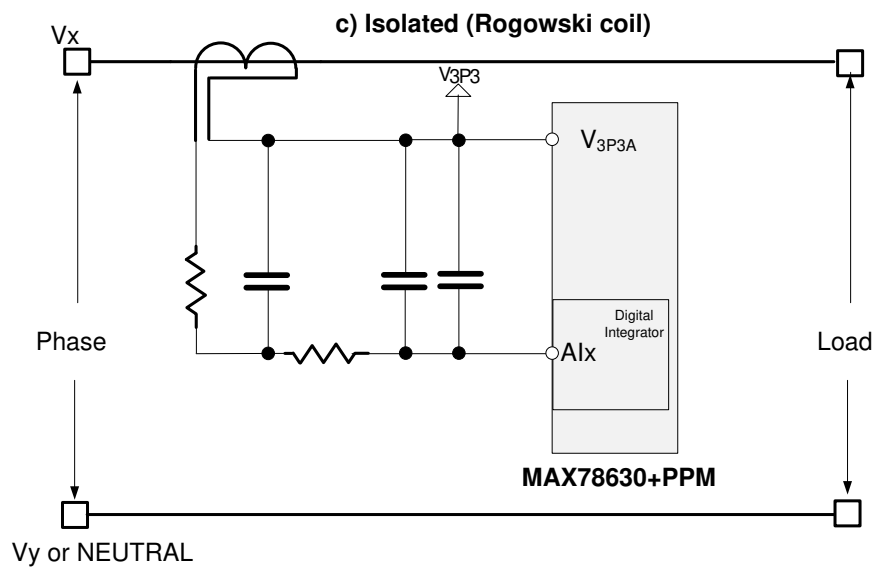
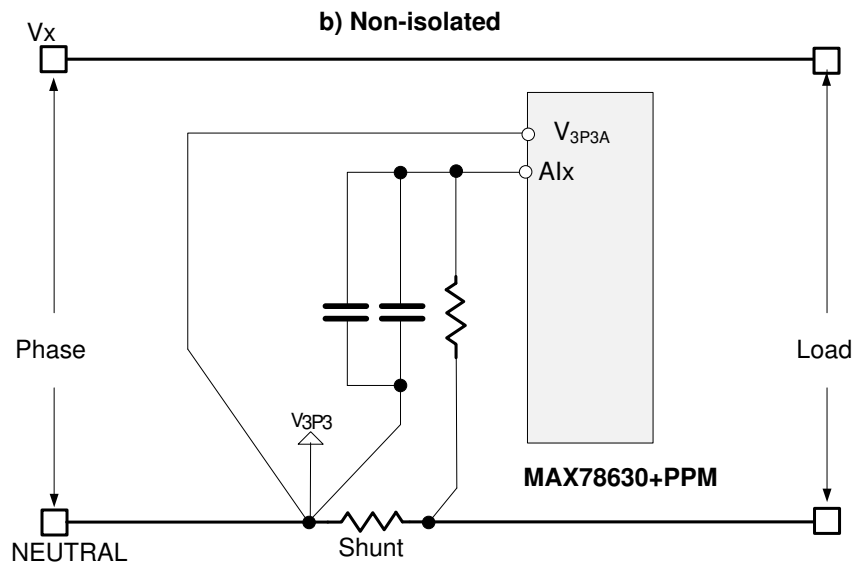
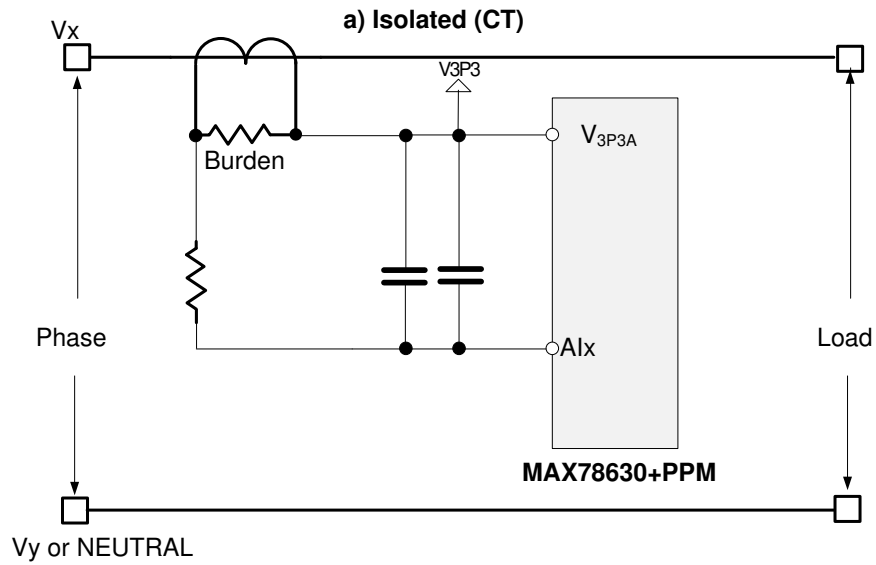
Three single-ended input pins (AVA, AVB and AVC) can be connected to external voltage sensors. The figure below shows example signal conditioning circuits for a voltage input in both isolated (via voltage transformers) and non-isolated (via a resistor divider circuit) cases. Complete system diagrams for wye- and a delta-connected three-phase system are shown in the [Applications Examples](#) section of this document. Consult application notes for more information on component selection and PCB design considerations.



### Current Inputs

Similarly, three single-ended input pins (AIA, AIB and AIC) can be connected to external current sensors. The figure on the following page shows example signal conditioning circuits for a current input. One diagram each is shown for measurement via a resistive shunt (a), a current transformer (b) and a Rogowski coil (c). The latter requires the user to enable the built-in digital integrator and implement a low pass filter. Complete system diagrams for wye- and a delta-connected three-phase system are shown in the [Applications Examples](#) section of this document. Consult application notes for more information on component selection and PCB design considerations.





### **Delta-Sigma A/D Converter**

A second-order Delta-Sigma converter digitizes the analog inputs. The converted data is then processed through an FIR filter.

### **Voltage Reference**

The device includes an on-chip precision band-gap voltage reference that incorporates auto-zero techniques as well as production trims to minimize errors caused by component mismatch and drift. The voltage reference is digitally compensated over temperature.

### **Die Temperature Measurement**

The device includes an on-chip die temperature sensor used for digital compensation of the voltage reference. It is also used to report temperature information to the user.

### **24-Bit Measurement Processor**

The MAX78630+PPM integrates a fixed-point 24-bit signal processor that performs all the digital signal processing necessary for energy measurement, alarm generation, calibration, compensation, etc. Functionality and operation of the device is determined by the firmware and described in the [Functional Description and Operation](#) section.

### **Flash and RAM**

The MAX78630+PPM includes 8KB of on-chip flash memory. The flash memory primarily contains program code, but also stores coefficients, calibration data, and configuration settings. The MAX78630+PPM includes 1.5KB of on-chip RAM which contains the values of input and output registers and is utilized by the FW for its operations.

### **Digital I/O Pins**

There are a total of sixteen digital input/outputs (DIOs) on the MAX78630+PPM device. Some are dedicated to serial interface communications and configuration. Others are multi-purpose I/O that can be used as simple push-pull outputs under user control or routed to special purpose internal signals, such as alarm signaling.

### **Communication Interfaces**

The MAX78630+PPM includes three communication interface options: UART, SPI, and I<sup>2</sup>C. Since the I/O pins are shared, only one mode is supported at a time. Interface configuration and address pins are sampled at power-on or reset to determine which interface will be active and to set device addresses.

## Functional Description and Operation

This section describes the MAX78630+PPM functionality. It includes measurements and relevant calculations, alarms, auxiliary functions such as calibrations, zero-crossing, etc.

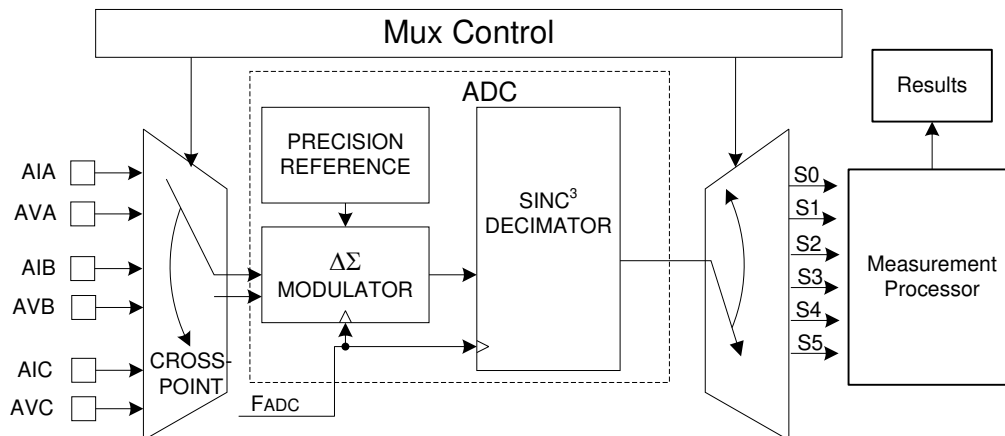
A set of input (write), output (read) and read/write registers are provided to allow access to calculated data and alarms and to configure the device. The input (write) registers values can be saved into flash memory through a specific command. The values saved into flash memory will be loaded in these registers at reset or power-on as defaults.

### Measurement Interface

The MAX78630+PPM incorporates a flexible measurement interface for simplified integration into any system. This section describes the configuration and signal conditioning of the analog inputs.

#### AFE Input Multiplexer

The MAX78630+PPM samples six (6) external sensors with an effective sample rate of 2.7kps for each multiplexer slot. Three analog input pins are defined as single ended voltage inputs and three as single ended current inputs.



Sensor Slot	Analog Input Pins	Input Type
S5	AIA	Current
S4	AVA	Voltage
S3	AIB	Current
S2	AVB	Voltage
S1	AIC	Current
S0	AVC	Voltage

## High Pass Filters and Offset Removal

Offset registers for each analog input contain values to be subtracted from the raw ADC outputs for the purpose of removing inherent system DC offsets from any calculated power and RMS values. These registers are signed fixed-point numbers with a possible range of -1.0 to 1.0-LSB. They default to 0 and can be either manually changed by the user or by the integrated offset calibration routines.

Register	Description
V1_OFFS	Voltage Input AV1 Offset Calibration
V2_OFFS	Voltage Input AV2 Offset Calibration
V3_OFFS	Voltage Input AV3 Offset Calibration
I1_OFFS	Current Input AI1 Offset Calibration
I2_OFFS	Current Input AI2 Offset Calibration
I3_OFFS	Current Input AI3 Offset Calibration

Alternatively, the user can enable an integrated High Pass Filter (HPF) to dynamically update the offset registers every accumulation interval. During each accumulation interval (or low-rate cycle) the HPF calculates the median or DC average of each input. Adjustable coefficients determine what portion of the measured offset is combined with the previous offset value.

The HPF\_COEF\_I and HPF\_COEF\_V registers contain signed fixed point numbers with a usable range of 0 to 1.0-LSB (negative values are not supported). By default, they are initialized to 0.5 (0x400000) meaning the new offset value will come from  $\frac{1}{2}$  of the measured offset and  $\frac{1}{2}$  will come from the previous offset value. Setting them to 1.0 (0x7FFFFFFF) causes the entire measured offset to be applied to the offset register enabling lump-sum offset removal. Setting them to zero disables any dynamic update of the offset registers by the HPF. The HPF coefficients apply to all three channels (current or voltage).

Register	Description
HPF_COEF_I	HPF coefficient for AIA, AIB and AIC current inputs
HPF_COEF_V	HPF coefficient for AVA, AVB and AVC voltage inputs

Using the offset calibration routine will automatically set the filter coefficients to zero to disable the HPF.

## Enabling the software integrators for Rogowski Coil current sensors

Rogowski Coil current sensors produce an output signal that is proportional to the derivative of current over time. Therefore, an integration filter is required to reconstruct the original current signal. The MAX78630+PPM provides such integrators and a configuration bit for each of the three current inputs to enable this feature.

Register[Bit]	Description
Config[EN_ROGA]	Enables the software integrator for input AIA
Config[EN_ROGB]	Enables the software integrator for input AIB
Config[EN_ROGC]	Enables the software integrator for input AIC

Enabling the software integrator will automatically disable the HPF and offset correction.

## Gain Correction

The system (sensors) and the MAX78630+PPM device inherently have gain errors that can be corrected by using the gain registers. These registers can be directly accessed and modified by an external host processor or automatically updated by an integrated self calibration routine.

Input gain registers are signed fixed-point numbers with the binary point to the left of bit 21. They are set to 1.0 by default and have a usable range of 0 to 4.0-LSB (negative values are not supported). The gain equation for each input X can be described as  $Y = \text{gain} * X$ .

Register	Description
V1_GAIN	Voltage Input AV1 Gain Calibration.
V2_GAIN	Voltage Input AV2 Gain Calibration
V3_GAIN	Voltage Input AV3 Gain Calibration.
I1_GAIN	Current Input AI1 Gain Calibration
I2_GAIN	Current Input AI2 Gain Calibration
I3_GAIN	Current Input AI3 Gain Calibration

### Die Temperature Compensation

The MAX78630+PPM has an on-chip temperature sensor that can be used by the measurement processor for monitoring the voltage reference error and made available to the user in the TEMPC register.

Setting the Temperature Compensation (TC) bit in the Command Register allows the firmware to further adjust the system gain based on measured die temperature. Die temperature offset is typically calibrated by the user during the calibration stage. Die temperature gain is set to a factory default value for most applications, but can be adjusted by the user.

Register	Description
T_OFFS	Die Temperature Offset Calibration.
T_GAIN	Die Temperature Slope Calibration. Set by factory.

### Voltage Reference Gain Adjustment

The on-chip precision bandgap voltage reference incorporates auto-zero techniques as well as production trims to maximize measurement accuracy. It can be assumed that the part is trimmed at 22°C to produce a uniform voltage reference gain at that temperature. The voltage reference is digitally compensated over changes in measured die temperature using a quadratic equation.

### Phase Compensation

Phase compensation registers are used to compensate for phase errors or time delays between the voltage input source and respective current source that are introduced by the off-chip sensor circuit. The user configurable registers are signed fixed point numbers with the binary point to the left of bit 21. Values are in units of high rate (2.7kHz) sample delays so each integer unit of delay is 370µs with a total possible delay of ±4 samples (approximately ±32° at 60Hz).

Register	Description
PHASECOMP1	Phase (delay) compensation for input current AI1
PHASECOMP2	Phase (delay) compensation for input current AI2
PHASECOMP3	Phase (delay) compensation for input current AI3

## Voltage Input Configuration

The MAX78630+PPM supports multiple analog input configurations for determining the voltages in a three-phase system. The CONFIG register is used to instruct the MAX78630+PPM how to compute them.

CONFIG Bits	Name	Function
22	INV_AV3	Invert voltage samples AV3
21	INV_AV2	Invert voltage samples AV2
20	INV_AV1	Invert voltage samples AV1
5	VDELTA	Compute Line-to-Line voltages
4:3	VPHASE	Missing sensor on voltage input 00: none missing 01: AV1 10: AV2 11: AV3

The VDELTA bit must be set whenever the voltage sensors measure phase voltages (line-to-neutral), but the load is connected in a Delta configuration. The MAX78630+PPM then computes line-to-line voltages from the inputs and uses those for all other computations.

The VPHASE setting determines how many voltage sensors are present, and in which phases. If three sensors are used, these bits should be set to zero. If two sensors are used, settings 01, 10 and 11 indicate the phase with no voltage sensor. This phase will then be computed such that  $VA+VB+VC$  equals to zero. Note that using two voltage sensors is not recommended in Wye-connected systems, as the above equation may not necessarily be true.

The INV\_AVx bits instruct the MAX78630+PPM to invert every sample of the corresponding voltage input, before performing any other computations based on the VDELTA and VPHASE settings.

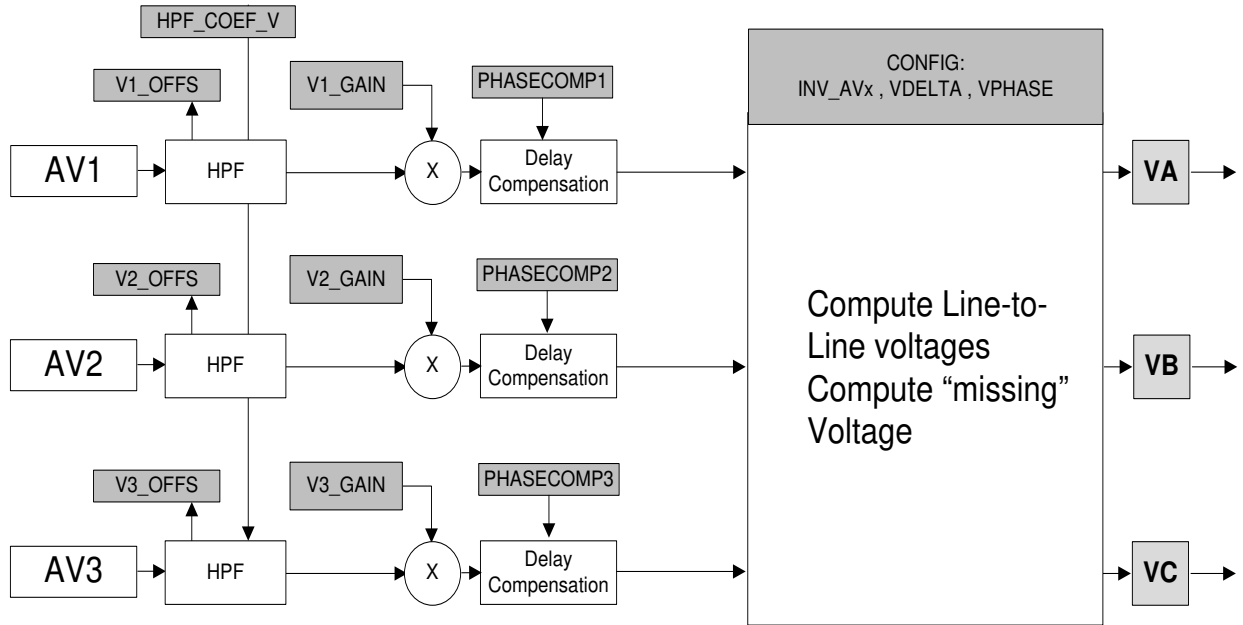
VDELTA	VPHASE	Voltage equations
0	00	VA, VB and VC measured on AV1, AV2 and AV3 inputs
0	01	VB and VC measured on AV2 and AV3 $VA = VC - VB$
0	10	VA and VC measured on AV1 and AV3 $VB = VA - VC$
0	11	VA and VB measured on AV1 and AV2 $VC = VB - VA$
1	00	Compute Line-to-Line voltages at high-rate $VA \Leftarrow VC - VA = VCA$ $VB \Leftarrow VA - VB = VAB$ $VC \Leftarrow VB - VC = VBC$
1	01 10 11	Invalid settings

**Note:** INV\_AVx settings are applied before these computations

The [Applications Examples](#) section provides the required settings for the different configurations.

**Voltage Input Flowchart**

The figure below illustrates the computational flowchart for VA, VB, and VC. The values for the voltage input configuration register can be saved in flash memory and automatically restored at power-on or reset.



## Current Input Configuration

The MAX78630+PPM supports multiple analog input configurations for determining the currents in a three-phase system. The CONFIG register is used to instruct the MAX78630+PPM how to compute them.

CONFIG Bits	Name	Function
2	INEUTRAL	Configuration uses a current sensor in the Neutral conductor. This sensor replaces the missing sensor (see IPHASE setting)
1:0	IPHASE	Missing sensor on current input 00: none missing 01: AI1 10: AI2 11: AI3

The IPHASE setting determines how many line current sensors are present, and for which phases. If three sensors are used, these bits should be set to zero. If two sensors are used, settings 01, 10 and 11 indicate the phase without a line current sensor. The current for this phase will then be computed according to the INEUTRAL and VDELTA settings. If VDELTA is cleared and IN can be assumed to be zero, the current is computed such that  $IA+IB+IC = 0$ . If VDELTA is set, the current in this phase is the difference between the two other currents (INEUTRAL must be cleared in these two cases).

When the INEUTRAL bit is set, a sensor in the neutral conductor replaces one of the three line current sensors. IN is directly measured from a sensor placed in the neutral conductor and the MAX78630+PPM calculates the current for the input with no line current sensor, such that  $IA+IB+IC = IN$  (IPHASE cannot be 00).

INEUTRAL	IPHASE	Current equations
0	00	IA, IB and IC measured on AI1, AI2 and AI3 inputs
0	01	IB and IC measured on AI2 and AI3 if VDELTA = 0 $\Rightarrow IA = -(IB + IC)$ if VDELTA = 1 $\Rightarrow IA = IB - IC$
0	10	IA and IC measured on AI1 and AI3 if VDELTA = 0 $\Rightarrow IB = -(IC + IA)$ if VDELTA = 1 $\Rightarrow IB = IC - IA$
0	11	IA and IB measured on AI1 and AI2 if VDELTA = 0 $\Rightarrow IC = -(IA + IB)$ if VDELTA = 1 $\Rightarrow IC = IA - IB$
1	00	Invalid setting
1	01	IB and IC measured on AI2 and AI3 IN measured on AI1 $IA = IN - (IB + IC)$
1	10	IA and IC measured on AI1 and AI3 IN measured on AI2 $IB = IN - (IC + IA)$
1	11	IA and IB measured on AI1 and AI2 IN measured on AI3 $IC = IN - (IA + IB)$

The [Applications Examples](#) section provides the required settings for different configurations.



### Pre-amp

By default, the full-scale signal that can be applied to the current inputs is  $V_{3P3A} \pm 250\text{mVpk}$  ( $176.78\text{mV}_{\text{RMS}}$ ). This setting provides the widest dynamic range and is recommended for most applications.

For applications requiring a much lower value shunt resistor, an optional pre-amplifier with an 8x gain is included for the current inputs. The maximum input signal that can be applied to the current inputs in this case is  $\pm 31.25\text{mVpk}$ .

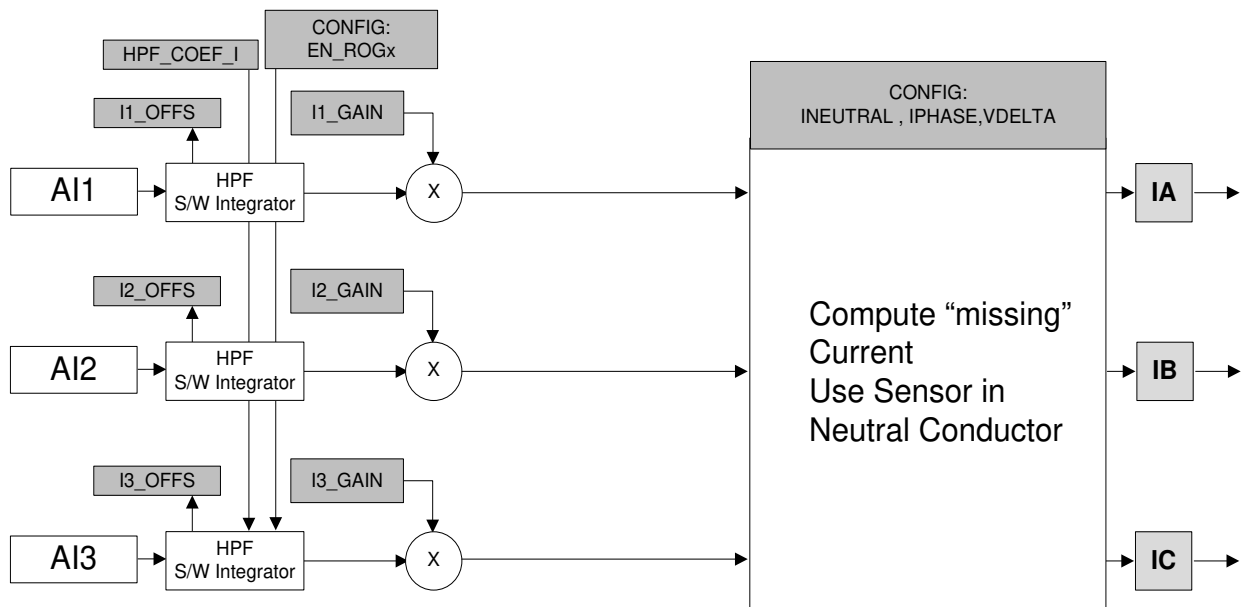
The CONFIG register is used to enable the Pre-amp.

CONFIG Bits	Name	Function
9	EN_PREAMPC	Enables the Pre-amp on input AIC
11	EN_PREAMPB	Enables the Pre-amp on input AIB
13	EN_PREAMPA	Enables the Pre-amp on input AIA

The gain is set by a ratio of internal resistors with one of the resistors in series from the input pad to the pre-amp itself. As such, the device must only be directly connected to a shunt with minimal resistance when using the pre-amp.

### Current Input Flowchart

The figure below illustrates the computational flowchart for IA, IB and IC. The values for current input configuration register can be saved in flash memory and automatically restored at power-on or reset.



## Data Refresh Rates

Instantaneous voltage and current measurement results are updated at the sample rate of 2.7kS/s and are generally not useful unless accessed with a high speed interface such as SPI. The CYCLE register is a 24-bit counter that increments every high-rate sample update and resets when low rate results are updated.

Low rate results, updated at a user configurable rate (also referred to as accumulation interval), are typically used and more suitable for most applications. The FRAME register is a counter that increments every accumulation interval. A data ready indicator in the STATUS register indicates when new data is available. Optionally, this indicator can be made available as a signal on one of the five Alarm output pins.

The high rate samples in one accumulation interval are averaged to produce a low-rate result, increasing their accuracy and repeatability. Low rate results include RMS voltages and currents, frequency, power, energy, and power factor. The accumulation interval can be based on a fixed number of ADC samples or locked to the incoming line voltage cycles.

If Line Lock is disabled, the accumulation interval defaults to a fixed time interval defined by the number of samples defined in the SAMPLES register (default of 540 samples or 0.2 seconds).

When the Line-Lock bit in the Command Register is set, and a valid AC voltage signal is present, the actual accumulation interval is stretched to the next positive zero crossing of the reference line voltage after the defined number of samples has been reached. If there is not a valid AC signal present and line lock is enabled, there is a 100 sample timeout implemented that would limit the accumulation interval to SAMPLES+100.

The DIVISOR register records the actual duration (number of high rate samples) of the last low rate interval whether or not Line-Lock is enabled.

Zero-crossing detection and line frequency for the purpose of determining the accumulation interval are derived from a composite signal  $V_{zc} = VA - 0.5 \cdot VB - 0.25 \cdot VC$ . For a three-phase system, this signal oscillates at the line frequency as long as any of the three voltages is present.

## Scaling Registers and Result Formats

All voltage, current and power data is reported in binary full-scale units with a value range of -1.0 to 1.0 less one LSB (S.23 format). For voltages and currents, all full-scale register readings correspond to the max analog input of 250mVpk (or 31.25mVpk with 8x gain from the pre-amp). As an example, if 230V-peak at the input to the voltage-divider gives 250mV-peak at the chip input, one would get a full-scale register reading of 1.0-LSB for instantaneous voltage. Similarly, if 30A at the sensor input provides 250mV to the chip input, a full-scale register value of 1.0-1LSB for instantaneous current would correspond to 30A. Full-scale power corresponds to the result of full-scale current and voltage so in this example, full-scale watts is 230 x 30 or 6900 watts.

Power Factors are reported as binary fixed-point number, with a range of -2 to +2 less one LSB (format S.22). Frequency data is reported as binary fixed-point number, with a range of 0 to +256Hz less one LSB (format S.16). Temperature data has a fixed scaling with a range of -16384°C to +16384°C less one LSB (format S.10). Energy data scaling is described in a different section of this document.

Nonvolatile registers (IFSCALE and VFSCALE) are provided for storing the real-world current and voltage levels that apply to the full-scale register readings for any given board design. Any host application can then format the measurement results to any data format as needed. The usage of these nonvolatile scratchpad registers is user defined and their content has no effect on the internal operations of the device.