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19-1086; Rev 1; 11/05

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

General Description

The MAX801/MAX808 microprocessor (µP) supervisory circuits monitor and control the activities of +5V µPs by providing backup-battery switchover, low-line indication, and µP reset. Additional features include a watchdog for the MAX801 and CMOS RAM write protection for the MAX808.

The MAX801/MAX808 offer a choice of reset-threshold voltage (denoted by suffix letter): 4.675V (L), 4.575V (N), and 4.425V (M). These devices are available in 8-pin DIP and SO packages.

Applications

Computers

Controllers

Intelligent Instruments

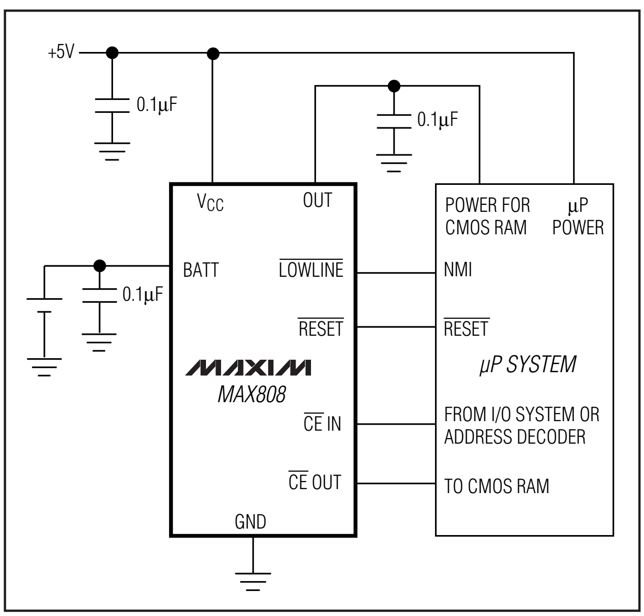
Critical µP Power Monitoring

Portable/Battery-Powered Equipment

Embedded Systems

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



Features

- ♦ **Precision Voltage Monitoring, ±1.5% Reset Accuracy**
- ♦ **200ms Power-OK/Reset Time Delay**
- ♦ **RESET Output (MAX808)**
  RESET and RESET Outputs (MAX801)
- ♦ **Watchdog Timer (MAX801)**
- ♦ **On-Board Gating of Chip-Enable Signals (MAX808):**
  Memory Write-Cycle Completion
  3ns CE Gate Propagation Delay
- ♦ **1µA Standby Current**
- ♦ **Power Switching:**
  250mA in V_{CC} Mode
  20mA in Battery-Backup Mode
- ♦ **MaxCap™/SuperCap™ Compatible**
- ♦ **RESET Guaranteed Valid to V_{CC} = 1V**
- ♦ **Low-Line Threshold 52mV Above Reset Threshold**

MaxCap is a trademark of The Carborundum Corp.
SuperCap is a trademark of Baknor Industries.

Ordering Information

PART*	TEMP RANGE	PIN-PACKAGE
MAX801_CPA	0°C to +70°C	8 Plastic DIP
MAX801_CSA	0°C to +70°C	8 SO
MAX801_EPA	-40°C to +85°C	8 Plastic DIP
MAX801_ESA	-40°C to +85°C	8 SO
MAX801_MJA	-55°C to +125°C	8 CERDIP**
MAX808_CPA	0°C to +70°C	8 Plastic DIP
MAX808_CSA	0°C to +70°C	8 SO
MAX808_EPA	-40°C to +85°C	8 Plastic DIP
MAX808_ESA	-40°C to +85°C	8 SO
MAX808_MJA	-55°C to +125°C	8 CERDIP**

**These parts offer a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.*
***Contact factory for availability and processing to MIL-STD-883.*

Devices in PDIP, SO and µMAX packages are available in both leaded and lead-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

SUFFIX	RESET THRESHOLD (V)		
	MIN	TYP	MAX
L	4.60	4.675	4.75
N	4.50	4.575	4.65
M	4.35	4.425	4.50

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

ABSOLUTE MAXIMUM RATINGS

Input Voltage (with respect to GND)
- V_{CC} ....-0.3V to +6V
- V_{BATT} ....-0.3V to +6V
- All Other Pins ....-0.3V to (V_{OUT} + 0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 500mA
- I_{BATT} Peak 250mA
- I_{BATT} Continuous 50mA
- GND 50mA
- All Other Inputs 50mA

Output Current
- OUT Peak 1.0A
- OUT Continuous 500mA
- All Other Outputs 50mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges
- MAX801_C_A/MAX808_C_A ....0°C to +70°C
- MAX801_E_A/MAX808_E_A ....-40°C to +85°C
- MAX801_MJA/MAX808_MJA ....-55°C to +125°C

Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10sec) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.6V to 5.5V for the MAX80_L, V_{CC} = 4.5V to 5.5V for the MAX80_N, V_{CC} = 4.35V to 5.5V for the MAX80_M; V_{BATT} = 2.8V; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range V_{CC}, BATT (Note 1)			0	X	5.5	V
V_{OUT} in Normal Operating Mode		V_{CC} = 4.5V, I_{OUT} = 25mA		V_{CC} - 0.02		V
		V_{CC} = 4.5V, I_{OUT} = 250mA, MAX80_C/E	V_{CC} - 0.38	V_{CC} - 0.25		
		V_{CC} = 4.5V, I_{OUT} = 250mA, MAX80_M	V_{CC} - 0.45			
		V_{CC} = 3V, V_{BATT} = 2.8V, I_{OUT} = 100mA	V_{CC} - 0.25	V_{CC} - 0.12		
V_{CC} to OUT On-Resistance		V_{CC} = 4.5V, I_{OUT} = 250mA, MAX80_C/E		1.0	1.5	Ω
		V_{CC} = 4.5V, I_{OUT} = 250mA, MAX80_M			1.8	
		V_{CC} = 3V, I_{OUT} = 100mA		1.2	2.5	
V_{OUT} in Battery-Backup Mode		V_{CC} = 0V, V_{BATT} = 4.5V, I_{OUT} = 20mA		V_{BATT} - 0.16		V
		V_{CC} = 0V, V_{BATT} = 2.8V, I_{OUT} = 10mA	V_{BATT} - 0.25	V_{BATT} - 0.12		
		V_{CC} = 0V, V_{BATT} = 2.0V, I_{OUT} = 5mA	V_{BATT} - 0.20	V_{BATT} - 0.08		
BATT to OUT On-Resistance		V_{CC} = 0V, V_{BATT} = 4.5V, I_{OUT} = 20mA		8		Ω
		V_{CC} = 0V, V_{BATT} = 2.8V, I_{OUT} = 10mA		12	25	
		V_{CC} = 0V, V_{BATT} = 2.0V, I_{OUT} = 5mA		16	40	
Supply Current in Normal Operating Mode (excludes I_{OUT})		MAX801		68	110	µA
		MAX808		48	90	
Supply Current in Battery-Backup Mode (excludes I_{OUT}) (Note 2)		V_{CC} = 0V, V_{BATT} = 2.8V, T_A = +25°C		0.4	1	µA
		V_{CC} = 0V, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, MAX80_C/E			5	
		V_{CC} = 0V, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, MAX80_M			50	
BATT Standby Current (Note 3)		V_{BATT} + 0.2V ≤ V_{CC}, T_A = +25°C	-0.1		0.1	µA
		V_{BATT} + 0.2V ≤ V_{CC}, T_A = T_{MIN} to T_{MAX}	-1.0		1.0	
Battery-Switchover Threshold		V_{BATT} = 2.8V, Power-up		V_{BATT} + 0.05		V
		V_{BATT} = 2.8V, Power-down		V_{BATT}		
Battery-Switchover Hysteresis				50		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.6V to 5.5V for the MAX80_L, V_{CC} = 4.5V to 5.5V for the MAX80_N, V_{CC} = 4.35V to 5.5V for the MAX80_M; V_{BATT} = 2.8V; T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RESET AND LOW-LINE							
Reset Threshold	V_{RST}	V_{CC} rising and falling	MAX80_L	4.600	4.675	4.750	V
			MAX80_N	4.500	4.575	4.650	
			MAX80_M	4.350	4.425	4.500	
Reset-Threshold Hysteresis					13		mV
$\overline{\text{LOWLINE}}$ to $\overline{\text{RESET}}$ Threshold Voltage	V_{LR}	V_{CC} falling		30	52	70	mV
$\overline{\text{LOWLINE}}$ Threshold, V_{CC} Rising	V_{LL}	MAX80_L			4.73	4.81	V
		MAX80_N			4.63	4.71	
		MAX80_M			4.48	4.56	
V_{CC} to $\overline{\text{RESET}}$ Delay	t_{RD}	V_{CC} falling at 1mV/µs			17		µs
V_{CC} to $\overline{\text{LOWLINE}}$ Delay	t_{LL}	V_{CC} falling at 1mV/µs			17		µs
$\overline{\text{RESET}}$ Active Timeout Period	t_{RP}	V_{CC} rising		140	200	280	ms
$\overline{\text{RESET}}$ Output Voltage		I_{SINK} = 50µA, V_{BATT} = 0V, V_{CC} falling	V_{CC} = 1.0V, MAX80_C			0.3	V
			V_{CC} = 1.2V, MAX80_E/M			0.3	
		I_{SINK} = 3.2mA, V_{CC} = 4.25V			0.1	0.4	
		I_{SOURCE} = 0.1mA		V_{CC} - 1.5	V_{CC} - 0.1		
$\overline{\text{RESET}}$ Output Short-Circuit Current	I_{SC}	Output sink current, V_{CC} = 4.25V			40		mA
		Output source current			1.6		
RESET Output Voltage (MAX801)		I_{SINK} = 3.2mA				0.4	V
		I_{SOURCE} = 5mA, V_{CC} = 4.25V		V_{CC} - 1.5			
RESET Output Short-Circuit Current (MAX801)	I_{SC}	Output sink current			55		mA
		Output source current, V_{CC} = 4.25V			15		
$\overline{\text{LOWLINE}}$ Output Voltage		I_{SINK} = 3.2mA, V_{CC} = 4.25V				0.4	V
		I_{SOURCE} = 5mA, V_{CC} = 4.25V		V_{CC} - 1.5			
$\overline{\text{LOWLINE}}$ Output Short-Circuit Current	I_{SC}	Output sink current, V_{CC} = 4.25V			40		mA
		Output source current			20		
WATCHDOG TIMER (MAX801)							
Watchdog Timeout Period	t_{WD}			1.12	1.6	2.24	sec
Minimum Watchdog Input Pulse Width		V_{IL} = 0.8V, V_{IH} = 0.75V x V_{CC}		100			ns
WDI Threshold Voltage (Note 4)	V_{IH}			0.75 x V_{CC}			V
	V_{IL}					0.8	
WDI Input Current		RESET deasserted, WDI = 0V		-50	-10		µA
		RESET deasserted, WDI = V_{CC}			16	50	

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.6V to 5.5V for the MAX80_L, V_{CC} = 4.5V to 5.5V for the MAX80_N, V_{CC} = 4.35V to 5.5V for the MAX80_M; V_{BATT} = 2.8V; $T_A = T_{MIN}$ to T_{MAX}. Typical values are at V_{CC} = 5V and T_A = +25°C, unless otherwise noted.)

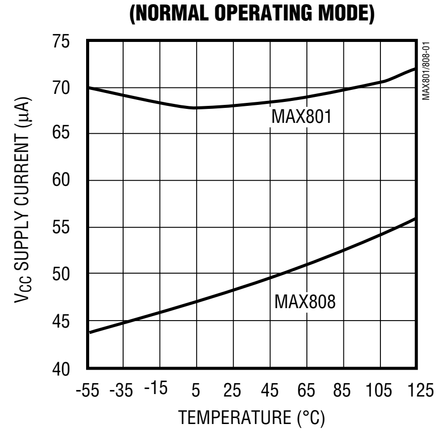
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHIP-ENABLE GATING (MAX808)						
$\overline{CE}$ IN Leakage Current		V_{CC} = 4.25V		±0.00002	±1	µA
$\overline{CE}$ IN to $\overline{CE}$ OUT Resistance (Note 5)		Enabled mode, $V_{CC} = V_{RST}$(max)		75	150	Ω
$\overline{CE}$ OUT Short-Circuit Current ($\overline{RESET}$ Active)		V_{CC} = 4.25V, $\overline{CE}$ OUT = 0V		15		mA
$\overline{CE}$ IN to $\overline{CE}$ OUT Propagation Delay (Note 6)		V_{CC} = 5V, C_{LOAD} = 50pF, 50Ω source-impedance driver		3	8	ns
$\overline{CE}$ OUT Output Voltage High ($\overline{RESET}$ Active)		V_{CC} = 4.25V, I_{OUT} = 2mA	3.5			V
		V_{CC} = 0V, I_{OUT} = 10µA	V_{BATT} - 0.1	V_{BATT}		V
$\overline{RESET}$ to $\overline{CE}$ OUT Delay (Note 7)		V_{CC} falling, $\overline{CE}$ IN = 0V		18		µs

Note 1: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2V.
Note 2: The supply current drawn by the MAX80_ from the battery (excluding I_{OUT}) typically goes to 15µA when (V_{BATT} - 0.1V) < V_{CC} < V_{BATT}. In most applications, this is a brief period as V_{CC} falls through this region (see *Typical Operating Characteristics*).
Note 3: "+" = battery-discharging current, "-" = battery-charging current.
Note 4: WDI is internally connected to a voltage divider between V_{CC} and GND. If unconnected, WDI is typically driven to 1.8V, disabling the watchdog function.
Note 5: The chip-enable resistance is tested with $V_{\overline{CE}\ IN} = V_{CC}$ / 2 and $I_{\overline{CE}\ IN}$ = 1mA.
Note 6: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ OUT.
Note 7: If $\overline{CE}$ IN goes high, $\overline{CE}$ OUT goes high immediately and stays high until reset is deasserted and $\overline{CE}$ IN is low.

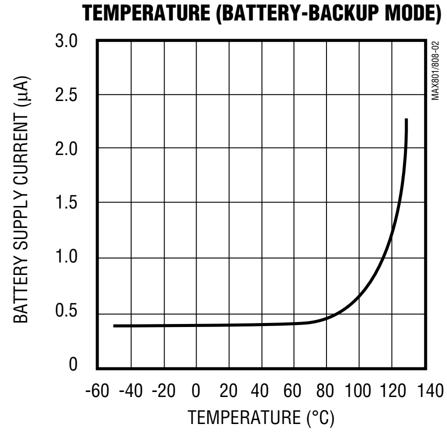
Typical Operating Characteristics

(V_{CC} = 5V, V_{BATT} = 2.8V, no load, T_A = +25°C, unless otherwise noted.)

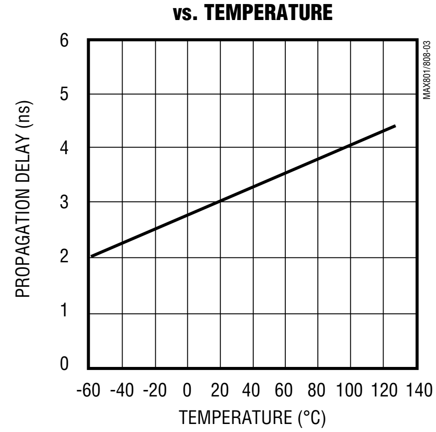
V_{CC} SUPPLY CURRENT vs. TEMPERATURE (NORMAL OPERATING MODE)



BATTERY SUPPLY CURRENT vs. TEMPERATURE (BATTERY-BACKUP MODE)



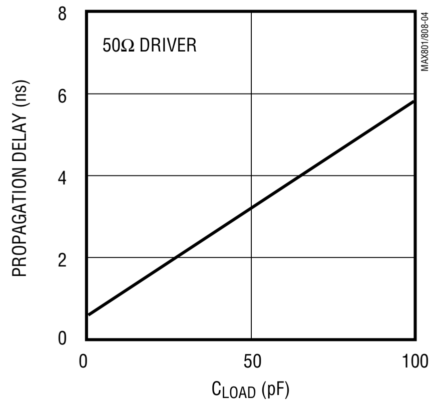
MAX808 CHIP-ENABLE PROPAGATION DELAY vs. TEMPERATURE



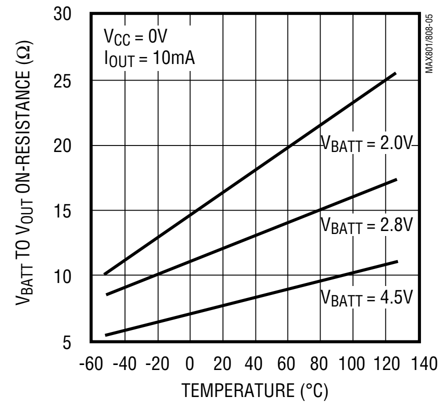
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{BATT} = 2.8V, no load, T_A = +25°C, unless otherwise noted.)

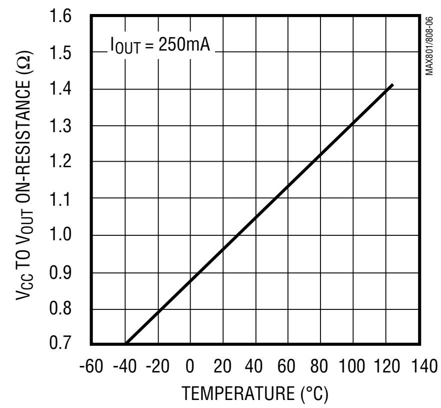
**MAX808
CHIP-ENABLE PROPAGATION DELAY
vs. $\overline{CE}$ OUT LOAD CAPACITANCE**



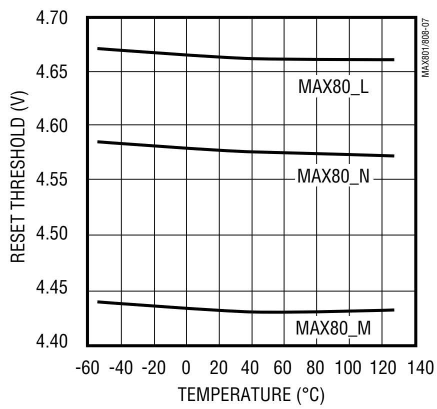
**BATT to OUT ON-RESISTANCE
vs. TEMPERATURE**



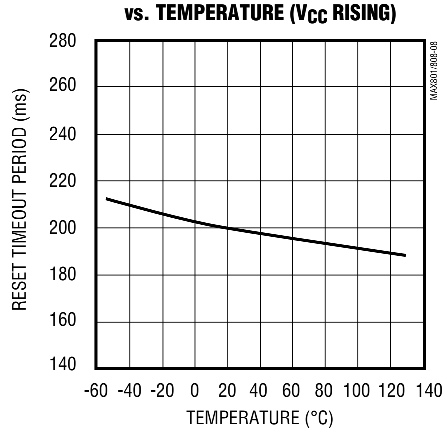
**V_{CC} to OUT ON-RESISTANCE
vs. TEMPERATURE**



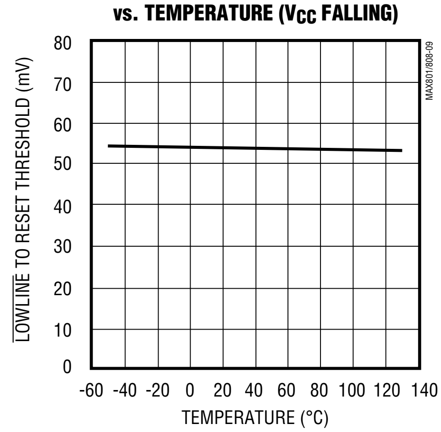
**RESET THRESHOLD
vs. TEMPERATURE**



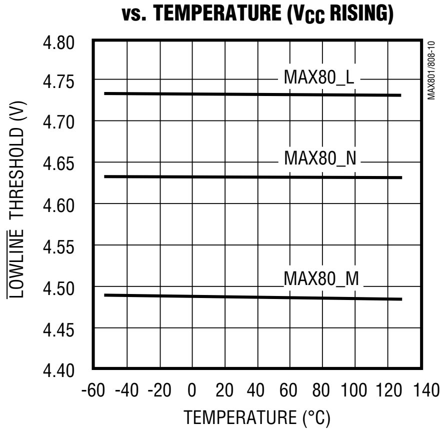
**RESET TIMEOUT PERIOD
vs. TEMPERATURE (V_{CC} RISING)**



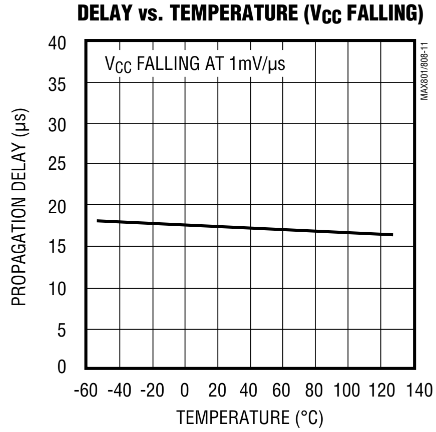
**$\overline{LOWLINE}$ to RESET THRESHOLD
vs. TEMPERATURE (V_{CC} FALLING)**



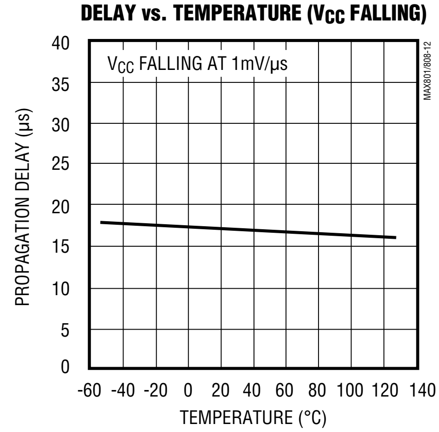
**$\overline{LOWLINE}$ THRESHOLD
vs. TEMPERATURE (V_{CC} RISING)**



**$\overline{LOWLINE}$ COMPARATOR PROPAGATION
DELAY vs. TEMPERATURE (V_{CC} FALLING)**



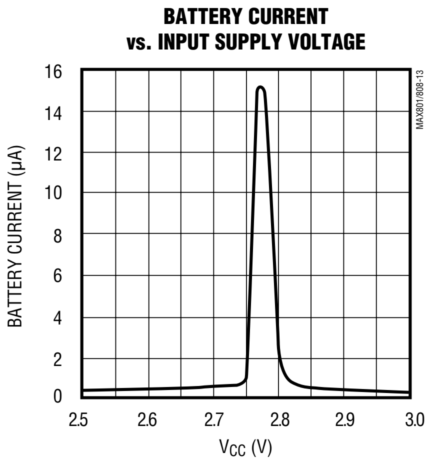
**RESET COMPARATOR PROPAGATION
DELAY vs. TEMPERATURE (V_{CC} FALLING)**

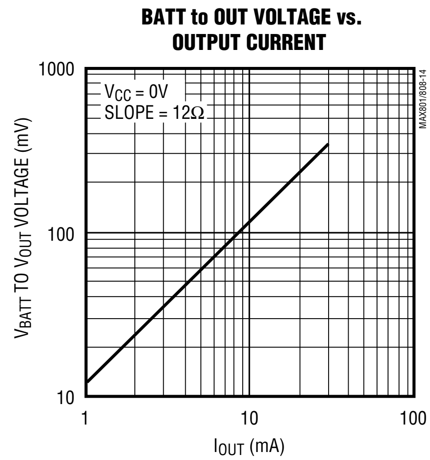


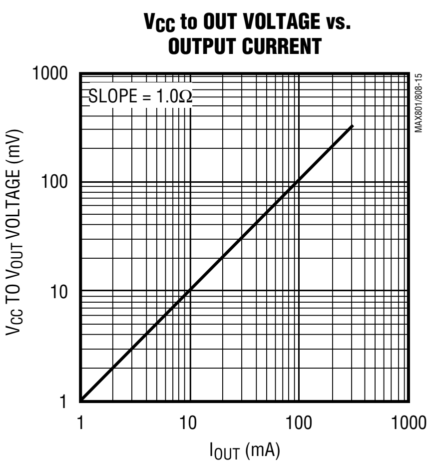
8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

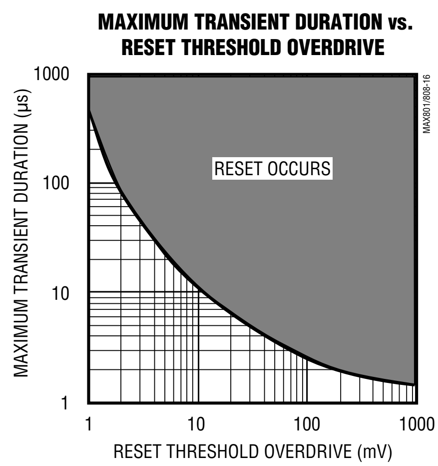
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{BATT} = 2.8V, no load, T_A = +25°C, unless otherwise noted.)









Pin Description

PIN		NAME	FUNCTION
MAX801	MAX808		
1	1	V_{CC}	Input Supply Voltage, nominally +5V. Bypass with a 0.1µF capacitor to GND.
2	2	$\overline{LOWLINE}$	Low-Line Comparator Output. This CMOS-logic output goes low when V_{CC} falls to 52mV above the reset threshold. Use $\overline{LOWLINE}$ to generate an NMI, initiating an orderly shut-down routine when V_{CC} is falling. $\overline{LOWLINE}$ swings between V_{CC} and GND.
3	3	$\overline{RESET}$	Active-Low Reset Output. $\overline{RESET}$ is triggered and stays low when V_{CC} is below the reset threshold (or during a watchdog timeout for the MAX801). It remains low 200ms after V_{CC} rises above the reset threshold (or 200ms after the watchdog timeout occurs). $\overline{RESET}$ has a strong pull-down but a relatively weak pull-up, and can be wire-OR connected to logic gates. Valid for V_{CC} ≥ 1V. $\overline{RESET}$ swings between V_{CC} and GND.
4	4	GND	Ground

Pin Description (continued)

PIN		NAME	FUNCTION
MAX801	MAX808		
5	—	RESET	Active-High Reset Output. RESET is the inverse of $\overline{RESET}$. It is a CMOS output that sources and sinks current. RESET swings between V_{CC} and GND.
—	5	$\overline{CE}$ OUT	Chip-Enable Output. Output to the chip-enable gating circuit. $\overline{CE}$ OUT is pulled up to the higher of V_{CC} or V_{BATT} when the chip-enable gate is disabled.
6	—	WDI	Watchdog Input. If WDI remains high or low longer than the watchdog timeout period (typically 1.6sec), $\overline{RESET}$ will be asserted for 200ms. Leave unconnected to disable the watchdog function.
—	6	$\overline{CE}$ IN	Chip-Enable Input
7	7	BATT	Backup-Battery Input. When V_{CC} falls below the reset threshold and V_{BATT}, OUT switches from V_{CC} to BATT. V_{BATT} may exceed V_{CC}. The battery can be removed while the MAX801/MAX808 is powered up, provided BATT is bypassed with a 0.1µF capacitor to GND. If no battery is used, connect BATT to ground and V_{CC} to OUT.
8	8	OUT	Output Supply Voltage to CMOS RAM. When V_{CC} exceeds the reset threshold or V_{BATT}, OUT connects to V_{CC}. When V_{CC} falls below the reset threshold and V_{BATT}, OUT connects to BATT. Bypass OUT with a 0.1µF capacitor to GND.

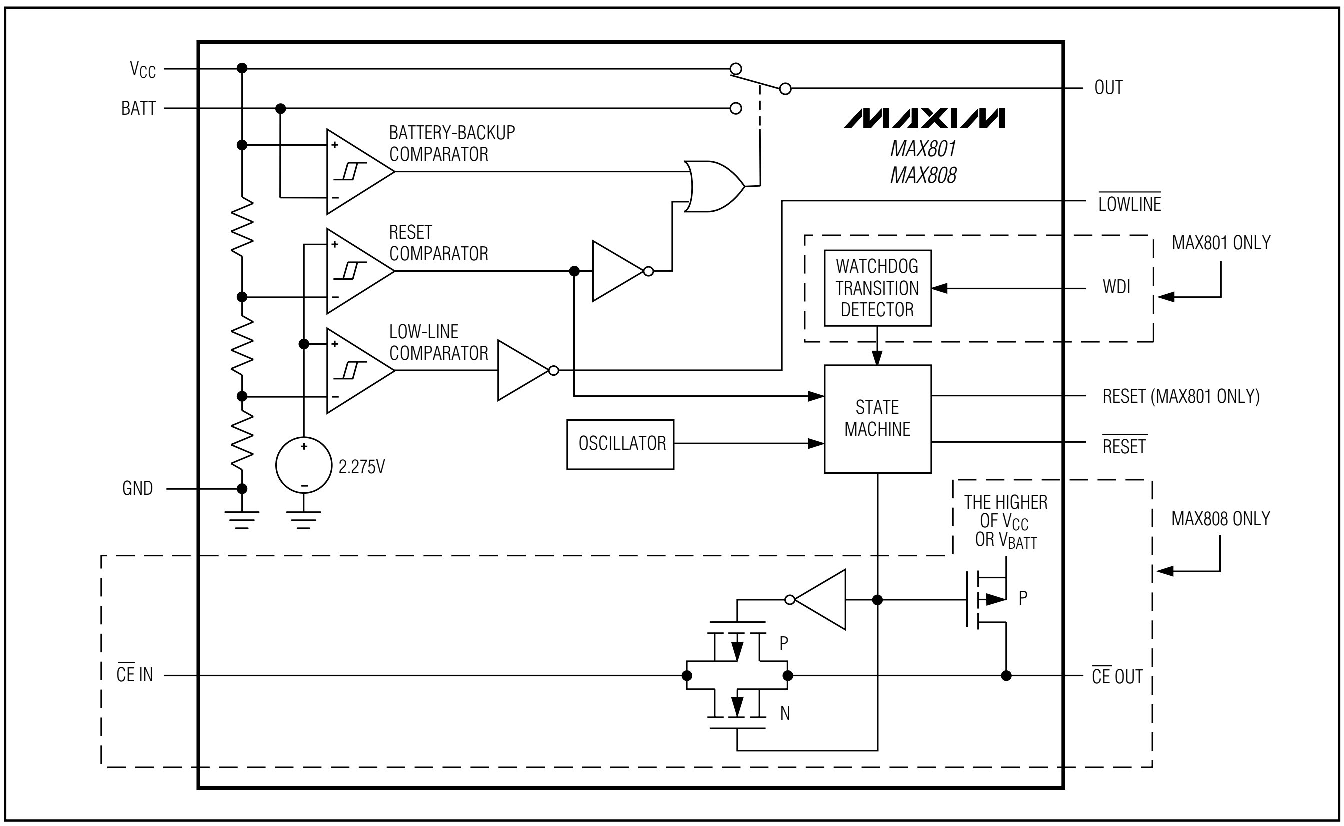


Figure 1. Functional Diagram

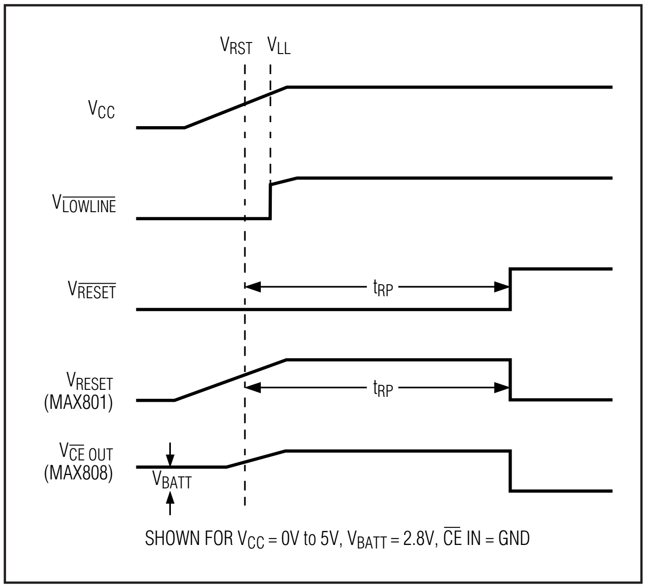


Figure 2a. Timing Diagram, V_{CC} Rising

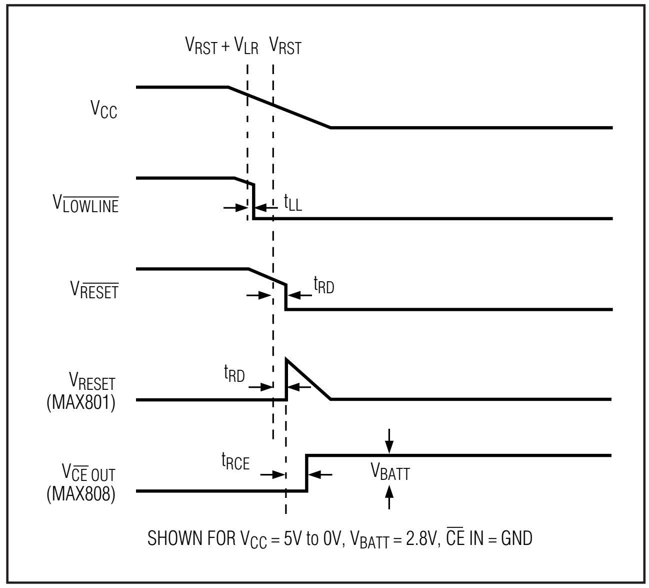


Figure 2b. Timing Diagram, V_{CC} Falling

Detailed Description

The MAX801/MAX808 microprocessor (µP) supervisory circuits provide power-supply monitoring and backup-battery switchover in µP systems. The MAX801 also provides program-execution watchdog functions (Figure 1). Use of BiCMOS technology results in an improved, 1.5% reset-threshold precision while keeping supply currents typically at 68µA (48µA for the MAX808). The MAX801/MAX808 are intended for battery-powered applications that require high reset-threshold precision, allowing a wide power-supply operating range while preventing the system from operating below its specified voltage range.

$\overline{\text{RESET}}$ and RESET Outputs

The MAX801/MAX808's $\overline{\text{RESET}}$ output ensures that the µP powers up in a known state, and prevents code-execution errors during power-down and brownout conditions. It does this by resetting the µP, terminating program execution when V_{CC} dips below the reset threshold. Each time $\overline{\text{RESET}}$ is asserted, it stays low for at least the 200ms reset timeout period (set by an internal timer) to ensure the µP has adequate time to return to an initial state. The internal timer restarts any time V_{CC} goes below the reset threshold (V_{RST}) before the reset timeout period is completed. The watchdog timer on the MAX801 can also initiate a reset (see the *MAX801 Watchdog Timer* section).

The $\overline{\text{RESET}}$ output is active low, and is implemented with a strong pull-down/relatively weak pull-up structure. It is guaranteed to be a logic low for $0V < V_{CC} < V_{RST}$, provided V_{BATT} is greater than 2V. Without a backup battery, $\overline{\text{RESET}}$ is guaranteed valid for $V_{CC} \geq 1V$.

The RESET output is the inverse of the $\overline{\text{RESET}}$ output; it both sources and sinks current and cannot be wire-OR connected.

Low-Line Comparator

The low-line comparator monitors V_{CC} with a threshold voltage typically 52mV above the reset threshold, with 13mV of hysteresis. Use $\overline{\text{LOWLINE}}$ to provide a non-maskable interrupt (NMI) to the µP when power begins to fall, initiating an orderly software shutdown routine. In most battery-operated portable systems, reserve energy in the battery provides ample time to complete the shutdown routine once the low-line warning is encountered and before reset asserts. If the system must contend with a more rapid V_{CC} fall time (such as when the main battery is disconnected, when a DC-DC converter shuts down, or when a high-side switch is opened during normal operation), use capacitance on the V_{CC} line to provide time to execute the shutdown routine (Figure 3). First calculate the worst-case time required for the system to perform its shutdown routine. Then, with worst-case shutdown time, worst-case load current, and minimum low-line to reset threshold ($V_{LR(min)}$),

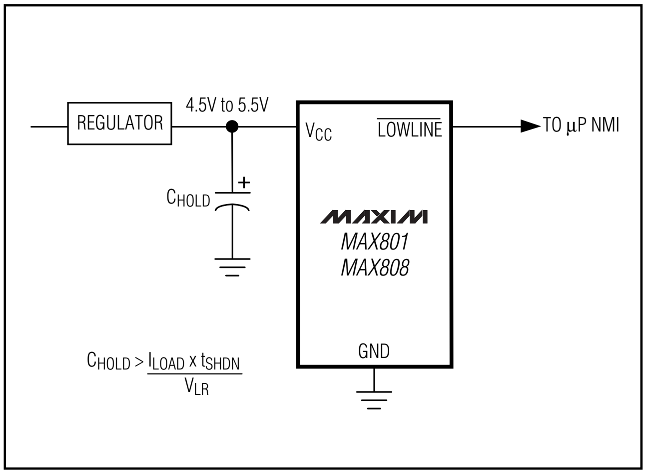


Figure 3. Using LOWLINE to Provide a Power-Fail Warning to the µP

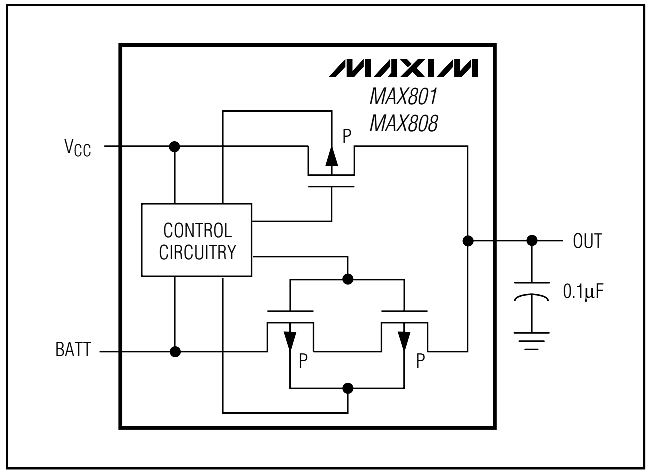


Figure 4. V_{CC} and BATT to OUT Switch

calculate the amount of capacitance required to allow the shutdown routine to complete before reset is asserted:

$$C_{HOLD} = (I_{LOAD} \times t_{SHDN}) / (V_{LR(min)})$$

where t_{SHDN} is the time required for the system to complete the shutdown routine (including the V_{CC} to low-line propagation delay), I_{LOAD} is the current being drained from the capacitor, and V_{LR} is the low-line to reset threshold.

Output Supply Voltage

The output supply (OUT) transfers power from V_{CC} or BATT to the µP, RAM, and other external circuitry. At the maximum source current of 250mA, V_{OUT} will typically be 220mV below V_{CC}. Decouple OUT with a 0.1µF capacitor to ground.

Battery-Backup Mode

Battery-backup mode preserves the contents of RAM in the event of a brownout or power failure. With a backup battery installed at BATT, the MAX801/MAX808 automatically switches RAM to backup power when V_{CC} falls. Two conditions are required for switchover to battery-backup mode: 1) V_{CC} must be below the reset threshold; 2) V_{CC} must be below V_{BATT}. Table 1 lists the status of inputs and outputs during battery-backup mode.

BATT is designed to conduct up to 20mA to OUT during battery backup. The PMOS switch on-resistance is approximately 12Ω. Figure 4 shows the two series pass elements (between the BATT input and OUT) that facilitate UL recognition. V_{BATT} can exceed V_{CC} during normal operation without causing a reset.

Table 1. Input and Output Status in Battery-Backup Mode

PIN		NAME	STATUS
MAX801	MAX808		
1	1	V_{CC}	Battery switchover comparator monitors V_{CC} for active switchover.
2	2	$\overline{\text{LOWLINE}}$	Logic low
3	3	$\overline{\text{RESET}}$	Logic low
4	4	GND	Ground—0V reference for all signals
5	—	RESET	Logic high; the open-circuit voltage is equal to V_{CC}.
—	5	$\overline{\text{CE}}$ OUT	Logic high. The open-circuit output voltage is equal to V_{BATT} (MAX808).
6	—	WDI	WDI is ignored and goes high impedance.
—	6	$\overline{\text{CE}}$ IN	High impedance (MAX808)
7	7	BATT	Supply current is 1µA max for $V_{BATT} \leq 2.8V$.
8	8	OUT	OUT is connected to BATT through two internal PMOS switches in series.

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

MAX801 Watchdog Timer

The watchdog monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, reset asserts for the reset timeout period. The internal 1.6sec timer is cleared when reset asserts or when a transition (low-to-high or high-to-low) occurs at WDI while reset is not asserted. The timer remains cleared and does not count as long as reset is asserted. It starts counting as soon as reset is released (Figure 5). Supply current is typically reduced by 10µA when WDI is at a valid logic level. To disable the watchdog function, leave WDI unconnected. An internal voltage divider sets WDI to about mid-supply, disabling the watchdog timer/counter.

MAX808 Chip-Enable Gating

The MAX808 provides internal gating of chip-enable (CE) signals to prevent erroneous data from corrupting CMOS RAM in the event of a power failure. During normal operation, the CE gate is enabled and passes all CE transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the CMOS RAM. The MAX808 uses a series transmission gate from the chip-enable input ($\overline{CE}$ IN) to the chip-enable output ($\overline{CE}$ OUT) (Figure 1). The 8ns max chip-enable propagation from $\overline{CE}$ IN to $\overline{CE}$ OUT enables the MAX808 to be used with most µPs.

The MAX808 also features write-cycle-completion circuitry. If V_{CC} falls below the reset threshold while the µP is writing to RAM, the MAX808 holds the CE gate enabled for 18µs to allow the µP to complete the write instruction. If the write cycle has not completed by the end of the 18µs period, the CE transmission gate turns off and $\overline{CE}$ OUT goes high. If the µP completes the write instruction during the 18µs period, the CE gate turns off (high impedance) and $\overline{CE}$ OUT goes high as soon as the µP pulls $\overline{CE}$ IN high. $\overline{CE}$ OUT remains high, even if $\overline{CE}$ IN falls low for any reason (Figure 6).

Chip-Enable Input

$\overline{CE}$ IN is high impedance (disabled mode) while reset is asserted. During a power-down sequence when V_{CC} passes the reset threshold, the CE transmission gate disables. $\overline{CE}$ IN becomes high impedance 18µs after reset asserts, provided $\overline{CE}$ IN is still low. If the µP completes the write instruction during the 18µs period, the CE gate turns off. $\overline{CE}$ IN becomes high impedance as soon as the µP pulls $\overline{CE}$ IN high. $\overline{CE}$ IN remains high impedance even if the signal at $\overline{CE}$ IN falls low (Figure 6). During a power-up sequence, $\overline{CE}$ IN remains high impedance (regardless of $\overline{CE}$ IN activity) until reset is deasserted following the reset timeout period.

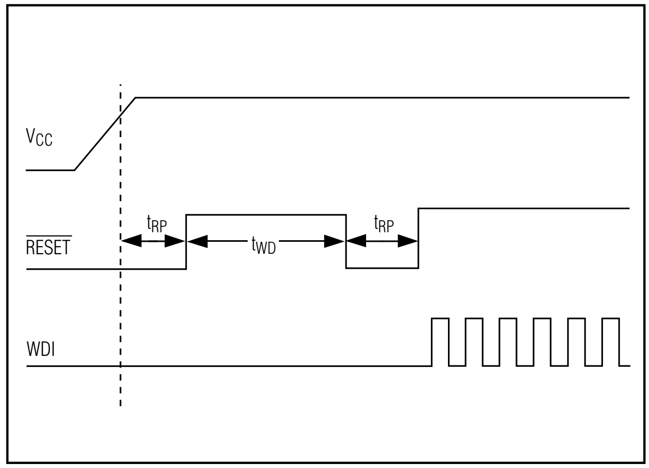


Figure 5. Watchdog Timing

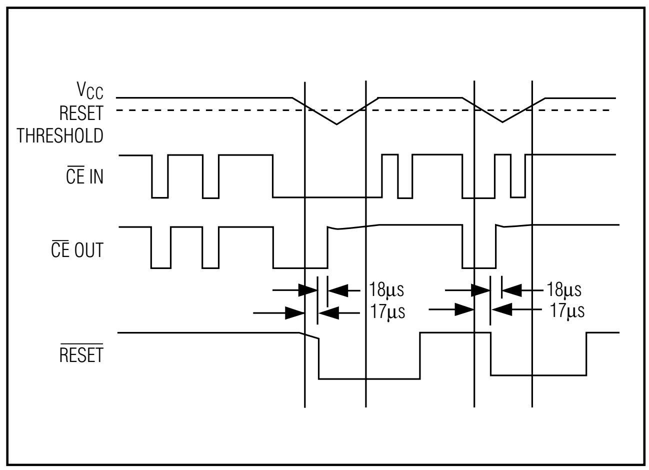


Figure 6. Chip-Enable Timing

In high-impedance mode, the leakage currents into this input are ±1µA max over temperature. In low-impedance mode, the impedance of $\overline{CE}$ IN appears as a 75Ω resistor in series with the load at $\overline{CE}$ OUT.

The propagation delay through the CE transmission gate depends on both the source impedance of the drive to $\overline{CE}$ IN and the capacitive loading on $\overline{CE}$ OUT (see the Chip-Enable Propagation Delay vs. $\overline{CE}$ OUT Load Capacitance graph in the *Typical Operating Characteristics*). The CE propagation delay is production tested from the 50% point on $\overline{CE}$ IN to the 50% point on $\overline{CE}$ OUT using a 50Ω driver and 50pF of load capacitance (Figure 7). For minimum propagation delay, minimize the capacitive load at $\overline{CE}$ OUT and use a low-output-impedance driver.

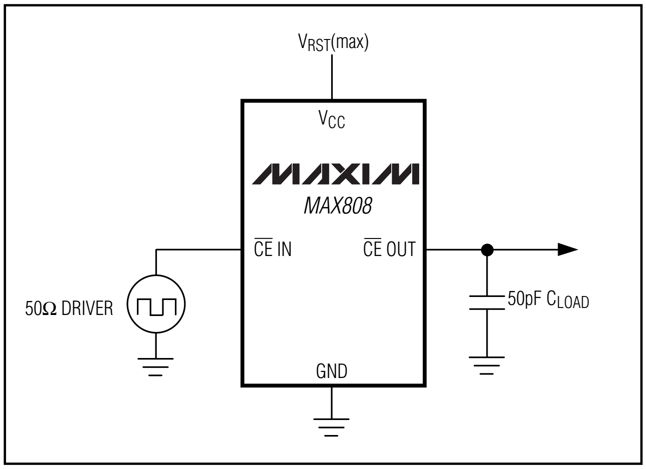


Figure 7. MAX808 CE Gate Test Circuit

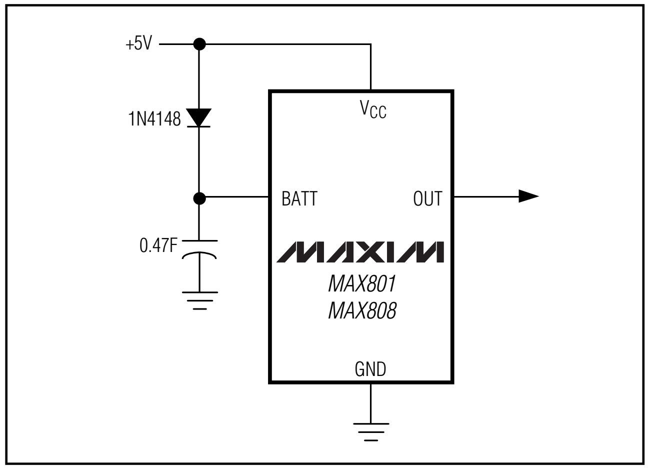


Figure 8. Using the MAX801/MAX808 with a SuperCap

Chip-Enable Output

In enabled mode, $\overline{CE}$ OUT's impedance is equivalent to 75Ω in series with the source driving $\overline{CE}$ IN. In disabled mode, the 75Ω transmission gate is off and $\overline{CE}$ OUT is actively pulled to the higher of V_{CC} or V_{BATT}. The source turns off when the transmission gate is enabled.

Applications Information

The MAX801/MAX808 are not short-circuit protected. Shorting OUT to ground, other than power-up transients such as charging a decoupling capacitor, may destroy the device. If long leads connect to the IC's inputs, ensure that these lines are free from ringing and other conditions that would forward bias the IC's protection diodes. Bypass OUT, V_{CC}, and BATT with 0.1µF capacitors to GND.

The MAX801/MAX808 operate in two distinct modes:

1) Normal Operating Mode, with all circuitry powered up. Typical supply current from V_{CC} is 68µA (48µA for the MAX808), while only leakage currents flow from the battery.
2) Battery-Backup Mode, where V_{CC} is below V_{BATT} and V_{RST}. The supply current from the battery is typically less than 1µA.

Using SuperCaps™ or MaxCaps™ with the MAX801/MAX808

BATT has the same operating voltage range as V_{CC}, and the battery-switchover threshold voltage is typically V_{BATT} when V_{CC} is decreasing or V_{BATT} + 0.05V when V_{CC} is increasing. This hysteresis allows use of a SuperCap (e.g., around 0.47F) and a simple charging circuit as a backup source (Figure 8). Since V_{BATT} can exceed V_{CC} while V_{CC} is above the reset threshold, no special precautions are needed when using these µP supervisors with a SuperCap.

Backup-Battery Replacement

The backup battery can be disconnected while V_{CC} is above the reset threshold, provided BATT is bypassed with a 0.1µF capacitor to ground. No precautions are necessary to avoid spurious reset pulses.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

The *Typical Operating Characteristics* show a graph of Maximum Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are not generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 40mV below the reset threshold and lasts for 3µs or less will not cause a reset pulse to be issued. A 0.1µF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

8-Pin µP Supervisory Circuits with ±1.5% Reset Accuracy

Watchdog Software Considerations

To help the watchdog timer keep a closer watch on software execution, you can set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop, where the watchdog timer continues to be reset within the loop, keeping the watchdog from timing out.

Figure 9 shows a sample flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, low at the beginning of every subroutine or loop, then high again when the program returns to the beginning. If the program should "hang" in any subroutine, the I/O would be continually set low and the watchdog timer would be allowed to time out, causing a reset or interrupt to be issued.

Maximum V_{CC} Fall Time

The V_{CC} fall time is limited by the propagation delay of the battery switchover comparator and should not exceed 0.03V/µs. A standard rule for filter capacitance on most regulators is around 100µF per Ampere of current. When the power supply is shut off or the main battery is disconnected, the associated initial V_{CC} fall rate is just the inverse, or 1A/100µF = 0.01V/µs.

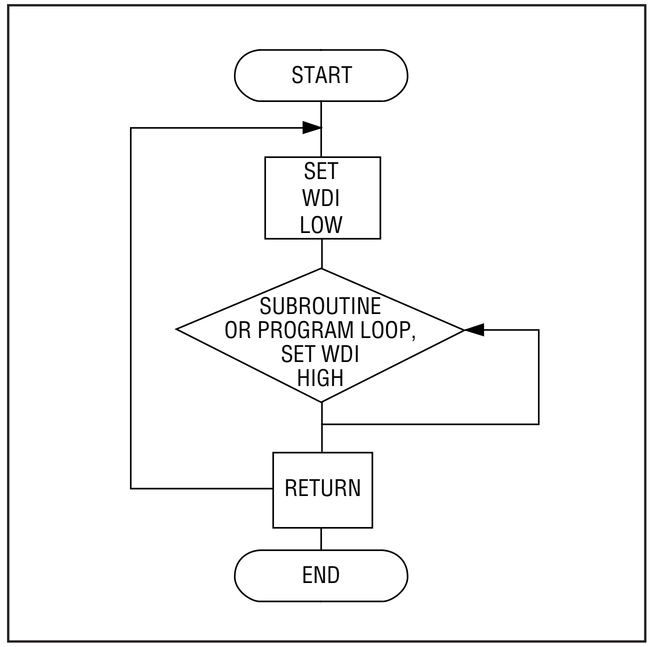
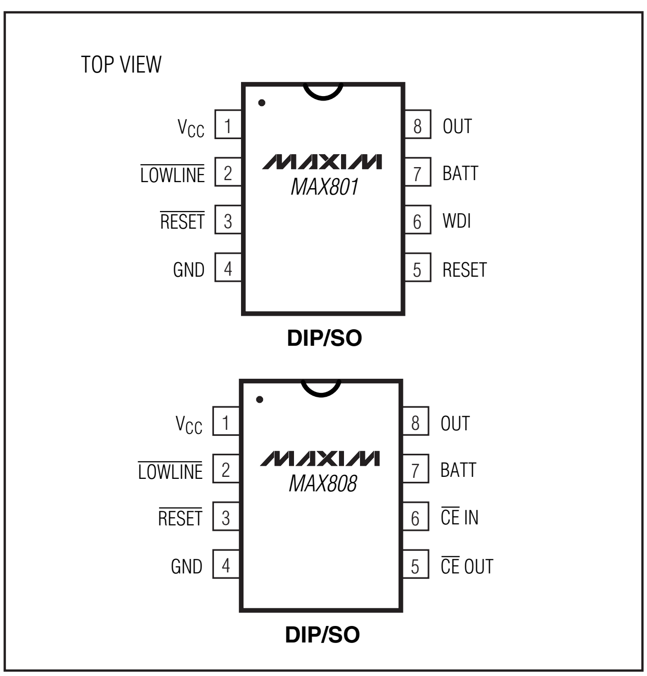


Figure 9. Watchdog Flow Diagram

Pin Configurations



Chip Information

TRANSISTOR COUNT: 922