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19-3178; Rev 0; 2/04

EVALUATION KIT AVAILABLE

Wide-Input, High-Frequency, Triple-Output Supplies with Voltage Monitor and Power-On Reset

General Description

The MAX8513/MAX8514 integrate a voltage-mode PWM step-down DC-DC controller and two LDO controllers, a voltage monitor, and a power-on reset for the lowest-cost power-supply and monitoring solution for xDSL modems, routers, gateways, and set-top boxes.

The DC-DC controller switching frequency can be set with an external resistor from 300kHz to 1.4MHz, to allow for the optimization of cost, size, and efficiency. For noise-sensitive applications, the DC-DC controller can also be synchronized to an external clock, minimizing noise interference. Operation above 1.1MHz reduces noise for high data-rate xDSL applications. An adjustable soft-start and adjustable foldback current limit provide reliable startup and fault protection. The DC-DC controller output voltage can be set externally to a voltage from 1.25V to 5.5V. Current limiting is accomplished by inductor current sensing for improved efficiency, or by an external sense resistor for better accuracy.

The MAX8513/MAX8514s' first LDO controller is designed to provide a low-cost, high-current regulated output from 0.8V to 5.5V using an N-channel MOSFET or a low-current output using a low-cost NPN transistor. The MAX8513's second regulator can be used to generate 0.8V to 27V output with a low-cost PNP transistor. Both LDO regulators can operate either from the DC-DC controller output or from a higher voltage derived with a flyback overwinding on the DC-DC converter inductor. The MAX8514's second LDO regulator is designed to provide a negative output with an NPN transistor.

A sequence input allows the outputs to either power up together, or for the DC-DC regulator to power up first and each LDO controller to power up in sequence. An input power-fail output ($\overline{PFO}$) is provided for input power-fail warning, such as in dying-gasp applications. A power-on reset circuit with a 140ms delay is also included to indicate when all outputs have achieved regulation and stabilized.

Applications

xDSL, Cable, ISDN Modems, and Routers

Wireless Routers

Set-Top Boxes

Automotive Dashboard Electronics

Pin Configurations appear at end of data sheet.

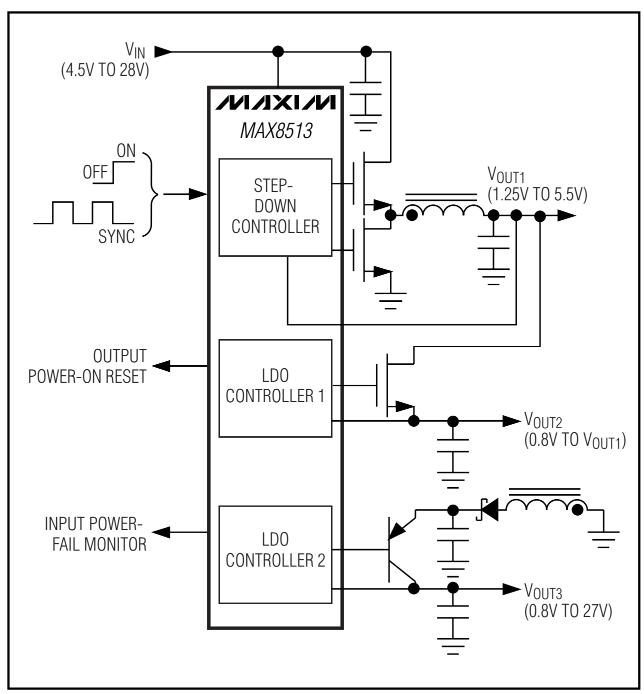
Features

- ♦ **Low-Cost DC-DC Controller with Two LDOs**
- ♦ **Wide Input Range: 4.5V to 28V**
- ♦ **300kHz to 1.4MHz Adjustable Switching Frequency**
- ♦ **Low Noise for High Data-Rate xDSL Applications**
- ♦ **Synchronizable to External Clock**
- ♦ **Adjustable Soft-Start**
- ♦ **Lossless Adjustable Foldback Current Limit**
- ♦ **Power-On Reset with 140ms Delay**
- ♦ **Adjustable Input Power-Fail Warning for Dying Gasp**
- ♦ **Selectable Output-Voltage Sequencing or Output-Voltage Tracking**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8513EEI	-40°C to +85°C	28 QSOP
MAX8514EEI	-40°C to +85°C	28 QSOP
MAX8514AEI	-40°C to +125°C	28 QSOP

Functional Diagram



Wide-Input, High-Frequency, Triple-Output Supplies with Voltage Monitor and Power-On Reset

ABSOLUTE MAXIMUM RATINGS

IN, DRV3P, SUP2 to GND.......................................-0.3V to +30V
DRV2 to GND ....-0.3V to (V_{SUP2} + 0.3V)
DRV3N to GND.....................(V_{SUP3N} - 28V) to (V_{SUP3N} + 0.3V)
FREQ, PFI, $\overline{PFO}$, $\overline{POR}$, SUP3N, SYNC/EN,
CSP, CSN to GND ....-0.3V to +6V
VL to GND ....-0.3V to the lesser of (V_{IN} + 0.3V) or +6V
COMP1, FB1, FB2, FB3P, FB3N, REF, ILIM,
SS, SEQ to GND.....................................-0.3V to (V_{VL} + 0.3V)
PVL to PGND...-0.3V to +6V
DL to PGND..-0.3V to (V_{PVL} + 0.3V)
BST to LX...-0.3V to +6V
DH to LX..-0.3V to (V_{BST} + 0.3V)
PGND to GND ....-0.3V to +0.3V
VL Short Circuit to GND ....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C).........860mW
Operating Temperature Range
MAX8513EEI, MAX8514EEI.............................-40°C to +85°C
MAX8514AEI..-40°C to +125°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
IN Operating Range			5.5		28.0	V
		IN = VL	4.5		5.5	
IN Supply Current		V_{FB1} = 1.3V, V_{FB2} = V_{FB3} = 1.0V, does not include switching current to PVL and BST, SYNC/EN = VL		2.6	3.2	mA
IN Shutdown Current		$V_{SYNC/EN}$ = 0, R_{FREQ} = 50kΩ		200	300	µA
VL REGULATOR						
VL Output Voltage		V_{IN} = 6V to 28V, I_{VL} = 0.1mA to 40mA	4.75	5	5.25	V
VL Dropout Voltage		From IN to VL, V_{IN} = 5V, I_{VL} = 40mA			560	mV
VL Line Regulation		V_{IN} = 6V to 28V, I_{VL} = 5mA		0.05		%
VL Undervoltage Threshold		VL rising, V_{HYST} = 675mV (typ)	3.6		4.2	V
OUT1 (BUCK CONVERTER)						
Output Voltage Range	V_{OUT1}	(Note 1)	1.25		5.50	V
FB1 Regulation Threshold	V_{FB1}		1.234	1.25	1.259	V
Error-Amplifier Open-Loop Voltage Gain	A_{VOL}		65	90		dB
FB1 Input Bias Current	I_{FB1_BIAS}	V_{FB1} = 1.3V	-200	+10	+200	nA
Error-Amplifier Gain Bandwidth				25		MHz
DH Output-Resistance High	R_{DH_HIGH}			1.5	2.55	Ω
DH Output-Resistance Low	R_{DH_LOW}			1.2	2.1	Ω
DL Output-Resistance High	R_{DL_HIGH}			2.5	5	Ω
DL Output-Resistance Low	R_{DL_LOW}			0.7	1.3	Ω
Driver Dead Time	t_{dt}	Starts from V_{DL} = 1V or (V_{DH} - V_{LX}) = 1V		50		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Threshold (Positive)	V_{CS}	V_{ILIM} = 2.00V, V_{CSN} = 0 to 5.5V	246	275	300	mV
		V_{ILIM} = 0.50V, V_{CSN} = 0 to 5.5V	50	67	81	
		V_{ILIM} = V_{VL}, V_{CSN} = 0 to 5.5V	151	170	188	
Current-Limit Threshold (Negative)	V_{CS}	V_{ILIM} = 2.00V, V_{CSN} = 0 to 5.5V	-333	-272	-199	mV
		V_{ILIM} = 0.50V, V_{CSN} = 0 to 5.5V	-90	-67	-42	
		V_{ILIM} = V_{VL}, V_{CSN} = 0 to 5.5V	-210	-166	-122	
CSP and CSN Bias Current		V_{CSP} = V_{CSN} = 0 to 5.5V	-120		+135	µA
ILIM Bias Current		V_{ILIM} = 1.25V	-5.3	-5	-4.7	µA
SS Soft-Start Charge Current		V_{SS} = 0.6V	15	25	35	µA
Soft-Start Discharge Resistance				100	200	Ω
LX, BST, PVL Leakage Current		V_{LX} = V_{IN} = 28V, V_{BST} = 33V, V_{PVL} = 5V, $V_{SYNC/EN}$ = 0		0.03	20	µA
FB1 Power-On Reset Threshold			1.08	1.125	1.20	V
OUT2 (POSITIVE LDO)						
SUP2 Operating Range	V_{SUP2}	(Note 1)	4.5		28.0	V
DRV2 Clamp Voltage	V_{DRV2}	V_{FB2} = 0.75V	7.75		9.00	V
SUP2 Supply Current				160	300	µA
SUP2 Shutdown Supply Current		$V_{SYNC/EN}$ = 0		3	10	µA
FB2 Regulation Voltage	V_{FB2}		0.784	0.80	0.808	V
FB2 Input Bias Current	I_{FB2_BIAS}	V_{FB2} = 0.75V		0.01	100	nA
DRV2 Output Current Limit		V_{IN} = 5V, V_{DRV2} = 5V, V_{FB2} = 0.77V	15	30		mA
DRV2 Output Current Limit During Soft-Start		V_{IN} = 6V, V_{DRV2} = 5V, V_{FB2} = 0.70V	8	10	12	mA
FB2 Power-On Reset Threshold			0.690	0.720	0.742	V
FB2 to DRV2 Transconductance	G_{C2}	I_{DRV2} = +250µA, -250µA	0.12	0.2	0.36	S
OUT3P (POSITIVE PNP LDO) (MAX8513 ONLY)						
DRV3P Operating Range	V_{DRV3P}		1		28	V
FB3P Regulation Voltage		V_{DRV3P} = 5V, I_{DRV3P} = 1mA	0.790	0.803	0.816	V
FB3P to DRV3P Large-Signal Transconductance	G_{C3P}	V_{DRV3P} = 5V, I_{DRV3P} = 0.5mA to 5mA	0.38	0.6	1.1	S
Feedback Input Bias Current		V_{FB3P} = 0.75V		0.01	100	nA
Driver Sink Current		V_{FB3P} = 0.75V, DRV3P = 2.5V	15	35		mA
		V_{FB3P} = 0.75V, DRV3P = 4.0V		40		
FB3P POR Threshold			0.690	0.720	0.742	V
FB3P Soft-Start Period				1312		Clock Cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT3N (NEGATIVE NPN LDO CONTROLLER) (MAX8514 ONLY)						
SUP3N Operating Range		(Note 1)	1.5		5.5	V
DRV3N Operating Range		(Note 1)	V_{SUP3N} - 21V		V_{SUP3N} - 1.5V	V
SUP3N Supply Current		V_{DRV3N} = 1.5V, V_{SUP3N} = 3.5V, I_{DRV3N} = -1mA (source)		1.1	2	mA
FB3N Regulation Voltage		V_{DRV3N} = 1.5V, V_{SUP3N} = 3.5V, I_{DRV3N} = -1mA (source)	-20	-5	+10	mV
FB3N to DRV3N Large-Signal Transconductance	G_{C3N}	V_{DRV3N} = 0, I_{DRV3N} = -0.5mA to -5mA (source)	0.225	0.36	0.550	S
Feedback Input Bias Current		V_{FB3N} = -100mV		60	1000	nA
Driver Source Current		V_{FB3N} = 200mV, V_{DRV3N} = 0, V_{SUP3N} = 3.5V	13	25		mA
FB3N POR Threshold			450	500	550	mV
FB3N Soft-Start Period				2048		Clock Cycles
REFERENCE						
REF Output Voltage	V_{REF}	-2µA < I_{REF} < +50µA	1.231	1.25	1.269	V
OSCILLATOR						
Frequency	f_S	R_{FREQ} = 10.7kΩ ±1% from FREQ to GND	1300	1390	1460	kHz
		R_{FREQ} = 15.0kΩ ±1% from FREQ to GND	933	985	1040	
		R_{FREQ} = 50.0kΩ ±1% from FREQ to GND	260	290	324	
FREQ Resistance-Frequency Product				15.0		MHz × kΩ
Maximum Duty Cycle (Measured at DH Pin)		R_{FREQ} = 10.7kΩ ±1% from FREQ to GND	77	83	91	%
		R_{FREQ} = 15.0kΩ ±1% from FREQ to GND	80	87	95	
		R_{FREQ} = 50.0kΩ ±1% from FREQ to GND	93	96	99	
Minimum On-Time (Measured at DH Pin)		R_{FREQ} = 10.7kΩ ±1% from FREQ to GND		20	62	ns
SYNC/EN Pulse Width		Low or high (Note 1)	200			ns
SYNC/EN Frequency Range		SYNC/EN input frequency needs to be within ±30% of the value set at the FREQ pin (Note 1)	200		1850	kHz
SYNC/EN Input Voltage, High			2.4			V
SYNC/EN Input Voltage, Low					0.8	V
SYNC/EN Input Current		$V_{SYNC/EN}$ = 0 to 5.5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SEQ, PFI, $\overline{PFO}$, $\overline{POR}$							
SEQ Input-Voltage High				2.4			V
SEQ Input-Voltage Low						0.8	V
SEQ Input Current		V_{SEQ} = 0 to V_{VL}			1	10	µA
$\overline{POR}$ Output-Voltage Low		V_{FB1}, V_{FB2}, V_{FB3P}, V_{FB3N}, out-of-regulation	$I_{\overline{POR}}$ = 1.6mA		10	200	mV
			$I_{\overline{POR}}$ = 0.1mA, V_{IN} = 1.0V		20	200	
$\overline{POR}$ Output Leakage Current		V_{FB1}, V_{FB2}, and V_{FB3P} or V_{FB3N}, in-regulation			0.001	1	µA
$\overline{POR}$ Power-Ready Delay Time		From V_{FB1}, V_{FB2}, and V_{FB3P} or V_{FB3N}, in-regulation to $\overline{POR}$ = high impedance		140	315	560	ms
PFI Input Threshold		Falling, V_{HYST} = 20mV		1.20	1.22	1.25	V
PFI Input Bias Current		V_{PFI} = 1.0V			0.1	100	nA
$\overline{PFO}$ Output-Voltage Low		PFI = 1.1V	$I_{\overline{PFO}}$ = 1.6mA		20	200	mV
			$I_{\overline{PFO}}$ = 0.1mA, V_{IN} = 1.0V		10	200	
$\overline{PFO}$ Output Leakage Current		PFI = 1.4V, $\overline{PFO}$ = 5V			0.001	1	µA
THERMAL PROTECTION							
Thermal Shutdown		Junction temperature rising			+170		°C
Thermal-Shutdown Hysteresis					25		°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = -40°C to +125°C** (Note 2), unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
GENERAL					
IN Operating Range			5.5	28.0	V
		IN = VL	4.5	5.5	
IN Supply Current		V_{FB1} = 1.3V, V_{FB2} = V_{FB3} = 1.0V, does not include switching current to PVL and BST, SYNC/EN = VL		3.2	mA
IN Shutdown Current		$V_{SYNC/EN}$ = 0, R_{FREQ} = 50kΩ		300	µA
VL REGULATOR					
VL Output Voltage		V_{IN} = 6V to 28V, I_{VL} = 0.1mA to 40mA	4.75	5.25	V
VL Dropout Voltage		From IN to VL, V_{IN} = 5V, I_{VL} = 40mA		610	mV
VL Undervoltage Threshold		VL rising, V_{HYST} = 675mV (typ)	3.6	4.2	V

Wide-Input, High-Frequency, Triple-Output Supplies with Voltage Monitor and Power-On Reset

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = -40°C to +125°C** (Note 2), unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
OUT1 (BUCK CONVERTER)					
Output Voltage Range	V_{OUT1}	(Note 1)	1.25	5.50	V
FB1 Regulation Threshold	V_{FB1}		1.225	1.265	V
Error-Amplifier Open-Loop Voltage Gain	A_{VOL}		65		dB
FB1 Input Bias Current	I_{FB1_BIAS}	V_{FB1} = 1.3V	-200	+200	nA
DH Output-Resistance High	R_{DH_HIGH}			2.55	Ω
DH Output-Resistance Low	R_{DH_LOW}			2.1	Ω
DL Output-Resistance High	R_{DL_HIGH}			5	Ω
DL Output-Resistance Low	R_{DL_LOW}			1.3	Ω
Current-Limit Threshold (Positive)	V_{CS}	V_{ILIM} = 2.00V, V_{CSN} = 0 to 5.5V	243	303	mV
		V_{ILIM} = 0.50V, V_{CSN} = 0 to 5.5V	49	83	
		V_{ILIM} = V_{VL}, V_{CSN} = 0 to 5.5V	147	190	
Current-Limit Threshold (Negative)	V_{CS}	V_{ILIM} = 2.00V, V_{CSN} = 0 to 5.5V	-333	-199	mV
		V_{ILIM} = 0.50V, V_{CSN} = 0 to 5.5V	-90	-42	
		V_{ILIM} = V_{VL}, V_{CSN} = 0 to 5.5V	-210	-122	
CSP and CSN Bias Current		V_{CSP} = V_{CSN} = 0 to 5.5V	-120	+135	µA
ILIM Bias Current		V_{ILIM} = 1.25V	-5.7	-4.3	µA
SS Soft-Start Charge Current		V_{SS} = 0.6V	15	35	µA
Soft-Start Discharge Resistance				200	Ω
LX, BST, PVL Leakage Current		V_{LX} = V_{IN} = 28V, V_{BST} = 33V, V_{PVL} = 5V, $V_{SYNC/EN}$ = 0		20	µA
FB1 Power-On Reset Threshold			1.08	1.20	V
OUT2 (POSITIVE LDO)					
SUP2 Operating Range	V_{SUP2}	(Note 1)	4.5	28.0	V
DRV2 Clamp Voltage	V_{DRV2}	V_{FB2} = 0.75V	7.75	9.00	V
SUP2 Supply Current				300	µA
SUP2 Shutdown Supply Current		$V_{SYNC/EN}$ = 0		10	µA
FB2 Regulation Voltage	V_{FB2}		0.775	0.816	V
FB2 Input Bias Current	I_{FB2_BIAS}	V_{FB2} = 0.75V		150	nA
DRV2 Output Current Limit		V_{IN} = 5V, V_{DRV2} = 5V, V_{FB2} = 0.77V	12		mA
DRV2 Output Current Limit During Soft-Start		V_{IN} = 6V, V_{DRV2} = 5V, V_{FB2} = 0.70V	8	12	mA
FB2 Power-On Reset Threshold			0.690	0.742	V
FB2 to DRV2 Transconductance	G_{C2}	I_{DRV2} = +250µA, -250µA	0.11	0.41	S

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{LX} = V_{SUP2} = 12V, V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P} = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = -40°C to +125°C** (Note 2), unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
OUT3P (POSITIVE PNP LDO) (MAX8513 ONLY)						
DRV3P Operating Range	V_{DRV3P}			1	28	V
FB3P Regulation Voltage		V_{DRV3P} = 5V, I_{DRV3P} = 1mA		0.780	0.820	V
FB3P to DRV3P Large-Signal Transconductance	G_{C3P}	V_{DRV3P} = 5V, I_{DRV3P} = 0.5mA to 5mA		0.3	1.4	S
Feedback Input Bias Current		V_{FB3P} = 0.75V			100	nA
Driver Sink Current		V_{FB3P} = 0.75V	DRV3P = 2.5V	15		mA
FB3P POR Threshold				0.690	0.742	V
OUT3N (NEGATIVE NPN LDO CONTROLLER) (MAX8514 ONLY)						
SUP3N Operating Range		(Note 1)		1.5	5.5	V
DRV3N Operating Range		(Note 1)		V_{SUP3N} - 21V	V_{SUP3N} - 1.5V	V
SUP3N Supply Current		V_{DRV3N} = 1.5V, V_{SUP3N} = 3.5V, I_{DRV3N} = -1mA (source)			2	mA
FB3N Regulation Voltage		V_{DRV3N} = 1.5V, V_{SUP3N} = 3.5V, I_{DRV3N} = -1mA (source)		-20	+10	mV
FB3N to DRV3N Large-Signal Transconductance	G_{C3N}	V_{DRV3N} = 0, I_{DRV3N} = -0.5mA to -5mA (source)		0.225	0.550	S
Feedback Input Bias Current		V_{FB3N} = -100mV			1500	nA
Driver Source Current		V_{FB3N} = 200mV, V_{DRV3N} = 0, V_{SUP3N} = 3.5V		13		mA
FB3N POR Threshold				450	550	mV
REFERENCE						
REF Output Voltage	V_{REF}	-2µA < I_{REF} < +50µA		1.22	1.27	V
OSCILLATOR						
Frequency	f_S	R_{FREQ} = 10.7kΩ ±1% from FREQ to GND		1300	1500	kHz
		R_{FREQ} = 15.0kΩ ±1% from FREQ to GND		917	1070	
		R_{FREQ} = 50.0kΩ ±1% from FREQ to GND		250	335	
Maximum Duty Cycle (Measured at DH Pin)		R_{FREQ} = 10.7kΩ ±1% from FREQ to GND		77	91	%
		R_{FREQ} = 15.0kΩ ±1% from FREQ to GND		80	95	
		R_{FREQ} = 50.0kΩ ±1% from FREQ to GND		93	99	
Minimum On-Time (Measured at DH Pin)		R_{FREQ} = 10.7kΩ ±1% from FREQ to GND			62	ns
SYNC/EN Pulse Width		Low or high (Note 1)		200		ns
SYNC/EN Frequency Range		SYNC/EN input frequency needs to be within ±30% of the value set at the FREQ pin (Note 1)		200	1850	kHz

Wide-Input, High-Frequency, Triple-Output Supplies with Voltage Monitor and Power-On Reset

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{LX} = V_{SUP2}$ = 12V, $V_{PVL} = V_{BST} - V_{LX} = V_{DRV3P}$ = 5V, V_{SUP3N} = 3.3V, V_{DRV3N} = -5V, C_{VL} = 4.7µF, C_{REF} = 0.22µF, R_{FREQ} = 15.0kΩ, **T_A = -40°C to +125°C** (Note 2), unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
SYNC/EN Input-Voltage High				2.4		V
SYNC/EN Input-Voltage Low					0.8	V
SYNC/EN Input Current		$V_{SYNC/EN}$ = 0 to 5.5V		-1	+1	µA
SEQ, PFI, $\overline{\text{PFO}}$, $\overline{\text{POR}}$						
SEQ Input-Voltage High				2.4		V
SEQ Input-Voltage Low					0.8	V
SEQ Input Current		V_{SEQ} = 0 to V_{VL}			10	µA
$\overline{\text{POR}}$ Output-Voltage Low		V_{FB1}, V_{FB2}, V_{FB3P}, V_{FB3N} out-of-regulation	$I_{\overline{POR}}$ = 1.6mA		200	mV
			$I_{\overline{POR}}$ = 0.1mA, V_{IN} = 1.0V		200	
$\overline{\text{POR}}$ Output Leakage Current		V_{FB1}, V_{FB2}, and V_{FB3P} or V_{FB3N}, in-regulation			1	µA
$\overline{\text{POR}}$ Power-Ready Delay Time		From V_{FB1}, V_{FB2}, and V_{FB3P} or V_{FB3N}, in-regulation to $\overline{\text{POR}}$ = high impedance		140	560	ms
PFI Input Threshold		Falling, V_{HYST} = 20mV		1.20	1.25	V
PFI Input Bias Current		V_{PFI} = 1.0V			300	nA
$\overline{\text{PFO}}$ Output-Voltage Low		PFI = 1.1V	$I_{\overline{PFO}}$ = 1.6mA		200	mV
			$I_{\overline{PFO}}$ = 0.1mA, V_{IN} = 1.0V		200	
$\overline{\text{PFO}}$ Output Leakage Current		PFI = 1.4V, $\overline{\text{PFO}}$ = 5V			1	µA

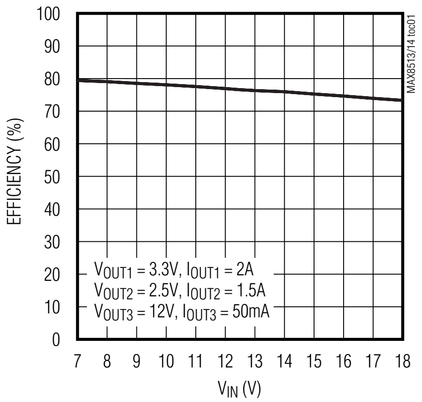
Note 1: Guaranteed by design, not production tested.

Note 2: Specifications to -40°C are guaranteed by design, not production tested.

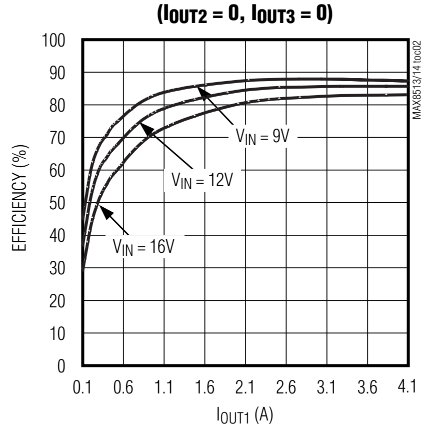
Typical Operating Characteristics

(Circuit of MAX8513 evaluation kit, V_{IN} = 12V, T_A = +25°C, f_S = 1.4MHz, unless otherwise noted.)

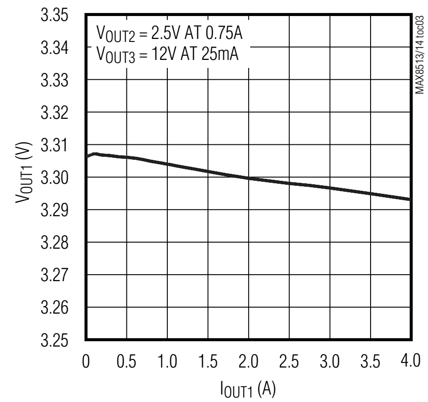
EFFICIENCY vs. INPUT VOLTAGE



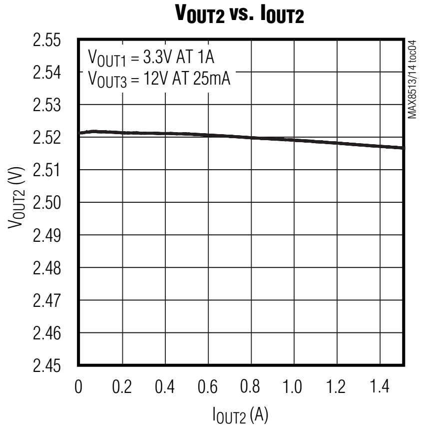
EFFICIENCY vs. I_{OUT1} (I_{OUT2} = 0, I_{OUT3} = 0)



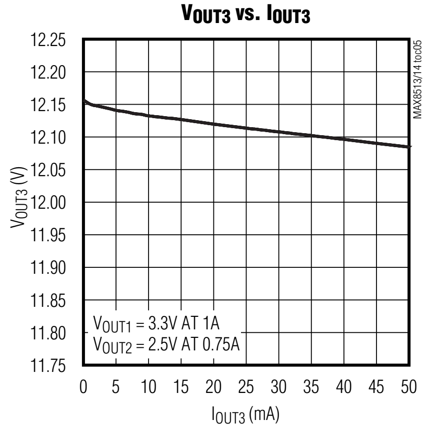
V_{OUT1} vs. I_{OUT1}



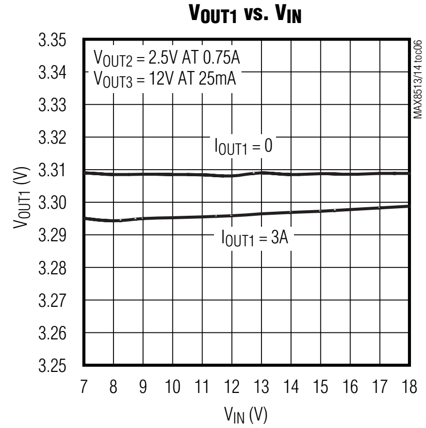
V_{OUT2} vs. I_{OUT2}



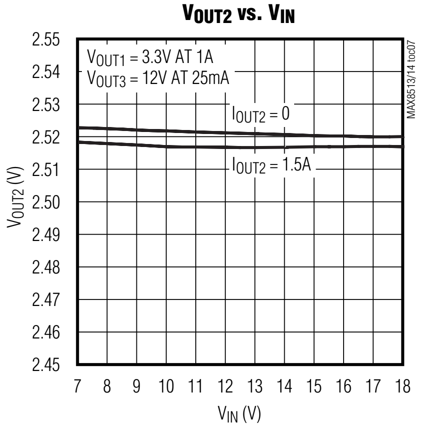
V_{OUT3} vs. I_{OUT3}



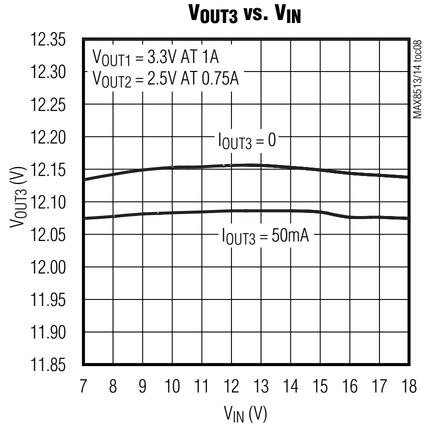
V_{OUT1} vs. V_{IN}



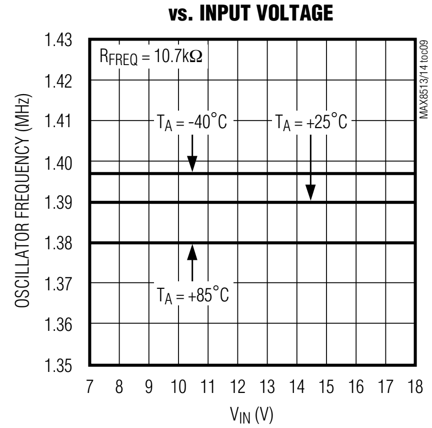
V_{OUT2} vs. V_{IN}



V_{OUT3} vs. V_{IN}



OSCILLATOR FREQUENCY vs. INPUT VOLTAGE

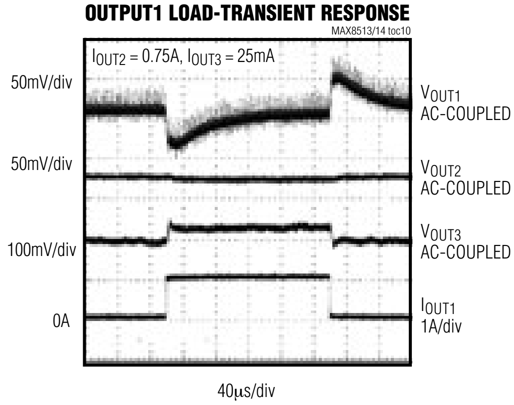


Wide-Input, High-Frequency, Triple-Output Supplies with Voltage Monitor and Power-On Reset

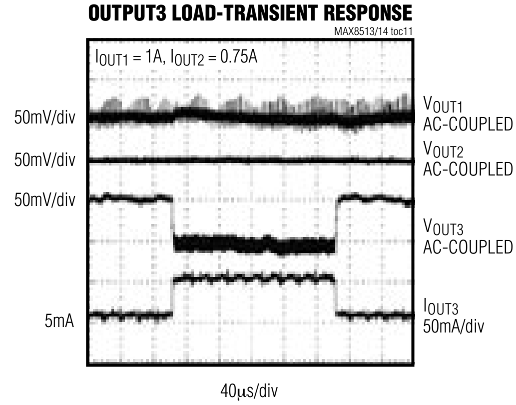
Typical Operating Characteristics (continued)

(Circuit of MAX8513 evaluation kit, V_{IN} = 12V, T_A = +25°C, f_S = 1.4MHz, unless otherwise noted.)

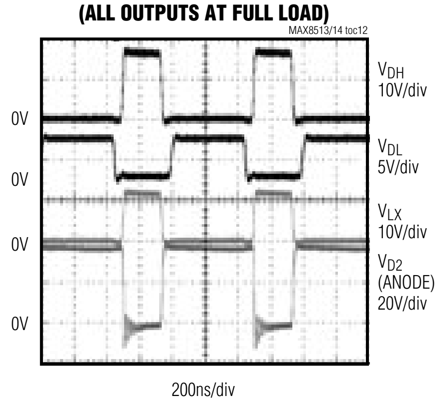
OUTPUT1 LOAD-TRANSIENT RESPONSE



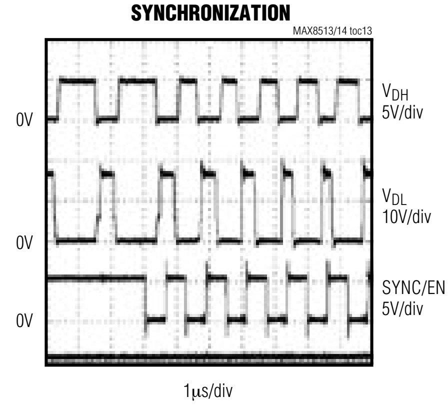
OUTPUT3 LOAD-TRANSIENT RESPONSE



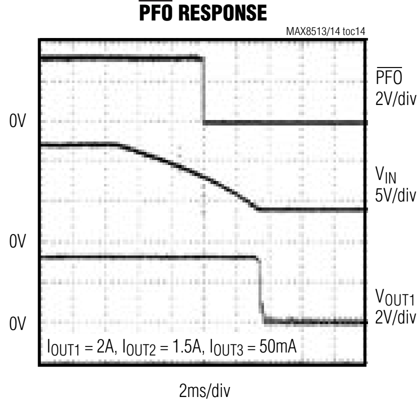
SWITCHING WAVEFORMS (ALL OUTPUTS AT FULL LOAD)



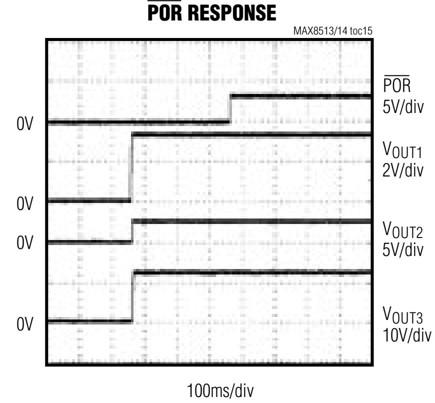
SYNCHRONIZATION



$\overline{\text{PFO}}$ RESPONSE

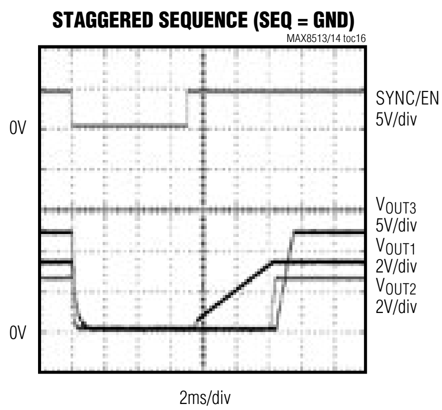


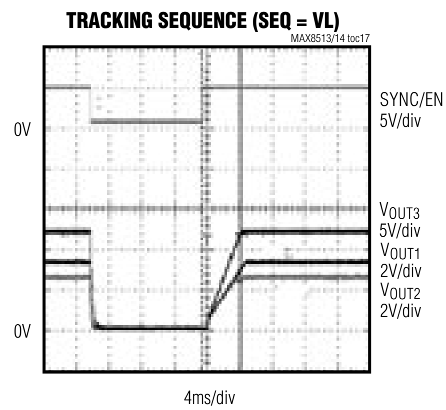
$\overline{\text{POR}}$ RESPONSE

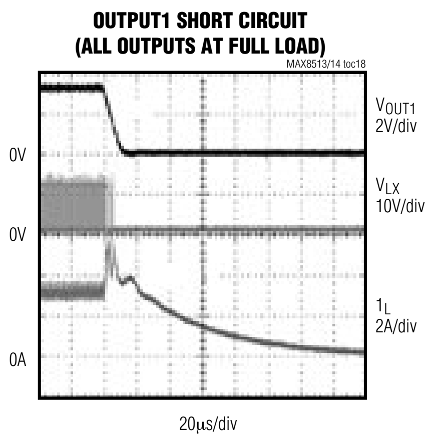


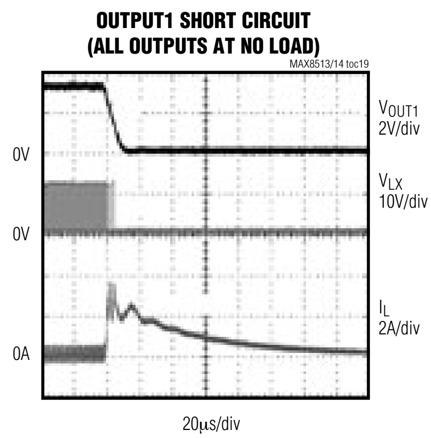
Typical Operating Characteristics (continued)

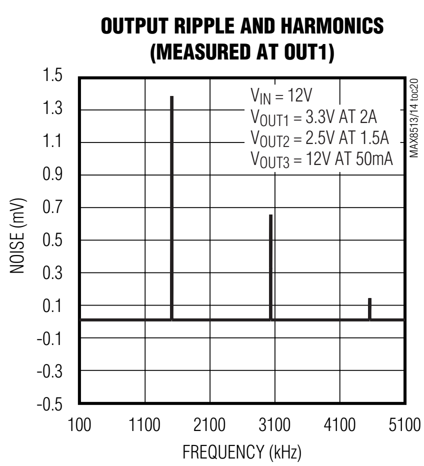
(Circuit of MAX8513 evaluation kit, V_{IN} = 12V, T_A = +25°C, f_S = 1.4MHz, unless otherwise noted.)











Pin Description

PIN NAME	MAX8513	MAX8514	FUNCTION
PFI	1	1	Power-Fail Input. Connect PFI to an external resistive-divider between IN, PFI, and GND. PFI senses V_{IN} to detect voltage failure. Trip falling threshold at this input is 1.22V, with 20mV of hysteresis.
$\overline{PFO}$	2	2	Power-Fail Output. Open-drain output that goes low if V_{PFI} < 1.22V.
DH	3	3	OUT1 High-Side Gate-Drive Output. DH drives the high-side N-channel MOSFET (Q1 in the *Typical Applications Circuits*). DH is a floating driver output that swings from LX to BST.
LX	4	4	OUT1 High-Side Driver Return Path. The high-side FET driver uses BST and LX for its respective high and low-side supplies.
BST	5	5	OUT1 Boost Capacitor Connection for High-Side Gate Drive. Connect a 0.1µF ceramic capacitor from BST to LX with a less than 5mm trace length.
DL	6	6	OUT1 Low-Side Gate-Drive Output. DL drives the low-side N-channel MOSFET (Q2 in the *Typical Applications Circuits*). DL swings from 0 to V_{PVL}.
PVL	7	7	OUT1 Gate-Drive Supply Bypass Connection. Connect PVL to VL through a 10Ω resistor (R15), and bypass PVL to PGND with a minimum 1µF capacitor (C1).
PGND	8	8	Power-Ground Connection and Low-Side Supply for Dl Driver
VL	9	9	Internal +5V Linear-Regulator Bypass Pin. Bypass VL to GND with a minimum 2.2µF ceramic capacitor (C10) and 5mm or less of trace length. VL should be connected to IN when V_{IN} < 5.5V.
COMP1	10	10	OUT1 Compensation Node. See the *OUT1 Compensation* section.
FB1	11	11	OUT1 Feedback Input. Connect a resistive-divider (R1, R2) from OUT1 to FB1 to GND to regulate FB1 at 1.25V.
FREQ	12	12	Oscillator Frequency-Set Input. A resistor from FREQ to GND sets the oscillator frequency from 300kHz to 1.4MHz (f = 15MHz x kΩ / R_{FREQ}). R_{FREQ} is still required if an external clock is used at SYNC/EN, and the SYNC/EN input frequency should be within ±30% of the frequency set by R_{FREQ}.
REF	13	13	1.25V Reference Output. Connect a 0.1µF or larger ceramic capacitor (C9) from REF to GND.
GND	14	14	Analog/Signal Ground
FB2	15	15	OUT2 Feedback Input. Connect a resistive-divider (R5, R6) from OUT2 to FB2 to GND to regulate FB2 to 0.8V.
DRV2	16	16	OUT2 Gate Drive. DRV2 connects to the gate of an external N-channel MOSFET to form a positive linear voltage regulator.
SUP2	17	17	Supply Input for DRV2. Connect to a voltage source of at least 1V above the maximum desired DRV2 gate voltage.

Pin Description (continued)

PIN NAME	MAX8513	MAX8514	FUNCTION
SEQ	18	18	Connect to VL for output tracking. Connect to GND for output staggered sequence. Staggered sequence ramps up V_{OUT2} and V_{OUT3} softly to avoid glitches on the previous voltage due to charging of the LDO's output capacitors.
SYNC/EN	19	19	Shutdown Control and Synchronization Input. There are three operating modes: • When SYNC/EN is low, the controller is off but the VL regulator is still running. • When SYNC/EN is high, the controller is enabled with the switching frequency set by R_{FREQ}. • When SYNC/EN is driven by an external clock, the controller is enabled and switches at the external clock frequency.
N.C.	20	—	No Connection. Not internally connected. Connect to GND or leave floating.
SUP3N	—	20	OUT3N Base-Drive Supply. Connect SUP3N to any positive voltage between 1.5V and 5.5V to provide power for the negative linear-regulator transistor driver.
DRV3P	21	—	OUT3P Base Drive. Connect DRV3P to the base of an external PNP pass transistor to form a positive linear voltage regulator.
DRV3N	—	21	OUT3N Base Drive. Connect DRV3N to the base of an external NPN pass transistor to form a negative linear voltage regulator.
IN	22	22	Main Voltage Input (4.5V to 28V). Bypass IN to GND, close to the IC, with a minimum 1µF ceramic capacitor (C2). IN powers the linear regulator whose output is VL.
$\overline{\text{POR}}$	23	23	Power-On Reset. Open-drain output that goes high after all outputs reach the regulation limit and a 315ms delay time has elapsed.
FB3P	24	—	OUT3P Feedback Input. FB3P is referenced to 0.8V and connects to a resistive-divider (R13, R14) to control a positive linear voltage regulator.
FB3N	—	24	OUT3N Feedback Input. Connect a resistive-divider (R13, R14) from OUT1 to FB3N to OUT3N to regulate FB3N to 0V.
ILIM	25	25	ILIM Set Input. Connect a resistive-divider (R17, R18) from OUT1 to ILIM to GND. See the *Current Limit* section.
CSP	26	26	Positive Current-Sense Input. Used to detect OUT1 current limit.
CSN	27	27	Negative Current-Sense Input. Used to detect OUT1 current limit.
SS	28	28	Analog Soft-Start Control Input. This pin goes into the positive input of the VOUT1's error amplifier. When the MAX8513/MAX8514 are turned on, SS is at GND and charges up to 1.25V with a constant 25µA. Connect a capacitor (C13) from SS to GND for the desired soft-start time.

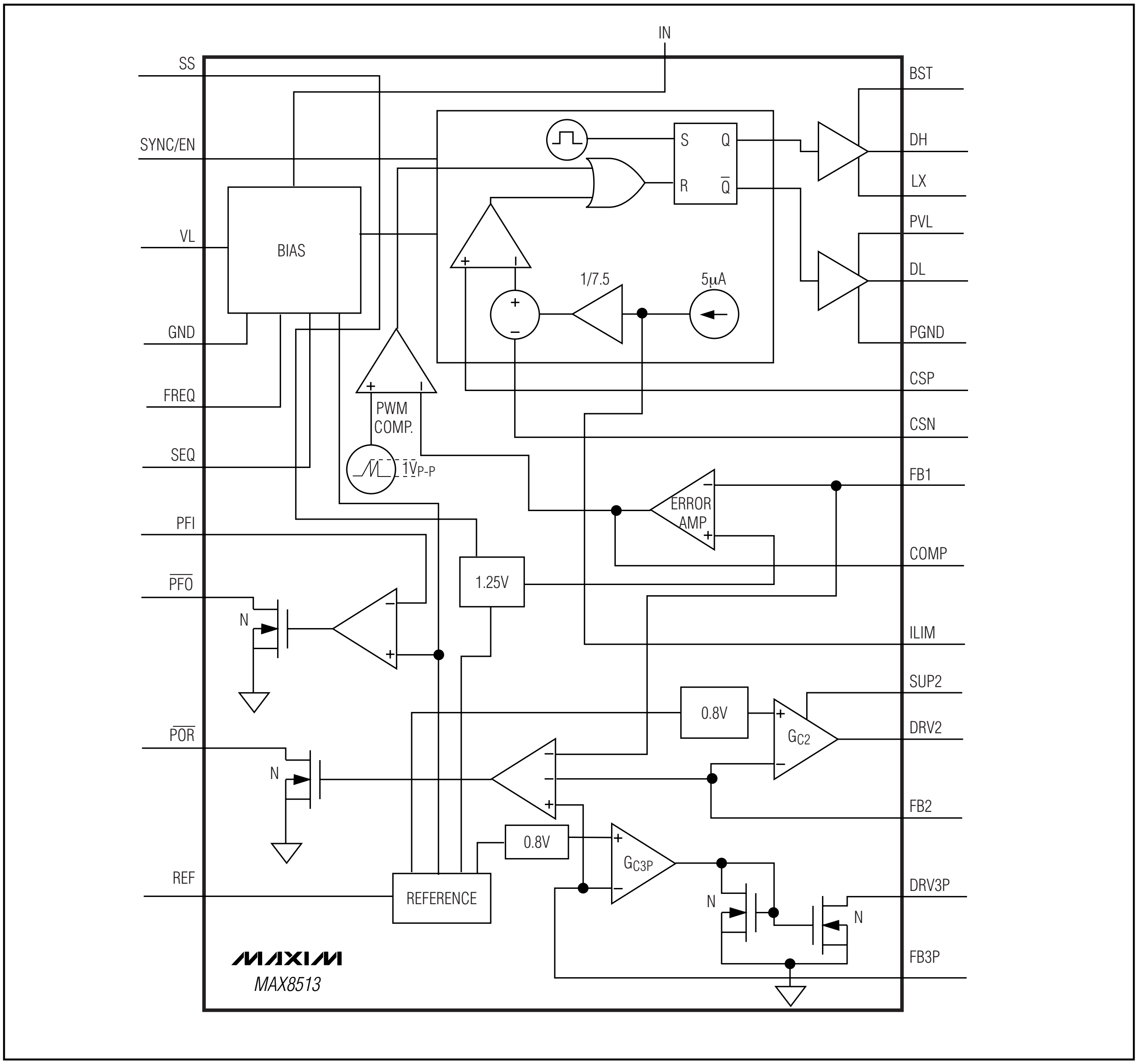


Figure 1. MAX8513 Functional Diagram

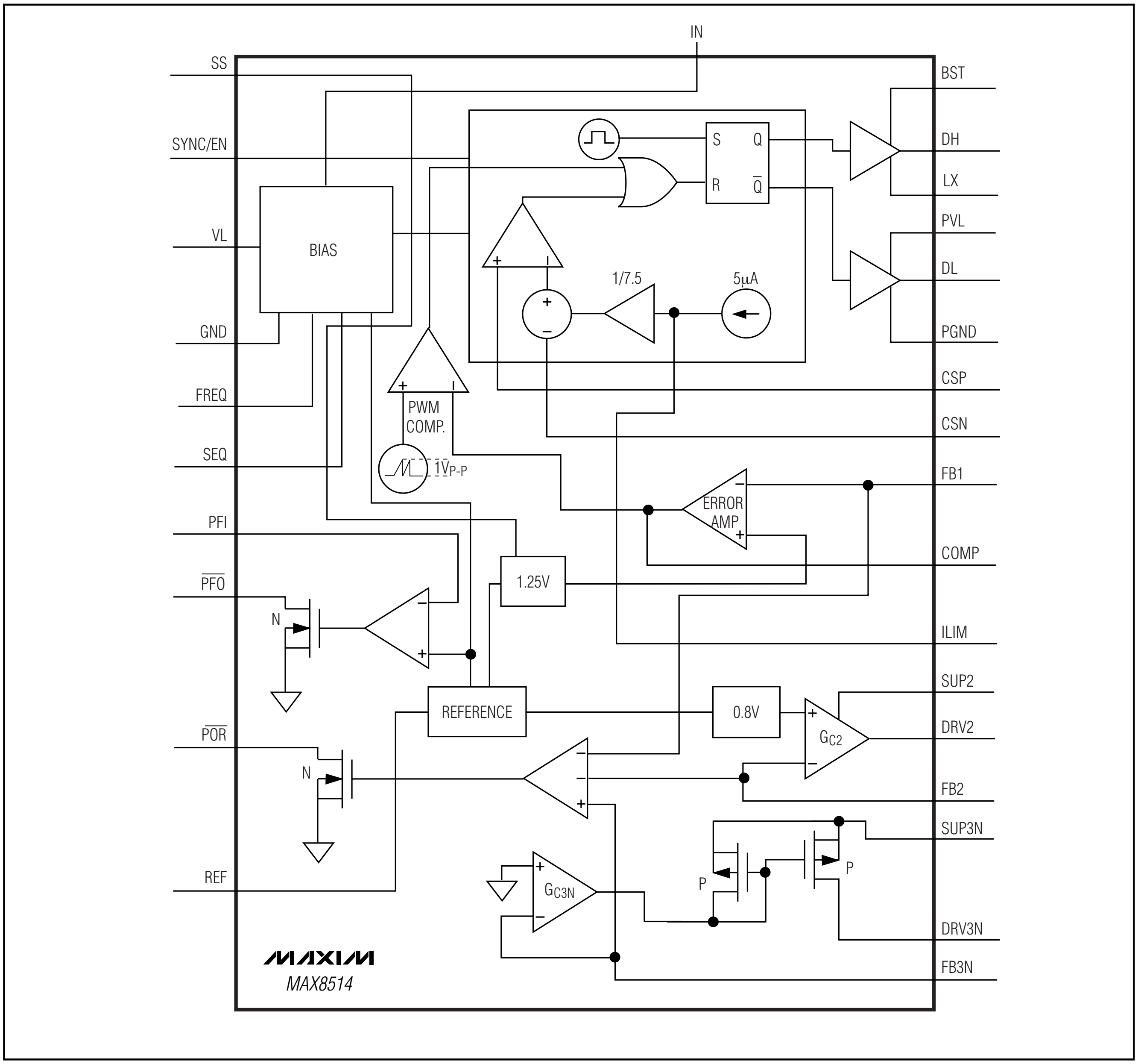


Figure 2. MAX8514 Functional Diagram

Detailed Description

The MAX8513/MAX8514 combine a step-down DC-DC converter and two LDOs, providing three output voltages for xDSL modem and set-top box applications. The switching frequency is set with an external resistor connected from the FREQ pin to GND, and is adjustable from 300kHz to 1.4MHz. The main step-down DC-DC controller operates in a voltage-mode, pulse-width-modulation (PWM) control scheme. The MAX8513/MAX8514 include two low-cost LDO controllers capable of delivering current from the DC-DC main output, an extra winding, the input, or from an alternate supply voltage. The first LDO controller drives an external NMOS or NPN with a maximum drive of 7.75V. The second LDO controller provides either a positive 0.8V to 27V output using an external PNP pass device, or a negative -1V to -18V output with an external NPN pass device.

DC-DC Controller

The MAX8513/MAX8514 step-down DC-DC converters use a PWM voltage-mode control scheme. An internal high-bandwidth (25MHz) operational amplifier is used as an error amplifier to regulate the output voltage. The output voltage is sensed and compared with an internal 1.25V reference to generate an error signal. The error signal is then compared with a fixed-frequency ramp by a PWM comparator to give the appropriate duty cycle to maintain output-voltage regulation. At the rising edge of the internal clock and when DL (the low-side MOSFET gate drive) is at 0V, the high-side MOSFET turns on. When the ramp voltage reaches the error-amplifier output voltage, the high-side MOSFET latches off until the next clock pulse. During the high-side MOSFET on-time, current flows from the input through the inductor to the output capacitor and load. At the moment the high-side MOSFET turns off, the energy stored in the inductor during the on-time is released to support the load. The inductor current ramps down through the low-side MOSFET body diode. After a fixed delay, the low-side MOSFET turns on to shunt the current from its body diode for a lower voltage drop to increase the efficiency. The low-side MOSFET turns off at the rising edge of the next clock pulse, and when its gate voltage discharges to zero, the high-side MOSFET turns on after an additional fixed delay and another cycle starts.

The MAX8513/MAX8514 operate in forced-PWM mode, so even under light load the controller maintains a constant switching frequency to minimize noise and possible interference with system circuitry.

Current Limit

The MAX8513/MAX8514s' switching regulator senses the inductor current either through the DC resistance of the inductor itself for lossless sensing, or through a series resistor for more accurate sensing. When using the DC resistance of the inductor, an RC filter circuit is needed (see R19, R20, and C14 of the *Typical Applications Circuits* and the *Current-Limit Setting* section). When peak voltage across the sensing circuit (which occurs at the peak of the inductor current) exceeds the current-limit threshold set by ILIM, the controller turns off the high-side MOSFET and turns on the low-side MOSFET. The inductor current ramps down and DH turns on again if the inductor current is below the current-limit threshold at the next clock pulse. The MAX8513/MAX8514 current-limit threshold can be set by two external resistors to be proportional to the output voltage with an adjustable offset level, providing foldback current-limit and short-circuit protection. This feature greatly reduces power dissipation and prevents overheating of external components during an indefinite short-circuit at the output. See the *Foldback Current Limit* section for how to set ILIM with external resistors. The current-limit threshold defaults to 170mV when ILIM is connected to VL, and in this case, the current limit functions as a constant current limit only. The LDO controllers do not have current limit and rely on input current limit for protection.

Synchronous-Rectifier Driver (DL)

Synchronous rectification reduces the conduction loss in the rectifier by replacing the normal Schottky catch diode with a low-on-resistance MOSFET switch. The MAX8513/MAX8514 also use the synchronous rectifier to ensure proper startup of the boost gate-drive circuit.

High-Side Gate-Drive Supply (BST)

A flying-capacitor boost circuit (see D1 and C3 in the *Typical Applications Circuits*) generates the gate-drive voltage for the high-side N-channel MOSFET. On startup, the synchronous rectifier (low-side MOSFET, Q2) forces LX to ground and charges the boost capacitor (C3) to V_{VL} - V_{DIODE}. On the second half-cycle, the controller turns on the high-side MOSFET by closing an internal switch between BST and DH. This boosts the voltage at BST to V_{VL} - V_{DIODE} + V_{IN}, providing the necessary gate-to-source voltage to turn on the high-side N-channel MOSFET.

Internal 5V Linear Regulator

All MAX8513/MAX8514 functions (except for the positive output LDO with an NFET or NPN, and the negative LDO on the MAX8514) are powered from the on-chip low-dropout 5V regulator with its input connected to IN. Bypass the regulator's output (VL) with a 2.2µF or greater ceramic capacitor. The V_{IN} to V_{VL} dropout voltage is typically 350mV, so when V_{IN} is greater than 5.5V, V_{VL} is typically 5V. If V_{IN} is between 4.5V and 5.5V, short VL to IN.

Undervoltage Lockout

If V_{VL} drops below 3.8V, the MAX8513/MAX8514 assume that the supply voltage is too low to make valid decisions. When this happens, the undervoltage lockout (UVLO) circuitry inhibits switching, forces $\overline{POR}$ and $\overline{PFO}$ low, and forces DL and DH gate drivers low. After V_{VL} rises above 3.9V, the controller powers up the outputs (see the *Startup* section).

Startup

The MAX8513/MAX8514 start switching when V_{VL} rises above the 3.9V UVLO threshold. However, the controller is not enabled unless all three of the following conditions are met:

1) V_{VL} exceeds the 3.9V UVLO threshold.
2) The internal reference exceeds 90% of its nominal value.
3) The thermal limit is not exceeded.

Once the MAX8513/MAX8514 assert the internal enable signal, the step-down controller starts switching and enables soft-start. The soft-start circuitry gradually ramps up to the reference voltage to control the rate-of-rise of the step-down controller and reduce input surge currents. The soft-start period is determined by the value of the capacitor from SS to GND (C13 in the *Typical Applications Circuits*). SS sources a constant 25µA to charge the soft-start capacitor to 1.25V.

Output-Voltage Sequencing

The MAX8513/MAX8514 can power up in either staggered-output sequencing or output tracking. For staggered-output sequencing, connect SEQ to GND. In this configuration, V_{OUT1} comes up first. When it reaches 90% of the nominal regulated value, V_{OUT2} is softly turned on. Once V_{OUT2} reaches 90% of its nominal regulated value, V_{OUT3} is softly turned on. Individual soft-start on OUT2 and OUT3 eliminates glitches on the previous stages due to the charging of output capacitors. See the *Typical Operating Characteristics* section for the startup and staggered-output-sequence waveforms.

Output-Voltage Tracking

When SEQ is connected to VL, all outputs rise up at the same time and the external series pass transistors are driven fully on until reaching the respective regulation limits. Since the LDOs are powered from the main DC-DC step-down converter, either directly or through a coupled winding on the inductor, their outputs track the DC-DC step-down output (OUT1). See the *Typical Operating Characteristics* section for the startup output-tracking waveforms.

Power-On Reset

The MAX8513/MAX8514 provide a power-on-reset ($\overline{POR}$) signal, which goes high 315ms after all outputs reach 90% of their nominal regulated value. Therefore, by the time $\overline{POR}$ goes high, all outputs are already stabilized at nominal regulated voltages. See the *Typical Operating Characteristics* section for the $\overline{POR}$ waveforms.

Input Power-Fail (PFI and PFO)

The MAX8513/MAX8514 have a built-in comparator to detect the input voltage with an external resistive-divider at PFI, with a threshold of 1.22V. When the input voltage drops and trips this comparator, the power-fail output ($\overline{PFO}$) goes low, while all outputs are still within regulation limits. This is typically used for input power-fail warning for orderly system shutdown. The amount of warning time depends on the input storage capacitor, the input PFI trip voltage level, the main step-down output voltage, the total output power, and the efficiency. See the *Design Procedure* section for how to calculate the input capacitor to meet the required warning time.

Enable and Synchronization

The MAX8513/MAX8514 can be turned on with logic high, and off with logic low at SYNC/EN. When SYNC/EN is driven with an external clock, the internal oscillator synchronizes the rising edge of the clock at SYNC/EN to DH going high. When being driven by a synchronization clock signal at SYNC/EN, the controller synchronizes to the external clock within two cycles. The frequency at SYNC/EN needs to be within ±30% of the value set by R_{FREQ}. See the *Switching-Frequency Setting* section.

Thermal-Overload Protection

Thermal-overload protection limits the total power dissipation in the MAX8513/MAX8514. When the junction temperature exceeds T_J = +170°C, a thermal sensor shuts down the device, forcing DL and DH low and allowing the IC to cool. The thermal sensor turns the part on again after the junction temperature cools by 25°C, resulting in a pulsed output during continuous thermal-overload conditions. During a thermal event, the main step-down converter and the linear regulators are turned off, $\overline{\text{POR}}$ and $\overline{\text{PFO}}$ go low, and soft-start is reset.

Design Procedure

OUT1 Voltage Setting

The output voltage is set by a resistive-divider network from OUT1 to FB1 to GND (see R1 and R2 in the *Typical Applications Circuits*). Select R2 between 5kΩ and 15kΩ. Then R1 can be calculated by:

$$R1 = R2 \times \left(\frac{V_{OUT1}}{1.25V} - 1\right)$$

Input Power-Fail Setting

The PFI input can monitor V_{IN} to determine if it is falling. When the voltage at PFI crosses 1.22V, the output ($\overline{\text{PFO}}$) goes low. The input voltage value at the PFI trip threshold, V_{PFI}, is set by a resistive-divider network from IN to PFI to GND (see the *Typical Applications Circuits*). Select R11, the resistor from PFI to GND between 10kΩ and 40kΩ. Then R10, the resistor from PFI to IN, is calculated by:

$$R10 = R11 \times \left(\frac{V_{PFI}}{1.22V} - 1\right)$$

Switching-Frequency Setting

The resistor connected from FREQ to GND, R_{FREQ} (R7 in the *Typical Applications Circuits*), sets the switching frequency, f_S, as shown by the equation below:

$$f_S = \frac{15 \times 10^9}{R_{FREQ}} \text{ Hz} \times \Omega$$

where R_{FREQ} is in ohms.

Inductor Value

There are several parameters that must be examined when determining which inductor to use: input voltage, output voltage, load current, switching frequency, and LIR. LIR is the ratio of peak-to-peak inductor ripple current to the maximum DC load current. A higher LIR value allows for a smaller inductor but results in higher losses and higher output ripple. A good compromise between size and efficiency is a 30% LIR. Once all of the parameters are chosen, the inductor value is determined as follows:

$$L = \frac{V_{OUT1} \times (V_{IN} - V_{OUT1})}{V_{IN} \times f_S \times I_{OUT1\_MAX} \times LIR}$$

where V_{OUT1} is the main switching regulator output and f_S is the switching frequency.

Choose a standard value close to the calculated value. The exact inductor value is not critical and can be adjusted to make tradeoffs between size, cost, and efficiency. Lower inductor values minimize size and cost, but also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but eventually resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. Find a low-loss inductor with the lowest possible DC resistance that fits the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well up to 300kHz. The chosen inductor's saturation current rating must exceed the peak inductor current as calculated below:

$$I_{PEAK} = I_{OUT1\_MAX} + \frac{(V_{IN} - V_{OUT1}) \times V_{OUT1}}{2 \times L \times f_S \times V_{IN}}$$

This peak value should be smaller than the value set at ILIM when V_{OUT1} is at its nominal regulated voltage (see the *Current Limit* and *Current-Limit Setting* sections).

In applications where a multiple winding inductor (coupled inductor) is used to generate the supply voltages for the LDOs, the inductance value calculated above is for the winding connected to the DC-DC step-down (primary windings) inductance. The inductance seen from the other windings (secondary windings) is proportional to the square of the turns ratio with respect to the primary winding.

The turns ratio is important since it sets the LDOs' supply voltage values. The voltage generated by the secondary winding (V_{SEC}) together with the rectifier diode and output capacitor is calculated as follows:

$$V_{SEC} = (V_{OUT1} + V_{Q2}) \times \left(\frac{n_2}{n_1}\right) - V_{D2}$$

where V_{Q2} and V_{D2} are the voltage drops across the low-side MOSFET on the primary side and the rectifier diode on the secondary side (Q2 and D2 in the *Typical Applications Circuits*). n_2 and n_1 are the number of turns of the secondary winding and the primary winding, respectively.

It is important to have the secondary winding tightly coupled with the primary winding to minimize leakage inductance for higher efficiency. The positive voltage generated by the secondary winding can also be stacked with the main DC-DC step-down converter output to further improve efficiency and reduce winding cost. In this case, the secondary-side voltage is:

$$V_{SEC} = \left(V_{OUT1} + V_{Q2}\right) \times \left(\frac{n_2}{n_1}\right) + V_{OUT1} - V_{D2}$$

Input Capacitor

The input-filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the AC-RMS current through the ESR of the input capacitor (C2 in the *Typical Applications Circuits*). The input capacitor must meet the ripple-current requirement (I_{IN_RMS}) imposed by the switching currents defined by the following equation:

$$I_{IN\_RMS} = \frac{I_{OUT1} \times \sqrt{V_{OUT1} \times \left(V_{IN} - V_{OUT1}\right)}}{V_{IN}}$$

I_{IN_RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT1}$), so $I_{IN\_RMS(MAX)} = I_{OUT1} / 2$. Ceramic capacitors are recommended due to their low ESR and ESL at high frequency, with relatively low cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

For applications that require input power-fail warning, such as dying gasp, add a large-value electrolytic capacitor (C_S) to the input as a local energy storage device to provide the power to the converter in case of input power-fail. The capacitor value must be high enough to meet the desired power-fail warning time, t_{WARN}, where t_{WARN} is the time from when PFI trips the $\overline{PFO}$ output to when the main output (OUT1) starts dropping out of regulation. The value of the storage capacitor, C_S, can be calculated as:

$$C_S = \left(0.5 \times \frac{P_{OUT1}}{\eta}\right) \times \left(\frac{1}{V_{PFI}} - \frac{1}{V_{DROOP}}\right) \times \frac{t_{WARN}}{\left(V_{PFI} - V_{DROOP}\right)}$$

where P_{OUT1} is the total output power, η is the total converter efficiency, V_{PFI} is the input voltage value at the input power-fail (PFI) trip threshold, and V_{DROOP} is the input voltage value where V_{OUT1} starts dropping out of regulation.

V_{PFI} and V_{DROOP} can be calculated as:

$$V_{PFI} = 1.22V \times \left(1 + \frac{R10}{R11}\right)$$

where R10 and R11 are the resistive-dividers from IN to PFI to GND in the *Typical Applications Circuits*.

$$V_{DROOP} = \frac{V_{OUT1}}{D_{MAX}}$$

where D_{MAX} is the maximum duty cycle.

To ensure for worst-case component tolerances such as capacitance of C_S, converter efficiency, V_{PFI}, and V_{DROOP}'s threshold over the operating temperature range, it is recommended to select C_S at least 1.5 times the calculated value above.

Output Capacitor

The key selection parameters for the output capacitor are the actual capacitance value, the equivalent series resistance (ESR), the equivalent series inductance (ESL), and the voltage-rating requirements. All of these affect the overall stability, output ripple voltage, and transient response.

The output ripple is composed of three components: variations in the charge stored in the output capacitor, the voltage drop across the capacitor's equivalent series resistance (ESR), and equivalent series inductance (ESL) caused by the current into and out of the capacitor.

The peak-to-peak output voltage ripple as a consequence of the ESR, ESL, and output capacitance is:

$$V_{RIPPLE(ESR)} = I_{P\text{-}P} \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{I_{P\text{-}P}}{8 \times C_{OUT} \times f_S}$$

where C_{OUT} is C4 in the *Typical Applications Circuits*.

$$V_{RIPPLE(ESL)} = \frac{V_{IN} \times ESL}{L1A + ESL}$$

$$\text{and } I_{P\text{-}P} = \left(\frac{V_{IN} - V_{OUT1}}{f_S L}\right)\left(\frac{V_{OUT1}}{V_{IN}}\right)$$

where $I_{P\text{-}P}$ is the peak-to-peak inductor current (see the *Inductor Selection* section). An approximation of the overall voltage ripple at the output is:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

While these equations are suitable for initial capacitor selection to meet the ripple requirement, final values may also depend on the relationship between the LC double-pole frequency and the capacitor ESR zero. Generally, the ESR zero is higher than the LC double pole (see the *Compensation Design* section). Solid polymer electrolytic or ceramic capacitors are recommended due to their low ESR and ESL at higher frequencies. Higher output current may require paralleling multiple capacitors to meet the output voltage ripple.

The MAX8513/MAX8514s' response to a load transient depends on the selected output capacitor. After a load transient, the output instantly changes by (ESR × ΔI_{OUT1}) + (ESL × dI_{OUT1} / dt). Before the controller can respond, the output deviates further depending on the inductor and output capacitor values. After a short period of time (see the *Typical Operating Characteristics*), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. With a higher bandwidth the response time is faster, preventing the output capacitor from further deviation from its regulating value. Be sure not to exceed the capacitor's voltage or current ratings.

MOSFET Selection

The MAX8513/MAX8514 drive two external, logic-level, N-channel MOSFETs as the circuit switch elements. The key selection parameters are:

- For on-resistance (R_{DS_ON}), the lower the better.
- Maximum drain-to-source voltage (V_{DS}) should be at least 20% higher than the input supply rail at the high-side MOSFET's drain.
- For gate charges (Q_{GS}, Q_{GD}, Q_{DS}), the lower the better.

Choose the MOSFETs with rated R_{DS_ON} at V_{GS} = 4.5V. For a good compromise between efficiency and cost, choose the high-side MOSFET (Q1 in the *Typical Applications Circuits*) that has conduction loss equal to switching loss at nominal input voltage and maximum output current. For the low-side MOSFET (Q2 in the *Typical Applications Circuits*), make sure that it does not spuriously turn on due to dV/dt caused by Q1 turning on as this results in shoot-through current degrading the efficiency. MOSFETs with a lower Q_{GD} / Q_{GS} ratio have higher immunity to dV/dt.

For proper thermal management, the power dissipation must be calculated at the desired maximum operating junction temperature, maximum output current, and worst-case input voltage. For Q2, the worst case is at V_{IN_MAX}. For Q1, it could be either at V_{IN_MIN} or V_{IN_MAX}. Q1 and Q2 have different loss components due to the circuit operation. Q2 operates as a zero voltage switch, where major losses are the channel conduction loss (P_{Q2CC}) and the body-diode conduction loss (P_{Q2DC}).

$$P_{Q2CC} = \left(1 - \frac{V_{OUT1}}{V_{IN}}\right) \times I_{OUT1}^2 \times R_{DS\_ON}$$

$$P_{Q2DC} = 2 \times I_{OUT1} \times V_F \times t_{dt} \times f_S$$

where V_F is the body-diode forward voltage drop, t_{dt} = 50ns is the dead time between Q1 and Q2 switching transitions, and f_S is the switching frequency.

The total losses for Q2 are:

$$P_{Q2\_TOTAL} = P_{Q2CC} + P_{Q2DC}$$

Q1 operates as a duty-cycle control switch and has the following major losses: the channel conduction loss (P_{Q1CC}), the V I overlapping switching loss (P_{Q1SW}), and the drive loss (P_{Q1DR}). Q1 does not have body-diode conduction loss because the diode never conducts current.

$$P_{Q1CC} = \frac{V_{OUT1}}{V_{IN}} \times I_{OUT1}^2 \times R_{DS\_ON}$$

where R_{DS_ON} is at the maximum operating junction temperature.

$$P_{Q1SW} = V_{IN} \times I_{OUT1} \times f_S \times \frac{(Q_{GS} + Q_{GD})}{I_{GATE}}$$

where I_{GATE} is the average DH high driver output-current capability determined by:

$$I_{GATE} = \frac{2.5V}{(R_{DH} + R_{GATE})}$$

where R_{DH} is the high-side MOSFET driver's on-resistance (1.5Ω typ) and R_{GATE} is the internal gate resistance of the MOSFET (≈2Ω).

$$P_{Q1DR} = Q_{GS} \times V_{GS} \times f_S \times \frac{R_{GATE}}{(R_{GATE} + R_{DH})}$$

where $V_{GS} \approx V_{VL} = 5V$.

The total power loss in Q1 is:

$$P_{Q1} = P_{Q1CC} + P_{Q1SW} + P_{Q1DR}$$

In addition to the losses above, allow approximately 20% more for additional losses due to MOSFET output capacitances and Q2 body-diode reverse recovery charge dissipated in Q1. This is not typically well-defined in MOSFET data sheets. Refer to the MOSFET data sheet for the thermal-resistance specification to calculate the PC board area needed to maintain the desired maximum operating junction temperature with the above calculated power dissipations.

To reduce EMI caused by switching noise, add a 0.1µF or larger ceramic capacitor from the high-side MOSFET drain to the low-side MOSFET source or add resistors in series with DH and DL to slow down the switching transitions. However, adding series resistors with DH and DL increases the power dissipation in the MOSFET when it switches, so be sure this does not overheat the MOSFET. The minimum load current must exceed the high-side MOSFET's maximum leakage current over temperature if fault conditions are expected.

MOSFET Snubber Circuit

Fast switching transitions cause ringing because of resonating circuit parasitic inductance and capacitance at the switching nodes. This high-frequency ringing occurs at LX's rising and falling transitions and can interfere with circuit performance and generate EMI. To dampen this ringing, a series-RC snubber circuit is added across each switch. The following is the procedure for selecting the value of the series-RC circuit:

1) Connect a scope probe to measure V_{LX} to GND, and observe the ringing frequency, f_R .
2) Find the capacitor value (connected from LX to GND) that reduces the ringing frequency by half.

The circuit parasitic capacitance (C_{PAR}) at LX is then equal to 1/3rd the value of the added capacitance above. The circuit parasitic inductance (L_{PAR}) is calculated by:

$$L_{PAR} = \frac{1}{(2\pi \times f_R)^2 \times C_{PAR}}$$

The resistor for critical dampening (R_{SNUB}) is equal to ($2\pi \times f_R \times L_{PAR}$). Adjust the resistor value up or down to tailor the desired damping and the peak voltage excursion. The capacitor (C_{SNUB}) should be at least 2 to 4 times the value of the C_{PAR} to be effective. The power loss of the snubber circuit is dissipated in the resistor (P_{RSNUB}) and can be calculated as:

$$P_{RSNUB} = C_{SNUB} \times (V_{IN})^2 \times f_S$$

where V_{IN} is the input voltage and f_S is the switching frequency. Choose an R_{SNUB} power rating that meets the specific application's derating rule for the power dissipation calculated.

Current-Limit Setting

The MAX8513/MAX8514 can provide foldback current limit or constant current limit. Unless constant current-limit operation is required, such as when driving a constant current load, foldback current limit should be implemented. Foldback current limit reduces the power dissipation of external components under overload or short-circuit conditions.

Foldback Current Limit

For foldback current limit, the current-limit threshold is set by an external resistive-divider from V_{OUT1} to ILIM to GND (R17 and R18 of the *Typical Applications Circuits*). This makes the voltage at ILIM a function of the internal 5µA current source and V_{OUT1}. The current-limit comparator threshold is equal to V_{ILIM} / 7.5. This threshold is compared with V_{SENSE}. V_{SENSE} is either the voltage across the current-sense resistor or, for lossless sensing, the voltage across the inductor. When V_{SENSE} exceeds the current-limit threshold, the high-side MOSFET turns off and the low-side MOSFET turns on. This allows for a current foldback feature that reduces the current-limit threshold during a short circuit. This makes the current threshold limit, when V_{OUT} = 0V, a percentage of the current-limit threshold, when V_{OUT1} is at its nominal regulated value.

Wide-Input, High-Frequency, Triple-Output Supplies with Voltage Monitor and Power-On Reset

To set the current limit and the current-limit foldback thresholds, first select the foldback current-limit ratio (P_{FB}). This ratio is the foldback current limit ($I_{LIMIT@0V}$) divided by the current limit when V_{OUT1} equals its nominal regulated voltage (I_{LIMIT}).

$$P_{FB} = \frac{I_{LIMIT@0V}}{I_{LIMIT}}$$

P_{FB} is typically set to 0.5. To calculate the values of R17 and R18 (in the *Typical Applications Circuits*), use the following equations:

$$R17 = \frac{(P_{FB} \times V_{OUT1})}{4.7\mu A \times (1 - P_{FB})}$$

$$R18 = \frac{(7.5 \times R_{CS\_MAX} \times I_{LIMIT} \times (1 - P_{FB})) \times R17}{V_{OUT1} - (7.5 \times R_{CS\_MAX} \times I_{LIMIT} \times (1 - P_{FB}))}$$

R_{CS_MAX} is the maximum sensing resistance at the high operating temperature. R_{CS} can either be the series resistance of the inductor or a discrete current-sense resistor value. I_{LIMIT} is the peak inductor current at maximum load, which equals:

$$I_{OUT1\_MAX} \times \left(\frac{1 + LIR}{2}\right)$$

If R18 results in a negative resistance, then decrease R_{CS}. This can be done by choosing an inductor with a lower DC resistance or a lower value discrete current-sense resistor.

Constant Current Limit

For constant current-limit operation, connect ILIM to VL for a default current-limit threshold of 170mV (typ). The sensing resistor value must then be chosen so that:

$$R_{CS\_MAX} \times I_{LIMIT} < 151mV$$

the minimum value of the default threshold.

Alternately, the constant current-limit threshold can also be set by using only R18, in which case R18 is calculated as follows:

$$R18 = 7.5 \times R_{CS\_MAX} \times \frac{I_{LIMIT}}{4.7\mu A}$$

When using the DC resistance of the inductor as a current-sense resistor, an RC filter is needed (R19 and C14 of the *Typical Applications Circuits*). Pick the value of the filter capacitor, C14, from 0.22µF to 1µF (ceramic X7R). Then calculate the value of R19 as follows:

$$R19 = \frac{L1A}{(2 \times R_{L\_DC} \times C14)}$$

R_{L_DC} is the nominal value of the inductor's DC resistance. Additionally, R20 (in the *Typical Applications Circuits*) is added in series with the CSN input to cancel the drop due to input bias current into CSP that develops across R19. R20 should be set equal to R19.

Compensation Design

The MAX8513/MAX8514 use a voltage-mode control scheme that regulates the output voltage by comparing the error-amplifier output (COMP) with a fixed internal ramp to produce the required duty cycle. The output lowpass LC filter creates a double pole at the resonant frequency, which has a gain drop of -40dB/decade and a phase shift of approximately -180°/decade. The error amplifier must compensate for this gain drop and phase shift to achieve a stable high-bandwidth closed-loop system.

The basic regulator loop consists of a power modulator, an output feedback divider, and an error amplifier. The power modulator has a DC gain set by V_{IN} / V_{RAMP} (V_{RAMP} = $1V_{P-P}$), with a double pole and a single zero set by the output inductance (L), the output capacitance (C_{OUT}) (C4 in the *Typical Applications Circuits*), and its equivalent series resistance (R_{ESR}). V_{RAMP} is the peak of the saw-toothed waveform at the input of the PWM comparator (see the *Functional Diagrams* in Figures 1 and 2). Below are equations that define the power modulator:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}}$$

$$f_{PMOD} = \frac{1}{2\pi\sqrt{L \times C_{OUT}}}$$

where L is L1A and C_{OUT} is C4 in the *Typical Applications Circuits*.

$$f_{ZESR} = \frac{1}{2\pi \times C_{OUT} \times R_{ESR}}$$

When the output capacitance is comprised of paralleling n number of identical capacitors whose values are C_{EACH} with ESR of R_{ESR_EACH}, then:

$$C_{OUT} = n \times C_{EACH} \text{ and}$$

$$R_{ESR} = \frac{R_{ESR\_EACH}}{n}$$

Thus the resulting f_{ZESR} is the same as that of each capacitor.

The crossover frequency (f_C), which is the frequency when the closed-loop gain is equal to unity, should be the smaller of 1/5th the switching frequency or 100kHz (see the *Switching-Frequency Setting* section):

$$f_C \le \frac{f_S}{5} \text{ or } 100\text{kHz}$$

The loop-gain equation at the crossover frequency is:

$$G_{EA(fc)} G_{MOD(fc)} = 1$$

where $G_{EA(fc)}$ is the error-amplifier gain at f_C, and $G_{MOD(fc)}$ is the power modular gain at f_C.

The loop compensation is affected by the choice of output-filter capacitor used, due to the position of its ESR zero frequency with respect to the desired closed-loop crossover frequency. Ceramic capacitors are used for higher switching frequencies (above 750kHz) because of low capacitance and low ESR; therefore, the ESR zero frequency is higher than the closed-loop crossover frequency. While electrolytic capacitors (e.g., tantalum, solid polymer, oscon, etc.) are needed for lower switching frequencies, because of high capacitance and ESR, the ESR zero frequency is typically lower than the closed-loop crossover frequency. Thus the compensation design procedure is separated into two cases:

Case 1: Ceramic Output Capacitor *(operating at high switching frequencies, $f_{ZESR} > f_C$)*

The modulator gain at f_C is:

$$G_{MOD(fc)} = G_{MOD(DC)} \left(\frac{f_{PMOD}}{f_C}\right)^2$$

Since the crossover frequency is lower than the output capacitors' ESR zero frequency and higher than the LC double-pole frequency, the error-amplifier gain must have a +20dB/decade slope at f_C. This +20dB/decade slope of the error amplifier at crossover then adds to the -40dB/decade slope of the LC double pole, and the resultant compensated loop crosses over at the desired -20dB/decade slope. The error amplifier has a dominant pole at very low frequency (≈0Hz), and two separate zeros at:

$$f_{Z1} = \frac{1}{2\pi \times R3 \times C5} \text{ and } f_{Z2} = \frac{1}{2\pi \times (R1 + R4) \times C11}$$

and poles at:

$$f_{P2} = \frac{1}{2\pi \times R4 \times C11} \text{ and } f_{P3} = \frac{1}{2\pi \times R3 \times \left(\frac{C5 \times C12}{C5 + C12}\right)}$$

The error-amplifier equivalent circuit and its gain vs. frequency plot are shown below in Figure 3.

In this case, f_{Z2} and f_{P1} are selected to have the converters' closed-loop crossover frequency, f_C, occur when the error-amplifier gain has a +20dB/decade slope between f_{Z2} and f_{P2}. The error-amplifier gain at f_C is:

$$G_{EA(fc)} = \frac{1}{G_{MOD(fc)}}$$

The gain of the error amplifier between f_{Z1} and f_{Z2} is:

$$G_{EA(fZ1\text{-}fZ2)} = G_{EA(fc)} \frac{f_{Z2}}{f_C} = \frac{f_{Z2}}{f_C G_{MOD(fc)}}$$

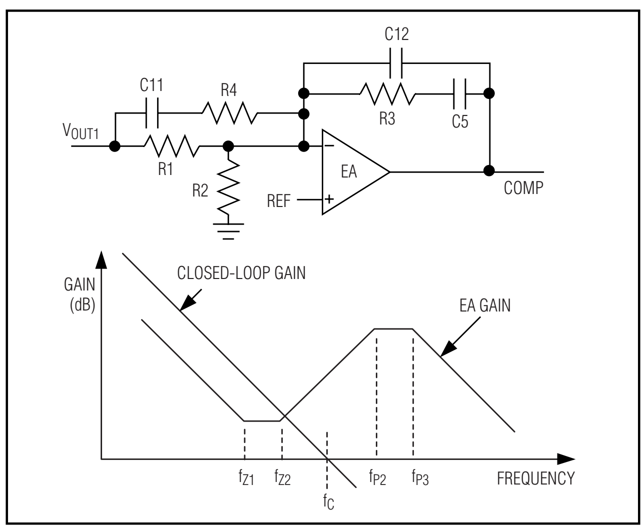


Figure 3. Case 1: Error-Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot)

This gain is also set by the ratio of R3/R1 where R1 is calculated in the *OUT1 Voltage Setting* section. Thus:

$$R3 = \frac{R1 \times f_{Z2}}{f_C \times G_{MOD(fc)}}$$

Due to the underdamped (Q > 1) nature of the output LC double pole, the error-amplifier zero frequencies must be set less than the LC double-pole frequency to provide adequate phase boost. Set the error-amplifier first zero, f_{Z1}, at 1/4th the LC double-pole frequency and the second zero, f_{Z2}, at the LC double-pole frequency. Hence:

$$C5 = \frac{2}{\pi \times R3 \times f_{PMOD}}$$

Set the error-amplifier f_{P2} at f_{ZESR}, and f_{P3} to 1/2 the switching frequency, if $f_{ZESR} < 1/2\ f_S$. If $f_{ZESR} > 1/2\ f_S$, then set f_{P2} at 1/2 f_S and f_{P3} at f_{ZESR}.

The gain of the error amplifier between f_{P2} and f_{P3} is set by the ratio of $R3/R_I$ and is equal to:

$$\frac{R3}{R_I} = G_{EA(fZ1\text{-}fZ2)} \frac{f_{P2}}{f_{PMOD}}$$

where R_I is the parallel combination of R1 and R4 and is equal to:

$$R_I = \frac{R1 \times R4}{R1 + R4}$$

Therefore:

$$R_I = \frac{R3 \times f_{PMOD}}{f_{P2} \times G_{EA(fZ1\text{-}fZ2)}} \text{ and}$$

$$R4 = \frac{R1 \times R_I}{R1 - R_I}$$

C11 can then be calculated as:

$$C11 = \frac{1}{2\pi \times R4 \times f_{P2}}$$

and C12 as:

$$C12 = \frac{C5}{\left(2\pi \times C5 \times R3 \times f_{P3} - 1\right)}$$

Below is a numerical example to calculate the error-amplifier compensation values used in the *Typical Applications Circuit* of Figure 5:

V_{IN} = 12V (nomimal input voltage)

V_{RAMP} = 1V

V_{OUT1} = 3.3V

V_{FB1} = 1.25V

L1A = 1.8µH

C4 = 47µF/ 6.3V ceramic, with R_{ESR} = 0.008Ω

f_S = 1.4MHz

The LC double-pole frequency is calculated as:

$$f_{PMOD} = \frac{1}{2\pi\sqrt{L1A \times C4}} = \frac{1}{2\pi\sqrt{1.8 \times 10^{-6} \times 47 \times 10^{-6}}} = 17.3\text{kHz}$$

$$f_{ZESR} = \frac{1}{2\pi \times R_{ESR} \times C4} = \frac{1}{2\pi \times 0.008 \times 47 \times 10^{-6}} = 423\text{kHz}$$

Pick R2 = 8.06kΩ.

$$R1 = 8.06\text{k}\Omega \times \left(\frac{3.3V}{1.25V} - 1\right) = 13.3\text{k}\Omega$$

The modulator gain at DC is:

$$G_{MOD(DC)} = \frac{V_{IN}}{V_{RAMP}} = 12$$

Pick f_C = 100kHz.

$$G_{MOD(fc)} = 12 \times \left(\frac{17.4\text{kHz}}{100\text{kHz}}\right)^2 = 0.363$$

$$G_{EA(fZ1–fZ2)} = \frac{f_{PMOD}}{f_C G_{MOD(fC)}} = \frac{17.4\text{kHz}}{100\text{kHz} \times 0.363} = 0.479$$

$$R3 = R1 \times G_{EA(fZ1–fZ2)} = 13.3\text{k}\Omega \times 0.479 = 6.37\text{k}\Omega$$

Use 6.8kΩ.

$$C5 = \frac{2}{\pi \times R3 \times f_{PMOD}} = \frac{2}{\pi \times 6.8k\Omega \times 17.4kHz} = 5.38nF$$

Use 4.7nF.

$$R_I = \frac{R3 \times f_{PMOD}}{f_{P2} \times G_{EA(fZ1\text{-}fZ2)}} = \frac{6.8k\Omega \times 17.4kHz}{423kHz \times 0.479} = 583\Omega$$

$$R4 = \frac{R1 \times R_I}{R1 - R_I} = \frac{13.3k\Omega \times 583\Omega}{13.3k\Omega - 583\Omega} = 609\Omega$$

Use 620Ω.

$$C11 = \frac{1}{2\pi \times R4 \times f_{P2}} = \frac{1}{2\pi \times 620\Omega \times 423kHz} = 607pF$$

Use 680pF.

Pick f_{P3} = 700kHz, which is the midpoint between f_{ZESR} and 1/2 the switching frequency.

$$C12 = \frac{C5}{(2\pi \times C5 \times R3 \times f_{P3}) - 1} = \frac{4.7nF}{(2\pi \times 4.7nF \times 6.8k\Omega \times 700kHz) - 1} = 33.7pF$$

Use 33pF.

Case 2: Electrolytic Output Capacitor *(operating at lower switching frequencies, $f_{ZESR} < f_C$)*

The modulator gain at f_C is:

$$G_{MOD(fc)} = G_{MOD(DC)} \frac{f_{PMOD}^{\;2}}{f_{ZESR} f_C}$$

The output capacitor's ESR zero frequency is higher than the LC double-pole frequency but lower than the closed-loop crossover frequency. Here the modulator already has a -20dB/decade slope; therefore, the error-amplifier gain must have a 0dB/decade slope at f_C, so the loop crosses over at the desired -20dB/decade slope. The error-amplifier circuit configuration is the same as Case 1; however, the closed-loop crossover frequency is now between f_{P2} and f_{P3}, as illustrated in Figure 4.

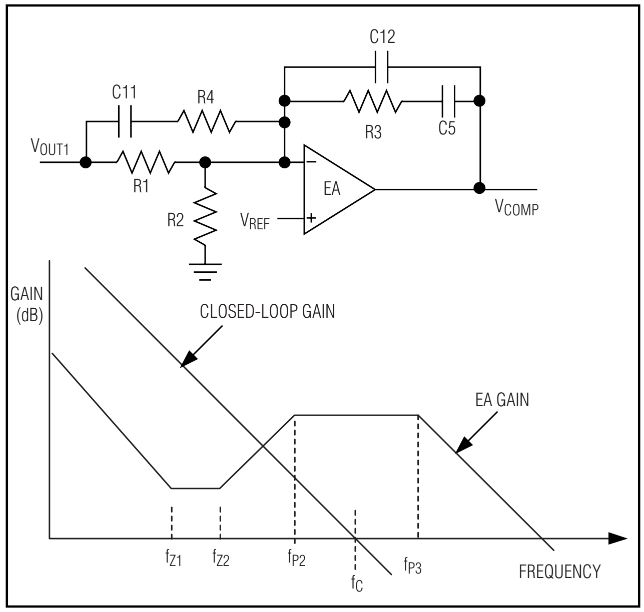


Figure 4. Case 2: Error-Amplifier Compensation Circuit (Closed-Loop and Error-Amplifier Gain Plot)

The equations that define the error amplifier's poles and zeroes (f_{Z1}, f_{Z2}, f_{P2}, and f_{P3}) are the same as for Case 1. However, f_{P2} is now lower than the closed-loop crossover frequency.

The error-amplifier gain at f_C is:

$$G_{EA(fc)} = \frac{1}{G_{MOD(fc)}}$$

And the gain of the error amplifier between f_{Z1} and f_{Z2} is:

$$G_{EA(fZ1\text{–}fZ2)} = G_{EA(fc)} \frac{f_{Z2}}{f_{P2}} = \frac{f_{Z2}}{f_{P2} G_{MOD(fc)}}$$

Due to the underdamped (Q > 1) nature of the output LC double pole, the error-amplifier zero frequencies must be set less than the LC double-pole frequency to provide adequate phase boost. Set the first zero of the error amplifier, f_{Z1}, at 1/4th the LC double-pole frequency. Set the second zero, f_{Z2}, at the LC double-pole frequency. Set the second pole, f_{P2}, at f_{ZESR}.