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MAX86140/ MAX86141

Best-in-Class Optical Pulse Oximeter and Heart-Rate Sensor for Wearable Health

General Description

The MAX86140/MAX86141 are ultra-low-power, completely integrated, optical data acquisition systems. On the transmitter side, the MAX86140/MAX86141 have three programmable high-current LED drivers that can be configured to drive up to six LEDs. With two MAX86140/MAX86141 devices working in master-slave mode, the LED drivers can drive up to twelve LEDs. On the receiver side, MAX86140 consists of a single optical readout channels, while the MAX86141 has two optical readout channels that can operate simultaneously. The devices have low-noise signal conditioning analog front-end (AFE) including 19-bit ADC, an industry-lead ambient light cancellation (ALC) circuit, and a picket fence detect and replace algorithm. Due to the low power consumption, compact size, easy/flexible-to-use and industry-lead ambient light rejection capability of MAX86140/MAX86141, the devices are ideal for a wide variety of optical-sensing applications, such as pulse oximetry and heart rate detection.

The MAX86140/MAX86141 operate on a 1.8V main supply voltage and a 3.1~5.5V LED driver supply voltage. Both devices support a standard SPI compatible interface and fully autonomous operation. Each device has a large 128-word built-in FIFO. The MAX86140/MAX86141 is available in compact wafer-level package (WLP) (2.048 x 1.848mm) with 0.4mm ball pitch.

Applications

- Wearable Devices for Fitness, Wellness and Medical Applications
- Optimized for Wrist, Finger, Ear, and Other Locations
- Optimized Performance to Detect
  - Optical Heart Rate
  - Oxygen Saturation (SpO_2)
  - Muscle Oxygen Saturation (SmO_2 and StO_2)

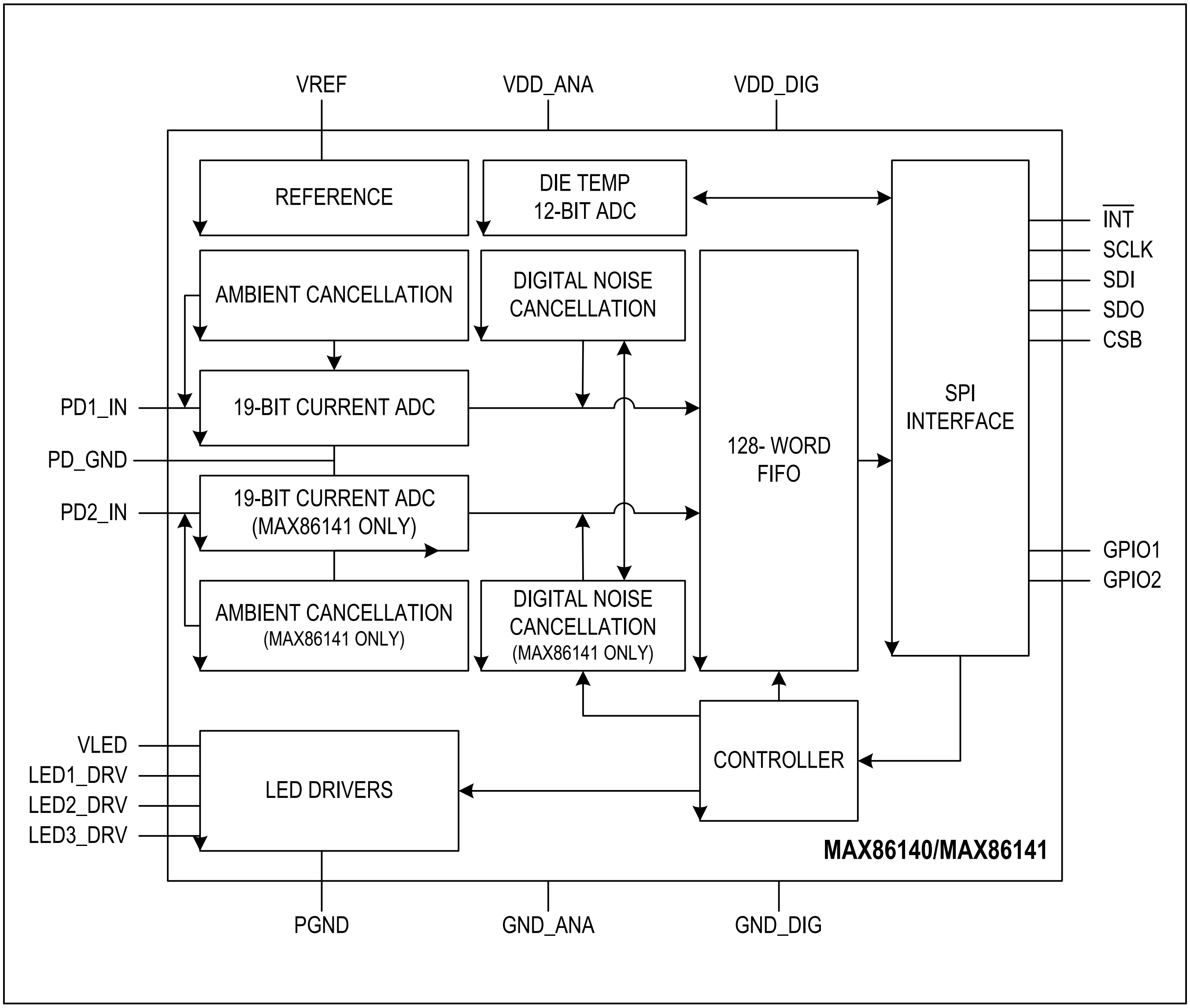
Benefits and Features

- Complete Single and Dual-Channel Optical Data Acquisition System
- Built-in Algorithm Further Enhances Rejection of Fast Ambient Transients
- Optimized Architecture for Transmissive and Reflective Heart Rate or SpO_2 Monitoring
- Low Dark Current Noise of < 50pA RMS (Sample to Sample Variance)
- Lower Effective Dark Current Noise Achievable Through Multiple Sample Modes and On-Chip Averaging
- High-Resolution, 19-Bit Charge Integrating ADC
- Three Low-Noise, 8-Bit LED Current DACs
- Excellent Dynamic Range > 90dB in White Card Loop-Back Test (Sample-to-Sample Variance)
- Dynamic Range Extendable to > 104dB for SpO_2 and > 110dB for HRM with Multiple Sample Modes and On-Chip Averaging
- Excellent Ambient Range and Rejection Capability
  - > 100µA Ambient Photodetector Current
  - > 70dB Ambient Rejection at 120Hz
- Ultra-Low-Power Operation for Body Wearable Devices
  - Low-Power Operation, Optical Readout Channel < 10µA (typ) at 25sps
  - Short Exposure Integration Period of 14.8µs, 29.4µs, 58.7µs, 117.3µs
  - Low Shutdown Current = 20µW (typ)
- Built-in Algorithm Further Enhances Rejection of Fast Ambient Transients
- Miniature 2.048 x 1.848mm, 5 x 4 0.4mm Ball Pitch WLP
- -40°C to +85°C Operating Temperature Range

Ordering Information appears at end of data sheet.

19-100051; Rev 1; 8/17

Simplified Block Diagram



Absolute Maximum Ratings

VDD_ANA to GND_ANA ....-0.3V to +2.2V
VDD_DIG to GND_ANA ....-0.3V to +2.2V
VDD_ANA to VDD_ANA......................................-0.3V to +0.3V
PGND to GND_ANA...-0.3V to +0.3V
SCLK, SDO, SDI, CSB, $\overline{INT}$ to GND_ANA ....-0.3V to +6.0V
GND_DIG to GND_ANA......................................-0.3V to +0.3V
VLED to PGND..-0.3V to +6.0V
LED_DRV1 to PGND ....-0.3V to V_{LED} + 0.3V
LED_DRV2 to PGND ....-0.3V to V_{LED} + 0.3V
LED_DRV3 to PGND ....-0.3V to V_{LED} + 0.3V
PD1_IN to GND_ANA..-0.3V to +2.2V
PD2_IN to GND_ANA .... -0.3V to +2.2V
PD_GND to GND_ANA.......................................-0.3V to +0.3V
All other pins to GND_ANA.................................-0.3V to +2.2V
Output Short-Circuit Duration...................................Continuous
Continuous Input Current Into Any Pin
(except LED_DRVx Pins) ....±20mA
Continuous Power Dissipation (WLP
(derate 5.5mW/°C above +70°C)) 440mW
Operating Temperature Range........................... -40°C to +85°C
Storage Temperature Range .... -40°C to +105°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

5 x 4 WLP

PACKAGE CODE	N201A2+1
Outline Number	21-100134
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	55.49°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(VDD_{ANA} = 1.8V, VDD_{DIG} = 1.8V, V_{LED} = 5.0V, ADC_RGE = 16μA, PPG_SR = 1024sps, PPG_TINT = 14.8μs, LED_SETLNG = 6μs, LEDx_RGE = 31mA, C_{PD} = 65pF, PD_BIAS = 0x1, $I_{exposure}$ = 1μA, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Readout Channel						
ADC Resolution				19		bits
ADC Full Scale Input Current		ADC_RGE = 0x0		4.0		μA
		ADC_RGE = 0x1		8.0		
		ADC_RGE = 0x2		16.0		
		ADC_RGE = 0x3		32.0		
ADC Integration Time	t_{INT}	PPG_TINT = 0x0		14.8		μs
		PPG_TINT = 0x1		29.4		
		PPG_TINT = 0x2		58.7		
		PPG_TINT = 0x3		117.3		
Minimum PPG Sample Rate		PPG_SR = 0x0A		8		sps
Maximum PPG Sample Rate		PPG_SR = 0x13		4096		sps
Sample Rate Error		From nominal as indicated in the PPG_SR table	-2		+2	%
DC Ambient Light Input Range	ALR	ALC = on, ALC_OVF = 1	100			μA
AC Ambient Light Rejection	AC_ALRR	ALC = on, $I_{ambient}$ = 1μA DC with ±0.4μA pk-pk 120Hz Sinwave		70		dB
DC Ambient Light Rejection		ALC = on, $I_{ambient}$ modulated between 0μA and 30μA, LED_SETLNG = 12μs, PPG_TINT = 117.3μs		0.5		nA
Dark Current Offset	DC_O	ALC = ON, PD_BIAS = 0x0, ADD_OFFSET = 1		±1		Counts
Dark Current Input Referred Noise		PPG_TINT = 14.8μs		262		pArms
		PPG_TINT = 29.4μs		128		
		PPG_TINT = 58.7μs		83		
		PPG_TINT = 117.3μs		56		pArms
Maximum Photodiode Input Capacitance	C_{pd}	$I_{ambient}$ = 0μA, less than 1nA of code shift; PD_BIAS = 0x1		65		pF
		PD_BIAS = 0x5		130		
		PD_BIAS = 0x6		260		
		PD_BIAS = 0x7		520		
VDD DC PSR		$I_{ambient}$ = 0μA, V_{DD} = 1.7V to 2.0V	-560	-330	+560	LSB/V
LED Driver						
LED Current Resolution				8		Bits
Driver DNL		LEDx_RGE = 124mA	-1		1	LSB
Driver INL		LEDx_RGE = 124mA		0.6		LSB

Electrical Characteristics (continued)

(VDD_{ANA} = 1.8V, VDD_{DIG} = 1.8V, V_{LED} = 5.0V, ADC_RGE = 16μA, PPG_SR = 1024sps, PPG_TINT = 14.8μs, LED_SETLNG = 6μs, LEDx_RGE = 31mA, C_{PD} = 65pF, PD_BIAS = 0x1, $I_{exposure}$ = 1μA, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full Scale LED Current (Note 3)	I_{LED}	LEDx_PA = 0xFF	LEDx_RGE = 0x0		31		mA
			LEDx_RGE = 0x1		62		
			LEDx_RGE = 0x2		93		
			LEDx_RGE = 0x3	117	124	129	
Minimum output voltage	V_{OL}	LEDx_PA = 0xFF, 95% of the desired LED current	LEDx_RGE = 0x0		160	253	mV
			LEDx_RGE = 0x1		317		
			LEDx_RGE = 0x2		495		
			LEDx_RGE = 0x3		700		
LED Driver DC PSR		V_{DD} = 1.8V, VLEDx_DRV = 0.9V, LEDx_PA = 0xFF, V_{LED} = 3.1 to 5.5V, LEDx_RGE = 124mA			-1	+400	μA/V
		V_{DD} = 1.7 to 2.0V, T_A = +25°C, LEDx_PA = 0xFF			110	1410	
LED1 Driver Compliance Interrupt	$LED1_{COMP}$				180		mV
Internal Die Temperature Sensor							
Temperature Sensor Accuracy		T_A = 25°C			1		°C
Temperature Sensor Minimum Range		Temperature error < 5°C			-40		°C
Temperature Sensor Maximum Range		Temperature error < 5°C			85		°C
Temperature ADC Acquisition Time					29		ms
Power Supply							
Power Supply Voltage	V_{DD}	Verified during PSRR Test		1.7	1.8	2.0	V
LED Supply Voltage	V_{LED}	Verified during PSRR Test		3.1		5.5	V

Electrical Characteristics (continued)

(VDD_{ANA} = 1.8V, VDD_{DIG} = 1.8V, V_{LED} = 5.0V, ADC_RGE = 16μA, PPG_SR = 1024sps, PPG_TINT = 14.8μs, LED_SETLNG = 6μs, LEDx_RGE = 31mA, C_{PD} = 65pF, PD_BIAS = 0x1, $I_{exposure}$ = 1μA, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VDD Supply Current	I_{DD}	MAX86140, Single LED Exposure/Sample. PPG_SR = 4096sps, LP_MODE = 0x0, LEDxPA = 0mA			660	780	μA
		MAX86140, Single LED Exposure/Sample, PW = 14.8μs, LP_MODE = 0x1, LEDx_PA = 0mA	PPG_SR = 256sps		80		
			PPG_SR = 100sps		32		
			PPG_SR = 50sps		16		
			PPG_SR = 25sps		8.5		
		MAX86140, Double LED Exposure/Sample, PPG_SR = 84sps, PW = 14.8μs, LP_MODE = 0x1, LEDx_PA = 0mA	Single pulse		42		μA
			Double pulse		89		μA
		MAX86141, Single LED Exposure/Sample. PPG_SR = 4096sps, LP_MODE = 0x0, LEDxPA = 0mA			978	1170	μA
		MAX86141, Single LED Exposure/Sample, LP_BOOST = 1, LEDx_PA = 0mA	PPG_SR = 256sps		115.5		
			PPG_SR = 100sps		46		
			PPG_SR = 50sps		23		
			PPG_SR = 25sps		11		
		MAX86141, Two LED Exposure/Sample, PPG_SR = 84sps, LP_BOOST = 1, LEDx_PA = 0mA	Single pulse		60		μA
			Double pulse		130		μA
		Die Temperature mode, SPS = 1, Optical channel(s) disabled			8		μA
VLED Supply Current	I_{LED}	Single LED exposure per Sample, PPG_TINT = 117.3μs, Single-Pulse, PPG_SR = 256sps, LEDx_PA = 0mA			0.22		μA
		Single LED exposure per Sample, PPG_TINT = 117.3μs, Single-Pulse, LEDx_PA = 62mA	PPG_SR = 256sps		1880		
			PPG_SR = 100sps		735		
			PPG_SR = 50sps		370		
			PPG_SR=25sps		185		
		Two LED exposure per sample, PPG_TINT = 117.3μs, LEDx_PA = 62mA, PPG_SR = 84sps	Single-Pulse		1240		μA
			Dual-Pulse		2480		
VDD Current in Shutdown		T_A = +25°C			0.6	2.5	μA
VLED Current in Shutdown		T_A = +25°C				1	μA

Electrical Characteristics (continued)

(VDD_{ANA} = 1.8V, VDD_{DIG} = 1.8V, V_{LED} = 5.0V, ADC_RGE = 16μA, PPG_SR = 1024sps, PPG_TINT = 14.8μs, LED_SETLNG = 6μs, LEDx_RGE = 31mA, C_{PD} = 65pF, PD_BIAS = 0x1, $I_{exposure}$ = 1μA, T_A = 25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital I/O Characteristics						
SDO Output Low Voltage	V_{OL_SDO}	I_{SINK} = 2mA			0.4	V
SDO Output High Voltage	V_{OH_SDO}	I_{SOURCE} = 2mA	V_{DD}-0.4			V
Open-Drain Output Low Voltage	V_{OL_OD}	I_{SINK} = 6mA, INTB, GPIO1, GPIO2			0.4	V
Input Voltage Low	V_{IL}	SDI, SCLK, CSB, GPIO1, GPIO2			0.4	V
Input Voltage High	V_{IH}	SDI, SCLK, CSB, GPIO1, GPIO2	1.4			V
Input Hysteresis	V_{HYS}	SDI, SCLK, CSB		330		mV
		GPIO1, GPO2		240		
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C (SDI, SCLK, CSB, GPIO1, GPIO2)		0.01	1	μA
Input Capacitance	C_{IN}	SDI, SCLK, CSB, GPIO1, GPIO2		10		pF
SPI Timing Charateristics						
SCLK Frequency	f_{SCLK}				8	MHz
SCLK Period	t_{CP}		125			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To 1st SCLK rising edge	20			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive rising edge preceding 1st rising edge	5			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 24th rising edge	500			ns
SCLK Rise to CSB Fall	t_{CSF}	Applies to 24th rising edge	500			ns
CSB Pulse Width High	t_{CSPW}		250			ns
SDI to SCLK Rise Setup Time	t_{DS}		10			ns
SDI to SCLK Rise Hold Time	t_{DH}		10			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 50pF			35	ns
CSB Fall to SDO Enabled	t_{DOE}	C_{LOAD} = 0pF	12			ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable Time			25	ns
GPIO1 External Sync Pulse Width	$t_{PLGPIO1}$		64			μs
GPIO2 External Clock Input (Note 4)	f_{GPIO2}	External Sample Reference Clock on GPIO2	31900		32868	Hz
GPIO2 External Clock Pulse Width	$t_{PWGPIO2}$		1			μs

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

Note 2: Specifications are guaranteed by Maxim Integrated's bench characterization and by 100% production test using proprietary ATE setup and conditions.

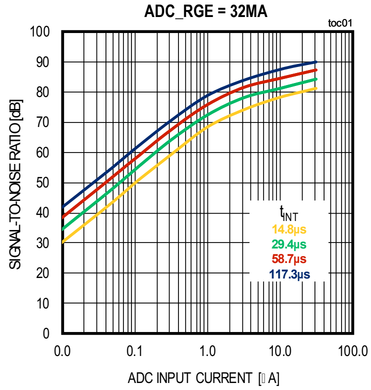
Note 3: The LED current is trim in production to meet the IR and RED ADC counts. Actual values may vary by up to ±50%. Values shown here are for 0% trim.

Note 4: See *Register Map/PPG Configuration 2 (0x12)* section for the sample rate by the external clock frequency. The sample rate will be shifted when the external clock frequency shifts.

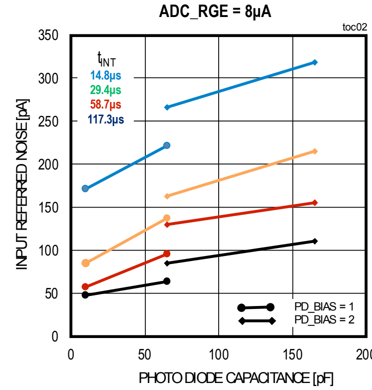
Typical Operating Characteristics

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)(T_A = +25°C, unless otherwise noted.)

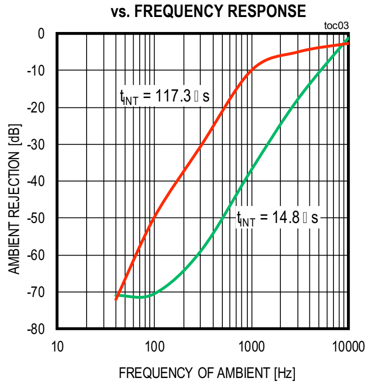
SIGNAL-TO-NOISE RATIO
vs. ADC INPUT CURRENT
ADC_RGE = 32MA



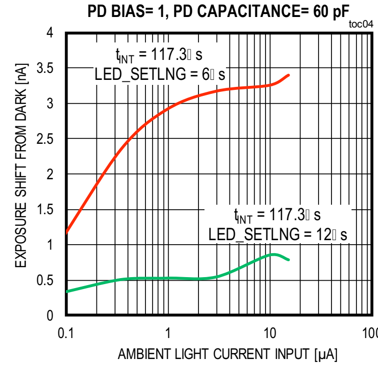
INPUT REFERRED NOISE
vs. PD CAPACITANCE
ADC_RGE = 8µA



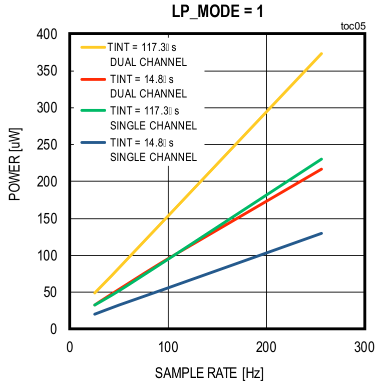
AMBIENT REJECTION
vs. FREQUENCY RESPONSE



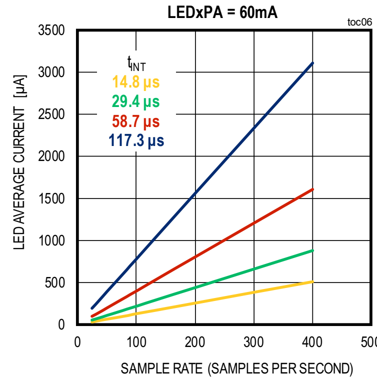
AMBIENT LIGHT REJECTION
EXPOSURE SHIFT vs. AMBIENT INPUT
PD BIAS= 1, PD CAPACITANCE= 60 pF



AFE POWER DISSIPATION
LP_MODE = 1

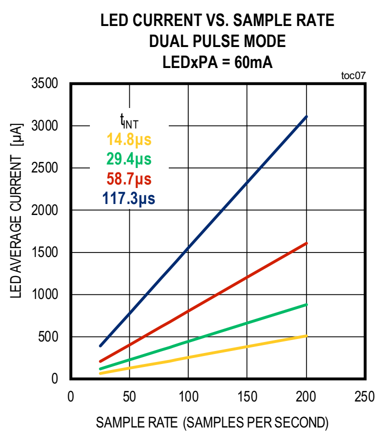


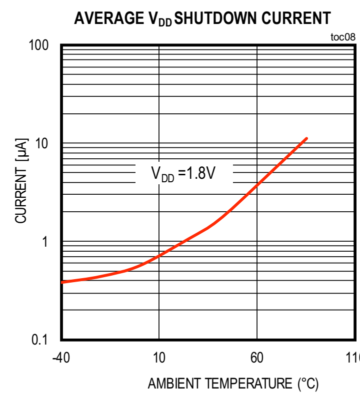
LED CURRENT vs. SAMPLE RATE
SINGLE PULSE MODE
LEDxPA = 60mA

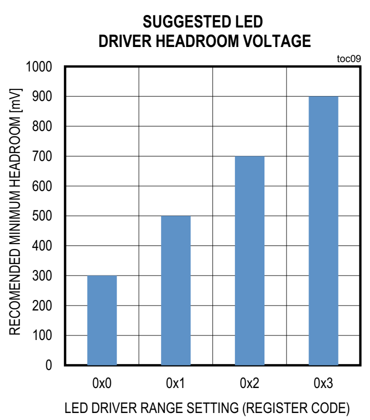


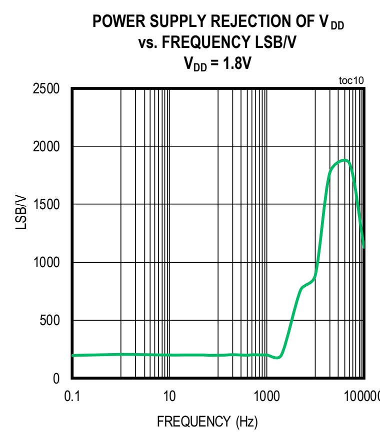
Typical Operating Characteristics (continued)

(V_{DD} = 1.8V, V_{LED} = 5.0V, GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)(T_A = +25°C, unless otherwise noted.)



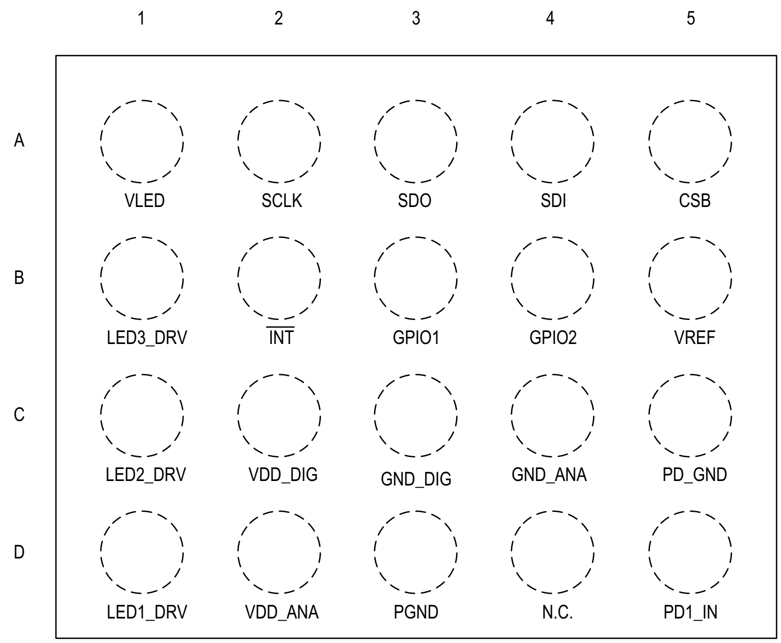




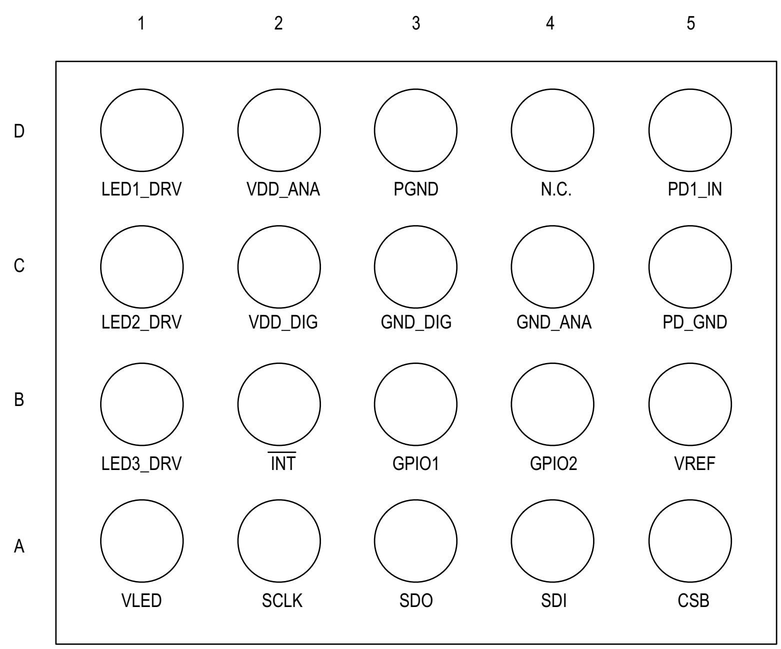


Pin Configurations

MAX86140

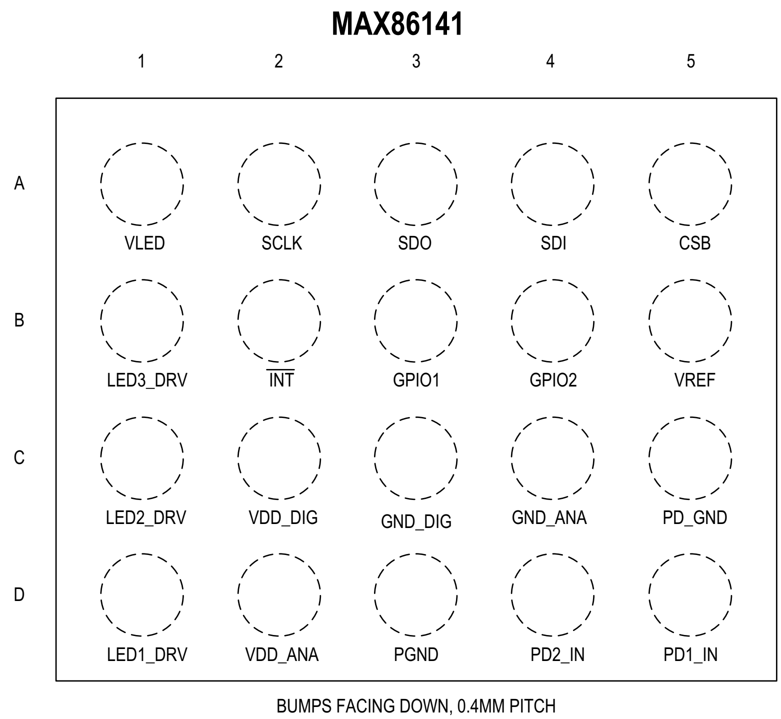


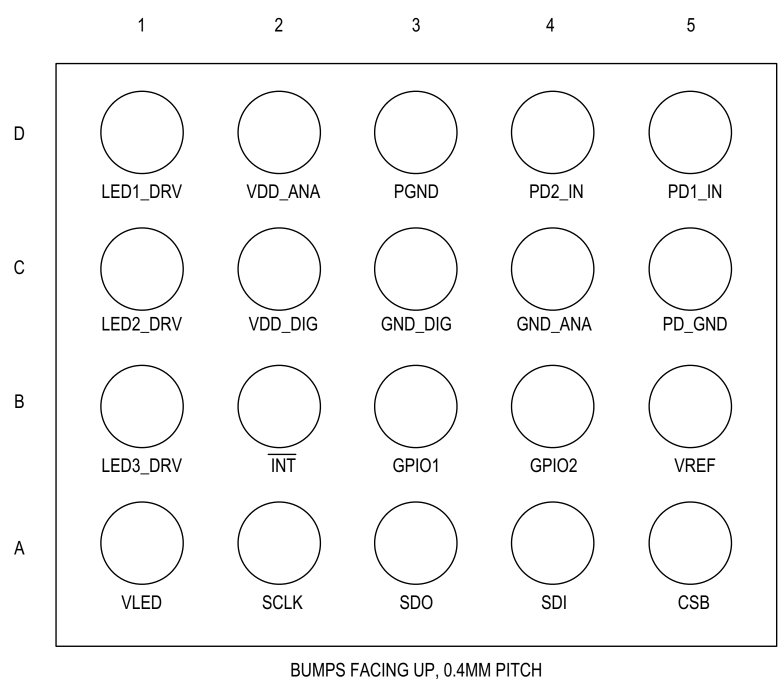
BUMPS FACING DOWN, 0.4MM PITCH



BUMPS FACING UP, 0.4MM PITCH

Pin Configurations (continued)





Pin Description

PIN		NAME	FUNCTION
MAX86140	MAX86141		
Power			
C2	C2	VDD_DIG	Digital Logic Supply. Connect to externally-regulated supply. Bypass to GND_DIG
C3	C3	GND_DIG	Digital Logic and Digital Pad Return. Connect to GND.
D2	D2	VDD_ANA	Analog Supply. Connect to externally-regulated supply. Bypass with a 0.1μF capacitor as close as possible to bump and a 10μF capacitor to GND_ANA.
C4	C4	GND_ANA	Analog Power Return. Connect to GND.
A1	A1	VLED	LED Power Supply Input. Connect to external voltage supply. Bypass with a 10μF capacitor to PGND.
D3	D3	PGND	LED Power Return. Connect to GND.
Control Interface			
A2	A2	SCLK	SPI Clock
A3	A3	SDO	SPI Data Ouput
A4	A4	SDI	SPI Data Input
A5	A5	CSB	SPI Chip select
B2	B2	$\overline{\text{INT}}$	Interrupt. Programmable open-drain Interrupt output signal pin (active-low).
B3	B3	GPIO1	General Purpose I/O. Open-drain when programmed as output (active-low).
B4	B4	GPIO2	General Purpose I/O. Open-drain when programmed as output (active-low).
Optical Pins			
—	D4	PD2_IN	Photodiode Cathode Input
D5	D5	PD1_IN	Photodiode Cathode Input
C5	C5	PD_GND	Photodiode Anode
D1	D1	LED1_DRV	LED Output Driver 1. Connect the LED cathode to LED1_DRV and its anode to the V_{LED} supply.
C1	C1	LED2_DRV	LED Output Driver 2. Connect the LED cathode to LED2_DRV and its anode to the V_{LED} supply.
B1	B1	LED3_DRV	LED Output Driver 3 Connect the LED cathode to LED3_DRV and its anode to the V_{LED} supply.
Reference			
B5	B5	VREF	Internal Reference Decoupling Point. Bypass with a 1μF capacitor to GND_ANA.
N.C.			
D4		N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.

Detailed Description

The MAX86140/MAX86141 are complete integrated optical data acquisition systems, ideal for optical pulse oximetry and heart rate detection applications. Both parts have been designed for the demanding requirements of mobile and wearable devices and require minimal external hardware components are necessary for integration into a wearable device. They include high-resolution, optical readout signal processing channels with robust ambient light cancellation and high-current LED driver DACs to form a complete optical readout signal chain.

The MAX86140/MAX86141 are fully adjustable through software registers and the digital output data is stored in a 128-word FIFO within the IC. The FIFO allows the MAX86140/MAX86141 to be connected to a microcontroller or processor on a shared bus, where the data is not being read continuously from the MAX86140/MAX86141's registers. Both operate in fully autonomous modes for low power battery applications.

The MAX86140 consists of a single optical readout channel, while the MAX86141 incorporates dual optical readout channels that operate simultaneously. Both parts have three LED drivers and are well suited for a wide variety of optical sensing applications.

The MAX86140/MAX86141 operate on a 1.8V main supply voltage, with a separate 3.1V to 5.0V LED driver power supply. Both devices have flexible timing and shutdown configurations as well as control of individual blocks so an optimized measurement can be made at minimum power levels.

Optical Subsystem

The optical subsystem in the MAX86140/MAX86141 is composed of ambient light cancellation (ALC), a continuous-time sigma-delta ADC, and proprietary discrete time filter. ALC incorporates a proprietary scheme to cancel ambient light generated photo diode current, allowing the sensor to work in high ambient light conditions. The optical ADC has programmable full-scale ranges of 4µA to 32µA. The internal ADC is a continuous time oversampling sigma delta converter with 19-bit resolution. The ADC output data rate can be programmed from 8sps (samples per second) to 8192sps. The MAX86140 includes a proprietary discrete time filter to reject 50Hz/60Hz interference and changing residual ambient light from the sensor measurements.

The MAX86140/MAX86141 supports Dynamic Power Down mode (Low-Power mode) in which the power consumption is decreased between samples. This mode is only supported for sample rates 128sps and below. For more details on the power consumption at each sample rates, refer to the *Electrical Characteristics* table.

LED Driver

The MAX86140/MAX86141 integrates three precision LED driver-current DACs that modulate LED pulses for a variety of optical measurements. The LED current DACs have 8-bits of dynamic range with four programmable full-scale ranges of 31mA, 62mA, 94mA, and 124mA. The LED drivers are low dropout current sources, allowing for low-noise, power-supply independent LED currents to be sourced at the lowest supply voltage possible; therefore minimizing LED power consumption. The LED pulse width can be programmed from 14.8µs to 117.3µs to allow the algorithms to optimize SpO_2 and HR accuracy at the lowest dynamic power consumption dictated by the application.

FIFO Configuration

The FIFO is 128 sample depth and is designed to support various data types, as shown in Table 2. Each sample width is 3 bytes, which includes a 5-bit tag width. The tag embedded in the FIFO_DATA is used to identify the source of each sample data. The description of each Tag is as shown in Table 3.

LED Sequence Control (address 0x20 ~ 0x22)

The data format in the FIFO, as well as the sequencing of exposures, are controlled by the LED Sequence Registers through LEDC1 through LEDC6. There are six LED Sequence Data Items available, as shown in Table 1. The exposure sequence cycles through the LED Sequence bit fields, starting from LEDC1 to LEDC6. The first LED Sequence field set to NONE (0000) ends the sequence.

Table 1. LED Sequence Control Registers

ADDRESS	REGISTER NAME	DEFAULT VALUE	B7	B6	B5	B4	B3	B2	B1	B0
0x20	LED Sequence Register 1	00	LEDC2[3:0]				LEDC1[3:0]			
0x21	LED Sequence Register 2	00	LEDC4[3:0]				LEDC3[3:0]			
0x22	LED Sequence Register 3	00	LEDC6[3:0]				LEDC5[3:0]			

Table 2 lists the codes for exposures selected in the LED sequence control registers.

Table 2. LED Sequence Register Data Type

LEDCN[3:0]	DATA TYPE
0000	NONE
0001	LED1
0010	LED2
0011	LED3
0100	LED1 and LED2 pulsed simultaneously
0101	LED1 and LED3 pulsed simultaneously
0110	LED2 and LED3 pulsed simultaneously
0111	LED1, LED2, and LED3 pulsed simultaneously
1000	Pilot on LED1
1001	DIRECT AMBIENT
1010	LED4 (external mux control)
1011	LED5 (external mux control)
1100	LED6 (external mux control)
1101	Reserved
1110	Reserved
1111	Reserved

Table 3 shows the format of the FIFO data along with the associated Tag. In a sample if a picket fence event is detected, the predicted value is pushed to the FIFO along with its tag (PPFx_LEDCx_DATA).

Table 3. FIFO Data and Tag

TAG[4:0]	DATA TYPE	FIFO_DATA[23:0]	COMMENTS
00001	PPG1_LEDC1_DATA	LEDC1_DATA[18:0]	If LEDC1 is non-zero
00010	PPG1_LEDC2_DATA	LEDC2_DATA[18:0]	If LEDC1 and LEDC2 are non-zero
00011	PPG1_LEDC3_DATA	LEDC3_DATA[18:0]	If LEDC1, LEDC2 and LEDC3 are non-zero
00100	PPG1_LEDC4_DATA	LEDC4_DATA[18:0]	If LEDC1, LEDC2, LEDC3, and LEDC4 are non-zero
00101	PPG1_LEDC5_DATA	LEDC5_DATA[18:0]	If LEDC1, LEDC2, LEDC3, LEDC4, and LEDC5 are non-zero
00110	PPG1_LEDC6_DATA	LEDC6_DATA[18:0]	If LEDC1, LEDC2, LEDC3, LEDC4, LEDC5, and LEDC6 are non-zero
00111	PPG2_LEDC1_DATA	LEDC1_DATA[18:0]	If LEDC1 is non-zero
01000	PPG2_LEDC2_DATA	LEDC2_DATA[18:0]	If LEDC1 and LEDC2 are non-zero
01001	PPG2_LEDC3_DATA	LEDC3_DATA[18:0]	If LEDC1, LEDC2, and LEDC3 are non-zero
01010	PPG2_LEDC4_DATA	LEDC4_DATA[18:0]	If LEDC1, LEDC2, LEDC3, and LEDC4 are non-zero
01011	PPG2_LEDC5_DATA	LEDC5_DATA[18:0]	If LEDC1, LEDC2, LEDC3, LEDC4, and LEDC5 are non-zero
01100	PPG2_LEDC6_DATA	LEDC6_DATA[18:0]	If LEDC1, LEDC2, LEDC3, LEDC4, LEDC5, and LEDC6 are non-zero
01101	PPF1_LEDC1_DATA	LEDC1_DATA[18:0]	If LEDC1 is non-zero (Picket Fence Event)
01110	PPF1_LEDC2_DATA	LEDC2_DATA[18:0]	If LEDC1 and LEDC2 are non-zero (Picket Fence Event)
01111	PPF1_LEDC3_DATA	LEDC3_DATA[18:0]	If LEDC1, LEDC2, and LEDC3 are non-zero (Picket Fence Event)
10000	Reserved	–	
10001	Reserved	–	
10010	Reserved	–	
10011	PPF2_LEDC1_DATA	LEDC1_DATA[18:0]	If LEDC1 is non-zero (Picket Fence Event)
10100	PPF2_LEDC2_DATA	LEDC2_DATA[18:0]	If LEDC1 and LEDC2 are non-zero (Picket Fence Event)
10101	PPF2_LEDC3_DATA	LEDC3_DATA[18:0]	If LEDC1, LEDC2, and LEDC3 are non-zero (Picket Fence Event)
10110	Reserved	–	
10111	Reserved	–	
11000	Reserved	–	
11001	PROX1_DATA	PROX1_DATA[18:0]	Only PILOT LED1 for LEDC1 is used
11010	PROX2_DATA	PROX2_DATA[18:0]	Only PILOT LED1 for LEDC1 is used
11011	Reserved	–	
11100	Reserved	–	
11101	Reserved	–	
11110	INVALID_DATA	Don't_care[18:0]	This tag indicates that there was an attempt to read an empty FIFO
11111	TIME_STAMP	TIME_STAMP[18:0]	If TIME_STAMP_EN = 1, this is TIME_STAMP

There are seven registers that control how the FIFO is configured and read out. These registers are illustrated below.

Table 4. PPG Configuration

ADDRESS	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x04	FIFO Write Pointer	–				FIFO_WR_PTR[6:0]			
0x05	FIFO Read Pointer	–				FIFO_RD_PTR[6:0]			
0x06	Overflow Counter	–				OVF_COUNTER[6:0]			
0x07	FIFO Data Counter	FIFO_DATA_COUNT[7:0]							
0x08	FIFO Data Register	FIFO_DATA[7:0]							
0x09	FIFO Configuration 1	–	FIFO_A_FULL[6:0]						
0x0A	FIFO Configuration 2	–	–	TIME_ STAMP_EN	FLUSH_ FIFO	FIFO_ STAT_CLR	A_FULL_ TYPE	FIFO_RO	–

Write Pointer (Register 0x04)

FIFO_WR_PTR[6:0] points to the FIFO location where the next item will be written. This pointer advances for each item pushed on to the FIFO by the internal conversion process. The write pointer is a 7-bit counter and will wrap around to count 0x00 on the next item after count 0x7F.

Read Pointer (Register 0x05)

FIFO_RD_PTR[6:0] points to the location from where the next item from the FIFO will be read via the serial interface. This advances each time an item is read from the FIFO. The read pointer can be both read and written to. This allows an item to be reread from the FIFO if it has not already been overwritten. The read pointer is updated from a 7-bit counter and will wrap around to count 0x00 from count 0x7F.

Overflow Counter (Register 0x06)

OVF_COUNTER[6:0] logs the number of items lost if the FIFO is not read in a timely fashion. This counter holds/saturates at count value 0x7F. When a complete item is popped from the FIFO (when the read pointer advances), the OVF_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred.

FIFO Data Counter (Register 0x07)

FIFO_DATA_COUNT[7:0] is a read-only register which holds the number of items available in the FIFO for the host to read. This increments when a new item is pushed to the FIFO, and decrements when the host reads an item from the FIFO.

FIFO Data (Register 0x08)

FIFO_DATA[7:0] is a read-only register used to retrieve data from the FIFO. It is important to burst read the item from the FIFO. Each item is three bytes. So burst reading three bytes at FIFO_DATA register via the serial interface advances the FIFO_RD_PTR. The format and data type of the data stored in the FIFO is determined by the Tag associated with data. Readout from the FIFO follows a progression defined by LED Sequence Control registers as well. This configuration is best illustrated by a few examples.

Assume it is desired to perform a SpO_2 measurement and also monitor the ambient level on the photodiode to adjust the IR and red LED intensity. To perform this measurement, configure the following registers:

LED Sequence Control

LEDC1 = 0x1	(LED1 exposure)
LEDC2 = 0x2	(LED2 exposure)
LEDC3 = 0x9	(DIRECT AMBIENT exposure)
LEDC4 = 0x0	(NONE)
LEDC5 = 0x0	(NONE)
LEDC6 = 0x0	(NONE)

PPG Configuration

PPG1_ADC_RGE[1:0]	(PPG1 Gain Range Control)
PPG2_ADC_RGE[1:0]	(PPG2 Gain Range Control)
PPG_TINT[1:0]	(LED Pulse-Width Control)
PPG_SR[3:0]	(Sample Rate)

LED Pulse Amplitude

LED1_PA[7:0]	(LED1 Drive Current)
LED2_PA[7:0]	(LED2 Drive Current)

When done so the sample sequence and the data format in the FIFO will follow the following time/location sequence.

tag 1, PPG1 LED1 data
tag 7, PPG2 LED1 data
tag 2, PPG1 LED2 data
tag 8, PPG2 LED2 data
tag 3, PPG1 Ambient data
tag 9, PPG2 Ambient data
tag 1, PPG1 LED1 data
tag 7, PPG2 LED1 data
tag 2, PPG1 LED2 data
tag 8, PPG2 LED2 data
tag 3, PPG1 Ambient data
tag 9, PPG2 Ambient data
.
.
.
tag 1, PPG1 LED1 data
tag 7, PPG2 LED1 data
tag 2, PPG1 LED2 data
tag 8, PPG2 LED2 data
tag 3, PPG1 Ambient data
tag 9, PPG2 Ambient data

where:

PPGm LED1 data = the ambient corrected exposure data from LED1 in PPGm channel
PPGm LED2 data = the ambient corrected exposure data from LED2 in PPGm channel
PPGm Ambient data = the direct ambient sample in PPGm channel
m is 1 of PPG1 channel, and 2 for PPG2 channel

For a second example, assume it is desired to pulse LED1 and LED2 simultaneously while also monitoring the ambient level.

LED Sequence Control

LEDC1 = 0x4	(LED1 and LED2 exposure)
LEDC2 = 0x9	(DIRECT AMBIENT exposure)
LEDC3 = 0x0	(NONE)
LEDC4 = 0x0	(NONE)
LEDC5 = 0x0	(NONE)
LEDC6 = 0x0	(NONE)

In this case, the sequencing in the FIFO will then be:

tag 1, PPG1 LED1+LED2 data
tag 7, PPG2 LED1+LED2 data
tag 2, PPG 1 Ambient data
tag 8, PPG 2 Ambient data
tag 1, PPG1 LED1+LED2 data
tag 7, PPG2 LED1+LED2 data
tag 2, PPG1 Ambient data
tag 8, PPG2 Ambient data
.
.
.
tag 1, PPG1 LED1+LED2 data
tag 7, PPG2 LED1+LED2 data
tag 2, PPG1 Ambient data
tag 8, PPG2 Ambient data

where:

PPGm LED1+LED2 data = the ambient corrected exposure data from LED1 and LED2 for PPGm channel
PPGm Ambient data = the direct ambient corrected sample for PPGm channel

The number of bytes of data for the PPG channel is given by: 2 x 3 x K x N

where:

K = the number of active exposures as defined in the LED Sequence Control registers 0x20, 0x21, and 0x22.
N = the number of samples in the FIFO

To calculate the number of available items one can perform the following pseudo-code:

```
read the OVF_COUNTER register
read the FIFO_DATA_COUNT register
if OVF_COUNTER == 0 //no overflow occurred
   NUM_AVAILABLE_SAMPLES = FIFO_DATA_COUNT
else
   NUM_AVAILABLE_SAMPLES = 128 // overflow occurred and data has been lost
endif
```

Table 6 shows the FIFO data format depends on the data type being stored. Optical data, whether full ambient corrected LED exposure, ambient corrected proximity or direct ambient sampled data is left-justified, as shown in Table 6. Bits F23:F19 of the FIFO word contains the tag that identifies the data.

Table 6. Optical FIFO Data Format

	FIFO DATA FORMAT (FIFO_DATA[23:0])																							
ADC Res	Tag (TAG[4:0])					ADC Value (FIFO_DATA[18:0])																		
	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0
19-bits	T4	T3	T2	T1	T0	O18	O17	O16	O15	O14	O13	O12	O11	O10	O9	O8	O7	O6	O5	O4	O3	O2	O1	O0

FIFO_A_FULL (address 0x09)

The FIFO_A_FULL[6:0] field in the FIFO Configuration 1 register (0x09) sets the watermark for the FIFO and determines when the A_FULL bit in the Interrupt_Status register (0x00) gets asserted. The A_FULL bit will be set when the FIFO contains 128 minus FIFO_A_FULL[6:0] items. When the FIFO is almost full, if the A_FULL_EN mask bit in the Interrupt_Enable register (0x03) is set, then A_FULL bit gets asserted in the Interrupt Status 1 register and this bit is routed to the INT pin on the serial interface. This condition should prompt the applications processor to read samples off of the FIFO before it fills. The A_FULL bit is cleared when the status register is read.

The application processor can read both the FIFO_WR_PTR and FIFO_RD_PTR to calculate the number of items available in the FIFO, or just read the OVF_COUNTER and FIFO_DATA_COUNT registers, and read as many items as it needs to empty the FIFO. Alternatively, if the applications always responds much faster than the selected sample rate, it could just read 128 minus FIFO_A_FULL[6:0] items when it gets A_FULL interrupt and be assured that all data from the FIFO are read.

FIFO_RO (Address 0x0A)

The FIFO_RO bit in the FIFO Configuration 2 register (0x0A) determines whether samples get pushed on to the FIFO when it is full. If push is enabled when FIFO is full, old samples are lost. If FIFO_RO is not set, the new sample is dropped and the FIFO is not updated.

A_FULL_TYPE (Address 0x0A)

The A_FIFO_TYPE bit defines the behavior of the A_FULL interrupt. If the A_FIFO_TYPE bit is set low, the A_FULL interrupt gets asserted when the A_FULL condition is detected and cleared by status register read, but reasserts for every sample if the A_FULL condition persists. If A_FIFO_TYPE bit is set high, the A_FULL interrupt gets asserted only when a new A_FULL condition is detected. The interrupt gets cleared on Interrupt Status 1 register read, and does not re-assert for every sample until a new a-full condition is detected.

FIFO_STAT_CLR (Address 0x0A)

The FIFO_STAT_CLR bit defines whether the A-FULL interrupt should get cleared by FIFO_DATA register read. If FIFO_STAT_CLR is set low, A_FULL and DATA_RDY interrupts do not get cleared by FIFO_DATA register read but get cleared by status register read. If FIFO_STAT_CLR is set high, A_FULL and DATA_RDY interrupts get cleared by a FIFO_DATA register read or a status register read.

FLUSH_FIFO (Address 0x0A)

The FIFO Flush bit is used for flushing the FIFO. The FIFO becomes empty and the FIFO_WR_PTR[6:0], FIFO_RD_PTR[6:0], FIFO_DATA_COUNT[7:0] and OVF_COUNTER[6:0] get reset to zero. FLUSH_FIFO is a self-clearing bit.

TIME_STAMP_EN (Address 0x0A)

When TIME_STAMP_EN bit is set to 1, the 19 bits time stamp gets pushed to the FIFO along with its Tag for every 8 samples. This timestamp is useful for aligning data from two devices after the host reads the FIFOs of those devices. When TIME_STAMP_EN bit is set to 0, the sample counter is not pushed to FIFO.

Pseudo-Code Example of Initializing the Optical AFE

The following pseudo-code shows an example of configuring MAX86140/MAX86141 for a SpO_2 applications, where LED1 and LED2 are IR and red LED, respectively.

```
DEVICE OPEN
START;
                                        // AFE Initialization
WRITE RESET[0] to 0x1;                  // Soft Reset (Register 0x0D[0])
DELAY 1ms;
WRITE SHDN[0] to 0x1;                   // Shutdown (Register 0x0D[1])
READ  Interrupt_Status_1;               // Clear Interrupt (Register 0x00)
READ  Interrupt_Status_2;               // Clear Interrupt (Register 0x01)
WRITE PPG_TINT[1:0] to 0x3;             // Pulse Width = 123.8ms (Register 0x11[1:0])
WRITE PPG1_ADC_RGE1:0] to 0x2;          // ADC Range = 16μA (Register 0x11[3:2])
WRITE PPG2_ADC_RGE1:0] to 0x2;          // ADC Range = 16μA (Register 0x11[3:2])
                                        // For MAX86141 when used in Dual Channel only
WRITE SMP_AVE[2:0] to 0x0;              // Sample Averaging = 1 (Register 0x12[2:0])
WRITE PPG_SR[4:0] to 0x00;              // Sample Rate = 25sps (Register 0x12[7:3])
WRITE LED_SETLNG[1:0] to 0x3;           // LED Settling Time = 12ms  (Register 0x13[7:6])
WRITE PD_BIAS1[2:0] to 0x01;            // PD 1 Biasing for Cpd = 0~65pF (Register 0x15[2:0])
WRITE PD_BIAS2[2:0] to 0x01;            // PD 1 Biasing for Cpd = 0~65pF (Register 0x15[2:0])
                                        // For MAX86141 when used in Dual Channel only
WRITE LED1_RGE[1:0] to 0x3;             // LED Driver 1 Range = 124mA (Register 0x15[2:0])
WRITE LED2_RGE[1:0] to 0x3;             // LED Driver 2 Range = 124mA (Register 0x15[2:0])
WRITE LED1_DRV[1:0] to 0x20;            // LED 1 Drive Current = 15.36mA (Register 0x23[7:0])
WRITE LED2_DRV[1:0] to 0x20;            // LED 2 Drive Current = 15.36mA (Register 0x24[7:0])
WRITE LP_Mode[0] to 0x1;                // Low Power mode enabled
                                        // FIFO Configuration
WRITE FIFO_A_FULL[6:0] to 0xF;          // FIFO INT triggered condition (Register 0x09[6:0])
WRITE FIFO_RO to 0x1;                   // FIFO Roll Over enabled (Register 0x0A[1])
WRITE A_FULL_EN to 0x1;                 // FIFO_A_FULL interrupt enabled (Register 0x02[7])
WRITE LEDC1[3:0] to 0x1;                // LED1 exposure configured in time slot 1
WRITE LEDC2[3:0] to 0x2;                // LED2 exposure configured in time slot 1
WRITE LEDC3[3:0] to 0x0;
WRITE LEDC4[3:0] to 0x0;
WRITE LEDC5[3:0] to 0x0;
WRITE LEDC6[3:0] to 0x0;
WRITE SHDN[0] to 0x0;                   // Start Sampling STOP;
```

Pseudo-Code for Interrupt Handling with FIFO_A_FULL

The following pseudo-code shows an example on handling the Interrupt when using A_FULL Interrupt.

```
Interrupt handlervoid irqHandler(void)
     {
       uint8_t intStatus;
       //Read Status
       ReadReg(0x00, &intStatus);

      if ( intStatus& 0x80 ) { //A FULL RDY
      device_data_read(); //Data Read Routine
      }
```

Pseudo-Code Example of Reading Data from FIFO

Example pseudo-code for reading data from FIFO when using single photodiode channel and two LED channels.

```
void device_data_read(void) {
    uint8_t sampleCnt;
    uint8_t regVal;
    uint8_t dataBuf[128*2*3];      //128 FIFO samples, 2 channel, 3 byte/channel

    int led1[32];
    int led2[32];

    ReadReg(0x07, &sampleCnt);

    //Read FIFO
    ReadFifo(dataBuf, sampleCnt * 3);
    int i = 0;
    for ( i = 0; i < sampleCnt; i++ ) {
        led1[i] = ((dataBuf[i*6+0] << 16 ) | (dataBuf[i*6+1] << 8) | (dataBuf[i*6+2])) &
0x7ffff;
        led2[i] = ((dataBuf[i*6+3] << 16 ) | (dataBuf[i*6+4] << 8) | (dataBuf[i*6+5])) &
0x7ffff;
    }
   }
```

Example pseudo-code for reading data from FIFO when using dual photodiode channels and two LED channels.

```
void device_data_read(void) {
    uint8_t sampleCnt;
    uint8_t regVal;
    uint8_t dataBuf[128*2*2*3];     //128 FIFO samples, 2 channel, 2 PD, 3 byte/channel


    int led1A[32];
    int led1B[32];
    int led2A[32];
    int led2B[32];

    ReadReg(0x07, &sampleCnt);

    //Read FIFO
    ReadFifo(dataBuf, sampleCnt * 3);
    int i = 0;
    for ( i = 0; i < sampleCnt; i++ ) {
        led1A[i] = ((dataBuf[i*12+0] << 16 ) | (dataBuf[i*12+1] << 8)  | (dataBuf[i*12+2])) &
0x7ffff;    // LED1, PD1
        led1B[i] = ((dataBuf[i*12+3] << 16 ) | (dataBuf[i*12+4] << 8)  | (dataBuf[i*12+5])) &
0x7ffff;    // LED1, PD2
        led2A[i] = ((dataBuf[i*12+6] << 16 ) | (dataBuf[i*12+7] << 8)  | (dataBuf[i*12+8])) &
0x7ffff;    // LED2, PD1
        led2B[i] = ((dataBuf[i*12+9] << 16 ) | (dataBuf[i*12+10] << 8) | (dataBuf[i*12+11]))
& 0x7ffff;   // LED2, PD2
    }
   }
```

Optical Timing

The MAX86140/MAX86141 optical controller is capable of being configured to make a variety of measurements. Each LED exposure is ambient light compensated before the ADC conversion.

The controller can be configured to pulse one, two or three LED drivers sequentially so as to make measurements at multiple wavelengths as is done in a pulse oximetry measurements or simultaneously to drive multiple LEDs such as is done with heart rate measurements on the wrist.

The controller is also configurable to measure direct ambient level for every exposure sample. The direct ambient measurement can be used to adjust the LED drive level to compensate for increased noise levels when high interfering ambient signals are present.

The following optical timing diagrams illustrate several possible measurement configurations.

One LED Pulsing with No Direct Ambient Sampling

The optical timing diagram below represents just LED1 pulsing during the exposure time with no direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with a single green LED. In this mode a single optical sampled value will appear successively in the FIFO.

One LED Pulsing with Direct Ambient Sampling

The optical timing diagram below represents just LED1 pulsing during the exposure time with direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with a single, green LED. In this mode a single optical sampled value followed by the ambient sampled value will appear successively in the FIFO.

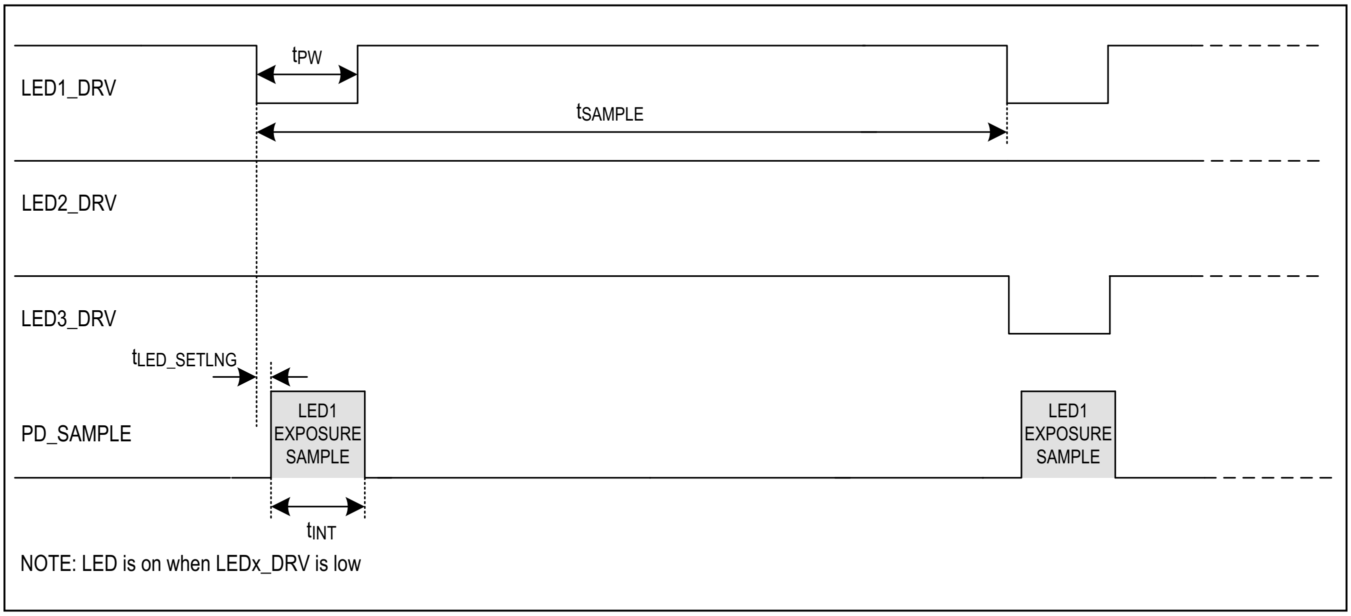


Figure 1. Timing for LED1 Pulsing with No Direct Ambient Sampling

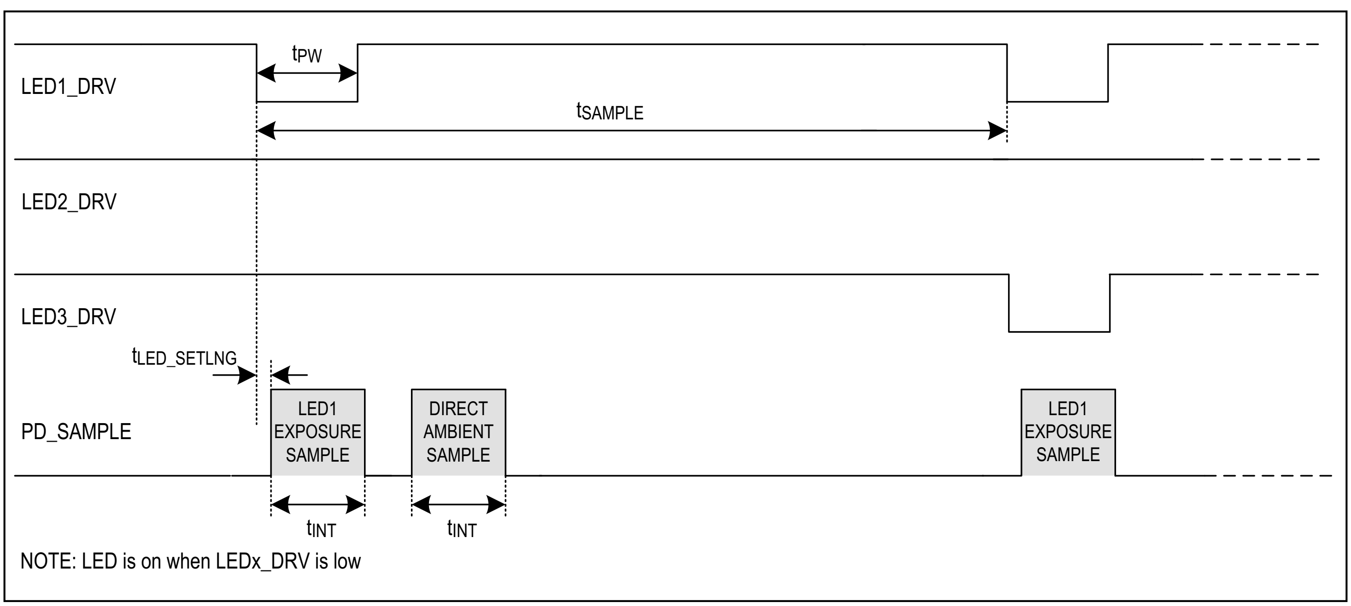


Figure 2. Timing for LED1 Pulsing with Direct Ambient Sampling

Two LEDs Pulse Simultaneously with Direct Ambient Sampling

The optical timing diagram below represents both LED1 and LED2 pulsing simultaneously with direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with two green LEDs. In this mode a single optical sampled value followed by the ambient sampled value will appear in successive the FIFO locations. The direct ambient sampling is typically used to compensate the LED drive levels as the optical noise level can be elevated from ambient shot noise.

All LED Pulsing Simultaneously with Direct Ambient Sampling

The optical timing diagram below represents all three LEDs pulsing simultaneously with direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with three green LEDs. In this mode, a single optical sampled value, followed by the ambient sampled value, will appear in successive the FIFO locations. The direct ambient sampling is typically used to compensate the LED drive levels as the optical noise level can be elevated from ambient shot noise.

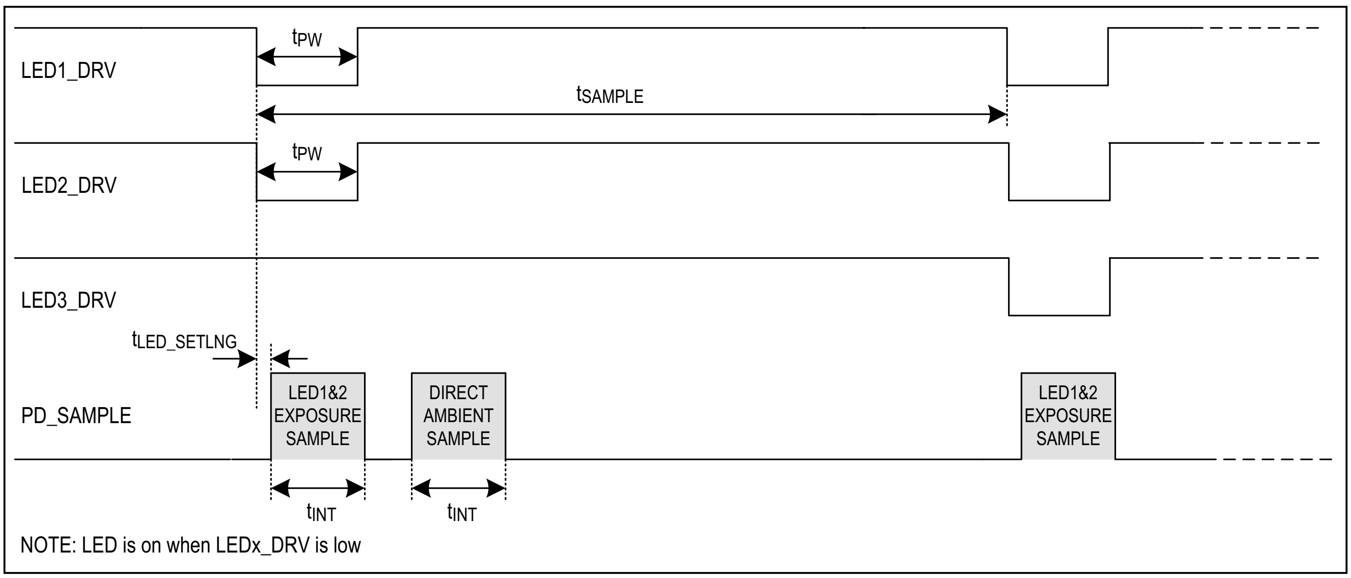


Figure 3. Timing for LED1 and LED2 Pulsing Simultaneously with Direct Ambient Sampling

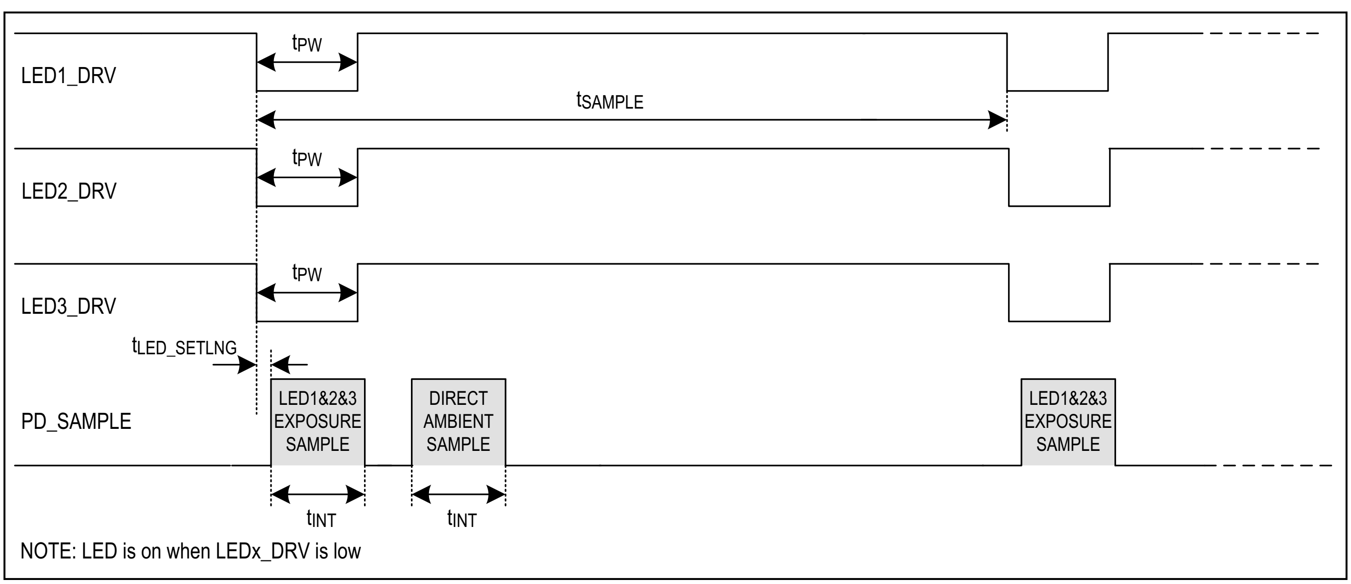


Figure 4. Timing for LED1, LED2, and LED3 Pulsing Simultaneously with Direct Ambient Sampling

Two LEDs Pulse Sequentially with Direct Ambient Sampling

The timing diagram below illustrates the optical timing when both LED1 and LED2 are enabled to pulse sequentially and direct ambient sampling is also enabled. This timing mode would be used when SpO_2 is being measured with IR and red LEDs. The optical sampled value for each LED will appear successively, followed by the direct ambient sampled value in the FIFO. when SpO_2 is being measured with IR and red LEDs. The optical sampled value for each LED will appear successively, followed by the direct ambient sampled value in the FIFO.

All LEDs Pulse Sequential with Direct Ambient Sampling

The optical timing diagram below illustrates the three LEDs pulsing sequentially, followed by a direct ambient sample. This timing mode would be used when heart rate on a green LED is combined with and SpO_2 measurement using IR and red LEDs.

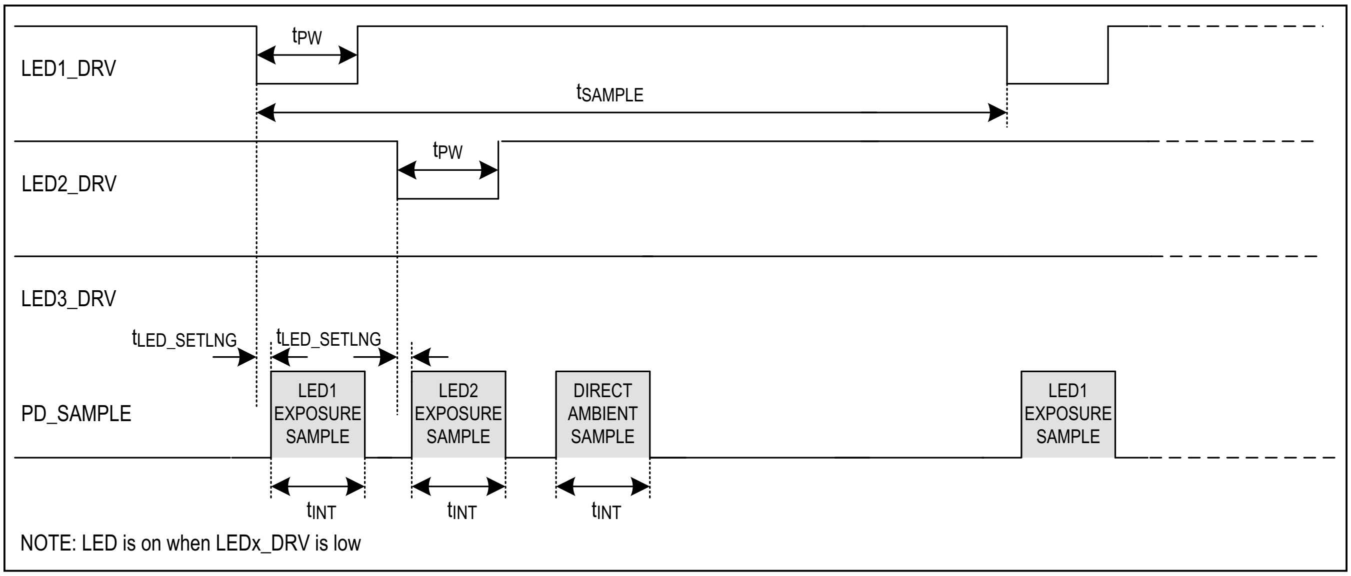


Figure 5. Timing for LED1 and LED2 Pulsing Sequentially with Direct Ambient Sampling

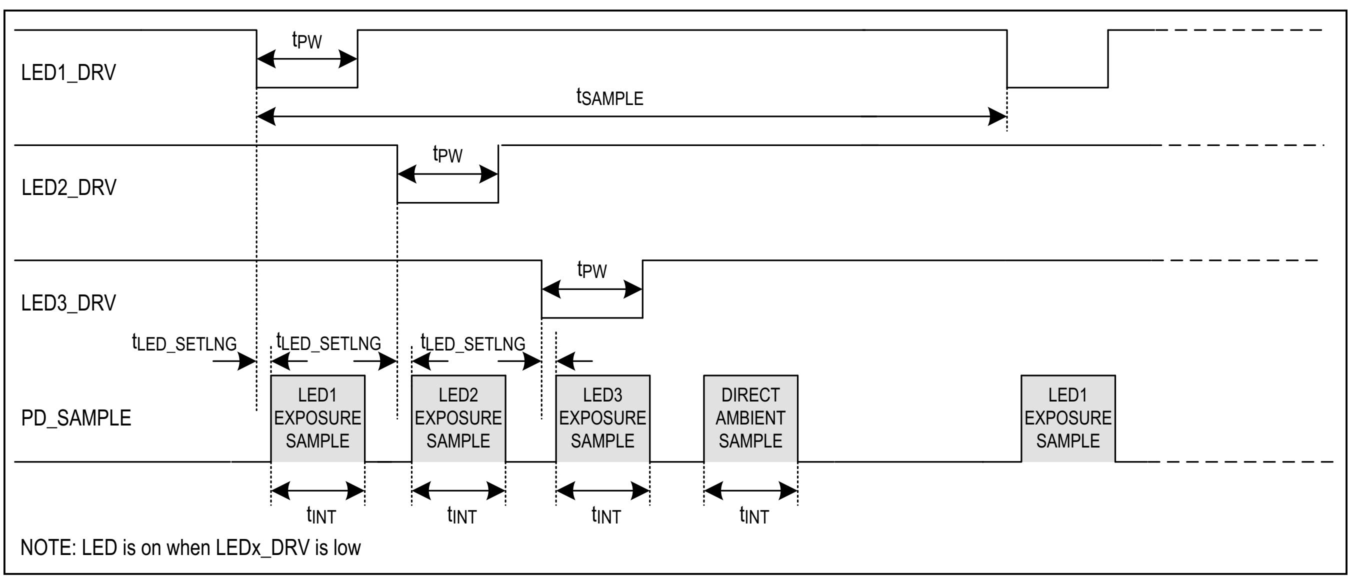


Figure 6. Timing for LED1, LED2, and LED3 Pulsing Sequentially with Direct Ambient Sampling