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MAX86160

Integrated Heart-Rate Sensor for In-Ear Applications

General Description

The MAX86160 is an integrated heart rate monitor sensor module designed for the demanding requirements of mobile, wearable, and hearable devices. It includes internal LEDs, photo-detector, and low-noise electronics with high-dynamic-range ambient light rejection. This integrated product is a complete system solution, and comes with plug-and-play software and robust algorithms to give meaningful outputs to the user with minimal additional design effort. The MAX86160 sensor module takes care of the most challenging parts of the design for fast time-to-market in mobile and wearable devices.

The MAX86160 operates on a 1.8V supply voltage, with a separate 3.3V/5.0V power supply for the internal LEDs. Communication to and from the module occurs entirely through a standard I²C-compatible interface. The module can be shut down through software with near zero standby current, allowing the power rails to remain powered at all times.

Benefits and Features

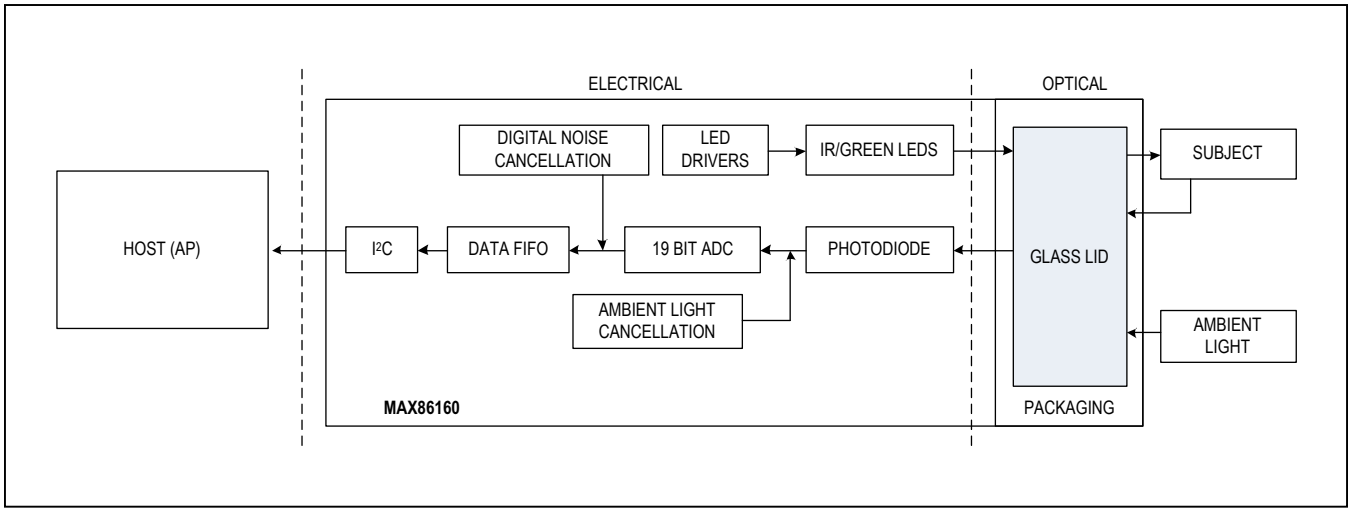
- Miniature 4.3mm x 2.8mm x 1.45mm 18-pin Optical Module
  - Optical-Grade, Robust Glass Eliminates Customer Cover Glass
- High In-Band 13Hz Signal-to-Noise Ratio (SNR) Reflective Heart Rate Monitor and Medical-Grade Pulse Oximeter
- Ultra Low-Power Operation for Mobile Device
  - Zero-Power Shutdown Current (0.7µA, typ)
- -40°C to +85°C Operating Temperature Range

Applications

- Wearable and Hearable Devices
- Smartphones/Tablets
- Disposable Patch Sensors
- Fitness Assistant Devices

Ordering Information **appears at end of data sheet.**

Simplified Block Diagram



19-8601; Rev 0; 9/16

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Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +2.2V
PGND to GND .....-0.3V to +0.3V
LED_DRVx, VLED to PGND .....-0.3V to +6.0V
V_{REF} to GND.....-0.3V to +2.2V
Output Short-Circuit Duration .....Continuous
Continuous Input Current Into Any Pin
(Except LED_DRVx Pins).....±20mA

Continuous Power Dissipation 440mW
SDA, SCL, INTB, GPIO to GND .....-0.3V to +6.0V
OESIP (derate 5.5mW/°C above +70°C) ..... -40°C to +85°C
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +105°C
Soldering Temperature (Reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

18-Lead OESIP

Package Code	F182A4+1
Outline Number	**21-100099**
Land Pattern Number	**90-100030**
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	174°C/W (Note 1)
Junction-to-Case Thermal Resistance (θ_{JC})	150°C/W (Note 1)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

((V_{DD} = 1.8V, V_{LED} = 3.3V(IR), V_{LED} = 5.0V (GREEN), GND = PGND = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Power Supply Voltage	V_{DD}		1.7	1.8	2.0	V
LED Supply Voltage for IR	V_{LED}		3.1	3.3	5.5	V
LED Supply Voltage for Green	V_{LED}		4.0	5.0	5.5	V
V_{DD} Supply Current	I_{DD}	Heart Rate Mode; PW = 50µs; SPS = 100; LED Driver = 0mA		400	750	µA
		Heart Rate Mode; PW = 50µs; SPS = 10; LED Driver = 0mA		400	750	
V_{DD} Current in Shutdown		T_A= 25°C		0.5	12	µA
V_{LED} Current in Shutdown		T_A = 25°C		0	1	µA
Internal Voltage Reference (Note 3)	V_{REF}	Bypass to GND with 1µF	1.192	1.204	1.215	V
PULSE OXIMETRY/HEART RATE SENSOR CHARACTERISTICS						
ADC Resolution				19		bits
IR ADC Count	IR_C	Proprietary ATE Setup. IR_PA = 0x13, PW = 50µS, SPS = 1000, T_A = +25°C	121,072	131,072	141,072	Counts
Green ADC Count	GREEN_C	Proprietary ATE Setup. GREEN_PA = 0x80, PW = 50µS, SPS = 1000, T_A = +25°C	111,072	131,072	151,072	Counts
Dark Current Counts	DC_C	ALC = ON, IR_PA = 0x00, PW = 50µS, SPS = 1000, PPG_ADC_RGE<1:0> = 8µA, T_A = +25°C		0.0001	0.02	% of FS
IR/GREEN ADC Count - PSRR (VDD)	PSRR_VDD	Propriety ATE setup, 1.7V < V_{DD} < 2.0V, IR_PA = 0x12, GREEN_PA = 0x80, PW = 50µS, SPS = 1000		0.5	1	% of FS
IR/GREEN ADC Count - PSRR (LED Driver Outputs)	PSRR_LED	Propriety ATE setup, 3.1V < V_{LED} < 5V(IR), 4V < V_{LED} < 5.5V (GREEN), IR_PA = 0x12, GREEN_PA = 0x80, PW = 50µS, SPS = 1000		0.05	0.5	% of FS
ADC Clock Frequency	CLK		9.649	9.846	10.043	MHz
IR LED CHARACTERISTICS (Note 5)						
LED Peak Wavelength	λ_P	I_{LED} = 20mA, T_A = +25°C	870	880	900	nm
GREEN LED CHARACTERISTICS (Note 5)						
LED Peak Wavelength	λ_P	I_{LED} = 20mA, T_A = +25°C	520	527	540	nm

Electrical Characteristics (continued)

((V_{DD} = 1.8V, V_{LED} = 3.3V(IR), V_{LED} = 5.0V (GREEN), GND = PGND = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED DRIVERS						
LED Current Resolution				8		bits
LED Drive Current Range (Note 4)	I_{LED}	V_{LED} = 5.0V (for GREEN), V_{LED} = 3.3V (for IR ONLY), LEDx_PA = 0xFF, LEDx_RGE[1:0] = 00		50		mA
		V_{LED} = 5.0V (for GREEN), V_{LED} = 3.3V (for IR ONLY), LEDx_PA = 0xFF, LEDx_RGE[1:0] = 01		100		
		V_{LED} = 5.0V (for GREEN), V_{LED} = 3.3V (for IR ONLY), LEDx_PA = 0xFF, LEDx_RGE[1:0] = 10		150		
		VLED = 5.0V (for GREEN), V_{LED} = 3.3V (for IR ONLY), LEDx_PA = 0xFF, LEDx_RGE[1:0] = 11		200		
DIGITAL CHARACTERISTICS (SDA, SCL, INT)						
Output Low Voltage SDA, INTB	V_{OL}	I_{SINK} = 6mA			0.4	V
I^2C Input Voltage Low	V_{IL_I2C}	SDA, SCL			0.4	V
I^2C Input Voltage High	V_{IH_I2C}	SDA, SCL	1.4			V
Input Hysteresis (Note 5)	V_{HYS}	SDA, SCL		200		mV
Input Capacitance (Note 5)	C_{IN}	SDA, SCL		10		pF
Input Leakage Current	I_{IN}	V_{IN} = 0V, T_A = +25°C (SDA, SCL)		0.01	1	µA
		V_{IN} = V_{DD}, T_A = +25°C (SDA, SCL)		0.01	1	
I^2C TIMING CHARACTERISTICS (SDA, SCL) (Note 5, Figure 1)						
I^2C Write Address				BC		Hex
I^2C Read Address				BD		Hex
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns

Electrical Characteristics (continued)

((V_{DD} = 1.8V, V_{LED} = 3.3V(IR), V_{LED} = 5.0V (GREEN), GND = PGND = 0V, T_A = +25°C, min/max are from T_A = -40°C to +85°C, unless otherwise noted.) (Note 2))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
Bus Capacitance	C_B				400	pF
SDA and SCL Receiving Rise Time	t_R		20 + $0.1C_B$		300	ns
SDA and SCL Receiving Fall Time	t_F		20 + $0.1C_B$		300	ns
SDA Transmitting Fall Time	t_F		20 + $0.1C_B$		300	ns

Note 2: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by Maxim Integrated's bench or proprietary automated test equipment (ATE) characterization.

Note 3: Internal Reference Voltage only.

Note 4: Whenever Green LED is used, V_{LED} must be 4.0V or above. For LED Current range more than 100mA (LEDx_RGE = 2'b1X), V_{LED} must be 4.5V or above.

Note 5: For design guidance only. Not production tested.

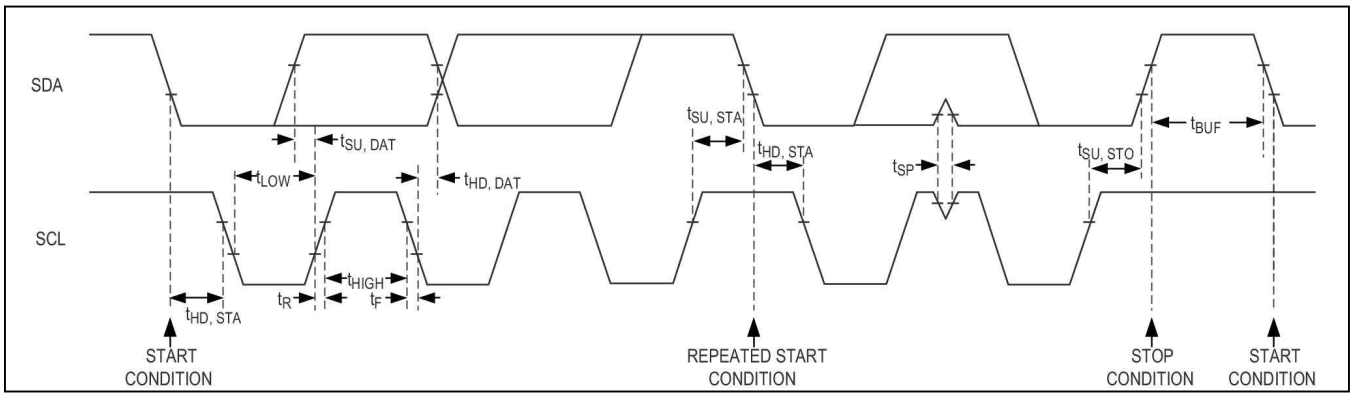
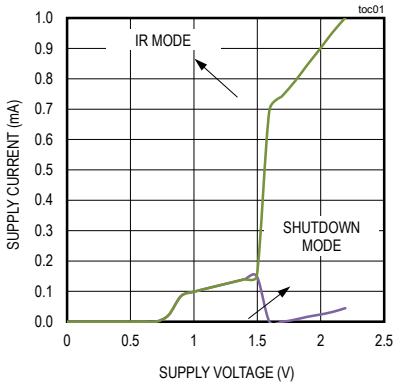


Figure 1. I²C-Compatible Interface Timing Diagram

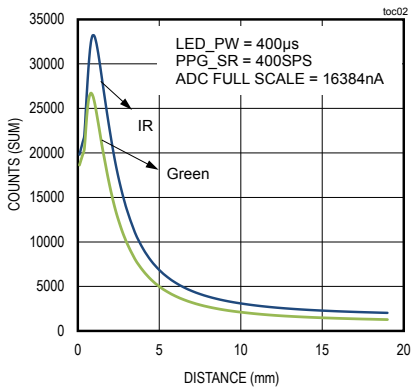
Typical Operating Characteristics

(V_{DD} = 1.8V, V_{LED} = 3.3V(IR), V_{LED} = 5.0V (GREEN), GND = PGND = 0V, T_A = +25°C, unless otherwise noted.)(T_A = +25°C, unless otherwise noted.)

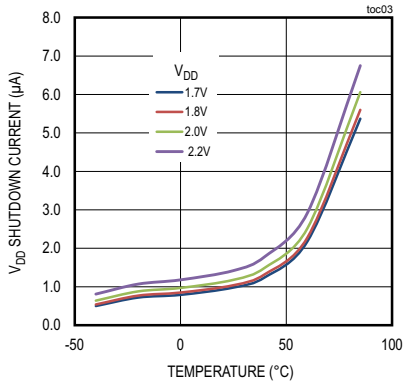
V_{DD} SUPPLY CURRENT vs. SUPPLY VOLTAGE



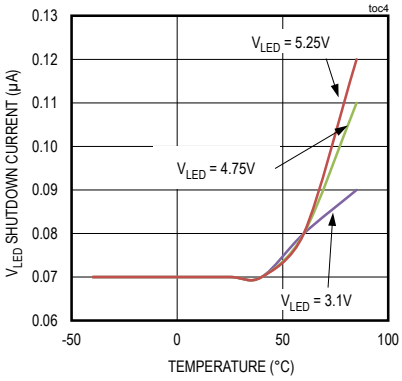
DC COUNTS vs. DISTANCE FOR COVER GLASS



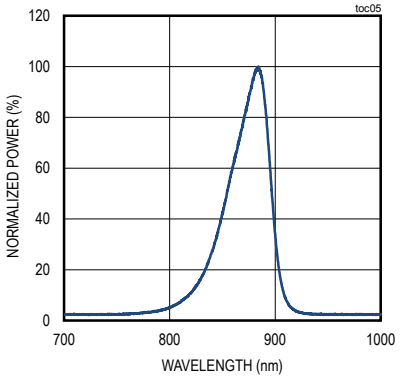
V_{DD} SHUTDOWN CURRENT vs. TEMPERATURE



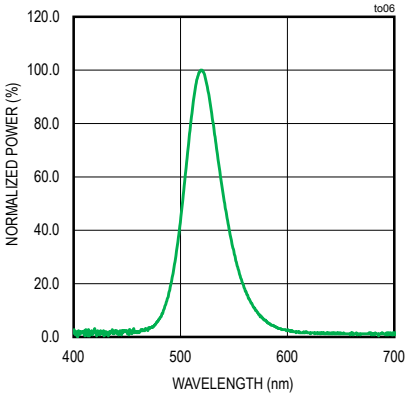
V_{LED} SHUTDOWN CURRENT vs. TEMPERATURE



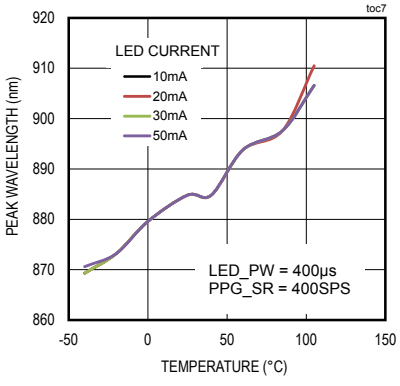
IR LED SPECTRA AT 25°C



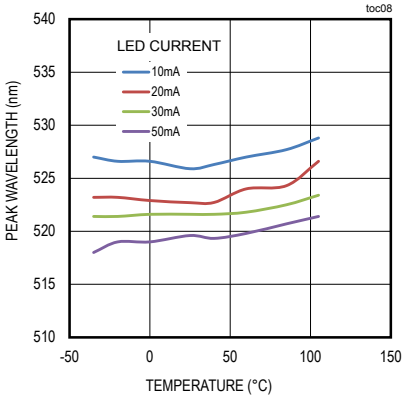
GREEN LED SPECTRA AT 25°C



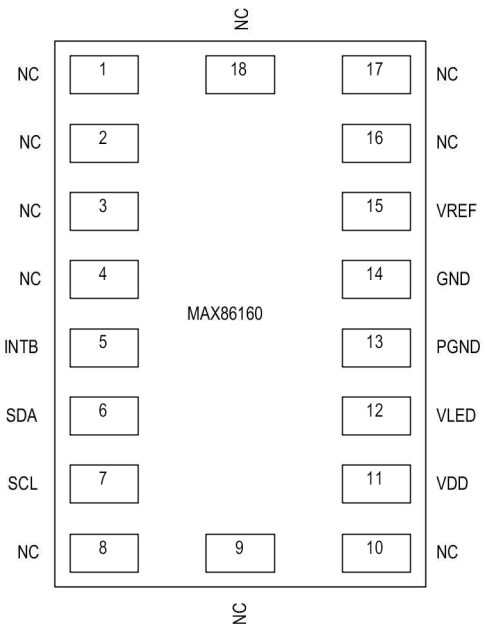
IR LED PEAK WAVELENGTH vs. TEMPERATURE



GREEN LED PEAK WAVELENGTH vs. TEMPERATURE



Pin Configurations

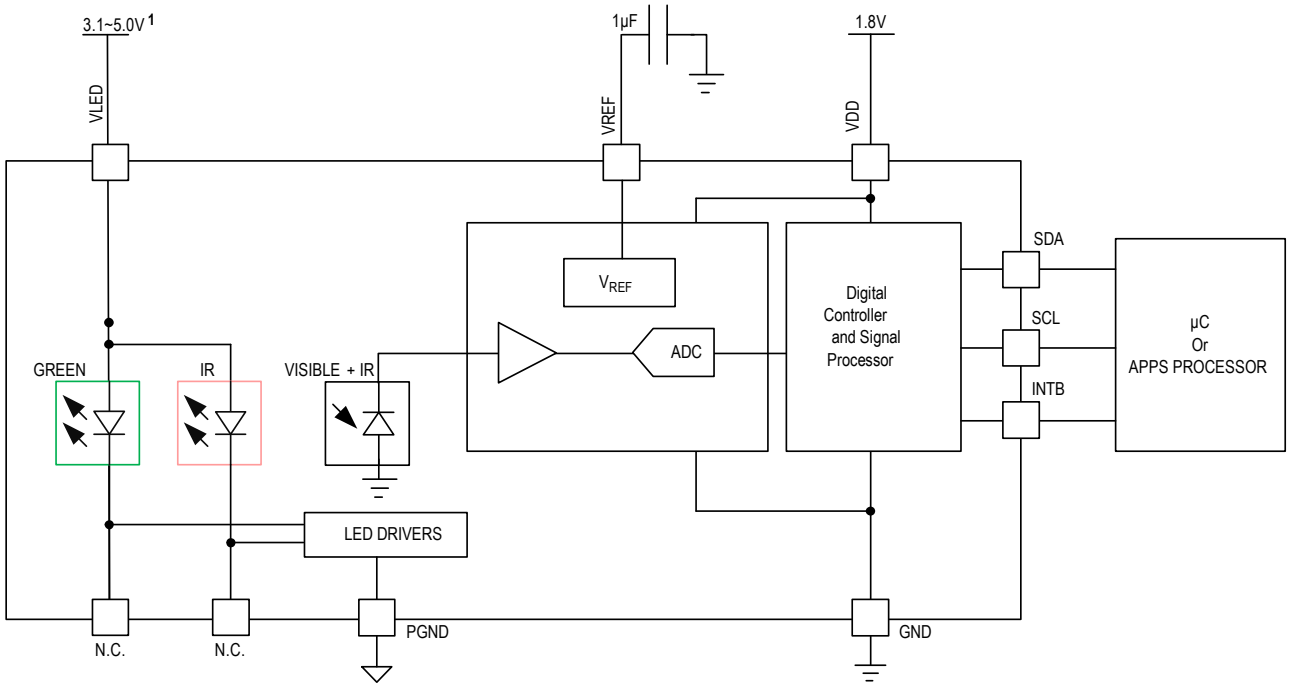


Pin Description

PIN	NAME	FUNCTION
POWER		
11	V_{DD}	Analog Supply. Connect to externally-regulated supply. Bypass to GND
12	V_{LED}	LED Power Supply Input. Connect to external battery supply. Bypass to PGND.
13	PGND	LED Power Return. Connect to GND.
14	GND	Analog Power Return. Connect to GND.
CONTROL INTERFACE		
5	INTB	Open-Drain Interrupt
6	SDA	I^2C Data
7	SCL	I^2C Clock
REFERENCE		
15	VREF	Internal Reference Decoupling Point. Bypass to GND.
N.C.		
1	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
2	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.

PIN MAX86160	NAME	FUNCTION
3	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
4	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
8	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
9	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
10	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
16	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
17	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.
18	N.C.	No Connection. Connect to unconnected PCB pad for mechanical stability. N.C. pins should not be connected to any signal, power, or ground pins.

Functional Diagram



Note 1: If Green LED is used, VLED must be 4.0V or above . For LED Current range more than 100mA (LEDx_RGE = 2'b1X), VLED must be 4.5V or above .

Detailed Description

The MAX86160 is a heart rate sensor system solution module designed for the demanding requirements of mobile and wearable devices. The MAX86160 maintains a very small total solution size without sacrificing optical or electrical performance. Minimal external hardware components are necessary for integration into a mobile device.The device is fully adjustable through software registers, and the digital output data is stored in a 32-deep FIFO within the device. The FIFO allows the device to be connected to a micro-controller or processor on a shared bus, where the data is not being read continuously from the MAX86160's registers.

HRM Subsystem

The HRM subsystem in the MAX86160 is composed of ambient light cancellation (ALC), a continuous-time sigma delta ADC, and proprietary discrete time filter. The ALC has an internal DAC to cancel ambient light and increase the effective dynamic range. The internal ADC is a continuous time oversampling sigma delta converter with 19-bit resolution. The ADC output data rate can be programmed from10sps (samples per second) to 3200sps. The MAX86160 includes a proprietary discrete time filter to reject 50Hz/60Hz interference and slow moving residual ambient noise.

LED Driver

The MAX86160 integrates green and infrared LED drivers to modulate LED pulses for HR measurements. The LED current can be programmed from 0mA to 200mA with proper V_{LED} supply voltage. The LED pulse width can be programmed from 50µs to 400µs to allow the algorithm to optimize HR accuracy and power consumption based on use cases.

Proximity Function

The MAX86160 includes a proximity function to save power and reduce visible light emission when the user's finger is not on the sensor. Proximity function is enabled by setting PROX_INT_EN to 1. When the HR function is initiated, the IR LED is turned on in proximity mode with a drive current set by the PILOT_PA register. When an object is detected by exceeding the IR ADC count threshold (set in the PROX_INT_ THRESH register), PROX_INT interrupt is asserted and the part transitions automatically to the normal HR Mode. To reenter PROX mode, a new HR reading must be initiated (even if the value is the same). The proximity function can be disabled by resetting PROX_INT_EN to 0. In that case, when the HR function is initiated in the FIFO Data Control registers, the HR mode begins immediately.

Register Map

ADDRESS	NAME	MSB							LSB
STATUS REGISTERS									
0x00	Interrupt Status 1[7:0]	A_FULL_	PPG_ RDY_	ALC_ OVF_	PROX_ INT_	–	–	–	PWR_ RDY_
0x01	Interrupt Status 2[7:0]	VDD_ OOR_	–	–	–	–	–	–	–
0x02	Interrupt Enable 1[7:0]	A_FULL_ EN_	PPG_ RDY_ EN_	ALC_ OVF_ EN_	PROX_ INT_EN_	–	–	–	–
0x03	Interrupt Enable 2[7:0]	VDD_ OOR_ EN_	–	–	–	–	–	–	–

Register Map (continued)

ADDRESS	NAME	MSB							LSB
FIFO REGISTERS									
0x04	FIFO Write Pointer[7:0]	–	–	–	FIFO_WR_PTR_[4:0]				
0x05	Overflow Counter[7:0]	–	–	–	OVF_COUNTER_[4:0]				
0x06	FIFO Read Pointer[7:0]	–	–	–	FIFO_RD_PTR_[4:0]				
0x07	FIFO Data Register[7:0]	FIFO_DATA_[7:0]							
0x08	FIFO Configuration[7:0]	–	A_FULL_CLR_	A_FULL_TYPE_	FIFO_ROLLS_ON_FULL_	FIFO_A_FULL_[3:0]			
FIFO DATA CONTROL									
0x09	FIFO Data Control Register 1[7:0]	FD2_[3:0]				FD1_[3:0]			
0x0A	FIFO Data Control Register 2[7:0]	FD4_[3:0]				FD3_[3:0]			
–									
SYSTEM CONTROL									
0x0D	System Control [7:0]	–	–	–	–	–	FIFO_EN_	SHDN_	RESET_
PPG Configuration									
0x0E	PPG Configuration 1 [7:0]	PPG_ADC_RGE_[1:0]		PPG_SR_[3:0]				PPG_LED_PW_[1:0]	
0x0F	PPG Configuration 2 [7:0]	–	–	–	–	–	SMP_AVE_[2:0]		
0x10	Prox Interrupt Threshold [7:0]	PROX_INT_THRESH_[7:0]							
LED Pulse Amplitude									
0x11	LED1 PA[7:0]	LED1_PA_[7:0]							
–									
0x13	LED3 PA[7:0]	LED3_PA_[7:0]							
0x14	LED Range[7:0]	–	–	LED3_RGE_[1:0]		–	–	LED1_RGE_[1:0]	
0x15	LED PILOT PA[7:0]	PILOT_PA_[7:0]							
–									
Part ID									
0xFF	Part ID[7:0]	PART_ID_[7:0]							

Interrupt Status 1 (0x00)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL	PPG_RDY	ALC_OVF	PROX_INT	–	–	–	PWR_RDY
Reset	0x0	0x0	0x0	0x0	–	–	–	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	–	–	–	Read Only

A_FULL: FIFO Almost Full Flag

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the FIFO buffer will overflow the threshold set by FIFO_A_FULL<3:0> on the next sample. This bit is cleared when the Interrupt Status 1 Register is read. It is also cleared when FIFO_DATA register is read, if A_FULL_CLR = 1

PPG_RDY: New PPG FIFO Data Ready

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	In HR modes, this interrupt triggers when there is a new sample in the data FIFO. The interrupt is cleared by reading the Interrupt Status 1 register (0x00), or by reading the FIFO_DATA register.

ALC_OVF: Ambient Light Cancellation Overflow

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	This interrupt triggers when the ambient light cancellation function of the HR photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC. The interrupt is cleared by reading the Interrupt Status 1 register (0x00).

PROX_INT: Proximity interrupt

If PROX_INT is masked then the prox mode is disabled and the select PPG begins immediately. This bit is cleared when the Interrupt Status 1 Register is read.

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that the proximity threshold has been crossed when in proximity mode.

PWR_RDY: Power Ready Flag

VALUE	ENUMERATION	DECODE
0	OFF	Normal Operation
1	ON	Indicates that VBATT went below the UVLO threshold. This bit is not triggered by a soft reset. This bit is cleared when Interrupt Status 1 Register is read.

Interrupt Status 2 (0x01)

BIT	7	6	5	4	3	2	1	0
Field	VDD_OOR	–	–	–	–	–	–	–
Reset	0x0	–	–	–	–	–	–	–
Access Type	Read Only	–	–	–	–	–	–	–

VDD_OOR: VDD Out-of-Range flag

This flag checks if the VDD_ANA supply voltage is outside supported range.

VALUE	ENUMERATION	DECODE
0	OFF	VDD_ANA between range.
1	ON	Indicated that VDD_ANA is greater than 2.05V or less than 1.65V. This bit is automatically cleared when the Interrupt Status 2 register is read. The detection circuitry has a 10ms delay time, and will continue to trigger as long as the VDD_ANA is out of range.

Interrupt Enable 1 (0x02)

BIT	7	6	5	4	3	2	1	0
Field	A_FULL_EN	PPG_RDY_EN	ALC_OVF_EN	PROX_INT_EN	–	–	–	–
Reset	0x0	0x0	0x0	0x0	–	–	–	–
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	–	–	–	–

A_FULL_EN: FIFO Almost Full Flag enable

VALUE	ENUMERATION	DECODE
0	OFF	A_FULL interrupt is disabled
1	ON	A_FULL interrupt is enabled

PPG_RDY_EN: New PPG FIFO Data Ready Interrupt enable

VALUE	ENUMERATION	DECODE
0	OFF	PPG_RDY interrupt is disabled
1	ON	PPG_RDY interrupt is enabled.

ALC_OVF_EN: Ambient Light Cancellation (ALC) Overflow Interrupt enable

The ALC_OVF flag will be triggered when the HRM photodiode has reached it’s maximum limit due to overflow. At this point, the ADC output will be affected by the ambient light.

VALUE	ENUMERATION	DECODE
0	OFF	ALC_OVF interrupt is disabled
1	ON	ALC_OVF interrupt is enabled

PROX_INT_EN: Proximity Interrupt enable

When the HR function is initiated, the IR LED is turned on in proximity mode with a drive current set by the PILOT_PA register. When an object is detected by exceeding the IR ADC count threshold (set in the PROX_INT_ THRESH register), PROX_INT interrupt is asserted and the part transitions automatically to the normal HR mode.

VALUE	ENUMERATION	DECODE
0	OFF	PROX_INT interrupt is disabled
1	ON	PROX_INT interrupt is enabled

Interrupt Enable 2 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	VDD_OOR_EN	–	–	–	–	–	–	–
Reset	0x0	–	–	–	–	–	–	–
Access Type	Write, Read	–	–	–	–	–	–	–

VDD_OOR_EN: VDD Out-of-Range Indicator enable

VALUE	ENUMERATION	DECODE
0	OFF	Disables the VDD_OVR interrupt
1	ON	Enables the VDD_OVR interrupt

FIFO Write Pointer (0x04)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FIFO_WR_PTR[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

FIFO_WR_PTR: FIFO Write Pointer

This points to the location where the next sample will be written. This pointer advances for each sample pushed on to the FIFO.

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	OVF_COUNTER[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Read Only				

OVF_COUNTER: FIFO Overflow Counter

When FIFO is full any new samples will result in new or old samples getting lost depending on FIFO_ROLLS_ON_FULL. OVF_COUNTER counts the number of samples lost. It saturates at 0x1F.

FIFO Read Pointer (0x06)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FIFO_RD_PTR[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

FIFO_RD_PTR: FIFO Read Pointer

The FIFO Read Pointer points to the location from where the processor gets the next sample from the FIFO through the I2C interface. This advances each time a sample is popped from the FIFO. The processor may also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO.

FIFO Data Register (0x07)

BIT	7	6	5	4	3	2	1	0
Field	FIFO_DATA[7:0]							
Reset	0x00							
Access Type	Write, Read							

FIFO_DATA: FIFO Data Register

This is a read-only register and is used to get data from the FIFO. See *FIFO Description* for more details.

FIFO Configuration (0x08)

BIT	7	6	5	4	3	2	1	0
Field	–	A_FULL_CLR	A_FULL_TYPE	FIFO_ROLLS_ON_FULL	FIFO_A_FULL[3:0]			
Reset	–	0x0	0x0	0x0	0xF			
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read			

A_FULL_CLR: FIFO Almost Full Interrupt Options

This defines whether the A-FULL interrupt should get cleared by FIFO_DATA register read.

VALUE	ENUMERATION	DECODE
0	RD_DATA_NOCLR	A_FULL interrupt does not get cleared by FIFO_DATA register read. It gets cleared by status register read.
1	RD_DATA_CLR	A_FULL interrupt gets cleared by FIFO_DATA register read or status register read.

A_FULL_TYPE: FIFO Almost Full Flag Options

This defines the behavior of the A_FULL interrupt.

VALUE	ENUMERATION	DECODE
0	AFULL_RPT	A_FULL interrupt gets asserted when the a_full condition is detected. It is cleared by status register read, but re-asserts for every sample if the a_full condition persists.
1	AFULL_ONCE	A_FULL interrupt gets asserted only when the a_full condition is detected. The interrupt gets cleared on status register read, and does not re-assert for every sample until a new a-full condition is detected.

FIFO_ROLLS_ON_FULL: FIFO Rolls on Full Options

This bit controls the behavior of the FIFO when the FIFO becomes completely filled with data.

- When the device is in PROX mode, the FIFO always rolls on full.
- Push to FIFO is enabled when FIFO is full if FIFO_ROLLS_ON_FULL = 1 and old samples are lost. Both FIFO_WR_PTR and FIFO_RD_PTR increment for each sample after the FIFO is full.
- Push to FIFO is disabled when FIFO is full if FIFO_ROLLS_ON_FULL = 0 and new samples are lost. FIFO_WR_PTR does not increment for each sample after the FIFO is full.

VALUE	ENUMERATION	DECODE
0	OFF	The FIFO stops on full.
1	ON	The FIFO automatically rolls over on full.

FIFO_A_FULL: FIFO Almost Full Value

These bits indicate how many new samples can be written to the FIFO before the interrupt is asserted. For example, if set to 0xF, the interrupt triggers when there is 17 empty space left (15 data samples), and so on.

FIFO_A_FULL<3:0>	FREE SPACE BEFORE INTERRUPT	# OF SAMPLES IN FIFO
0000	0	32
0001	1	31
0010	2	30
0011	3	29
----	----	----
1110	14	18
1111	15	17

FIFO Data Control Register 1 (0x09)

BIT	7	6	5	4	3	2	1	0
Field	FD2[3:0]				FD1[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

FD2: FIFO Data Time Slot 2

These bits set the data type for element 2 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3 and FD4 according to the table below. For restriction on data type sequences please see the FLEX FIFO document.

FD2<3:0>	DATA TYPE	FD2<3:0>	DATA TYPE	FD2<3:0>	DATA TYPE	FD2<3:0>	DATA TYPE
0000	Reserved	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	Reserved	1101	Reserved
0010	Reserved	0110	Reserved	1010	Reserved	1110	Reserved
0011	PPG_LED3	0111	Pilot LED3	1011	Reserved	1111	Reserved

FD1: FIFO Data Time Slot 1

These bits set the data type for element 1 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3, and FD4 according to the table below. For restriction on data type sequences please refer to the *FIFO Description* section.

FD1<3:0>	DATA TYPE	FD1<3:0>	DATA TYPE	FD1<3:0>	DATA TYPE	FD1<3:0>	DATA TYPE
0000	Reserved	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED 1	1001	Reserved	1101	Reserved
0010	Reserved	0110	Reserved	1010	Reserved	1110	Reserved
0011	PPG_LED3	0111	Pilot LED3	1011	Reserved	1111	Reserved

FIFO Data Control Register 2 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	FD4[3:0]				FD3[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

FD4: FIFO Data Time Slot 4

These bits set the data type for element 4 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3, and FD4 according to the table below. For restriction on data type sequences please see the FLEX FIFO document.

FD4<3:0>	DATA TYPE	FD4<3:0>	DATA TYPE	FD4<3:0>	DATA TYPE	FD4<3:0>	DATA TYPE
0000	Reserved	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	Reserved	1101	Reserved
0010	Reserved	0110	Reserved	1010	Reserved	1110	Reserved
0011	PPG_LED3	0111	Pilot LED3	1011	Reserved	1111	Reserved

FD3: FIFO Data Time Slot 3

These bits set the data type for element 3 of the FIFO.

The FIFO can hold up to 32 samples. Each sample can hold up to four elements and each element is 3 bytes wide. The data type that gets stored in the 3 bytes is configured by FD1, FD2, FD3, and FD4 according to the table below. For restriction on data type sequences please refer to the *FIFO Description* section.

FD3<3:0>	DATA TYPE	FD3<3:0>	DATA TYPE	FD3<3:0>	DATA TYPE	FD3<3:0>	DATA TYPE
0000	Reserved	0100	Reserved	1000	Reserved	1100	Reserved
0001	PPG_LED1	0101	Pilot LED1	1001	Reserved	1101	Reserved
0010	Reserved	0110	Reserved	1010	Reserved	1110	Reserved
0011	PPG_LED3	0111	Pilot LED3	1011	Reserved	1111	Reserved

System Control (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	FIFO_EN	SHDN	RESET
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

FIFO_EN: FIFO Enable

VALUE	ENUMERATION	DECODE
0	OFF	Push to FIFO is disabled, but the read and write pointers and the data in the FIFO are all held at their values before FIFO_EN is set to 0.
1	ON	The FIFO is enabled. When this bit is set the FIFO is flushed of all old data and the new samples start loading from pointer zero.

SHDN: Shutdown Control

The part can be put into a power-save mode by setting this bit to one. While in power-save mode, all registers retain their values, and write/read operations function as normal. All interrupts are cleared to zero in this mode.

VALUE	ENUMERATION	DECODE
0	OFF	The part is in normal operation. No action taken.
1	ON	The part can be put into a power-save mode by writing a ‘1’ to this bit. While in this mode all registers remain accessible and retain their data. ADC conversion data contained in the registers are previous values. Writeable registers also remain accessible in shutdown. All interrupts are cleared. In this mode the oscillator is shutdown and the part draws minimum current. If this bit is asserted during a active conversion then the conversion completes before the part shuts down.

RESET: Reset Control

When this bit is set, the part initiates a forced power-on-reset sequence. All configuration, threshold and data registers including distributed registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

VALUE	ENUMERATION	DECODE
0	OFF	The part is in normal operation. No action taken.
1	ON	The part initiates a forced power-on-reset sequence. All configuration, threshold and data registers including distributed registers are reset to their power-on-state. This bit then automatically becomes ‘0’ after the reset sequence is completed.

PPG Configuration 1 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	PPG_ADC_RGE[1:0]		PPG_SR[3:0]				PPG_LED_PW[1:0]	
Reset	0x0		0x0				0x0	
Access Type	Write, Read		Write, Read				Write, Read	

PPG_ADC_RGE: PPG ADC Range Control

These bits set the ADC range of the PPG sensor as shown in the table below.

PPG_ADC_RGE<1:0>	LSB [PA]	FULL SCALE [NA]
00	7.8125	4096
01	15.625	8192
10	31.25	16384
11	62.5	32768

PPG_SR: PPG Sample Rate Control

PPG Sample Rate Control

These bits set the effective sampling rate of the PPG sensor as shown in the table below.

Note: If a sample rate is set can not be supported by the selected pulse width and LED mode then the highest available sample rate will be automatically set. The user can read back this register to confirm the sample rate.

PPG_SR<3:0>	SAMPLES PER SECOND	PULSES PER SAMPLE, N
0000	10	1
0001	20	1
0010	50	1
0011	84	1
0100	100	1
0101	200	1
0110	400	1
0111	800	1

PPG_SR<3:0>	SAMPLES PER SECOND	PULSES PER SAMPLE, N
1000	1000	1
1001	1600	1
1010	3200	1
1011	10	2
1100	20	2
1101	50	2
1110	84	2
1111	100	2

Maximum Sample Rates Supported for all the Pulse Widths and Number of LEDs:

NUMBER OF ADC CONVERSIONS PER SAMPLE	PPG_LED_PW = 0 (50US)	PPG_LED_PW = 1 (100US)	PPG_LED_PW = 2 (200US)	PPG_LED_PW = 3 (400US)
1 LED, N = 1	3200	1600	1000	1000
2 LED, N = 1	1600	800	800	400
1 LED, N = 2	100	100	100	100
2 LED, N = 2	100	100	100	84

PPG_LED_PW: LED Pulse Width Control

These bits set the pulse width of the LED drivers and the integration time of PPG ADC as shown in the table below.

PPG_LED_PW<1:0>	PULSE WIDTH [US]	INTEGRATION TIME [US]	RES BITS
00	50	50	19
01	100	100	19
10	200	200	19
11	400	400	19

PPG Configuration 2 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SMP_AVE[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

SMP_AVE: Sample Averaging Options

To reduce the amount of data throughput, adjacent samples (in each individual channel) can be averaged and decimated on the chip by setting this register.

These bits set the number of samples that are averaged on chip before being written to the FIFO.

SMP_AVE[2:0]	SAMPLE AVERAGE
000	1 (No Averaging)
001	2
010	4
011	8
100	16
101	32
110	32
111	32

Prox Interrupt Threshold (0x10)

BIT	7	6	5	4	3	2	1	0
Field	PROX_INT_THRESH[7:0]							
Reset	0x00							
Access Type	Write, Read							

PROX_INT_THRESH: Proximity Mode Interrupt Threshold

This register sets the IR ADC count that will trigger the beginning of HR mode. The threshold is defined as the 8 MSB bits of the ADC count. For example, if PROX_INT_THRESH[7:0] = 0x01, then an ADC value of 1023 (decimal) or higher triggers the PROX interrupt. If PROX_INT_THRESH[7:0] = 0xFF, then only a saturated ADC triggers the interrupt.

LED1 PA (0x11)

BIT	7	6	5	4	3	2	1	0
Field	LED1_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED1_PA: LED 1 (IR) Current Pulse Amplitude.

These bits set the nominal current pulse amplitude of LED 1, as shown in the table below.

LED1_RGE<1:0>	00 (50MA)	01 (100MA)	10 (150MA)	11 (200MA)
LED1_PA<7:0>	LED Current[mA]	LED Current[mA]	LED Current[mA]	LED Current[mA]
00000000	0	0	0	0
00000001	0.2	0.4	0.6	0.8
00000010	0.4	0.8	1.2	1.6
00000011	0.6	1.2	1.8	2.4
.....				
11111100	50.4	100.8	151.2	201.6
11111101	50.6	101.2	151.8	202.4
11111110	50.8	101.6	152.4	203.2
11111111	51	102	153	204
LSB	0.2	0.4	0.6	0.8

Note: *For LED Current more than 100mA, VLED must be 4.5V or above.*

LED3 PA (0x13)

BIT	7	6	5	4	3	2	1	0
Field	LED3_PA[7:0]							
Reset	0x00							
Access Type	Write, Read							

LED3_PA: LED 3 (Green) Current Pulse Amplitude

These bits set the nominal current pulse amplitude of LED 3, as shown in the table below.

LED3_RGE<1:0>	00 (50MA)	01 (100MA)	10 (150MA)	11 (200MA)
LED3_PA<7:0>	LED Current[mA]	LED Current[mA]	LED Current[mA]	LED Current[mA]
00000000	0	0	0	0
00000001	0.2	0.4	0.6	0.8
00000010	0.4	0.8	1.2	1.6
00000011	0.6	1.2	1.8	2.4
.....				
11111100	50.4	100.8	151.2	201.6
11111101	50.6	101.2	151.8	202.4
11111110	50.8	101.6	152.4	203.2
11111111	51	102	153	204
LSB	0.2	0.4	0.6	0.8

Note: *For LED Current more than 100mA, VLED must be 4.5V or above.*

LED Range (0x14)

BIT	7	6	5	4	3	2	1	0
Field	–	–	LED3_RGE[1:0]		–	–	LED1_RGE[1:0]	
Reset	–	–	0x00		–	–	0x00	
Access Type	–	–	Write, Read		–	–	Write, Read	

LED3_PA: LED 3 (Green) Current Pulse Amplitude

These bits set the nominal current pulse amplitude of LED 3, as shown in the table below.

LED3_RGE<1:0>	LED CURRENT[MA]
00	50
01	100
10	150
11	200