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EVALUATION KIT AVAILABLE

High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

General Description

The MAX8660/MAX8661 power management ICs (PMICs) power applications processors (APs) in smart cellular phones, PDAs, Internet appliances, and other portable devices.

Four step-down DC-DC outputs, three linear regulators, and an 8th always-on LDO are integrated with power-management functions. Two dynamically controlled DC-DC outputs power the processor core and internal memory. Two other DC-DC converters power I/O, memory, and other peripherals. Additional functions include on/off control for outputs, low-battery detection, reset output, and a 2-wire I²C serial interface. The MAX8661 functions the same as the MAX8660, except it lacks the REG1 step-down regulator and the REG7 linear regulator.

All step-down DC-to-DC outputs use fast 2MHz PWM switching and tiny external components. They automatically switch from PWM to high-efficiency, light-load operation to reduce operating current and extend battery life. In addition, a forced-PWM option allows low-noise operation at all loads. Overvoltage lockout protects the device against inputs up to 7.5V.

Applications

PDAs, Palmtops, and Wireless Handhelds

Smart Cell Phones

Personal Media Players

Portable GPS Navigation

Digital Cameras

Features

- **Optimized for Marvell's PXA300 and Armada 100 Family of Processors**
- **Protected to 7.5V—Shutdown Above 6.3V**
- **Four Synchronous Step-Down Converters REG1, REG2, REG3, REG4**
- **Four LDO Regulators REG5, REG6, REG7, REG8**
- **2MHz Switching Allows Small Components**
- **Low, 20µA Deep-Sleep Current**
- **Low-Battery Monitor and Reset Output**

Ordering Information

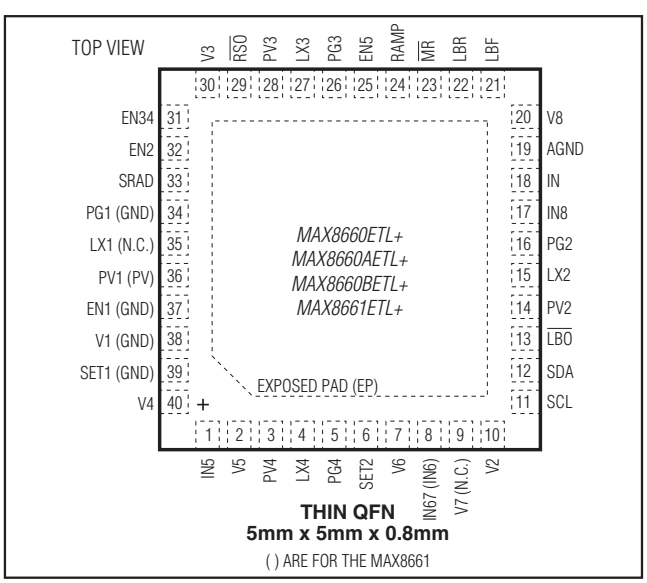
PART	PIN-PACKAGE	OPTIONS
MAX8660ETL+	40 Thin QFN	V1: 3.3V, 3.0V, 2.85V V2: 3.3V, 2.5V, 1.8V V3: 1.4V (default) V4: 1.4V (default)
MAX8660ETL/V+	40 Thin QFN	V1: 3.3V, 3.0V, 2.85V V2: 3.3V, 2.5V, 1.8V V3: 1.4V (default) V4: 1.4V (default)

Note: *All devices are specified over the -40°C to 85°C operating temperature range.*

+Denotes lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Ordering Information continued at end of data sheet.

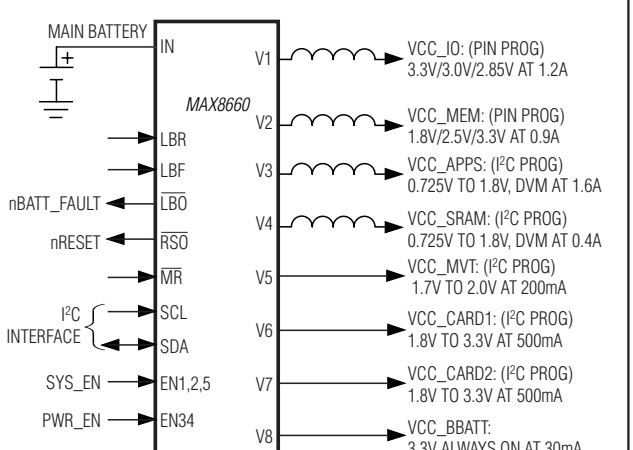
Pin Configuration



THIN QFN
5mm x 5mm x 0.8mm

( ) ARE FOR THE MAX8661

Simplified Functional Diagram



High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

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High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

ABSOLUTE MAXIMUM RATINGS

IN, IN5, IN6, IN67, EN2, EN34, EN5, $\overline{LBO}$, $\overline{RSO}$, $\overline{MR}$, SET1, SET2, V1, V2, V3, V4, SCL, SDA, SRAD to AGND .....-0.3V to +7.5V
LBF, LBR, EN1, RAMP to AGND .....-0.3V to (V_{IN} + 0.3V)
V8 to AGND.....-0.3V to (V_{IN8} + 0.3V)
V5 to AGND.....-0.3V to (V_{IN5} + 0.3V)
V6, V7 to AGND.....-0.3V to (V_{IN67} + 0.3V)
PV1 to PG1 .....-0.3V to +7.5V
PV2 to PG2 .....-0.3V to +7.5V
PV3 to PG3 .....-0.3V to +7.5V
PV4 to PG4 .....-0.3V to +7.5V
PV, PV1, PV2, PV3, PV4, IN8 to IN .....-0.3V to +0.3V
LX1 Continuous RMS Current (Note 1) 2.3A
LX2 Continuous RMS Current (Note 1) 2.0A
LX3 Continuous RMS Current (Note 1) 2.6A
LX4 Continuous RMS Current (Note 1) 1.0A
PG1, PG2, PG3, PG4, EP to AGND.....-0.6V to +0.6V
GND to AGND .....-0.3V to +0.3V
All REGx Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 35.7mW/°C above +70°C).....2857mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: LX_ has internal clamp diodes to PG_ and PV_. Applications that forward bias these diodes must take care not to exceed the IC's package power-dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PV1, PV2, PV3, PV4, IN, IN8 Supply Voltage Range	V_{IN}	PV1, PV2, PV3, PV4, IN, and IN8 must be connected together externally		2.6		6.0	V
IN Undervoltage-Lockout Threshold	V_{UVLO}	V_{IN} rising		2.250	2.400	2.550	V
		V_{IN} falling		2.200	2.350	2.525	
IN Overvoltage-Lockout Threshold	V_{OVLO}	V_{IN} rising		6.20	6.35	6.50	V
		V_{IN} falling		6.00	6.15	6.30	
Input Current	I_{IN} + I_{PV1} + I_{PV2} + I_{PV3} + I_{PV4} + I_{IN5} + I_{IN67} + I_{IN8}	No load; SDA = SCL = V8	Only V8 on (deep-sleep power mode)		20		µA
			V1, V2, and V8 on; V1 and V2 in normal (skip) operating mode		50		
			V1, V2, V5, and V8 on (sleep power mode); V1 and V2 in normal (skip) operating mode		90		
			V1, V2, V3, V4, V5, and V8 on (run power mode); V1, V2, V3, and V4 in normal (skip) operating mode		140		
			V1, V2, V3, V4, V5, V6, V7, and V8 (all on); V1, V2, V3, and V4 in normal (skip) operating mode		250		
		Undervoltage lockout, V_{IN} = 2.2V			1.5		
		Overvoltage lockout, V_{IN} = 6.5V			25		

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Switching Frequency	f_{SW}			1.9	2.0	2.1	MHz
REG1—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER (MAX8660, MAX8660A, MAX8660B only)							
V1 Voltage Accuracy (MAX8860/MAX8860B)	V1	SET1 = IN, V_{PV1} = 4.2V, load = 600mA		3.250	3.300	3.350	V
		SET1 not connected, V_{PV1} = 3.6V, load = 600mA		2.955	3.000	3.045	
		SET1 = AGND, V_{PV1} = 3.6V, load = 600mA		2.807	2.850	2.893	
V1 Voltage Accuracy (MAX8660A)	V1	SET1 = IN, V_{PV1} = 4.2V, load = 600mA		2.463	2.500	2.538	V
		SET1 not connected, V_{PV1} = 3.6V, load = 600mA		1.970	2.000	2.030	
		SET1 = AGND, V_{PV1} = 3.6V, load = 600mA		1.773	1.800	1.827	
V1 Load Regulation		Load = 0 to 1200mA			-1.5		%/A
V1 Line Regulation					0.15		%/V
SET1 Input Leakage Current					0.01		µA
V1 Dropout Voltage		Load = 800mA (Notes 3, 4)			150		mV
		Load = 1200mA (Notes 3, 4)			200		
p-Channel On-Resistance	R_{P1}				0.12		Ω
n-Channel On-Resistance	R_{N1}				0.15		Ω
p-Channel Current-Limit Threshold	I_{LIM1}			1.5	1.8	2.2	A
n-Channel Zero-Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-975		mA
REG1 Maximum Output Current	I_{OUT1}	2.6V ≤ V_{PV1} ≤ 6V (Note 5)		1.2			A
V1 Bias Current					5		µA
LX1 Leakage Current		V_{PV1} = 6V, LX1 = PG1 or PV1, V_{EN1} = 0V	T_A = +25°C	-2	±0.03	+2	µA
			T_A = +85°C		±0.2		
Soft-Start Ramp Rate (MAX8660/MAX8860B)		To V1 = 3.3V (total ramp time is 450µs for all V1 output voltages)		5	7	9	mV/µs
Soft-Start Ramp Rate (MAX8660A)		To V1 = 2.5V (total ramp time is 450µs for all V1 output voltages)		3	5	7	mV/µs
V5 to V1 Enable Time	$t_{VMHVSH1}$	Figure 6			350		µs
Internal Off-Discharge Resistance					650		Ω
Minimum Duty Cycle		Forced-PWM mode only, min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REG2—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER							
V2 Voltage Accuracy (MAX8660/MAX8860B)	V2	SET2 = IN, V_{PV2} = 4.2V, load = 600mA		3.250	3.300	3.350	V
		SET2 not connected, V_{PV2} = 3.6V, load = 600mA		2.463	2.500	2.538	
		SET2 = AGND, V_{PV2} = 3.6V, load = 600mA		1.773	1.800	1.827	
V2 Voltage Accuracy (MAX8660A)	V2	SET2 = IN, V_{PV2} = 4.2V, load = 600mA		2.463	2.500	2.538	V
		SET2 not connected, V_{PV2} = 3.6V, load = 600mA		1.970	2.000	2.030	
		SET2 = AGND, V_{PV2} = 3.6V, load = 600mA		1.773	1.800	1.827	
V2 Load Regulation		Load = 0 to 900mA			-1.7		%/A
V2 Line Regulation					0.15		%/V
SET2 Input Leakage Current					0.01		µA
V2 Dropout Voltage		Load = 900mA (Notes 3, 4)			225		mV
p-Channel On-Resistance	R_{P2}				0.18		Ω
n-Channel On-Resistance	R_{N2}				0.15		Ω
p-Channel Current-Limit Threshold	I_{LIM2}			1.10	1.30	1.50	A
n-Channel Zero Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-800		mA
REG2 Maximum Output Current	I_{OUT2}	2.6V ≤ V_{PV2} ≤ 6V (Note 5)		0.9			A
V2 Bias Current					5		µA
LX2 Leakage Current		V_{PV2} = 6V, LX2 = PG2 or PV2, V_{EN2} = 0V	T_A = +25°C	-2	±0.03	+2	µA
			T_A = +85°C		0.2		
Soft-Start Ramp Rate		To V2 = 1.8V (total ramp time is 450µs for all V2 output voltages)		2	4	6	mV/µs
V5 to V2 Enable Time	$t_{VMHVSH2}$	Figure 6			350		µs
Internal Off-Discharge Resistance					650		Ω
Minimum Duty Cycle		Forced-PWM mode only; min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%
REG3—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER							
V3 Output Voltage Accuracy	V3	MAX8860/MAX8660A/MAX8661 REG3 default output voltage, V_{PV3} = 3.6V, load = 600mA		1.379	1.400	1.421	V
		MAX8860B REG3 default output voltage, V_{PV3} = 3.6V, load = 600mA		1.133	1.150	1.167	
		REG3 serial programmed from 0.9V to 1.8V, load = 600mA (Note 6)		-1.5		+1.5	%
V3 Load Regulation		Load = 0 to 1600mA			-17		mV/A
V3 Line Regulation		(Note 7)			0.05		%/V
p-Channel On-Resistance	R_{P3}				0.12		Ω
n-Channel On-Resistance	R_{N3}				0.08		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
p-Channel Current-Limit Threshold	I_{LIM3}			1.85	2.15	2.45	A
n-Channel Zero-Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-0.8		A
REG3 Maximum Output Current	I_{OUT3}	2.6V ≤ V_{PV3} ≤ 6V (Note 5)		1.6			A
V3 Bias Current					0.01		µA
LX3 Leakage Current		V_{PV3} = 6V, LX3 = PG3 or PV3, V_{EN34} = 0V	T_A = +25°C	-2	+0.03	+2	µA
			T_A = +85°C		0.24		
Soft-Start Ramp Rate		MAX8660/MAX8660A/MAX8661, R_{RAMP} = 56kΩ to 1.4V			8		mV/µs
		MAX8660B, R_{RAMP} = 56kΩ to 1.15V			6.7		
V3 Dynamic-Change Ramp Rate		R_{RAMP} = 56kΩ			10		mV/µs
EN34 to V3 Enable Time	$t_{PHLVTH3}$	MAX8660/MAX8660A/MAX8661, powering up to 1.4V, Figure 6, R_{RAMP} = 56kΩ			400		µs
		MAX8660B, powering up to 1.15V, Figure 6, R_{RAMP} = 56kΩ			400		
Internal Off-Discharge Resistance					550		Ω
Minimum Duty Cycle		Forced-PWM mode only, min duty cycle in skip mode is 0%			16.7		%
Maximum Duty Cycle					100		%
REG4—SYNCHRONOUS STEP-DOWN DC-DC CONVERTER							
V4 Output Voltage Accuracy	V4	MAX8660/MAX8660A/MAX8661 REG4 default output voltage, V_{PV4} = 3.6V, load = 200mA		1.379	1.400	1.421	V
		MAX8660B REG4 default output voltage, V_{PV4} = 3.6V, load = 200mA		1.133	1.150	1.167	
		REG4 serial programmed from 0.9V to 1.8V, load = 200mA (Note 6)		-1.5		+1.5	%
V4 Load Regulation		Load = 0 to 400mA			-40		mV/A
V4 Line Regulation		(Note 7)			0.1		%/V
p-Channel On-Resistance	R_{P4}				0.37		Ω
n-Channel On-Resistance	R_{N4}				0.3		Ω
p-Channel Current-Limit Threshold	I_{LIM4}			0.65	0.78	0.90	A
n-Channel Zero-Crossing Threshold					25		mA
n-Channel Negative Current Limit		Forced-PWM mode only			-975		mA
REG4 Maximum Output Current	I_{OUT4}	2.6V ≤ V_{PV4} ≤ 6V (Note 5)		0.4			A
V4 Bias Current					0.01		µA
LX4 Leakage Current		V_{PV4} = 6V, LX4 = PG4 or PV4, V_{EN34} = 0V	T_A = +25°C	-2	±0.02	+2	µA
			T_A = +85°C		0.12		
Soft-Start Ramp Rate		MAX8660/MAX8660A/MAX8661, R_{RAMP} = 56kΩ to 1.4V			8		mV/µs
		MAX8660B, R_{RAMP} = 56kΩ to 1.15V			6.7		
V4 Dynamic-Change Ramp Rate		R_{RAMP} = 56kΩ			10		mV/µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN34 to V4 Enable Time	$t_{PHLVTH4}$	MAX8660/MAX8660A/MAX8661, powering up to 1.4V, Figure 6, R_{RAMP} = 56kΩ		400		µs
		MAX8660B, powering up to 1.15V, Figure 6, R_{RAMP} = 56kΩ		400		
Internal Off-Discharge Resistance				550		Ω
Minimum Duty Cycle		Forced-PWM mode only, minimum duty cycle in skip mode is 0%		16.7		%
Maximum Duty Cycle				100		%
REG5 LDO						
IN5 Input Voltage Range	V_{IN5}		2.35		V_{IN}	V
V5 Output Voltage	V5	REG5 default output voltage, 2.35V ≤ V_{IN5} ≤ 6V, load = 0 to 200mA	1.764	1.800	1.836	V
		REG5 serial programmed from 1.7V to 2.0V, 2.35V ≤ V_{IN5} ≤ 6V, load = 0 to 200mA	-2		+2	%
V5 Output Current Limit	I_{OUT5}		225	350	500	mA
V5 Output-Voltage Noise		10Hz to 100kHz, I_{OUT5} = 10mA		160		$µV_{RMS}$
V5 Power-Supply Rejection		V_{IN5} = (V5 + 1V), I_{OUT5} = 10mA, f = 10kHz		40		dB
V5 Soft-Start Ramp Rate		Powering up to 1.8V (total ramp time is 225µs for all V5 output voltages)	5	7	9	mV/µs
EN5 to V5 Enable Time	t_{SEHVMH}	Figure 6		290		µs
V5 Dynamic-Change Ramp Rate		R_{RAMP} = 56kΩ		10		mV/µs
Internal Off-Discharge Resistance				2		kΩ
REG6, REG7 LDOs						
IN67 Input Voltage Range	V_{IN67}		2.35		V_{IN}	V
REG6 and REG7 Output Voltage (POR Default to 0V, Set by Serial Input)	V6 V7	Setting from 1.8V to 3.3V in 0.1V steps, load = 0 to 300mA	-3		+3	%
V6, V7 Dropout Voltage		3V mode, load = 300mA (Note 3)		55	100	mV
V6, V7 Output Current Limit	I_{OUT6} I_{OUT7}	V_{IN67} = 3.6V		750		mA
V6, V7 Soft-Start Ramp Rate		Powering up to 3.3V (total ramp time is 450µs for all V6/V7 output voltages)	5	7	9	mV/µs
Internal Off-Discharge Resistance				350		Ω
REG8 ALWAYS-ON LDO						
V8 Output Voltage	V8	Load = 0 to 15mA	3.168	3.300	3.432	V
		Load = 30mA	2.800	3.2	3.432	
V8 Dropout Voltage		Load = 15mA (Note 3)		180		mV
V8 Output Current Limit	I_{OUT8}	V8 = 2.5V	30	70	135	mA
Internal Off-Discharge Resistance				1.5		kΩ
LOW-BATTERY DETECTOR (LBF, LBR, $\overline{LBO}$)						
Low-Battery Falling Threshold	V_{LBFTH}		1.182	1.200	1.218	V
Low-Battery Rising Threshold	V_{LBRTH}		1.231	1.250	1.268	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{LBO}$, $\overline{RSO}$ Output-High Leakage Current		V_{IN} = 6V, T_A = +25°C			0.2	µA
$\overline{LBO}$ Output Low Level		2.6V ≤ V_{IN} ≤ 6V, sinking 3mA			0.2	V
		V_{IN} = 1V, sinking 100µA			0.4	
Minimum V_{IN} for $\overline{LBO}$ Assertion		$\overline{LBO}$ is forced low when the device is in UVLO	1			V
$\overline{LBO}$ Deassert Delay	t_{VBHBFH}	Figure 6	0	3		µs
LBF and LBR Input Bias Current		T_A = +25°C	-50	0	+50	nA
		T_A = +85°C		0.5		
RESET ($\overline{MR}$, $\overline{RSO}$)						
$\overline{RSO}$ Threshold	V_{RSOTH}	Voltage on V8, falling, hysteresis is 5% (typ)	2.1	2.2	2.3	V
$\overline{RSO}$ Deassert Delay	$t_{VBHRSTH}$	Figure 6	20	24	28	ms
$\overline{RSO}$ Output-High Leakage Current		V_{IN} = 6V, T_A = +25°C			0.2	µA
$\overline{RSO}$ Output Low Level		2.6V ≤ V_{IN} ≤ 6V, sinking 3mA			0.2	V
		V_{IN} = 1V, sinking 100µA			0.4	
Minimum V_{IN} for $\overline{RSO}$ Assertion		$\overline{RSO}$ is forced low when the device is in UVLO	1			V
$\overline{MR}$ Input High Level		2.6V ≤ V_{IN} ≤ 6V	1.4			V
$\overline{MR}$ Input Low Level		2.6V ≤ V_{IN} ≤ 6V			0.4	V
$\overline{MR}$ Input Leakage Current		V_{IN} = 6V, T_A = +25°C	-0.2		+0.2	µA
$\overline{MR}$ Minimum Pulse Width	t_{MR}			1		µs
THERMAL-OVERLOAD PROTECTION						
Thermal-Shutdown Temperature		T_J rising		+160		°C
Thermal-Shutdown Hysteresis				15		°C
ENABLE INPUTS (EN1, EN2, EN34, EN5)						
EN_ Input High Level		2.6V ≤ V_{IN} ≤ 6V	1.4			V
EN_ Input Low Level		2.6V ≤ V_{IN} ≤ 6V			0.4	V
EN_ Input Leakage Current		V_{IN} = 6V, T_A = +25°C	-0.2		+0.2	µA
I²C LOGIC (SDA, SCL, SRAD)						
SCL, SDA Input High Voltage			1.4			V
SCL, SDA Input Low Voltage					0.4	V
SCL, SDA Input Hysteresis				0.1		V
SCL, SDA Input Current		T_A = +25°C, IN = AGND, V_{IN} = 6V	-10		+10	µA
SDA Output Low Voltage		2.6V ≤ V_{IN} ≤ 6V, sinking 3mA			0.2	V
SRAD Input High Level		2.6V ≤ V_{IN} ≤ 6V	1.4			V
SRAD Input Low Level		2.6V ≤ V_{IN} ≤ 6V			0.4	V
SRAD Input Leakage Current		V_{IN} = 6V, T_A = +25°C	-0.2		+0.2	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = V_{IN5} = V_{IN67} = V_{IN8} = 3.6V, Figure 3, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING						
Clock Frequency	f_{SCL}				400	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$	Figure 8	0.6			µs
CLK Low Period	t_{LOW}		1.3			µs
CLK High Period	t_{HIGH}		0.6			µs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$	Figure 8	0.6			µs
DATA Hold Time	$t_{HD;DAT}$	Figure 9	0			µs
DATA Set-Up Time	$t_{SU;DAT}$	Figure 9	100			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$	Figure 8	0.6			µs
Bus-Free Time Between STOP and START	t_{BUF}		1.3			µs
Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA and CLK Signals				50		ns

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 3: The dropout voltage is defined as V_{IN} - V_{OUT} when V_{OUT} is 100mV below the nominal value of V_{OUT}.

Note 4: Dropout voltage (V_{DO}) is a function of the p-channel switch resistance (R_P) and the inductor resistance (R_L). The given values assume R_L = 50mΩ for the REG1 inductor and 67mΩ for the REG2 inductor:

$$V_{DO} = I_{LOAD} (R_P + R_L)$$

Note 5: The maximum output current is guaranteed by correlation to the p-channel current-limit threshold, p-channel on-resistance, n-channel on-resistance, oscillator frequency, input voltage range, and output voltage range. The maximum output current in the *Electrical Characteristics* table is the worst-case output current for the components shown in Figure 3 over then entire specified range of input and output voltage. More output current may be available when alternate components and voltage ranges are used. See the *Step-Down Converter Output Current* section for more information.

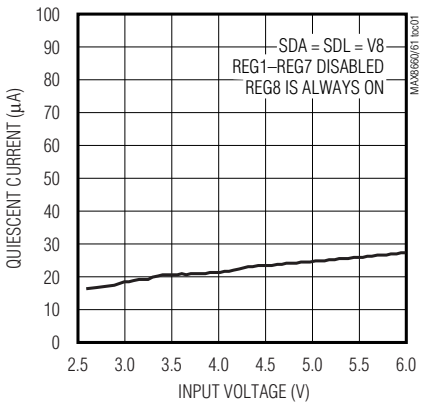
Note 6: Tested at 1.4V default output voltage for the MAX8660, MAX8660A, and MAX8661. Tested at 1.15V default output voltage for the MAX8660B.

Note 7: All output voltages are possible in normal mode. In forced-PWM mode, the minimum output voltage is limited by 0.167 x V_{IN}. For example, with V_{IN} = 5.688V, the minimum output is 0.95V.

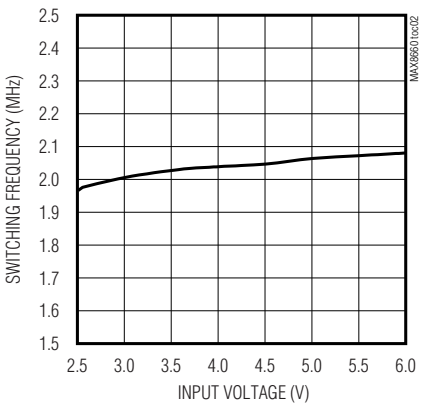
Typical Operating Characteristics

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

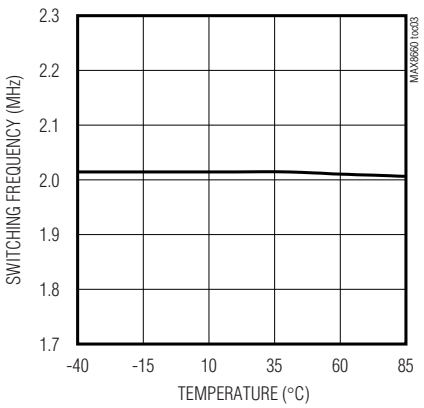
QUIESCENT CURRENT vs. INPUT VOLTAGE



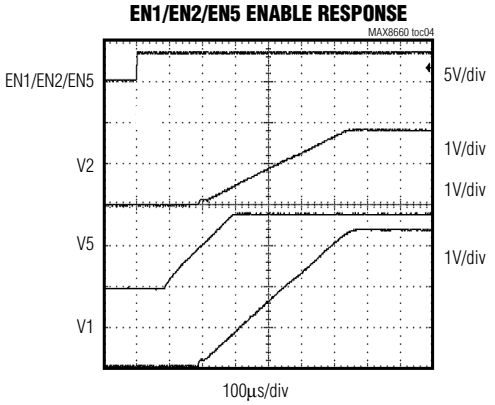
SWITCHING FREQUENCY vs. INPUT VOLTAGE



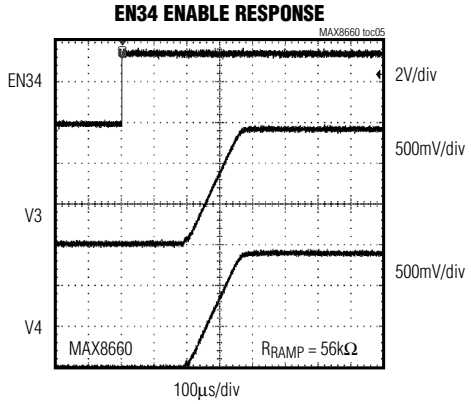
SWITCHING FREQUENCY vs. TEMPERATURE



EN1/EN2/EN5 ENABLE RESPONSE



EN34 ENABLE RESPONSE

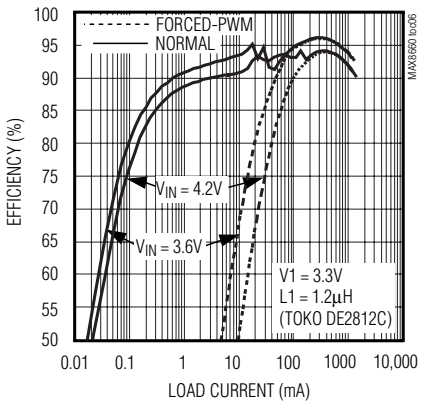


High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

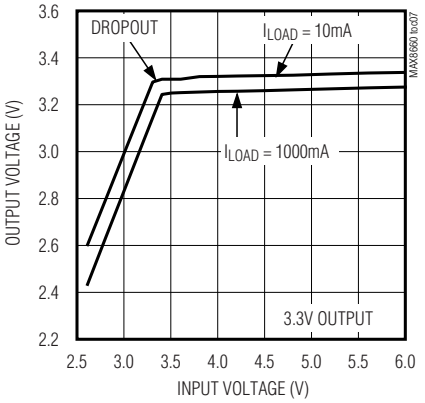
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

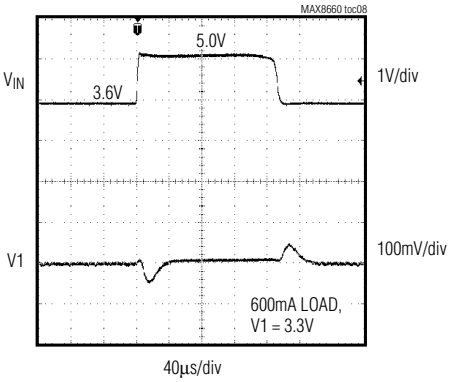
REG1 EFFICIENCY vs. LOAD CURRENT



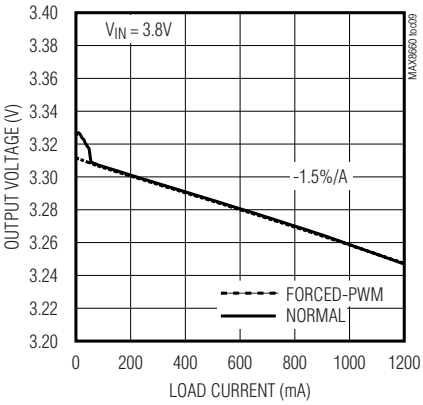
REG1 OUTPUT VOLTAGE vs. INPUT VOLTAGE



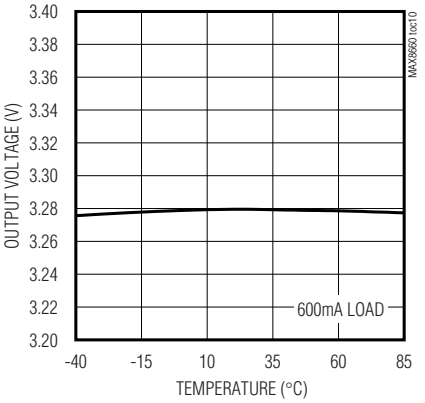
REG1 LINE TRANSIENT



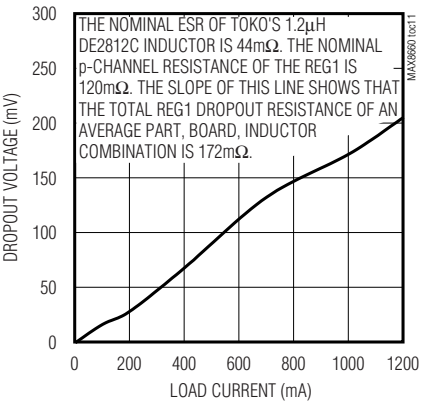
REG1 LOAD REGULATION



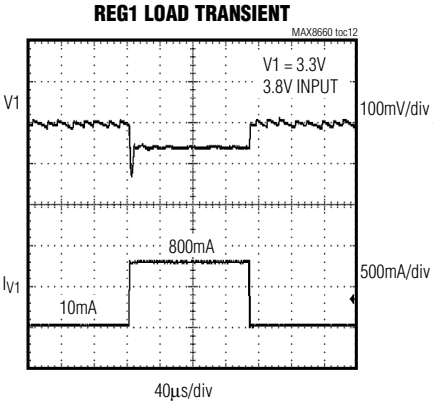
REG1 OUTPUT VOLTAGE vs. TEMPERATURE



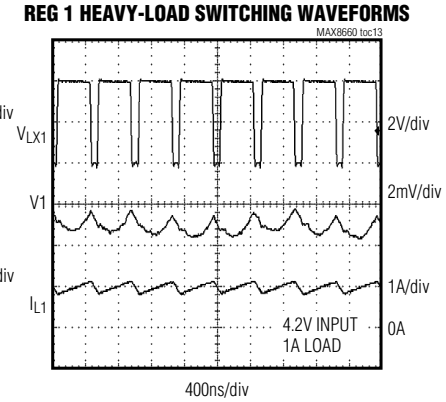
REG1 DROPOUT VOLTAGE vs. LOAD CURRENT



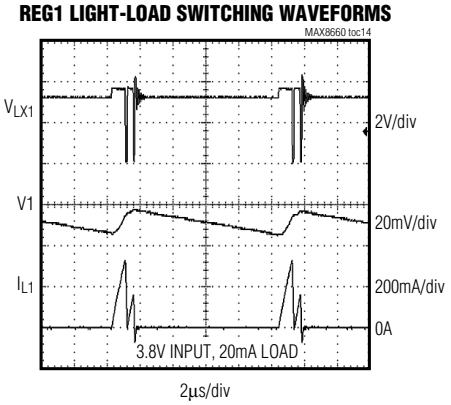
REG1 LOAD TRANSIENT



REG 1 HEAVY-LOAD SWITCHING WAVEFORMS



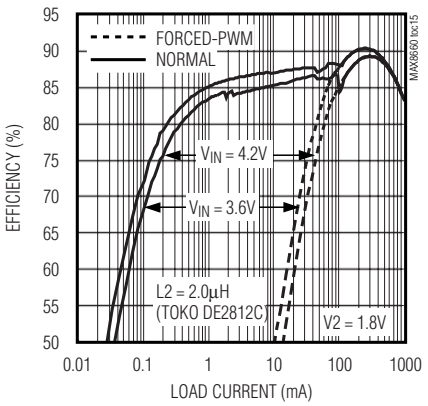
REG1 LIGHT-LOAD SWITCHING WAVEFORMS



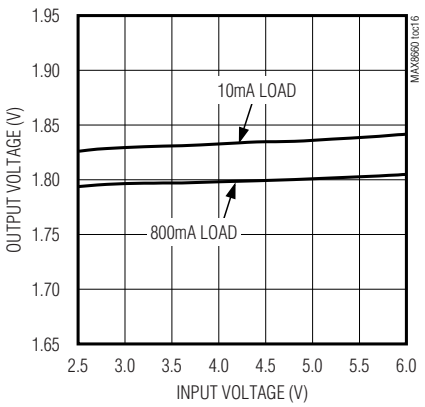
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

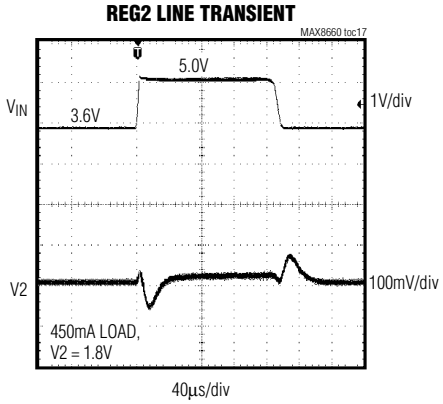
REG2 EFFICIENCY vs. LOAD CURRENT



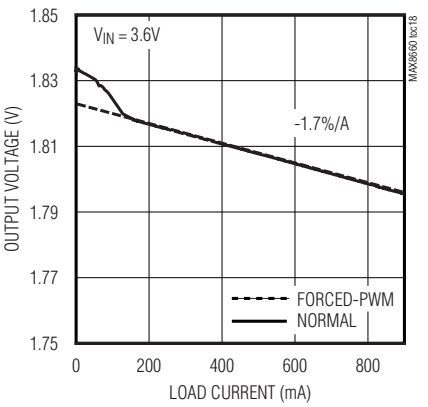
REG2 OUTPUT VOLTAGE vs. INPUT VOLTAGE



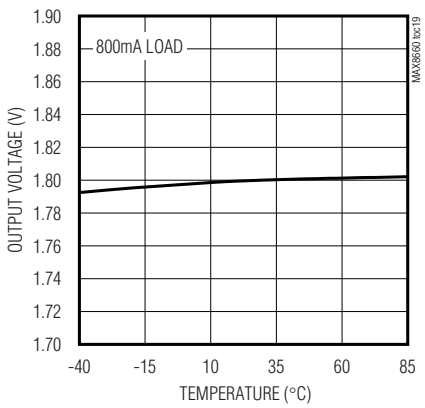
REG2 LINE TRANSIENT



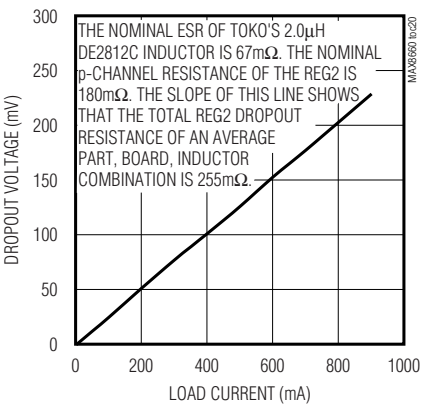
REG2 LOAD REGULATION



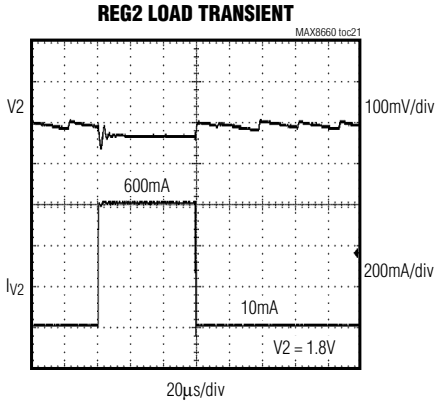
REG2 OUTPUT VOLTAGE vs. TEMPERATURE



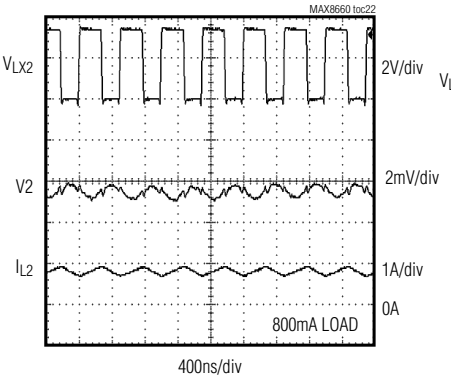
REG2 DROPOUT VOLTAGE vs. LOAD CURRENT



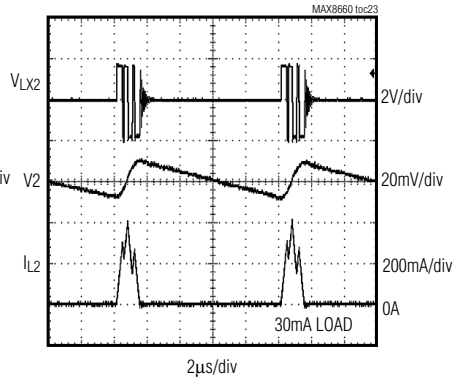
REG2 LOAD TRANSIENT



REG2 HEAVY-LOAD SWITCHING WAVEFORMS



REG2 LIGHT-LOAD SWITCHING WAVEFORMS

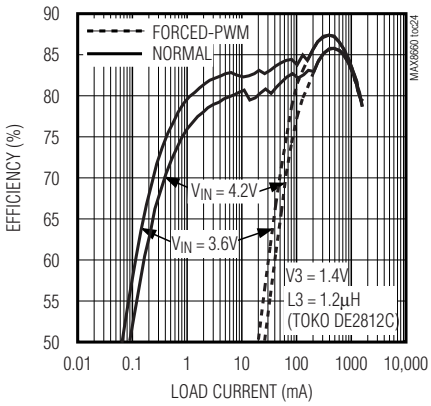


High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

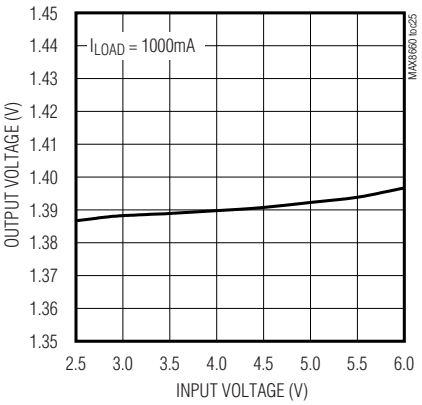
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

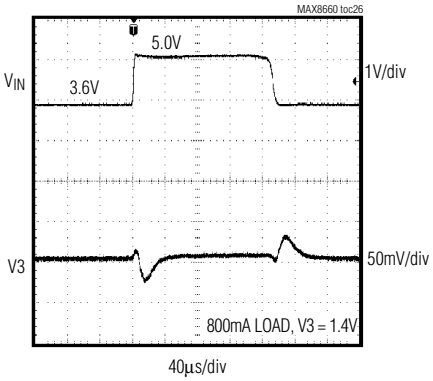
REG3 EFFICIENCY vs. LOAD CURRENT



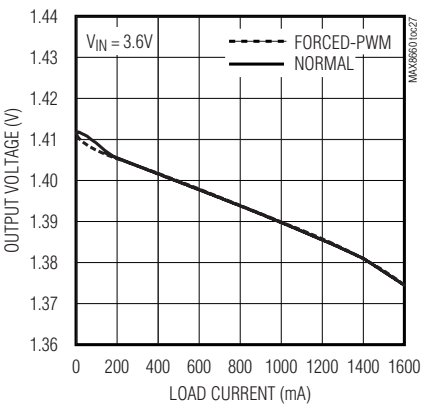
REG3 OUTPUT VOLTAGE vs. INPUT VOLTAGE



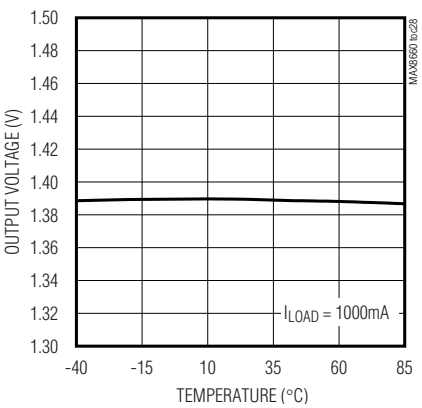
REG3 LINE TRANSIENT



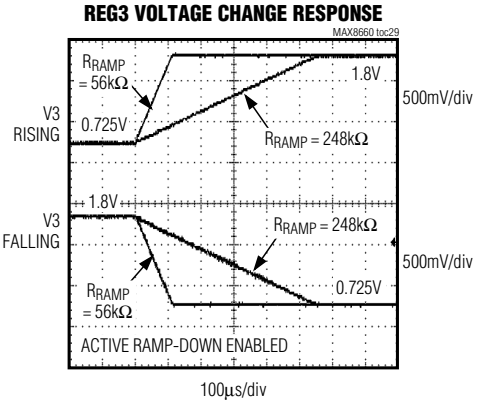
REG3 LOAD REGULATION



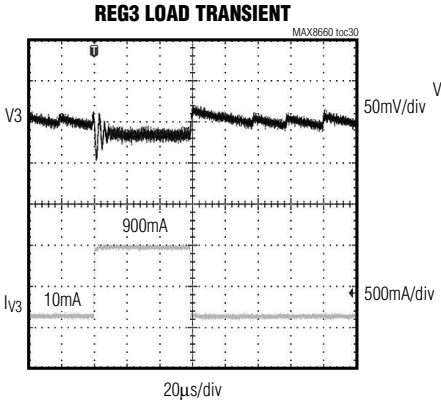
REG3 OUTPUT VOLTAGE vs. TEMPERATURE



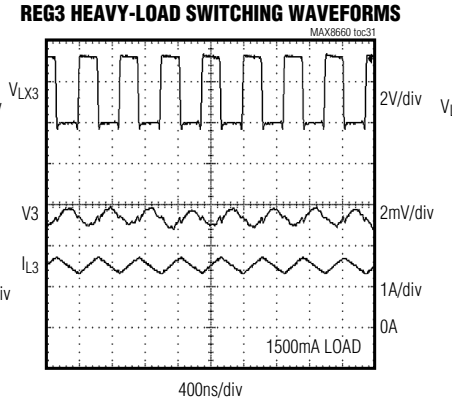
REG3 VOLTAGE CHANGE RESPONSE



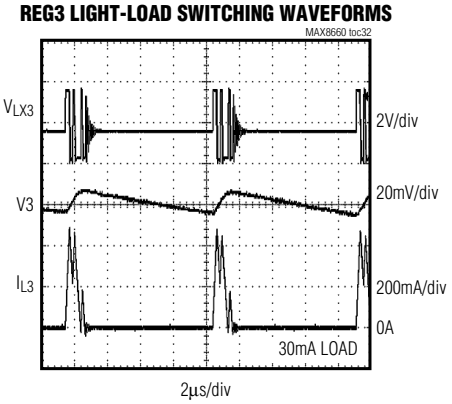
REG3 LOAD TRANSIENT



REG3 HEAVY-LOAD SWITCHING WAVEFORMS



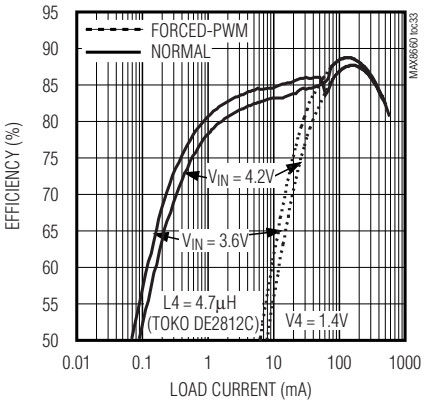
REG3 LIGHT-LOAD SWITCHING WAVEFORMS



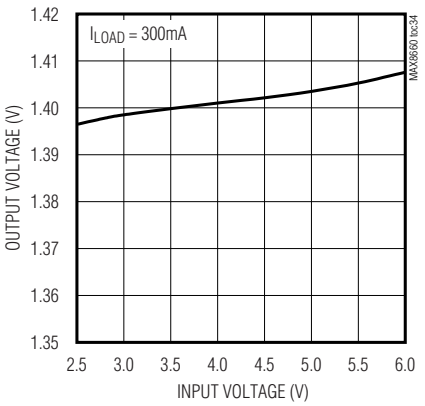
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

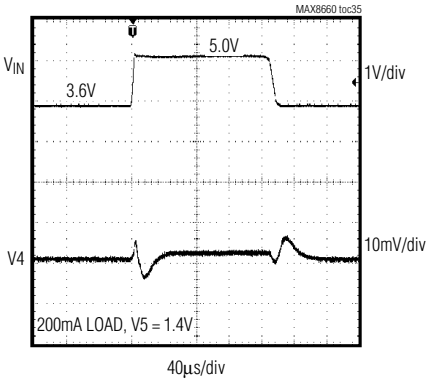
REG4 EFFICIENCY vs. LOAD CURRENT



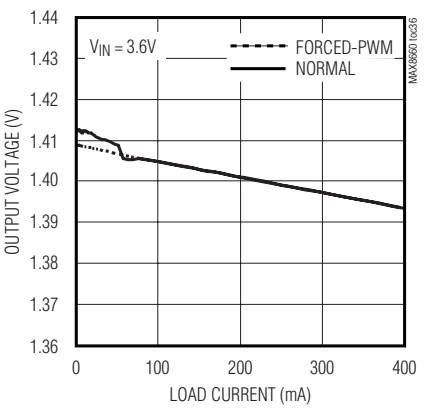
REG4 OUTPUT VOLTAGE vs. INPUT VOLTAGE



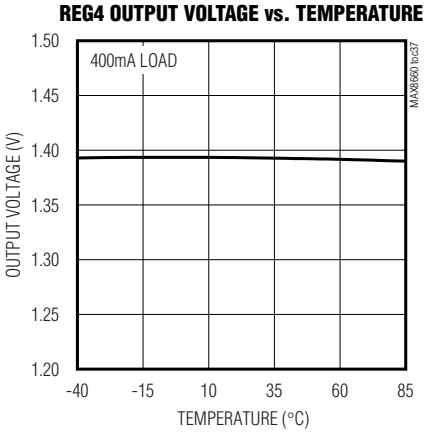
REG4 LINE TRANSIENT



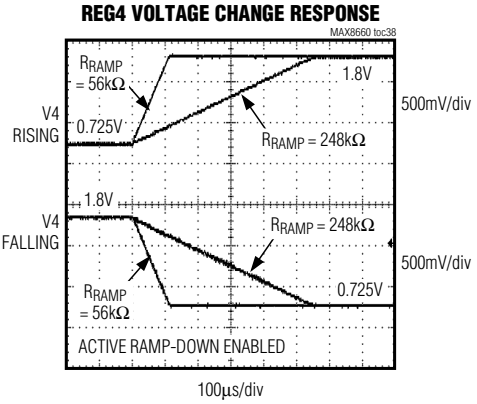
REG4 LOAD REGULATION



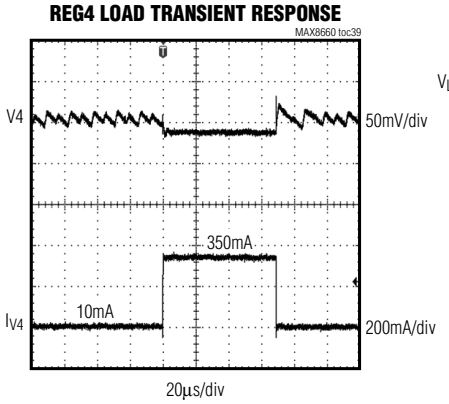
REG4 OUTPUT VOLTAGE vs. TEMPERATURE



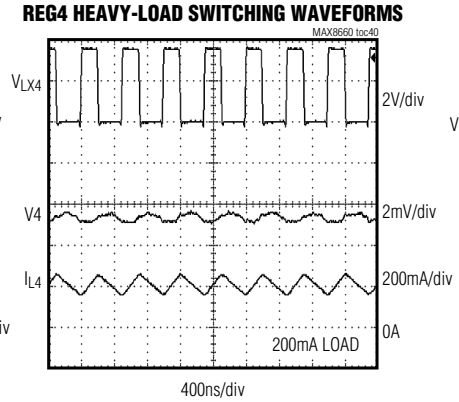
REG4 VOLTAGE CHANGE RESPONSE



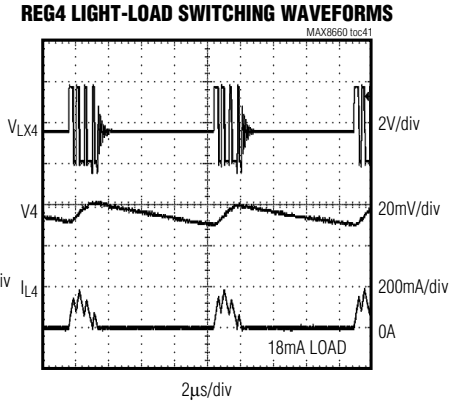
REG4 LOAD TRANSIENT RESPONSE



REG4 HEAVY-LOAD SWITCHING WAVEFORMS



REG4 LIGHT-LOAD SWITCHING WAVEFORMS

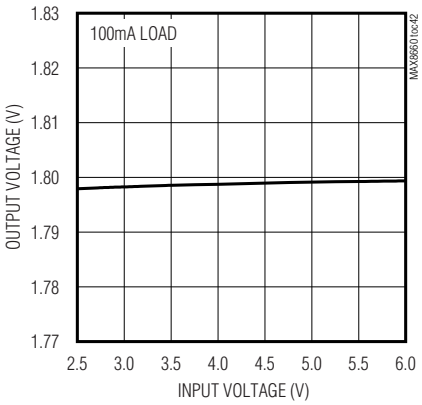


High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

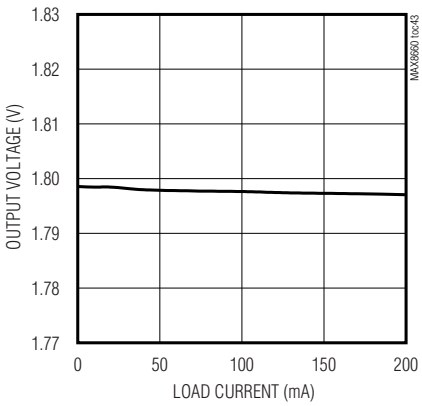
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

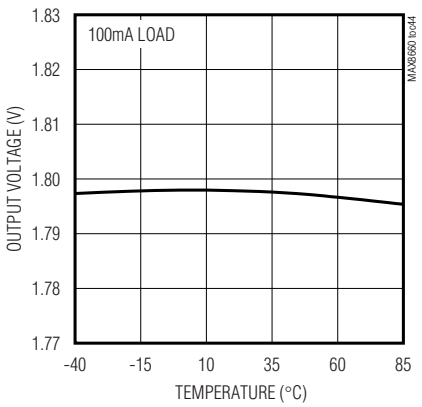
REG5 OUTPUT VOLTAGE vs. INPUT VOLTAGE



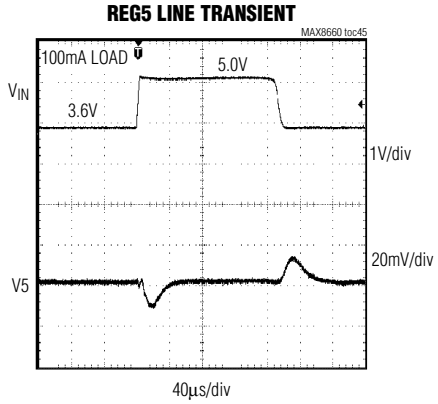
REG5 OUTPUT VOLTAGE vs. LOAD CURRENT



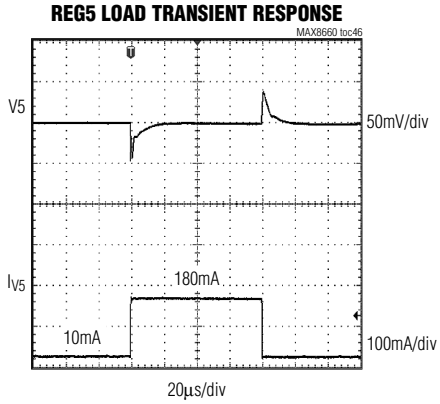
REG5 OUTPUT VOLTAGE vs. TEMPERATURE



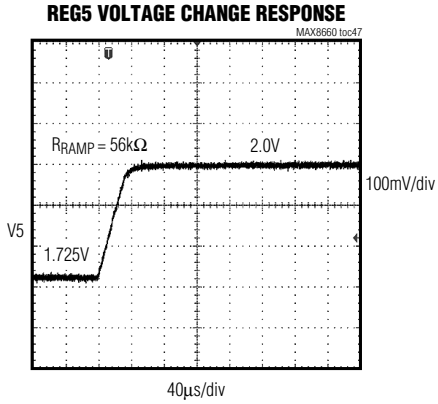
REG5 LINE TRANSIENT



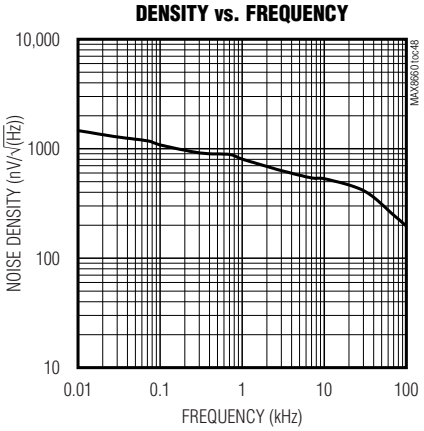
REG5 LOAD TRANSIENT RESPONSE



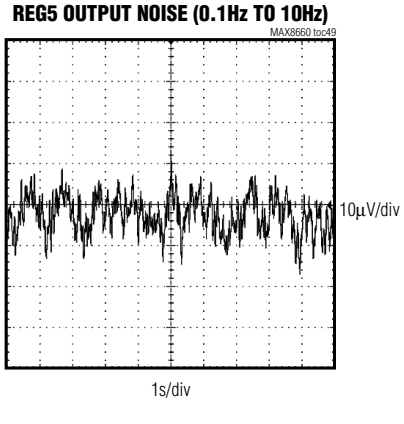
REG5 VOLTAGE CHANGE RESPONSE



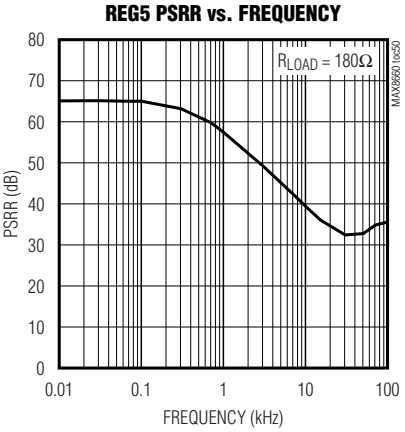
REG5 OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



REG5 OUTPUT NOISE (0.1Hz TO 10Hz)



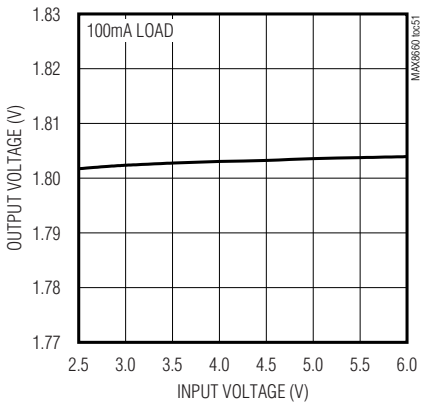
REG5 PSRR vs. FREQUENCY



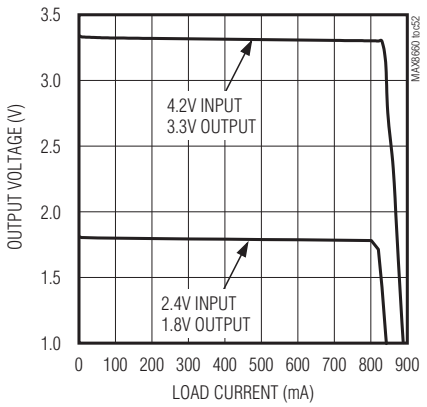
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

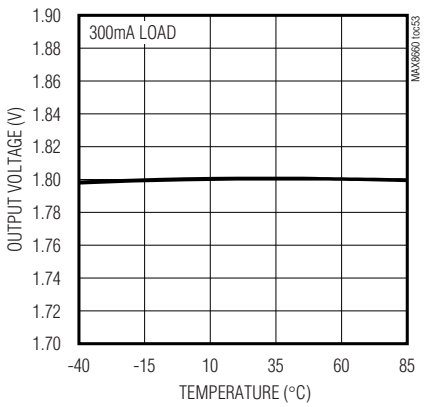
REG6/REG7 OUTPUT VOLTAGE vs. INPUT VOLTAGE



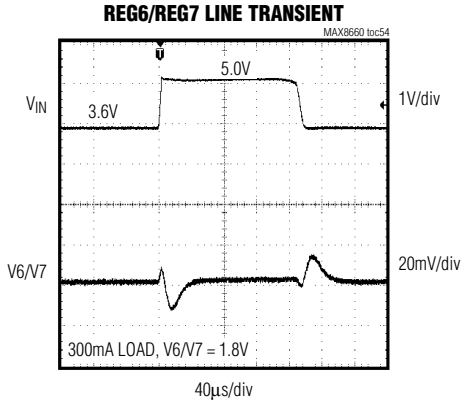
REG6/REG7 OUTPUT VOLTAGE vs. LOAD CURRENT



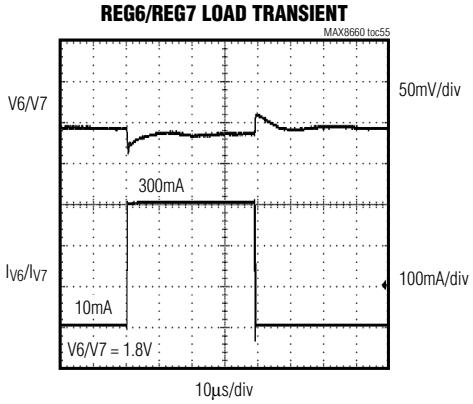
REG6/REG7 OUTPUT VOLTAGE vs. TEMPERATURE



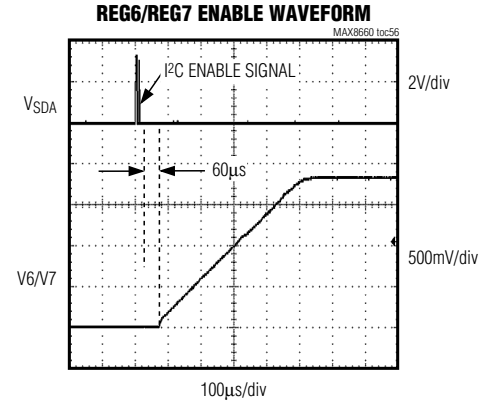
REG6/REG7 LINE TRANSIENT



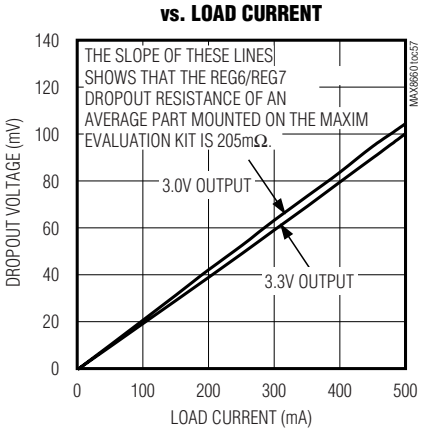
REG6/REG7 LOAD TRANSIENT



REG6/REG7 ENABLE WAVEFORM



REG6/REG7 DROPOUT OUTPUT VOLTAGE vs. LOAD CURRENT

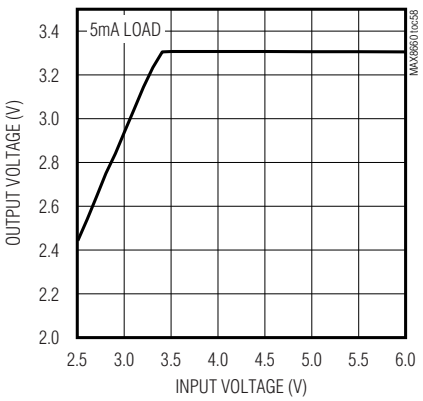


High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

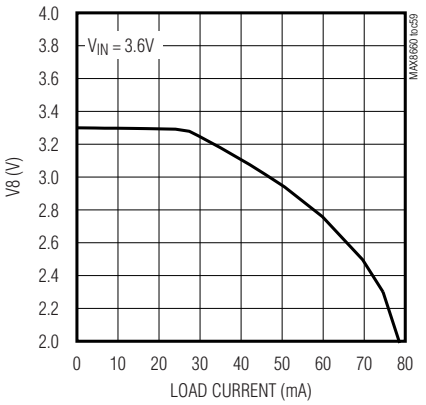
Typical Operating Characteristics (continued)

(Circuit of Figure 3, V_{IN} = 3.6V, T_A = +25°C, unless otherwise noted.)

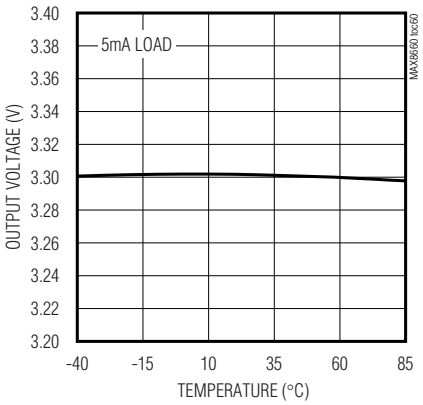
REG8 OUTPUT VOLTAGE vs. INPUT VOLTAGE



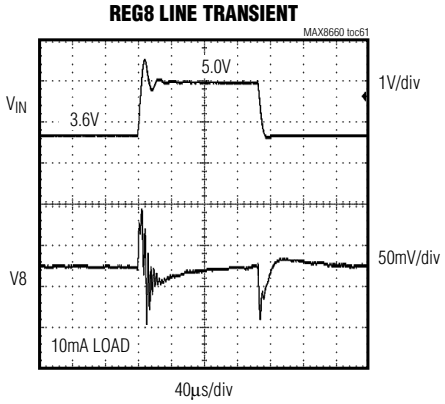
REG8 LOAD REGULATION



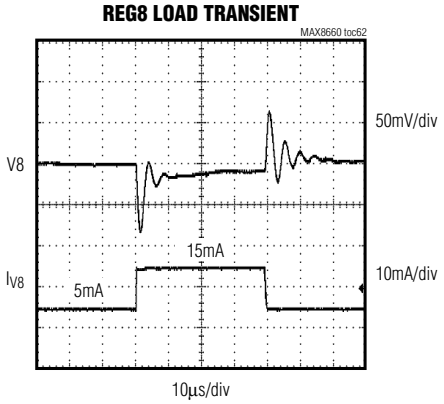
REG8 OUTPUT VOLTAGE vs. TEMPERATURE



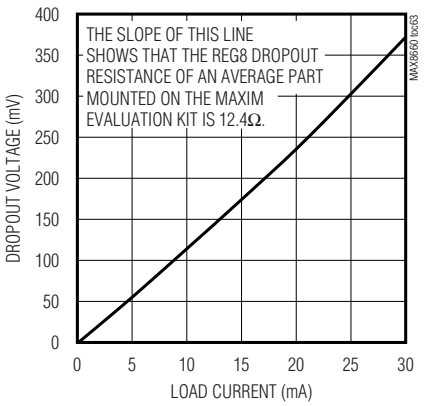
REG8 LINE TRANSIENT



REG8 LOAD TRANSIENT



REG8 DROPOUT VOLTAGE vs. LOAD CURRENT



Pin Description

PIN		NAME	FUNCTION
MAX8660	MAX8661		
1	1	IN5	REG5 Power Input. Connect IN5 to IN to ensure V5 rises first to meet the Marvell PXA3xx processor's sequencing requirements. If adherence to this sequencing specification is not required, connect IN5 to V1, V2, or another supply between 2.35V and V_{IN}. See the *Linear Regulators (REG5–REG8)* section for more information.
—	2	V5	REG5 Linear-Regulator Output. V5 defaults to 1.8V and is adjustable from 1.7V to 2.0V through the serial interface. The input to the V5 regulator is IN5. Use V5 to power *VCC_MVT, VCC_BG, VCC_OSC13M,* and *VCC_PLL* on Marvell PXA3xx processors. V5 is internally pulled to AGND through 2kΩ when REG5 is shut down.
3	3	PV4	REG4 Power Input. Connect a 4.7µF ceramic capacitor from PV4 to PG4. All PV pins and IN must be connected together externally.
4	4	LX4	REG4 Switching Node. Connect LX4 to the REG4 inductor. LX4 is high impedance when REG4 is shut down.
5	5	PG4	REG4 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
6	6	SET2	REG2 Voltage Select Input. SET2 is a tri-level logic input. Connect SET2 to select the V2 output voltage as detailed in Table 4. The REG2 output voltage selected by SET2 is latched at the end of the REG2 soft-start period. Changes to SET2 after the startup period have no effect.
7	7	V6	REG6 Linear-Regulator Output. REG6 is activated and programmed through the serial interface to output from 1.8V to 3.3V in 0.1V steps. REG6 is off by default. V6 is internally pulled to AGND through 350Ω when REG6 is shut down. V6 optionally powers *VCC_CARD1* on Marvell PXA3xx processors.
8	—	IN67	REG6 and REG7 Power Input. IN67 is typically connected to IN. IN67 can also be connected to any supply between 2.35V to V_{IN}.
—	8	IN6	REG6 Power Input. IN6 is typically connected to IN. IN6 can also be connected to any supply between 2.35V to V_{IN}.
9	—	V7	REG7 Linear-Regulator Output. REG7 is activated and programmed through the serial interface to output from 1.8V to 3.3V in 0.1V steps. REG7 is off by default. V7 is internally pulled to AGND through 350Ω when REG7 is shut down. V7 optionally powers *VCC_CARD2* on Marvell PXA3xx processors.
—	9	N.C.	No Internal Connection
10	10	V2	REG2 Voltage Sense Input. Connect V2 directly to the REG2 output voltage. The output voltage of REG2 is selected by SET2. V2 is internally pulled to AGND through 650Ω when REG2 is shut down. V2 powers *VCC_MEM* on Marvell PXA3xx processors.
11	11	SCL	Serial-Clock Input. See the *I²C Interface* section.
12	12	SDA	Serial-Data Input. See the *I²C Interface* section.
13	13	$\overline{LBO}$	Low-Battery Output. $\overline{LBO}$ is an open-drain output that pulls low when LBF is below its threshold. $\overline{LBO}$ typically connects to the *nBATT_FAULT* input of the applications processor to indicate that the battery has been removed or discharged.
14	14	PV2	REG2 Power Input. Connect a 4.7µF ceramic capacitor from PV2 to PG2. All PV pins and IN must be connected together externally.
15	15	LX2	REG2 Switching Node. Connect LX2 to the REG2 inductor. LX2 is high impedance when REG2 is shut down.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8660	MAX8661		
16	16	PG2	REG2 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
17	17	IN8	REG8 Input Power Connection. IN8 must be connected to IN.
18	18	IN	Main Battery Input. This input provides power to the IC. Connect a 0.47µF ceramic capacitor from IN to AGND.
19	19	AGND	Analog Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
20	20	V8	REG8 Always-On 3.3V LDO Output. REG8 is the first regulator that powers up in the MAX8660/MAX8661. REG8 is supplied from IN and supplies up to 30mA. V8 is internally pulled to AGND through 1.5kΩ during IN undervoltage or overvoltage lockout. Connect V8 to *VCC_BBATT* on Marvell PXA3xx processors.
21	21	LBF	Low-Battery Detect Falling Input. The LBF threshold is 1.20V. Connect LBF to LBR for 50mV hysteresis. Use a three-resistor voltage-divider for larger hysteresis. LBF sets the falling voltage at which $\overline{LBO}$ goes low. See the *Low-Battery Detector ($\overline{LBO}$, LBF, LBR)* section for more information.
22	22	LBR	Low-Battery Detect Rising Input. The LBR threshold is 1.25V. Connect LBF to LBR for 50mV hysteresis. Use a three-resistor voltage-divider for larger hysteresis. LBR sets the rising voltage at which $\overline{LBO}$ goes high. See the *Low-Battery Detector ($\overline{LBO}$, LBF, LBR)* section for more information.
23	23	$\overline{MR}$	Manual Reset Input. A low $\overline{MR}$ input causes $\overline{RSO}$ to go low and resets all serial programmed registers to their default values. See the *Reset Output ($\overline{RSO}$) and $\overline{MR}$ Input* section for more information.
24	24	RAMP	Ramp-Rate Input. Connect a resistor from RAMP to AGND to set the regulator ramp rates. See the *Ramp-Rate Control (RAMP)* section for more information.
25	25	EN5	REG5 Enable Input. Drive EN5 high to turn on REG5. EN5 has hysteresis so an RC can be used to implement manual sequencing with respect to other inputs. EN5 is typically driven by the *SYS_EN* output of an Marvell PXA3xx processor.
26	26	PG3	REG3 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
27	27	LX3	REG3 Switching Node. Connect LX3 to the REG3 inductor. LX3 is high impedance when REG3 is shut down.
28	28	PV3	REG3 Power Input. Connect a 4.7µF ceramic capacitor from PV3 to PG3. All PV pins and IN must be connected together externally.
29	29	$\overline{RSO}$	Open-Drain Reset Output. $\overline{RSO}$ typically connects to the *nRESET* input on an applications processor. An output low from the MAX8660/MAX8661 $\overline{RSO}$ resets all serial programmed registers to their default values and causes the processor to enter its reset state. See the *Reset Output ($\overline{RSO}$) and $\overline{MR}$ Input* section for more information.
30	30	V3	REG3 Voltage Sense Input. Connect V3 directly to the REG3 output voltage. The output voltage is adjustable from 0.725V to 1.8V through the serial interface. V3 is internally pulled to AGND through 550Ω when REG3 is shut down. V3 connects to *VCC_APPS* on Marvell PXA3xx processors.
31	31	EN34	REG3 and REG4 Active-High Hardware Enable Input. Drive EN34 high to enable both REG3 and REG4. Drive EN34 low to allow the serial interface to enable REG3 and REG4 independently. EN34 has hysteresis so an RC can be used to implement manual sequencing with respect to other inputs. EN34 is typically driven by the *PWR_EN* output of an Marvell PXA3xx processor. See the *REG3/REG4 Enable (EN34, EN3, EN4)* section for more information.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8660	MAX8661		
32	32	EN2	REG2 Enable Input. Drive EN2 high to turn on REG2. EN2 has hysteresis so that an RC can be used to implement manual sequencing with respect to other inputs. EN2 is typically driven by the *SYS_EN* output of an Marvell PXA3xx processor.
33	33	SRAD	Serial-Address Input. Connect SRAD to AGND for a 7-bit slave address of 0110 100 (0x68). Connect SRAD to IN to change the address to 0110 101 (0x6A). The eighth slave address bit is always zero since the MAX8660/MAX8661 are write-only. See the *Slave Address* section for more information.
34	—	PG1	REG1 Power Ground. Connect PG1, PG2, PG3, PG4, and AGND together. Refer to the MAX8660 EV kit data sheet for more information.
—	34	GND	Ground. Connect all GND pins to EP.
35	—	LX1	REG1 Switching Node. Connect LX1 to the REG1 inductor. LX1 is high impedance when REG1 is shutdown.
—	35	N.C.	No Internal Connection
36	—	PV1	REG1 Power Input. Connect a 4.7µF ceramic capacitor from PV1 to PG1. All PV pins and IN must be connected together externally.
—	36	PV	Power Input. All PV pins and IN must be connected together externally.
37	—	EN1	REG1 Enable Input. Drive EN1 high to turn on REG1. EN1 has hysteresis so that an RC can be used to implement manual sequencing with respect to other inputs. EN1 is typically driven by the *SYS_EN* output of an applications processor.
—	37	GND	Ground. Connect all GND pins to EP.
38	—	V1	REG1 Voltage Sense Input. Connect V1 directly to the REG1 output voltage. The output voltage of REG1 is selected by SET1. Connect V1 to *VCC_IOx* of the applications processor. V1 is internally pulled to AGND through 650Ω when REG1 is shut down.
—	38	GND	Ground. Connect all GND pins to EP.
39	—	SET1	REG1 Voltage Select Input. SET1 is a tri-level logic input. Connect SET1 to select the V1 output voltage as detailed in Table 3. The REG1 output voltage selected by SET1 is latched at the end of the REG1 soft-start period. Changes to SET1 after the startup period have no effect.
—	39	GND	Ground. Connect all GND pins to EP.
40	40	V4	REG4 Feedback Sense Input. Connect V4 directly to the REG4 output voltage. The REG4 output voltage is adjustable from 0.725V to 1.8V with the serial interface. V4 is internally pulled to AGND through 550Ω when REG4 is shut down. V4 powers *VCC_SRAM* on the applications processor.
—	—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PG1, PG2, PG3, PG4, and AGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

High-Efficiency, Low-IQ, PMICs with Dynamic Voltage Management for Mobile Applications

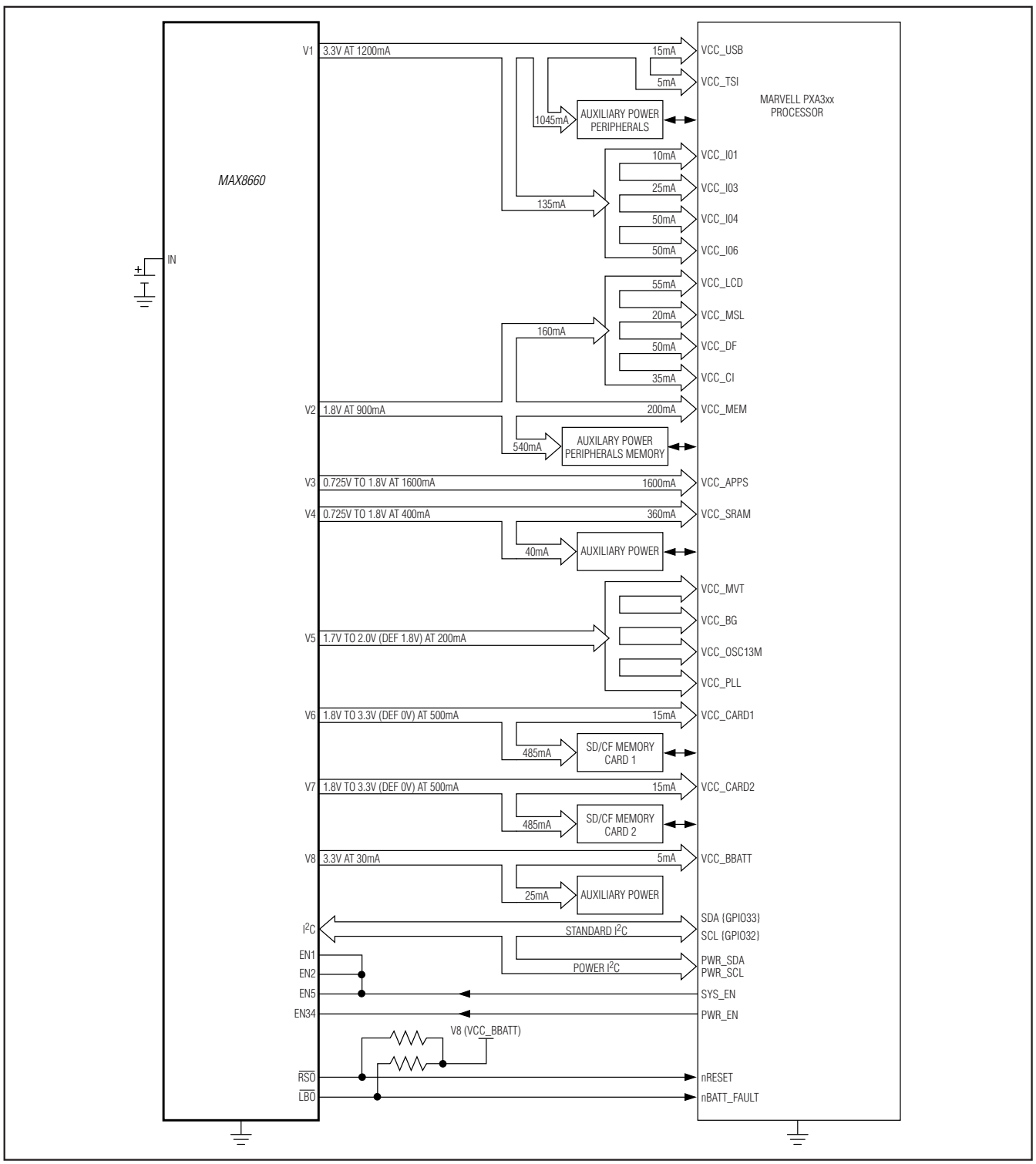


Figure 1. Example MAX8660 Connection to Marvell PXA3xx Processor. This is one example only. Other connections are also supported.

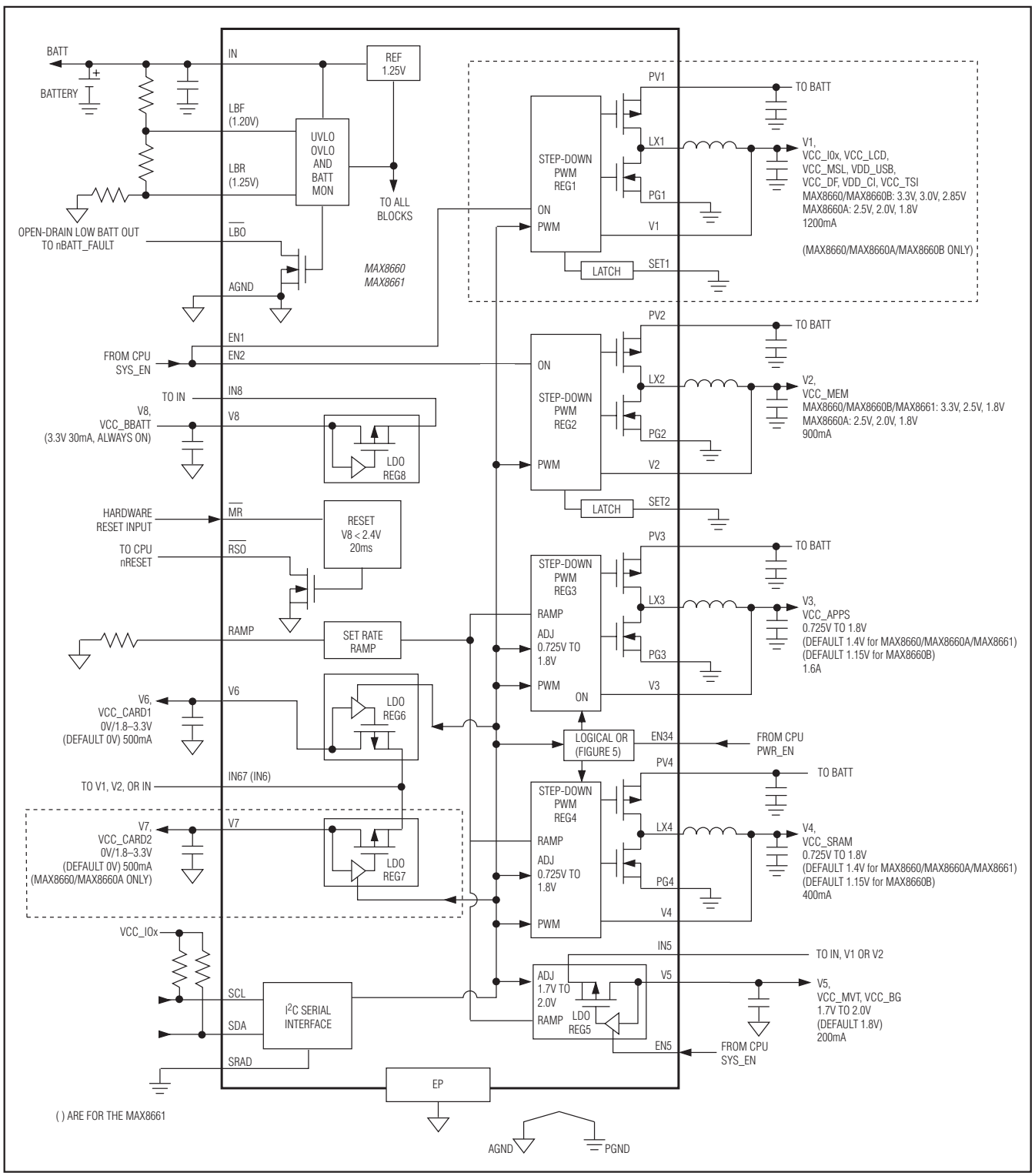


Figure 2. Functional Diagram

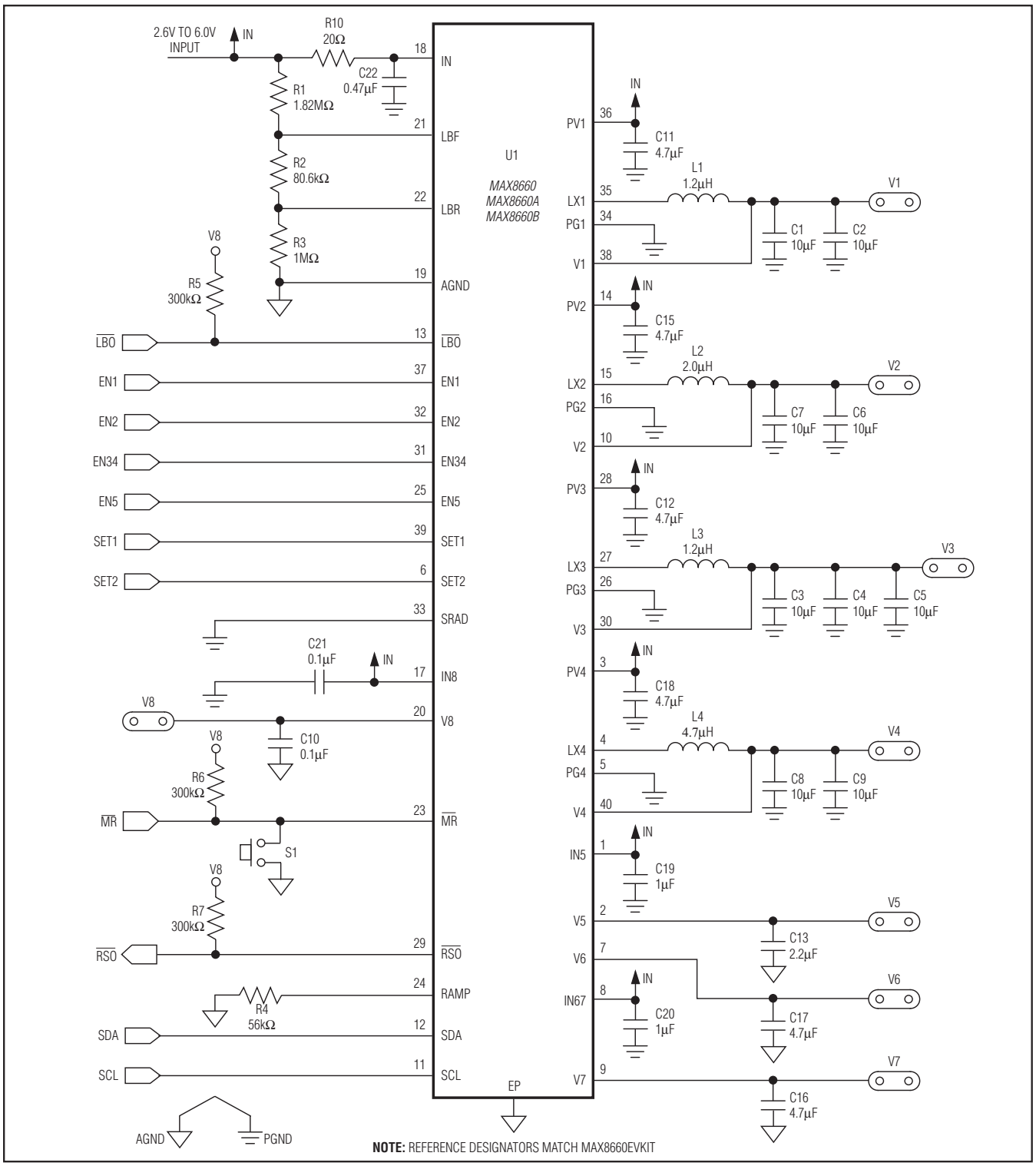


Figure 3. Typical Applications Circuit

Detailed Description

The MAX8660/MAX8661 PMICs are optimized for devices using the applications processors, including smart cellular phones, PDAs, Internet appliances, and other portable devices requiring substantial computing and multimedia capability and low power consumption. The MAX8660/MAX8661 comply with the specifications for Marvell's PXA300 family (PXA3xx) and Marvell's Armada 100 family (PXA16x) of processors.

As shown in Figure 2, the MAX8660 integrates eight high-performance, low-operating-current power supplies. REG1–REG4 are step-down DC-DC converters, and REG5–REG8 are linear regulators. Other functions include low-battery detection ($\overline{LBO}$), a reset output ($\overline{RSO}$), a manual reset input ($\overline{MR}$), and a 2-wire I²C serial interface. The MAX8661 functions the same as the MAX8660, but does not have the REG1 step-down regulator and the REG7 linear regulator.

The operating input voltage range is from 2.6V to 6.0V, allowing use with a 1-cell Li+ battery, 3-cell NiMH, or a 5V input. Input protection is provided with undervoltage and overvoltage lockouts. Overvoltage lockout protects the device against inputs up to 7.5V.

Maxim vs. Marvell PXA3xx Terminology

The MAX8660/MAX8661 are compatible with Marvell's PXA3xx processor. Figure 1 shows one of many possible connections between the PXA3xx processor and the MAX8660/MAX8661. To facilitate system development with PXA3xx processors, this document uses both Maxim and Marvell terminology. Marvell terminology appears in parentheses and italics. For example, this document refers to "V8 (*VCC_BBATT)"* because the MAX8660 V8 output powers the Marvell *VCC_BBATT* power domain. Tables 1 and 2 outline Maxim and Marvell terminology.

Table 1. Maxim and Marvell PXA3xx Power Domain Terminology

POWER DOMAIN	POWER DOMAIN ACCEPTABLE VOLTAGE	COMPATIBLE MAXIM POWER DOMAIN	DESCRIPTION
VCC_IO1 *VCC_IO3* *VCC_IO4* *VCC_IO6*	1.8V ±10% or 3.0V ±10% or 3.3V ±10%	V1 or V2	• Peripheral I/O supply for UARTs, standard I²C, power I²C, audio interface, SSPs, PWMs, etc. (*VCC_IO1,VCC_IO3, VCC_IO4, VCC_IO6*)
VCC_LCD *VCC_MSL* *VCC_CI* *VCC_DF*	1.8V ±10% or 3.0V ±10%	V1 or V2	• LCD interface logic (*VCC_LCD*) • Fast serial interface (*VCC_MSL*) • Camera flash interface (*VCC_CI*) • Data flash interface (*VCC_DF*)
VCC_MEM	1.8V ±100mV	V2	• I/O supply for high-speed memory
VCC_APPS	0.95V to 1.41V ±5%	V3	• Main processor core
VCC_SRAM	1.08V to 1.41V ±100mV	V4	• Internal SRAM memory
VCC_MVT *VCC_BG* *VCC_OSC13M* *VCC_PLL*	1.8V ±100mV	V5	• Internal logic and I/O blocks (*VCC_MVT*) • Bandgap reference (*VCC_BG*) • 13MHz oscillator (*VCC_OSC13M*) • Phase-locked loop (PLL) and oscillator (*VCC_PLL*)
VCC_CARD1	1.8V ±10% or 3.0V ±10% or 3.3V ±10%	V6	• Removable storage and USIM card supply
VCC_CARD2	1.8V ±10% or 3.0V ±10% or 3.3V ±10%	V7	• Removable storage and USIM card supply
VCC_BBATT	3.0V ±1V	V8	• Regulated battery voltage
VCC_USB	3.3V ±300mV	V1 or V2 (if programmed to 3.3V)	• Universal serial bus (*VCC_USB*)
VCC_TSI	3.3V ±300mV	V1 or V2 (if programmed to 3.3V)	• Touch-screen interface (*VCC_TSI*)