19-0885; Rev 0; 8/07

EVALUATION KIT AVAILABLE

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

General Description

The MAX8671X integrated power-management IC (PMIC) is ideal for use in portable media players and other handheld devices. In addition to five regulated output voltages, the MAX8671X integrates a 1-cell lithium ion (Li+) or lithium polymer (Li-Poly) charger and Smart Power Selector™ with dual (AC-to-DC adapter and USB) power inputs. The dual-input Smart Power Selector supports end products with dual or single power connectors. All power switches for charging and switching the system load between battery and external power are included on-chip. No external MOSFETs are required.

Maxim's Smart Power Selector makes the best use of limited USB or AC-to-DC adapter power. Battery charge current and input current limit are independently set. Input power not used by the system charges the battery. Charge current and DC current limit are programmable up to 1A while USB input current can be set to 100mA or 500mA. Automatic input selection switches the system load from battery to external power. Other features include overvoltage protection, charge status and fault outputs, power-OK monitors, charge timer, and battery thermistor monitor. In addition, on-chip thermal limiting reduces battery charge rate to prevent charger overheating.

The MAX8671X offers adjustable voltages for all outputs. Similar parts with factory-preset output voltages are also available (contact factory for availability).

Applications

Portable Audio Players

GPS Portable Navigators

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

Features

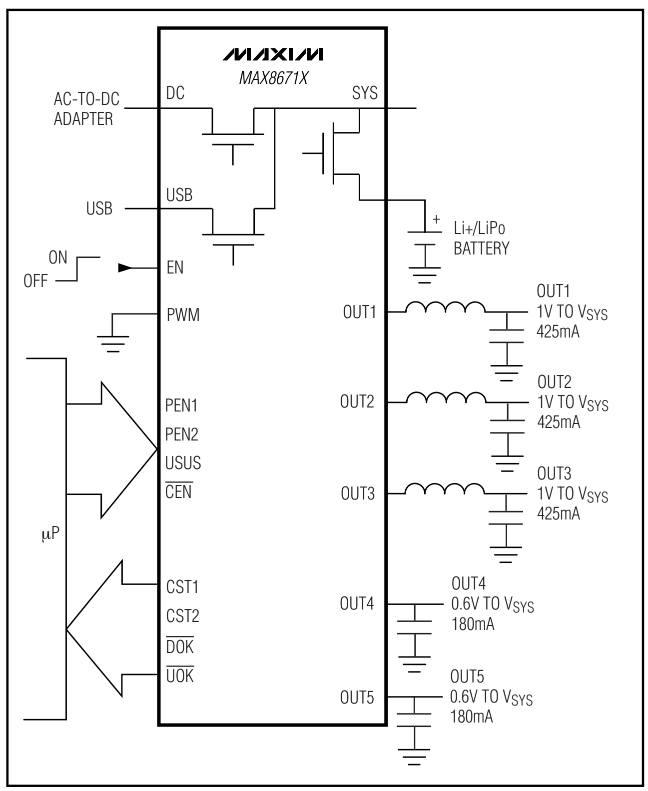
- ♦ **16V-Tolerant USB and DC Inputs**
- ♦ **Automatically Powers from External Power or Battery**
- ♦ **Operates with No Battery Present**
- ♦ **Single-Cell Li+/Li-Poly Charger**
- ♦ **Three 2MHz Step-Down Regulators**
  Up to 96% Efficiency
- ♦ **Two Low I_Q Linear Regulators**
- ♦ **Output Power-Up Sequencing**
- ♦ **Thermal-Overload Protection**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8671XETL+	-40°C to +85°C	40 Thin QFN-EP* 5mm x 5mm	T4055-1

+Denotes a lead-free package.
**EP = Exposed paddle.*

Simplified Applications Circuit



PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

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ABSOLUTE MAXIMUM RATINGS

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SYS, BAT, PV1, PV2, PV3 to AGND..........................-0.3V to +6V
PG1, PG2, PG3, AGND ....-0.3V to +0.3V
PV1, PV2, PV3 to SYS...-0.3V to +0.3V
VL to AGND ....-0.3V to +4.0V
CISET, DISET, BVSET, CT, THM to AGND..-0.3V to (V_{VL} + 0.3V)
PV4, PV5, BP, FB1, FB2, FB3 to AGND ....-0.3V to (V_{SYS} + 0.3V)
PEN2, USUS, $\overline{CEN}$, EN, PWM to AGND ....-0.3V to +6V
CST1, CST2, $\overline{DOK}$, $\overline{UOK}$ to AGND ....-0.3V to +6V
OUT4, FB4 to AGND ....-0.3V to (V_{PV4} + 0.3V)
OUT5, FB5 to AGND ....-0.3V to (V_{PV5} + 0.3V)
LX1, LX2, LX3 Continuous RMS Current (Note 1).................1.5A
BAT Continuous Current 1.5A
SYS Continuous Current 1.5A
Continuous Power Dissipation (T_A = +70°C)
40-Pin, 5mm x 5mm, Thin QFN (derate 35.7mW/°C above +70°C)...2857mW
Operating Junction Temperature.....................................+150°C
Storage Junction Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: LX_ has internal clamp diodes to PG_ and PV_. Applications that forward bias these diodes must take care not to exceed the package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; V_{THM} = V_L/2, $V_{PG\_}$ = V_{AGND} = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, V_{PEN1} = V_{PEN2} = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC POWER INPUT (V_{DC} = 5.0V, EN = low)							
DC Voltage Range	V_{DC}	Operating voltage		4.1		6.6	V
		Withstand voltage		0		14	
SYS Regulation Voltage	V_{SYS_REG}	V_{DC} = 6V, USUS = low, $\overline{CEN}$ = high, system current is less than the input current limit		5.2	5.3	5.4	V
DC Undervoltage Threshold	V_{DCL}	V_{DC} rising, 500mV typical hysteresis		3.95	4.00	4.05	V
DC Overvoltage Threshold	V_{DCH}	V_{DC} rising, 400mV typical hysteresis		6.8	6.9	7.0	V
DC Current Limit	I_{DCLIM}	V_{DC} = 6V, V_{SYS} = 5V USB unconnected, $\overline{CEN}$ = low, T_A = +25°C, VL = no load (Note 3)	PEN1 = low, PEN2 = low, USUS = low	90	95	100	mA
			PEN1 = low, PEN2 = high, USUS = low	450	475	500	
			PEN1 = high, R_{DISET} = 3kΩ	950	1000	1050	
R_{DISET} Resistance Range				3		6	kΩ
DC Quiescent Current	I_{DCIQ}	PEN1 = low, USUS = high			0.11		mA
		USUS = low, $\overline{CEN}$ = low; I_{SYS} = 0mA, I_{BAT} = 0mA, EN = low; VL no load			1.1		
		USUS = low, $\overline{CEN}$ = high; I_{SYS} = 0mA, V_{EN} = 0V, VL no load			0.7		
Minimum DC-to-BAT Voltage Headroom		V_{DC} falling, 200mV hysteresis		0	15	30	mV
Minimum DC-to-SYS Voltage Headroom		V_{DC} falling, 200mV hysteresis		0	15	30	mV
DC-to-SYS Dropout Resistance	R_{DS}	V_{DC} = 5V, I_{SYS} = 400mA, USUS = low			0.325	0.600	Ω

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND}$ = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2}$ = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC-to-SYS Soft-Start Time	$t_{SS\text{-}D\text{-}S}$	Starting DC when no USB present		1.0		ms
		Starting DC with USB present		35		µs
DC Thermal-Limit Temperature		Die temperature at which current limit is reduced		+100		°C
DC Thermal-Limit Gain		Amount of input current reduction above thermal-limit temperature		5		%/°C
USB POWER INPUT (V_{USB} = 5.0V, EN = low)						
USB Voltage Range	V_{USB}	Operating voltage	4.1		6.6	V
		Withstand voltage	0		14	
SYS Regulation Voltage	V_{SYS_REG}	V_{USB} = 6V, USUS = low, $\overline{CEN}$ = high, system current is less than the input current limit	5.2	5.3	5.4	V
USB Undervoltage Threshold	V_{USBL}	V_{USB} rising, 500mV hysteresis	3.95	4.0	4.05	V
USB Overvoltage Threshold	V_{USBH}	V_{USB} rising, 400mV hysteresis	6.8	6.9	7.0	V
USB Current Limit	I_{USBLIM}	V_{USB} = 6V, V_{SYS} = 5V, DC unconnected, $\overline{CEN}$ = low, T_A = +25°C, I_{VL} = 0A (Note 3); PEN2 = low, USUS = low	90	95	100	mA
		V_{USB} = 6V, V_{SYS} = 5V, DC unconnected, $\overline{CEN}$ = low, T_A = +25°C, I_{VL} = 0A (Note 3); PEN2 = high, USUS = low	450	475	500	
USB Quiescent Current	I_{USBIQ}	USUS = high		0.11		mA
		USUS = low, $\overline{CEN}$ = low; I_{SYS} = 0mA, I_{BAT} = 0mA, VL no load		1.1	2.0	
		USUS = low, $\overline{CEN}$ = high; I_{SYS} = 0mA, VL no load		0.7	1.3	
Minimum USB-to-BAT Voltage Headroom		V_{USB} falling, 200mV hysteresis	0	15	30	mV
Minimum USB-to-SYS Voltage Headroom		V_{USB} falling, 200mV hysteresis	0	15	30	mV
USB-to-SYS Dropout Resistance	R_{US}	V_{USB} = 5V, I_{SYS} = 400mA, USUS = low		0.325	0.600	Ω
USB-to-SYS Soft-Start Time	$t_{SS\text{-}U\text{-}S}$			1.0		ms
USB Thermal-Limit Temperature		Die temperature at which current limit is reduced		100		°C
USB Thermal-Limit Gain		Amount of input current reduction above thermal-limit temperature		5		%/°C
SYSTEM (V_{DC} = 5.0V, EN = low)						
System Operating Voltage Range	V_{SYS}		2.6		5.5	V
System Undervoltage Threshold	V_{UVLO_SYS}	SYS falling, 100mV hysteresis	2.45	2.50	2.55	V

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND}$ = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2}$ = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BAT-to-SYS Reverse Regulation Voltage	V_{BSREG}	DC or USB and BAT are sourcing current	BAT is sourcing 105mA	65	82	115	mV
			BAT is sourcing 905mA		130		
Quiescent Current	I_{PV1} + I_{PV2} + I_{PV3} + I_{PV4} + I_{PV5} + I_{SYS}	DC and USB unconnected, EN = low, V_{BAT} = 4V			0	10	µA
		$V_{DC} = V_{USB}$ = 5V, USUS = high, PEN1 = low, EN = low, V_{BAT} = 4V			0	10	
		DC and USB unconnected, EN = high, V_{BAT} = 4V (step-down converters are not in dropout), PWM = low (Note 4)			155	285	
		DC and USB unconnected, EN = high, V_{BAT} = 2.8V (at least one step-down converter is in dropout), PWM = low (Note 4)			425	550	
		$V_{DC} = V_{USB}$ = 5V, USUS = high, EN = high, V_{BAT} = 4V, PWM = low (Note 4)			180	320	
		DC and USB unconnected, EN = high, V_{BAT} = 4.0V, PWM = high			9		mA
BATTERY CHARGER (V_{DC} = 5.0V, EN = low)							
BAT-to-SYS On-Resistance	R_{BS}	V_{USB} = 0V, V_{BAT} = 4.2V, I_{SYS} = 1A			0.08	0.16	Ω
BAT Regulation Voltage (Figure 6)	V_{BATREG}	BVSET = VL or BVSET unconnected	T_A = +25°C	4.174	4.200	4.221	V
			T_A = -40°C to +85°C	4.145	4.200	4.242	
		BVSET = AGND	T_A = +25°C	4.073	4.100	4.121	
			T_A = -40°C to +85°C	4.047	4.100	4.141	
		R_{BVSET} = 49.9kΩ to AGND	T_A = +25°C	4.325	4.350	4.376	
			T_A = -40°C to +85°C	4.297	4.350	4.398	
BAT Recharge Threshold	$V_{BATRCHG}$	(Note 5)		-170	-120	-70	mV
BAT Prequalification Threshold	V_{BATPRQ}	V_{BAT} rising, 180mV hysteresis, Figure 6		2.9	3.0	3.1	V
R_{CISET} Resistance Range		Guaranteed by BAT fast-charge current limit		3		15	kΩ
CISET Voltage	V_{CISET}	R_{CISET} = 7.5kΩ, I_{BAT} = 267mA, Figure 9		0.9	1.0	1.1	V

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1\mu F$, $C_{OUT5} = 1\mu F$, $C_{SYS} = 10\mu F$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3k\Omega$, $R_{CISET} = 3k\Omega$, $C_{VL} = 0.1\mu F$, $C_{CT} = 0.15\mu F$, $C_{BP} = 0.01\mu F$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BAT Fast-Charge Current Limit		Low-power USB charging from the USB input, DC unconnected, $R_{CISET} = 3k\Omega$, PEN2 = low, USUS = low	87	92	100	mA
		Low-power USB charging from the DC input, $R_{CISET} = 3k\Omega$, PEN1 = low, PEN2 = low, USUS = low	87	92	100	
		High-power USB charging from the USB input, DC unconnected, $R_{CISET} = 3k\Omega$, PEN2 = high, USUS = low	450	472	500	
		High-power USB charging from the DC input, $R_{CISET} = 3k\Omega$, PEN2 = high, USUS = low	450	472	500	
		AC-to-DC adapter charging from the DC input, $R_{DISET} = 3k\Omega$, $R_{CISET} = 15k\Omega$, PEN1 = high	170	200	230	
		AC-to-DC adapter charging from the DC input, $R_{DISET} = 3k\Omega$, $R_{CISET} = 7.5k\Omega$, PEN1 = high	375	400	425	
		AC-to-DC adapter charging from the DC input, $R_{DISET} = 3k\Omega$, $R_{CISET} = 3.74k\Omega$, PEN1 = high	750	802	850	
BAT Prequalification Current		$V_{BAT} = 2.5V$, $R_{CISET} = 3.74k\Omega$	65	82	100	mA
Top-Off Threshold		$T_A = +25°C$, $R_{CISET} = 3.74k\Omega$ (Note 6)	20	30	40	mA
BAT Leakage Current		EN = low, $T_A = +25°C$: No DC or USB power connected		0	+5	µA
		EN = low, $T_A = +25°C$: DC and/or USB power connected, $\overline{CEN}$ = high	-5	1	+5	
Charger Soft-Start Time	t_{SS_CHG}	Slew rate		450		mA/ms
		Time from 0mA to 500mA		1.10		ms
		Time from 0mA to 100mA		0.22		
		Time from 100mA to 500mA		0.88		
Timer Accuracy		$C_{CT} = 0.15\mu F$	-20		+20	%
Timer Suspend Threshold		CISET voltage when the fast-charge timer suspends; 300mV translates to 20% of the maximum fast-charge current limit	250	300	350	mV
Timer Extend Threshold		CISET voltage when the fast-charge timer suspends; 750mV translates to 50% of the maximum fast-charge current limit	700	750	800	mV

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1µF$, $C_{OUT5} = 1µF$, $C_{SYS} = 10µF$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3kΩ$, $R_{CISET} = 3kΩ$, $C_{VL} = 0.1µF$, $C_{CT} = 0.15µF$, $C_{BP} = 0.01µF$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prequalification Time	t_{PQ}	C_{CT} = 0.15µF		33		min
Fast-Charge Time	t_{FC}	C_{CT} = 0.15µF		660		min
Top-Off Time	t_{TO}			15		s
THERMISTOR INPUT (THM) (V_{DC} = 5.0V, EN = low)						
THM Threshold, Cold	V_{THMC}	V_{THM} rising, 65mV hysteresis	73.0	74.0	75.5	% of V_{VL}
THM Threshold, Hot	V_{THMH}	V_{THM} falling, 65mV hysteresis	27.0	28.4	30.0	% of V_{VL}
THM Input Leakage Current	I_{THM}	THM = AGND or VL, T_A = +25°C	-0.100	0.001	+0.200	µA
		THM = AGND or VL, T_A = +85°C		0.01		
POWER SEQUENCING (Figures 11 and 12)						
EN to REG3 Enable Delay	t_{D1}			120		µs
REG1 Soft-Start Time	t_{SS1}			2.6		ms
REG3 to REG1/2 Delay	t_{D2}			0.4		ms
REG2 Soft-Start Time	t_{SS2}			2.6		ms
REG3 Soft-Start Time	t_{SS3}			2.6		ms
REG1/2 to REG4 Delay	t_{D3}			0.3		ms
REG4 Soft-Start Time	t_{SS4}			3.0		ms
REG5 Soft-Start Time	t_{SS5}			3.0		ms
REGULATOR THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_J rising		+165		°C
Thermal Shutdown Hysteresis				15		°C
REG1—SYNCHRONOUS STEP-DOWN CONVERTER						
Input Voltage		PV1 supplied from SYS		V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_L = 0.13Ω (Note 7)	425			mA
FB1 Voltage		(Note 8)	0.997	1.012	1.028	V
Adjustable Output Voltage Range			1		V_{SYS}	V
FB1 Leakage Current		V_{FB1} = 1.012V, T_A = +25°C	-50	-5	+50	nA
		V_{FB1} = 1.012V, T_A = +85°C		-5		
Load Regulation		PWM mode		4.4		%/A
Line Regulation		PWM mode (Note 9)		1		%/D
p-Channel On-Resistance		V_{PV1} = 4V, I_{LX1} = 180mA		165	330	mΩ
n-Channel On-Resistance		V_{PV1} = 4V, I_{LX1} = 180mA		200	400	mΩ
p-Channel Current-Limit Threshold			0.555	0.615	0.675	A

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{CEN}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1µF$, $C_{OUT5} = 1µF$, $C_{SYS} = 10µF$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3kΩ$, $R_{CISET} = 3kΩ$, $C_{VL} = 0.1µF$, $C_{CT} = 0.15µF$, $C_{BP} = 0.01µF$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, $T_A = -40°C$ to $+85°C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Skip Mode Transition Current		(Note 10)			60		mA
n-Channel Zero-Crossing Threshold					10		mA
Maximum Duty Cycle					100		%
Minimum Duty Cycle		PWM mode			12.5		%
Internal Oscillator Frequency				1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN = low, resistance from LX1 to PG1		0.5	1.0	2.0	kΩ
REG2—SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV2 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_L = 0.13Ω (Note 7)		425			mA
FB2 Voltage		(Note 8)		0.997	1.012	1.028	V
Adjustable Output Voltage Range				1		V_{SYS}	V
FB2 Leakage Current		V_{FB2} = 1.012V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-50		
Load Regulation		PWM mode			4.4		%/A
Line Regulation		PWM mode (Note 9)			1		%/D
p-Channel On-Resistance		V_{PV2} = 4V, I_{LX2} = 180mA			200	400	mΩ
n-Channel On-Resistance		V_{PV2} = 4V, I_{LX2} = 180mA			150	265	mΩ
p-Channel Current-Limit Threshold				0.555	0.615	0.675	A
Skip Mode Transition Current		(Note 10)			60		mA
n-Channel Zero-Crossing Threshold					10		mA
Maximum Duty Cycle					100		%
Minimum Duty Cycle		PWM mode			12.5		%
Internal Oscillator Frequency				1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN = low, resistance from LX2 to PG2		0.5	1.0	2.0	kΩ
REG3—SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV3 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_L = 0.13Ω (Note 7)		425			mA
FB3 Voltage		(Note 8)		0.997	1.012	1.028	V
Adjustable Output Voltage Range				1		V_{SYS}	V
FB3 Leakage Current		V_{FB2} = 1.012V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-50		
Load Regulation		PWM mode			4.4		%/A

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; V_{THM} = V_L/2, $V_{PG\_}$ = V_{AGND} = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, V_{PEN1} = V_{PEN2} = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Regulation		PWM mode (Note 9)			1		%/D
p-Channel Current-Limit Threshold				0.555	0.615	0.675	A
Skip Mode Transition Current		(Note 10)			60		mA
n-Channel Zero-Crossing Threshold					10		mA
p-Channel On-Resistance		V_{PV3} = 4V, I_{LX3} = 180mA			230	460	mΩ
n-Channel On-Resistance		V_{PV3} = 4V, I_{LX3} = 180mA			120	210	mΩ
Maximum Duty Cycle					100		%
Minimum Duty Cycle		PWM mode			12.5		%
Internal Oscillator Frequency				1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN = low, resistance from LX3 to PG3		0.5	1.0	2.0	kΩ
REG4—LINEAR REGULATOR							
PV4 Operating Range	V_{PV4}			1.7		V_{SYS}	V
PV4 Undervoltage Lockout Threshold		V_{PV4} rising, 100mV hysteresis		1.55	1.60	1.65	V
FB4 Voltage		No load		0.582	0.600	0.618	V
FB4 Leakage Current		V_{FB4} = 0.6V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-5		
Drop-Out Resistance		PV4 to OUT4, V_{PV4} = 3.3V			0.45		Ω
		PV4 to OUT4, V_{PV4} = 2.0V			0.75	1.8	
Current Limit		V_{FB4} = 0.54V		200	230	265	mA
		V_{FB4} = 0V			235		
Output Noise		10Hz to 100kHz; C_{OUT4} = 3.3µF, I_{OUT4} = 10mA, V_{PV4} = 2V, V_{OUT4} set for 1.8V			120		µV_{RMS}
PSRR		f = 1kHz, I_{OUT4} = 10mA, V_{PV4} = 2V, V_{OUT4} set for 1.8V			67		dB
		f = 10kHz, I_{OUT4} = 10mA, V_{PV4} = 2V, V_{OUT4} set for 1.8V			50		
Internal Discharge Resistance in Shutdown		EN = low, resistance from OUT4 to AGND		0.5	1.0	2.0	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{\text{UOK}}$, $\overline{\text{DOK}}$, LX_ unconnected; $V_{THM} = V_L/2$, $V_{PG\_} = V_{AGND} = 0V$, $V_{BAT} = 4V$, $\overline{\text{CEN}}$ = low, USUS = low, EN = high, $V_{PEN1} = V_{PEN2} = 3.3V$, $V_{PWM} = 0V$, $C_{OUT4} = 1\mu F$, $C_{OUT5} = 1\mu F$, $C_{SYS} = 10\mu F$, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, $R_{DISET} = 3k\Omega$, $R_{CISET} = 3k\Omega$, $C_{VL} = 0.1\mu F$, $C_{CT} = 0.15\mu F$, $C_{BP} = 0.01\mu F$, $V_{FB1} = 1.1V$, $V_{FB2} = 1.1V$, $V_{FB3} = 1.1V$, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REG5—LINEAR REGULATOR							
PV5 Operating Range	V_{PV5}			1.7		V_{SYS}	V
PV5 Undervoltage Lockout Threshold		V_{PV5} rising, 100mV hysteresis		1.55	1.60	1.65	V
FB5 Voltage		No load		0.582	0.600	0.618	V
FB5 Leakage Current		$V_{FB5} = 0.6V$	T_A = +25°C	-50	-5	+50	nA
FB5 Leakage Current		$V_{FB5} = 0.6V$	T_A = +85°C		-5		nA
Drop-Out Resistance		V_{PV5} to OUT5, $V_{PV5} = 3.3V$			0.45		Ω
Drop-Out Resistance		V_{PV5} to OUT5, $V_{PV5} = 2.0V$			0.75	1.8	Ω
Current Limit		$V_{FB5} = 0.54V$		200	230	265	mA
Current Limit		$V_{FB5} = 0V$			235		mA
Output Noise		10Hz to 100kHz, $C_{OUT5} = 2.2\mu F$, $I_{OUT5} = 10mA$, $V_{PV5} = 3.5V$, V_{OUT5} set for 3.3V			180		μV_{RMS}
PSRR		f = 1kHz, $I_{OUT5} = 10mA$, $V_{PV5} = 3.5V$, V_{OUT5} set for 3.3V			62		dB
PSRR		f = 10kHz, $I_{OUT5} = 10mA$, $V_{PV5} = 3.5V$, V_{OUT5} set for 3.3V			44		dB
Internal Discharge Resistance in Shutdown		EN = low, resistance from OUT5 to AGND		0.5	1.0	2.0	kΩ
VL—LINEAR REGULATOR							
VL Voltage	V_{VL}	I_{VL} = 0mA to 3mA		3.0	3.3	3.6	V
LOGIC ($\overline{\text{UOK}}$, $\overline{\text{DOK}}$, PEN1, PEN2, USUS, $\overline{\text{CEN}}$, CST1, CST2, EN, PWM)							
Logic Input-Voltage Low		V_{USB} or V_{DC} = 4.1V to 6.6V, V_{SYS} = 2.6V to 5.5V				0.6	V
Logic Input-Voltage High		V_{USB} or V_{DC} = 4.1V to 6.6V, V_{SYS} = 2.6V to 5.5V		1.3			V
Logic Input Leakage Current		V_{LOGIC} = 0V to 5.5V	T_A = +25°C		0.001	1	µA
Logic Input Leakage Current		V_{LOGIC} = 0V to 5.5V	T_A = +85°C		0.01		µA
Logic Output-Voltage Low		$I_{SINK} = 1mA$			10	30	mV
Logic Output-High Leakage Current		$V_{LOGIC} = 5.5V$	T_A = +25°C		0.001	1	µA
Logic Output-High Leakage Current		$V_{LOGIC} = 5.5V$	T_A = +85°C		0.01		µA
TRI-STATE INPUT (BVSET)							
BVSET Input-Voltage Low		V_{USB} or V_{DC} = 4.1V to 6.6V				0.3	V
BVSET Input-Voltage Mid		V_{USB} or V_{DC} = 4.1V to 6.6V		1.2		V_{VL} - 1.2	V

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

ELECTRICAL CHARACTERISTICS (continued)

(DC, USB, BVSET, $\overline{UOK}$, $\overline{DOK}$, LX_ unconnected; V_{THM} = V_L/2, $V_{PG\_}$ = V_{AGND} = 0V, V_{BAT} = 4V, $\overline{CEN}$ = low, USUS = low, EN = high, V_{PEN1} = V_{PEN2} = 3.3V, V_{PWM} = 0V, C_{OUT4} = 1µF, C_{OUT5} = 1µF, C_{SYS} = 10µF, PV1 = PV2 = PV3 = PV4 = PV5 = SYS, R_{DISET} = 3kΩ, R_{CISET} = 3kΩ, C_{VL} = 0.1µF, C_{CT} = 0.15µF, C_{BP} = 0.01µF, V_{FB1} = 1.1V, V_{FB2} = 1.1V, V_{FB3} = 1.1V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BVSET Input-Voltage High		V_{USB} or V_{DC} = 4.1V to 6.6V	V_{VL} - 0.3		V_{VL} + 0.3	V
Internal BVSET Pullup Resistance				52.5		kΩ
External BVSET Pulldown Resistance for Midrange Voltage	R_{BVSET}		45	50	55	kΩ

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 3: The USB/DC current limit does not include the VL output current. See the *VL Linear Regulator* section for more information.

Note 4: Quiescent current excludes the energy needed for the REG1–REG5 external resistor-dividers. All typical operating characteristics include the energy for the REG1–REG5 external resistor-dividers. For the circuit of Figure 1, the typical quiescent current with DC and USB unconnected, EN = high, V_{BAT} = 4V, and PWM = low is 175µA.

Note 5: The charger transitions from done to fast-charge mode at this BAT recharge threshold (Figure 7).

Note 6: The charger transitions from fast-charge to top-off mode at this top-off threshold (Figure 7).

Note 7: The maximum output current is guaranteed by correlation to the p-channel current-limit threshold, p-channel on-resistance, n-channel on-resistance, oscillator frequency, input voltage range, and output voltage range. The parameter is stated for a 4.7µH inductor with 0.13Ω series resistance. See the *Step-Down Converter Output Current* section for more information.

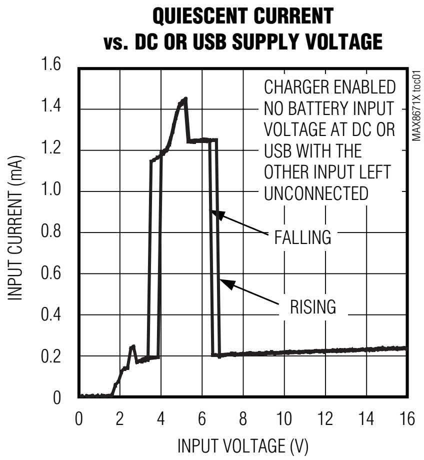
Note 8: The step-down output voltages are 1% high with no load due to the load-line architecture. When calculating the external resistor-dividers, use an FB_ voltage of 1.000V.

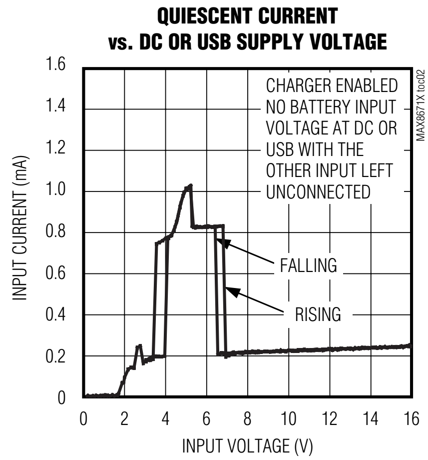
Note 9: Line regulation for the step-down converters is measured as $\Delta V_{OUT}/\Delta D$, where D is the duty cycle (approximately V_{OUT}/V_{IN}).

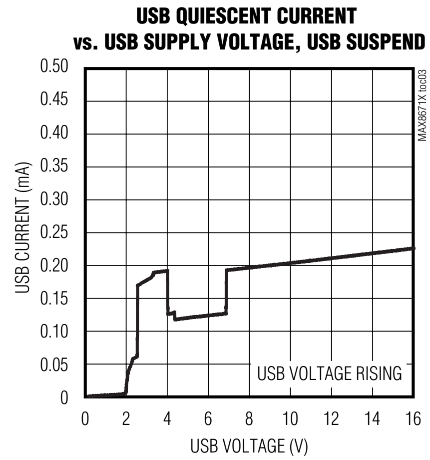
Note 10: The skip mode current threshold is the transition point between fixed-frequency PWM operation and skip mode operation. The specification is given in terms of output load current for inductor values shown in the typical application circuits.

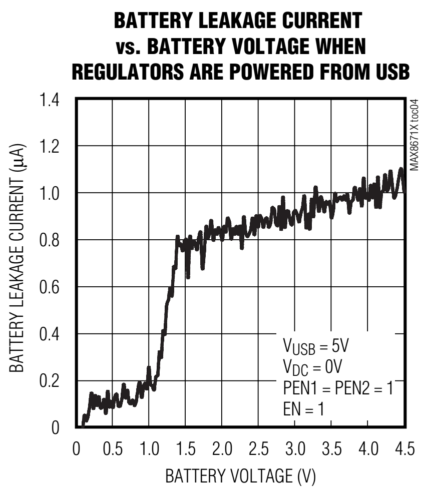
Typical Operating Characteristics

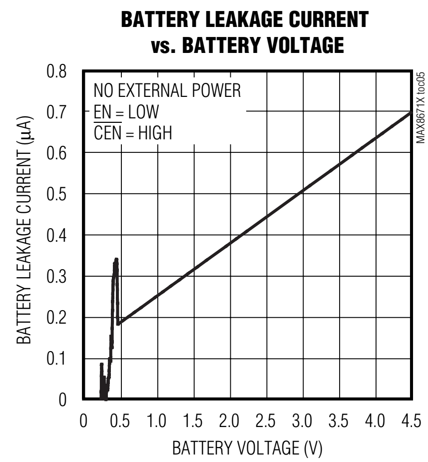
(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)









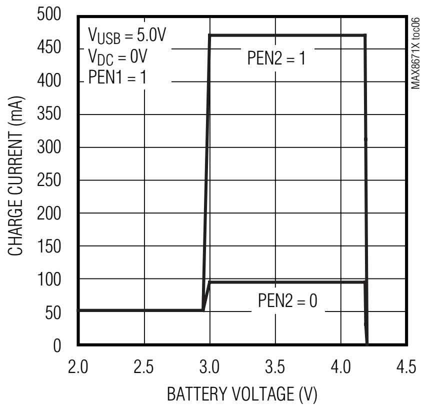


PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

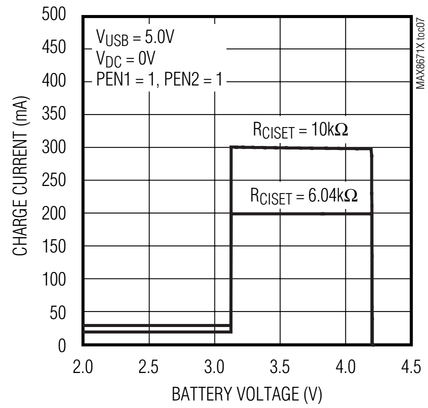
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

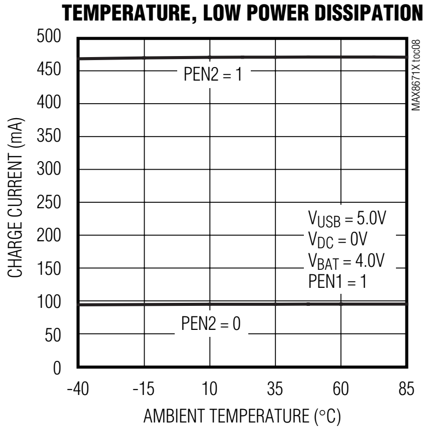
CHARGE CURRENT vs. BATTERY VOLTAGE WITH USB INPUT



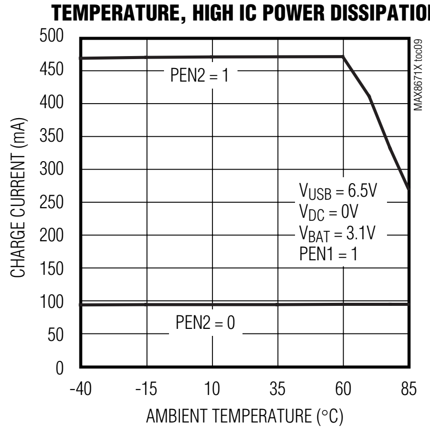
CHARGE CURRENT vs. BATTERY VOLTAGE



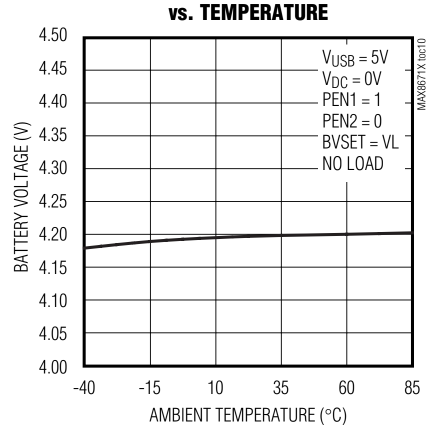
CHARGE CURRENT vs. AMBIENT TEMPERATURE, LOW POWER DISSIPATION



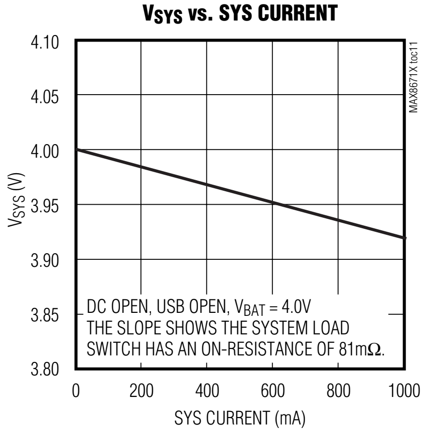
CHARGE CURRENT vs. AMBIENT TEMPERATURE, HIGH IC POWER DISSIPATION



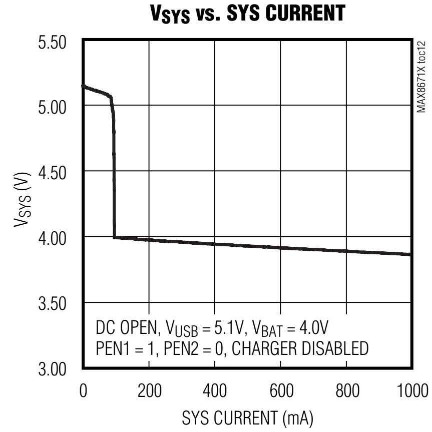
BATTERY REGULATION VOLTAGE vs. TEMPERATURE



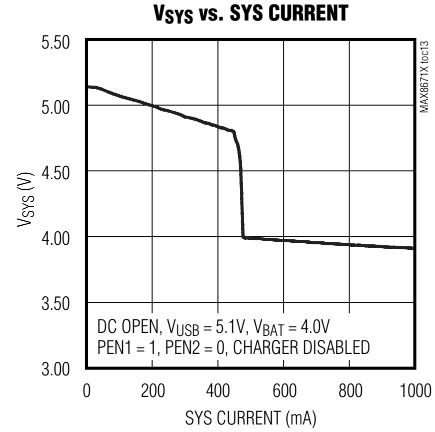
V_{SYS} vs. SYS CURRENT



V_{SYS} vs. SYS CURRENT



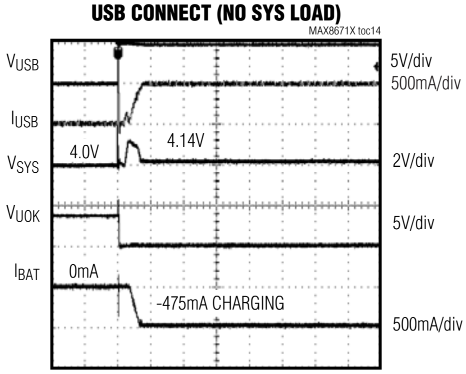
V_{SYS} vs. SYS CURRENT



Typical Operating Characteristics (continued)

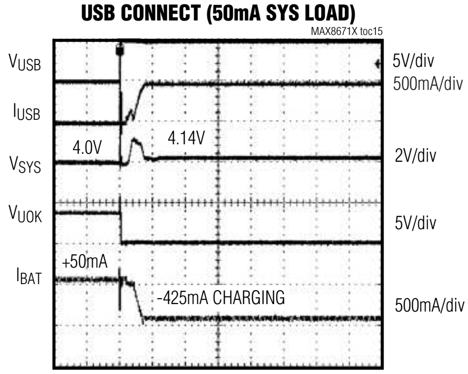
(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

USB CONNECT (NO SYS LOAD)



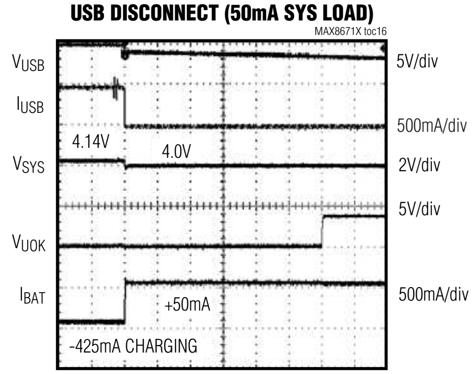
2ms/div
0mA LOAD ON SYS, 4.0V BATTERY, 5.0V USB INPUT

USB CONNECT (50mA SYS LOAD)



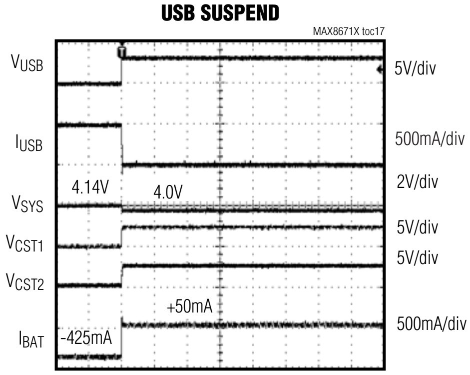
2ms/div
50mA LOAD ON SYS, 4.0V BATTERY, 5.0V USB INPUT

USB DISCONNECT (50mA SYS LOAD)



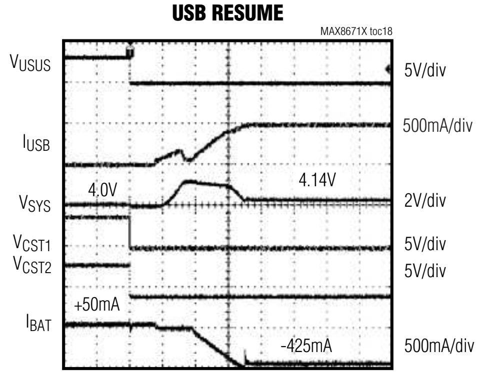
2ms/div
50mA LOAD ON SYS, 4.0V BATTERY, 5.0V USB INPUT

USB SUSPEND



400µs/div
50mA LOAD ON SYS, 4.0V BATTERY, 5.0V USB INPUT

USB RESUME



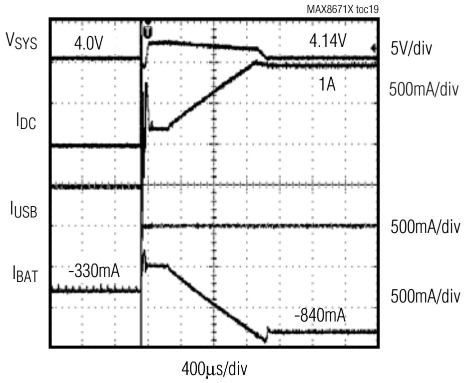
400µs/div
50mA LOAD ON SYS, 4.0V BATTERY, 5.0V USB INPUT

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Typical Operating Characteristics (continued)

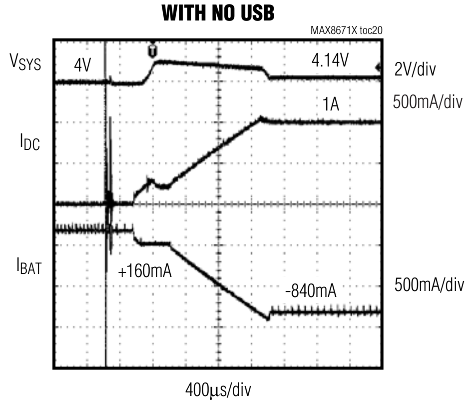
(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

AC-TO-DC ADAPTER CONNECT WITH USB



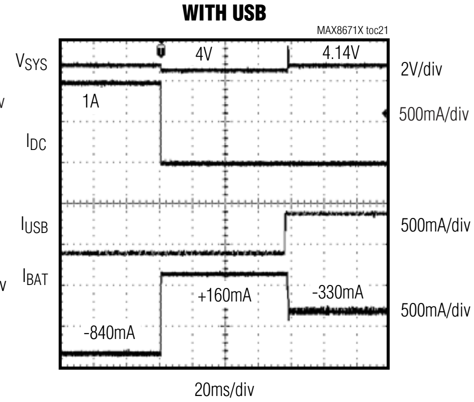
25Ω LOAD ON SYS, PEN1 = PEN2 = HIGH 1A DC LIMIT, R_{DISET} = 3.01kΩ

AC-TO-DC ADAPTER CONNECT WITH NO USB



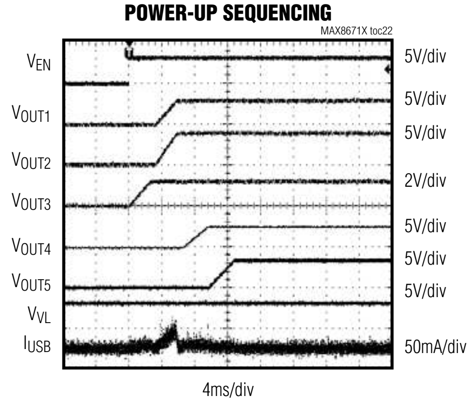
25Ω LOAD ON SYS, PEN1 = PEN2 = HIGH 1A DC LIMIT

AC-TO-DC ADAPTER DISCONNECT WITH USB



25Ω LOAD ON SYS, PEN1 = PEN2 = HIGH 1A DC LIMIT

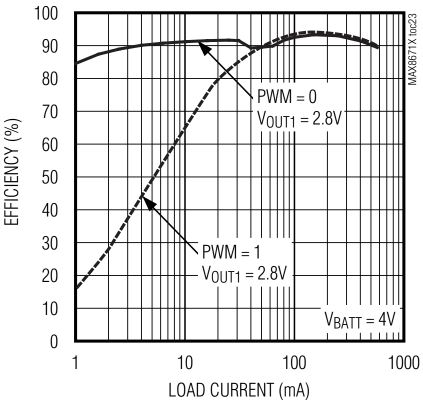
POWER-UP SEQUENCING



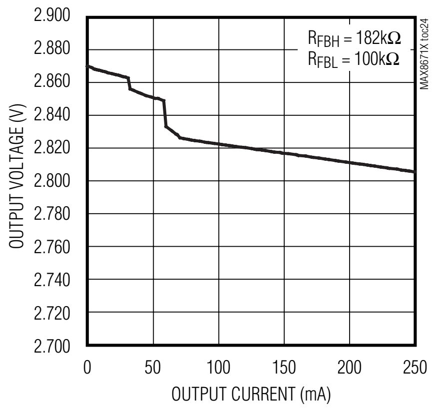
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

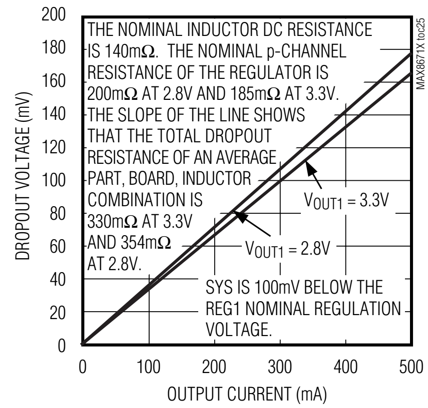
REG1 EFFICIENCY vs. LOAD CURRENT



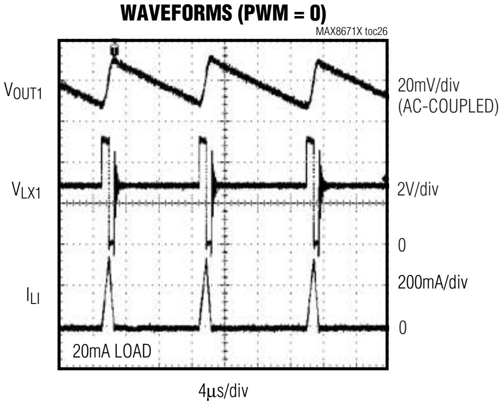
REG1 LOAD REGULATION



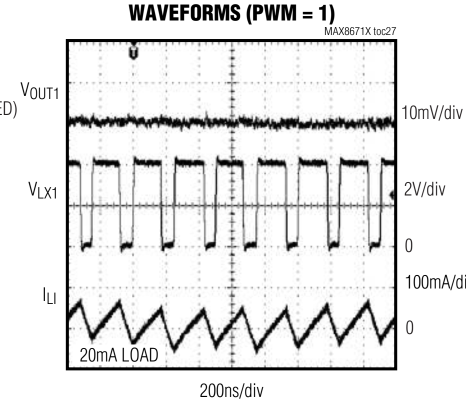
REG1 DROPOUT VOLTAGE vs. LOAD CURRENT



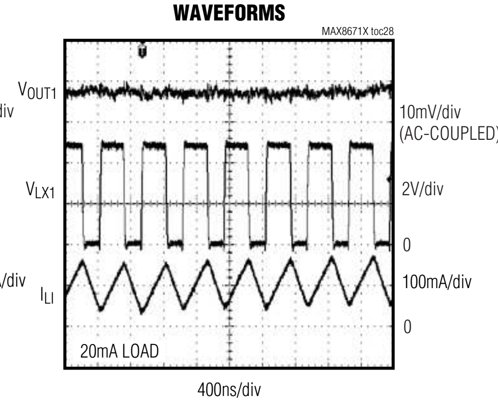
REG1 LIGHT-LOAD SWITCHING WAVEFORMS (PWM = 0)



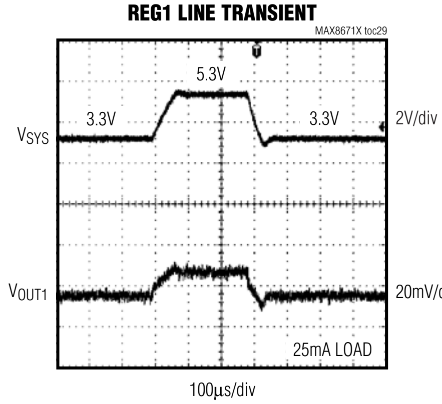
REG1 LIGHT-LOAD SWITCHING WAVEFORMS (PWM = 1)



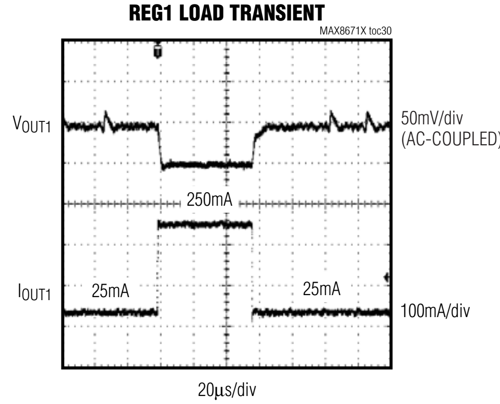
REG1 HEAVY-LOAD SWITCHING WAVEFORMS



REG1 LINE TRANSIENT



REG1 LOAD TRANSIENT

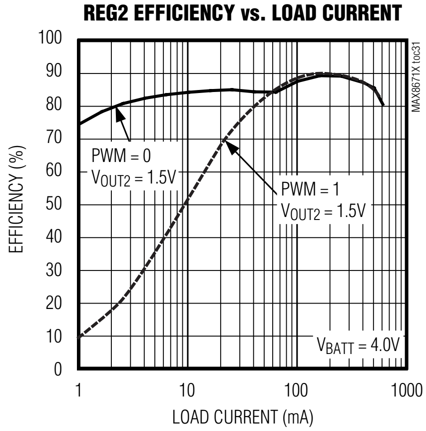


PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

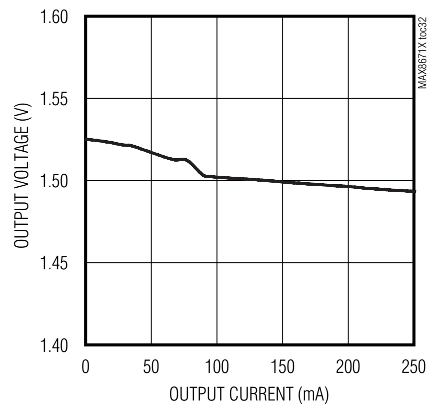
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

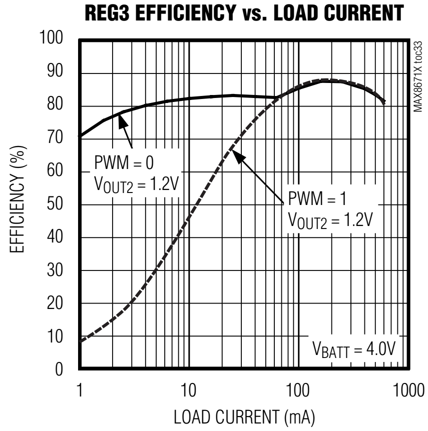
REG2 EFFICIENCY vs. LOAD CURRENT



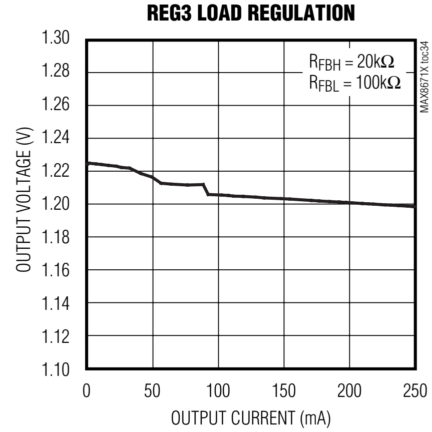
REG2 LOAD REGULATION



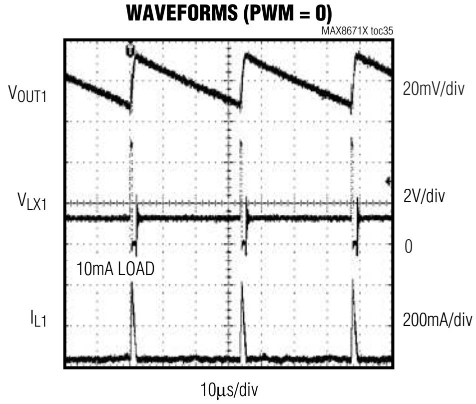
REG3 EFFICIENCY vs. LOAD CURRENT



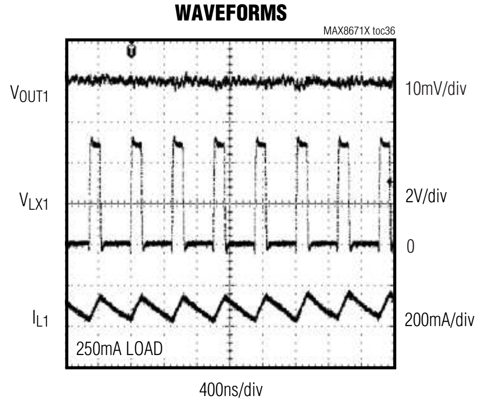
REG3 LOAD REGULATION



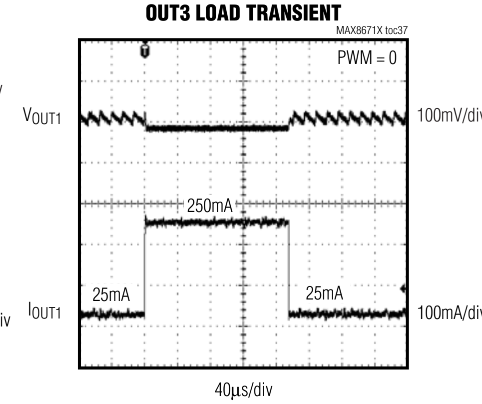
OUT3 LIGHT-LOAD SWITCHING WAVEFORMS (PWM = 0)



OUT3 HEAVY-LOAD SWITCHING WAVEFORMS



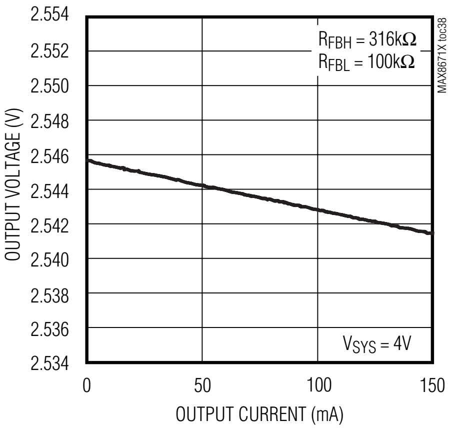
OUT3 LOAD TRANSIENT



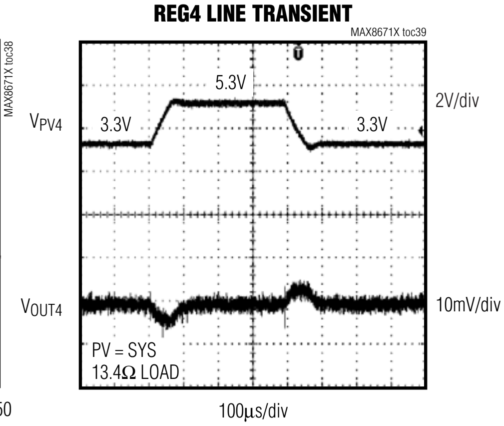
Typical Operating Characteristics (continued)

(Circuit of Figure 1, I_{VL} = 0mA, T_A = +25°C, unless otherwise noted.)

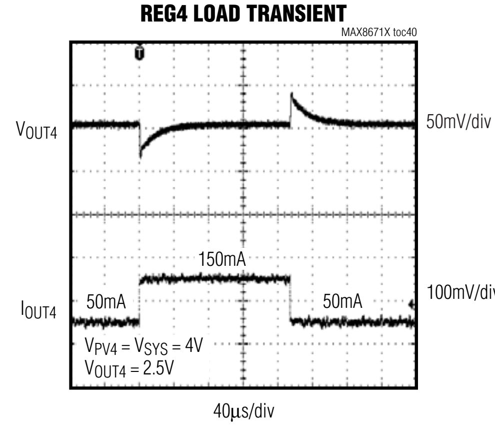
REG4 LOAD REGULATION



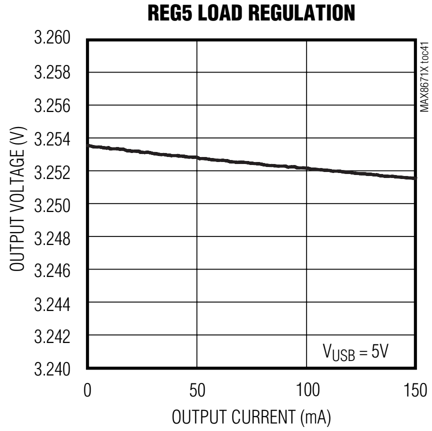
REG4 LINE TRANSIENT



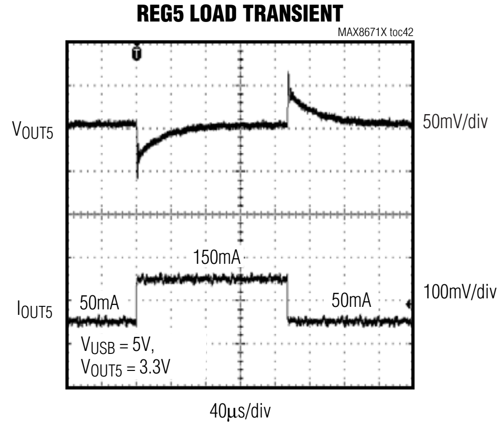
REG4 LOAD TRANSIENT



REG5 LOAD REGULATION



REG5 LOAD TRANSIENT



PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Pin Description

PIN	NAME	FUNCTION
1	USUS	USB Suspend Digital Input. As shown in Table 1, driving USUS high suspends the DC or USB inputs if they are configured as a USB power input.
2	DC	DC Power Input. DC is capable of delivering 1A to SYS. DC supports both AC adaptors and USB inputs. As shown in Table 1, the DC current limit is controlled by PEN1, PEN2, USUS, and R_{DISET}.
3	USB	USB Power Input. USB is capable of delivering 0.5A to SYS. As shown in Table 1, the USB current limit is controlled by PEN1, PEN2, and USUS.
4	FB5	Feedback Input for REG5. Connect FB5 to the center of a resistor voltage-divider from OUT5 to AGND to set the REG5 output voltage from 0.6V to V_{PV5}.
5	PV5	Power Input for REG5. Connect PV5 to SYS, or a supply between 1.7V and V_{SYS}. Bypass PV5 to power ground with a 1µF ceramic capacitor.
6	OUT5	Linear Regulator Power Output. OUT5 is internally pulled to AGND by 1kΩ in shutdown.
7	PG2	Power Ground for the REG2 Step-Down Regulator
8	LX2	Inductor Switching Node for REG2. LX2 is internally pulled to PG2 by 1kΩ in shutdown.
9	PV2	Power Input for the REG2 Step-Down Regulator. Connect PV2 to SYS. Bypass PV2 to PG2 with a 4.7µF ceramic capacitor.
10	$\overline{CEN}$	Active-Low Charger Enable Input. Pull $\overline{CEN}$ low to enable the charger, or drive $\overline{CEN}$ high to disable charging. The battery charger is also disabled when USUS is high.
11	FB2	Feedback Input for REG2. Connect FB2 to the center of a resistor voltage-divider from the REG2 output capacitors to AGND to set the output voltage from 1V to V_{SYS}.
12	$\overline{DOK}$	Active-Low, Open-Drain DC Power-OK Output. $\overline{DOK}$ is low when V_{DC} is within its valid operating range.
13	FB4	Feedback Input for REG4. Connect FB4 to the center of a resistor voltage-divider from the REG4 output capacitors to AGND to set the output voltage from 0.6V to V_{PV4}.
14	BP	Reference Noise Bypass. Bypass BP with a low-leakage 0.01µF ceramic capacitor for reduced noise on the LDO outputs.
15	OUT4	Linear Regulator Power Output. OUT4 is internally pulled to AGND in shutdown.
16	PV4	Power Input for REG4. Connect PV4 to SYS, or a supply between 1.7V and V_{SYS}. Bypass PV4 to power ground with a 1µF ceramic capacitor.
17	BVSET	Battery Regulation Voltage Set Node. Drive BVSET low to set the regulation voltage to 4.1V. Connect BVSET to VL or leave unconnected to set the regulation voltage to 4.2V. Connect BVSET to AGND through a 50kΩ resistor to set the regulation voltage to 4.350V.
18	AGND	Ground. AGND is the low-noise ground connection for the internal circuitry.
19	FB1	Feedback Input for REG1. Connect FB1 to the center of a resistor voltage-divider from the REG1 output capacitors to AGND to set the output voltage from 1V to V_{SYS}.
20	EN	Regulator Enable Input. Drive EN high to enable all regulator outputs. The sequencing is shown in Figure 11. Drive EN low to disable the regulators.
21	PWM	Forced-PWM Input. Connect PWM high for forced-PWM operation on REG1, REG2, and REG3. Connect PWM low for auto PWM operation. **Do not change PWM on-the-fly.** See the *PWM* section for more information.
22	PV1	Power Input for the REG1 Step-Down Regulator. Connect PV1 to SYS. Bypass PV1 to PG1 with a 4.7µF ceramic capacitor.

Pin Description (continued)

PIN	NAME	FUNCTION
23	LX1	Inductor Switching Node for REG1. LX1 is internally pulled to PG1 by 1kΩ in shutdown.
24	PG1	Power Ground for the REG1 Step-Down Regulator
25	PG3	Power Ground for the REG3 Step-Down Regulator
26	LX3	Inductor Switching Node for REG3. LX3 is internally pulled to PG3 by 1kΩ in shutdown.
27	PV3	Power Input for the REG3 Step-Down Regulator. Connect PV3 to SYS. Bypass PV3 to PG3 with a 4.7µF ceramic capacitor.
28	VL	IC Supply Output. VL is an LDO output that powers the MAX8671X internal battery-charger circuitry. VL provides 3.3V at 3mA to power external circuitry when DC or USB is present. Connect a 0.1µF capacitor from VL to AGND.
29	FB3	Feedback Input for REG3. Connect FB3 to the center of a resistor voltage-divider from the REG3 output capacitors to AGND to set the output voltage from 1V to V_{SYS}.
30	DISET	DC Input Current-Limit Select Input. Connect a resistor from DISET to AGND (R_{DISET}) to set the DC current limit. See Table 2 for more information.
31	CISET	Charge Rate Select Input. Connect a resistor from CISET to AGND (R_{CISET}) to set the fast-charge current limit, prequalification-charge current limit, and top-off threshold.
32	CT	Charge Timer Programming Node. Connect a capacitor from CT to AGND (C_{CT}) to set the time required for a fault to occur in fast-charge or prequalification modes. Connect CT to AGND to disable the fast-charge and prequalification timers.
33	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor that has a good thermal contact with the battery from THM to AGND. Connect a resistor equal to the thermistor resistance at +25°C from THM to VL. Charging is suspended when the battery is outside the hot or cold limits.
34	BAT	Positive Battery Terminal Connection. Connect BAT to the positive terminal of a single-cell Li+/Li-Poly battery.
35	SYS	System Supply Output. Bypass SYS to power ground with a 10µF ceramic capacitor. When a valid voltage is present at USB or DC and not suspended (USUS = low), SYS is limited to 5.3V ($V_{SYS-REG}$). When the system load (I_{SYS}) exceeds the input current limit, SYS drops below V_{BAT} by V_{BSREG} allowing both the external power source and the battery service SYS. SYS is connected to BAT through an internal system load switch (R_{BS}) when a valid source is not present at USB or DC.
36	PEN1	Input Current-Limit Control 1. See Table 1 for more information.
37	CST2	Open-Drain Charger Status Output 2. CST1 and CST2 indicate four different charger states. See Table 3 for more information.
38	$\overline{UOK}$	Active-Low, Open-Drain USB Power-OK Output. $\overline{UOK}$ is low when V_{USB} is within its valid operating range.
39	CST1	Open-Drain Charger Status Output 1. CST1 and CST2 indicate four different charger states. See Table 3 for more information.
40	PEN2	Input Current-Limit Control 2. See Table 1 for more information.
—	EP	Exposed Paddle. Connect the exposed paddle to AGND. Connecting the exposed paddle does not remove the requirement for proper ground connections to AGND, PG1, PG2, and PG3.

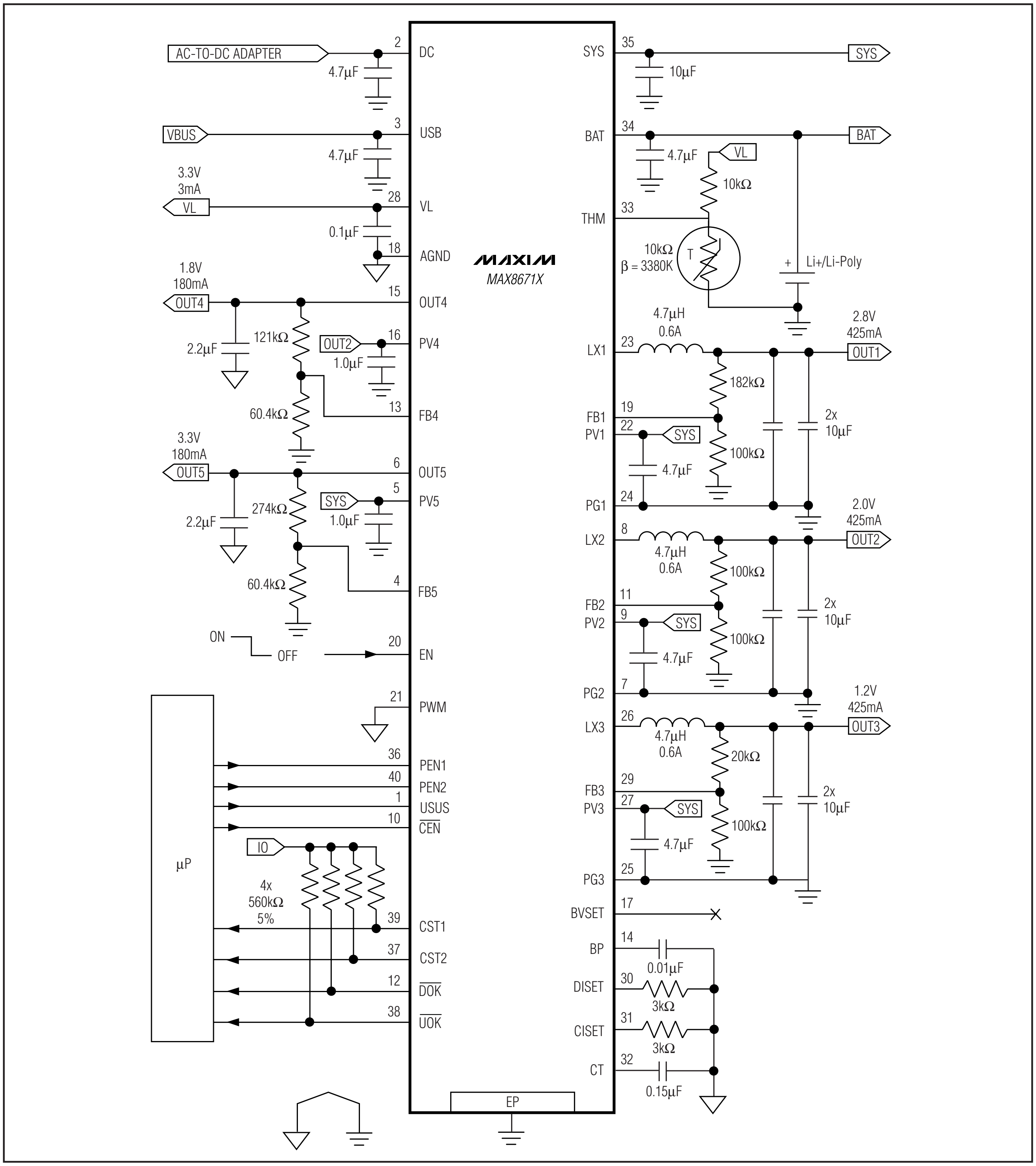


Figure 1. MAX8671X Typical Application Circuit

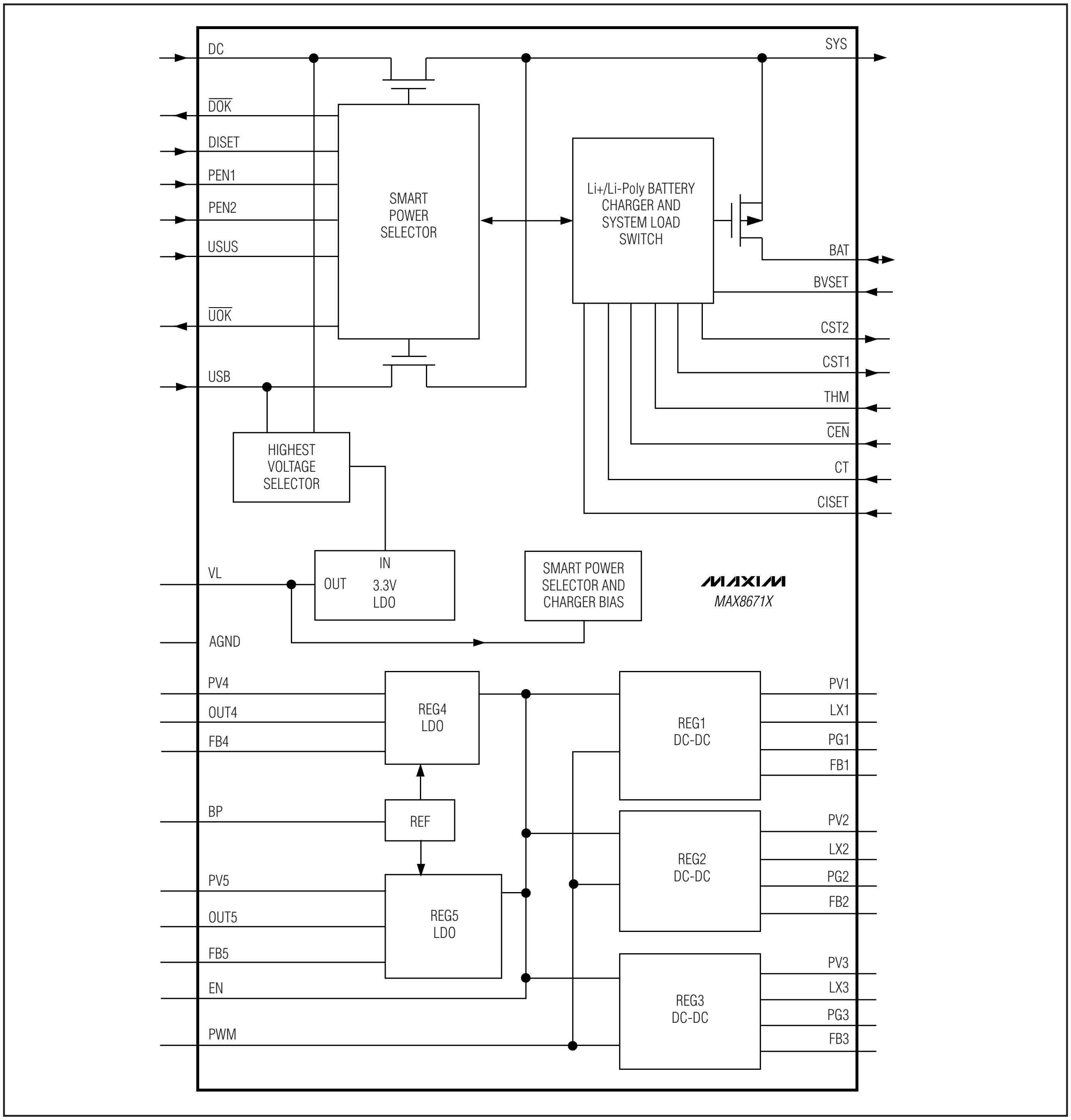


Figure 2. Functional Diagram

PMIC with Integrated Charger and Smart Power Selector for Handheld Devices

Detailed Description

The MAX8671X highly integrated PMIC is ideally suited for use in portable audio player and handheld applications. As shown in Figure 2, the MAX8671X integrates USB power input, AC-to-DC adapter power input (DC), Li+/Li-Poly battery charger, three step-down regulators, two linear regulators, and various monitoring and status outputs. The MAX8671X offers adjustable output voltages for all outputs.

Smart Power Selector

The MAX8671X Smart Power Selector seamlessly distributes power between the two current-limited external inputs (USB and DC), the battery (BAT), and the system load (SYS). The basic functions performed are:

- With both an external power supply (USB or DC) and battery (BAT) connected:

  When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.

  When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load through the internal system load switch.
- When the battery is connected and there is no external power input, the system (SYS) is powered from the battery.
- When an external power input is connected and there is no battery, the system (SYS) is powered from the external power input.

The dual-input Smart Power Selector supports end products with dual and single external power inputs. For end products with dual external power inputs, connect these inputs directly to the DC and USB nodes of the MAX8671X. For end products with a single input, connect the single input to the DC node and connect USB to ground or leave it unconnected. In addition to AC-to-DC adapters current limits, the DC input also supports USB current limit to allow for end products

Table 1. Input Limiter Control Logic

POWER SOURCE	$\overline{DOK}$	$\overline{UOK}$	PEN1	PEN2	USUS	DC INPUT CURRENT LIMIT	USB INPUT CURRENT LIMIT	MAXIMUM CHARGE CURRENT*
AC-to-DC Adapter at DC Input	L	X	H	X	X	I_{DCLIM}	USB input off, DC input has priority	Lower of I_{CHGMAX} and I_{DCLIM}
USB Power at DC Input	L	X	L	L	L	100mA		Lower of I_{CHGMAX} and 100mA
	L	X	L	H	L	500mA		Lower of I_{CHGMAX} and 500mA
	L	X	L	X	H	Suspend		0
USB Power at USB Input, DC Unconnected	H	L	X	L	L	No DC input	100mA	Lower of I_{CHGMAX} and 100mA
	H	L	X	H	L		500mA	Lower of I_{CHGMAX} and 500mA
	H	L	X	X	H		Suspend	0
DC and USB Unconnected	H	H	X	X	X		No USB input	0

**Charge current cannot exceed the input current limit. Charge can be less than the maximum charge current if the total SYS load exceeds the input current limit.*

X = Don't care.

with a single power input to operate from either an AC-to-DC adapter or USB host (see Table 1).

A thermal-limiting circuit reduces the battery charger rate and external power-source current to prevent the MAX8671X from overheating.

System Load Switch

An internal 80mΩ (R_{BS}) MOSFET connects SYS to BAT when no voltage source is available at DC or USB. When an external source is detected at DC or USB, this switch is opened and SYS is powered from the valid input source through the Smart Power Selector.

When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load through the internal system load switch. If the system load continuously exceeds the input current limit, the battery does not charge, even though external power is connected. This is not expected to occur in most cases because high loads usually occur only in short peaks. During these peaks, battery energy is used, but at all other times the battery charges.

USB Power Input (USB)

USB is a current-limited power input that supplies the system (SYS) up to 500mA. The USB to SYS switch is a linear regulator designed to operate in dropout. This linear regulator prevents the SYS voltage from exceeding 5.3V. USB is typically connected to the V_{BUS} line of the universal serial bus (USB) interface. As shown in Table 1, USB supports three different current limits that are set with the PEN2 and USUS digital inputs. These current limits are ideally suited for use with USB power.

The operating voltage range for USB is 4.1V to 6.6V, but it can tolerate up to 14V without damage. When the USB input voltage is below the undervoltage threshold (V_{USBL}, 4V typ) it is considered invalid. Similarly, if the USB voltage is above the overvoltage threshold (V_{USBH}, 6.9V typ) it is considered invalid. When the USB voltage is below the battery voltage, it is considered invalid. The USB power input is disconnected when the USB voltage is invalid. As shown in Table 1, when power is available at the DC input, it has priority over the USB input. Bypass USB to ground with at least a 4.7µF capacitor.

To support USB power sources at the USB input drive PEN2 and USUS to select between three internally set USB-related current limits as shown in Table 1. Choose 100mA for low-power USB mode. Choose 500mA for high-power USB mode. Choose suspend to reduce the USB current to 0.11mA (typ) for both USB suspend mode and unconfigured OTG mode. To comply with the USB 2.0 specification, each device must be initially configured for low power. After USB enumeration, the device can switch from low power to high power if given permission from the USB host. The MAX8671X does not perform enumeration. It is expected that the system communicates with the USB host and commands the MAX8671X through its PEN1, PEN2, and USUS inputs. When the load exceeds the input current limit, SYS drops to 82mV below BAT and the battery supplies supplemental load current.

The MAX8671X reduces the USB current limit by 5%/°C when the die temperature exceeds +100°C. The system load (I_{SYS}) has priority over the charger current, so input current is first reduced by lowering charge current. If the junction temperature still reaches +120°C in spite of charge current reduction, no input current is drawn from USB; the battery supplies the entire load and SYS is regulated below BAT by V_{BSREG}. Note that this on-chip thermal-limiting circuit is not related to and operates independently from the thermistor input.

If the USB power input is not required, connect USB to ground or leave it unconnected. When both DC and USB inputs are powered, the DC input has priority.