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19-3357; Rev 0; 8/04

Dual-Phase MOSFET Drivers with Temperature Sensor

General Description

The MAX8702/MAX8703 dual-phase noninverting MOSFET drivers are designed to work with PWM controller ICs, such as the MAX8705/MAX8707, in notebook CPU core and other multiphase regulators. Applications can either step down directly from the battery voltage to create the core voltage, or step down from a low-voltage system supply. The single-stage conversion method allows the highest possible efficiency, while the 2-stage conversion at higher switching frequency provides the minimum possible physical size.

Each MOSFET driver is capable of driving 3nF capacitive loads with only 19ns propagation delay and 8ns typical rise and fall times. Larger capacitive loads are allowable but result in longer propagation and transition times. Adaptive dead-time control helps prevent shoot-through currents and maximizes converter efficiency.

The MAX8702/MAX8703 feature zero-crossing comparators on each channel. When enabled, these comparators permit the drivers to be used in pulse-skipping operation, thereby saving power at light loads. A separate shutdown control is also included that disables all functions, drops quiescent current to 2µA, and sets DH low and DL high.

The MAX8702 integrates a resistor-programmable temperature sensor. An open-drain output ($\overline{DRHOT}$) signals to the system when the local die temperature exceeds the set temperature. The MAX8702/MAX8703 are available in a thermally-enhanced 20-pin thin QFN package.

Applications

Multiphase High-Current Power Supplies

2- to 4-Cell Li+ Battery to CPU Core Supplies

Notebook and Desktop Computers

Servers and Workstations

Pin Configuration appears at end of data sheet.

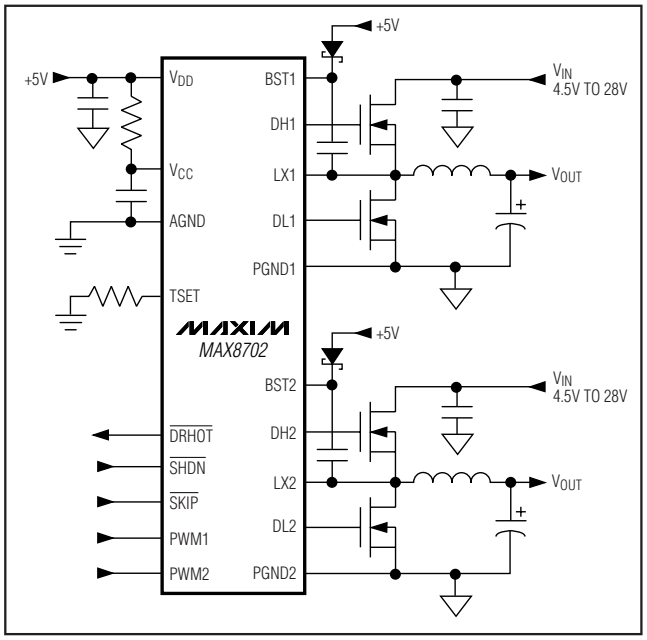
Features

- **Dual-Phase MOSFET Driver**
- **0.35Ω (typ) On-Resistance and 5A (typ) Drive Current**
- **Drives Large Synchronous-Rectifier MOSFETs**
- **Integrated Temperature Sensor (MAX8702 Only)**
  Resistor Programmable
  Open-Drain Driver Hot Indicator ($\overline{DRHOT}$)
- **Adaptive Dead Time Prevents Shoot-Through**
- **Selectable Pulse-Skipping Mode**
- **4.5V to 28V Input Voltage Range**
- **Thermally Enhanced Low-Profile Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	DESCRIPTION
MAX8702ETP	-40°C to +100°C	20 Thin QFN 4mm x 4mm	Dual-Phase Driver with Temp. Sensor
MAX8703ETP	-40°C to +100°C	20 Thin QFN 4mm x 4mm	Dual-Phase Driver without Temp. Sensor

Minimal Operating Circuit



Dual-Phase MOSFET Drivers with Temperature Sensor

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND .....-0.3V to +6V
V_{DD} to AGND .....-0.3V to +6V
PGND_ to AGND .....-0.3V to +0.3V
$\overline{SKIP}$, $\overline{SHDN}$, $\overline{DRHOT}$, TSET to AGND .....-0.3V to +6V
PWM_ to AGND .....-0.3V to +6V
DL_ to PGND_ .....-0.3V to (V_{DD} + 0.3V)
LX_ to AGND .....-2V to +30V
DH_ to LX_ .....-0.3V to ($V_{BST\_}$ + 0.3V)
BST_ to LX_ .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
20-Pin 4mm x 4mm Thin QFN
(derate 16.9mW/°C above +70°C) 1349mW
Operating Temperature Range .....-40°C to +100°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2. V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = 5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC}			4.5		5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	85mV typical hysteresis	V_{CC} rising	3.4	3.85	4.1	V
			V_{CC} falling	3.3	3.75	4.0	
V_{CC} Quiescent Current (Note 1)	I_{CC}	$\overline{SKIP}$ = AGND, PWM_ = AGND			200	400	µA
		$\overline{SKIP}$ = AGND, PWM_ = V_{CC}			2	3	mA
V_{DD} Quiescent Current	I_{DD}	$\overline{SKIP}$ = AGND, PWM_ = AGND			1	5	µA
V_{CC} Shutdown Current		$\overline{SHDN}$ = $\overline{SKIP}$ = AGND			2	5	µA
V_{DD} Shutdown Current		$\overline{SHDN}$ = $\overline{SKIP}$ = AGND			1	5	µA
GATE DRIVERS AND DEAD-TIME CONTROL (Figure 1)							
DL_ Propagation Delay	t_{PWM-DL}	PWM_ high to DL_ low			19		ns
	t_{DH-DL}	DH_ low to DL_ high			36		
DH_ Propagation Delay	t_{DL-DH}	DL_ low to DH_ high			25		ns
	t_{PWM-DH}	PWM_ low to DH_ low			23		
DL_ Transition Time	t_{F_DL}	DL_ falling, 3nF load			11		ns
	t_{R_DL}	DL_ rising, 3nF load			8		
DH_ Transition Time	t_{F_DH}	DH_ falling, 3nF load			14		ns
	t_{R_DH}	DH_ rising, 3nF load			16		
DH_ On-Resistance (Note 2)	R_{DH}	$V_{BST\_}$ - $V_{LX\_}$ = 5V			1.0	4.5	Ω
DL_ On-Resistance (Note 2)	R_{DL_HIGH}	High state (pullup)			1.0	4.5	Ω
	R_{DL_LOW}	Low state (pulldown)			0.35	2.0	
DH_ Source/Sink Current	I_{DH}	$V_{DH\_}$ = 2.5V, $V_{BST\_}$ - $V_{LX\_}$ = 5V			1.5		A
DL_ Source Current	I_{DL_SOURCE}	$V_{DL\_}$ = 2.5V			1.5		A
DL_ Sink Current	I_{DL_SINK}	$V_{DL\_}$ = 5V			5		A
Zero-Crossing Threshold		$V_{PGND\_}$ - $V_{LX\_}$, $\overline{SKIP}$ = AGND			2.5		mV
TEMPERATURE SENSOR							
Temperature Threshold Accuracy		T_A = +85°C to +125°C, 10°C falling hysteresis		-5		+5	°C
$\overline{DRHOT}$ Output Low Voltage		I_{SINK} = 3mA				0.4	V
$\overline{DRHOT}$ Leakage Current		High state, $V_{\overline{DRHOT}}$ = 5.5V				1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2. V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = 5V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Shutdown Threshold		10°C hysteresis		+160		°C
LOGIC CONTROL SIGNALS						
Logic Input High Voltage		$\overline{SHDN}$, $\overline{SKIP}$, PWM1, PWM2	2.4			V
Logic Input Low Voltage		$\overline{SHDN}$, $\overline{SKIP}$, PWM1, PWM2			0.8	V
Logic Input Current		$\overline{SHDN}$, $\overline{SKIP}$, PWM1, PWM2	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2. V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = 5V, **T_A = -40°C to +100°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC}			4.5		5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	85mV typical hysteresis	V_{CC} rising	3.4		4.1	V
			V_{CC} falling	3.3		4.0	
V_{CC} Quiescent Current	I_{CC}	$\overline{SKIP}$ = AGND, PWM_ = PGND_				450	µA
		$\overline{SKIP}$ = AGND, PWM_ = V_{CC}				3	mA
V_{DD} Quiescent Current	I_{DD}	$\overline{SKIP}$ = AGND, PWM_ = PGND_, T_A = -40°C to +85°C				5	µA
V_{CC} Shutdown Current		$\overline{SHDN}$ = $\overline{SKIP}$ = AGND, T_A = -40°C to +85°C				5	µA
V_{DD} Shutdown Current		$\overline{SHDN}$ = $\overline{SKIP}$ = AGND, T_A = -40°C to +85°C				5	µA
GATE DRIVERS AND DEAD-TIME CONTROL							
DH_ On-Resistance (Note 2)	R_{DH}	$V_{BST\_}$ - $V_{LX\_}$ = 5V			1.0	4.5	Ω
DL_ On-Resistance (Note 2)	R_{DL_HIGH}	High state (pullup)			1.0	4.5	Ω
	R_{DL_LOW}	Low state (pulldown)			0.35	2.0	
TEMPERATURE SENSOR							
$\overline{DRHOT}$ Output Low Voltage		I_{SINK} = 3mA				0.4	V
LOGIC CONTROL SIGNALS							
Logic Input High Voltage		$\overline{SHDN}$, $\overline{SKIP}$, PWM1, PWM2		2.4			V
Logic Input Low Voltage		$\overline{SHDN}$, $\overline{SKIP}$, PWM1, PWM2				0.8	V

Note 1: Static drivers instead of pulsed-level translators.

Note 2: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the thin QFN package.

Note 3: Specifications from -40°C to +100°C are guaranteed by design, not production tested.

Dual-Phase MOSFET Drivers with Temperature Sensor

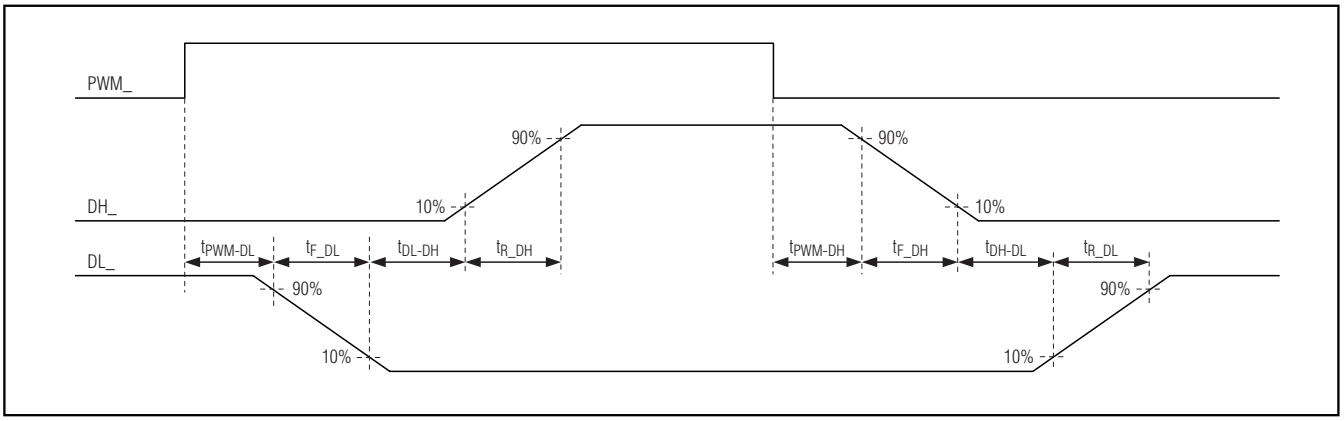
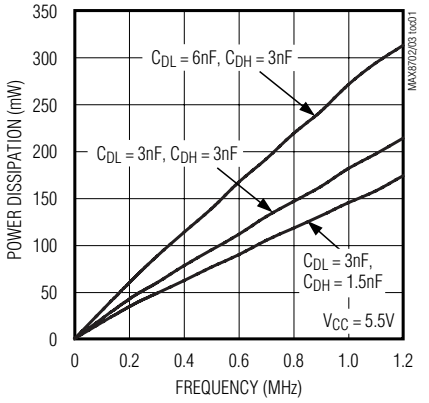


Figure 1. Timing Definitions Used in the Electrical Characteristics

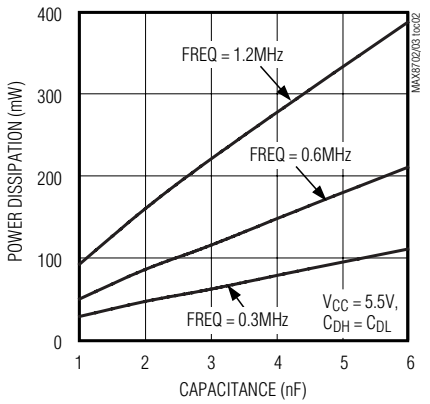
Typical Operating Characteristics

(Circuit of Figure 2. V_{IN} = 12V, V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = 5V, T_A = +25°C unless otherwise noted.)

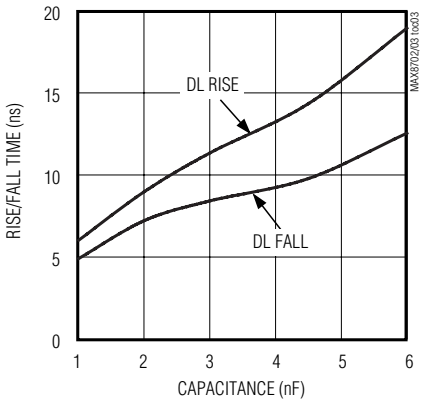
POWER DISSIPATION vs. FREQUENCY (SINGLE PHASE, BOTH DRIVERS SWITCHING)



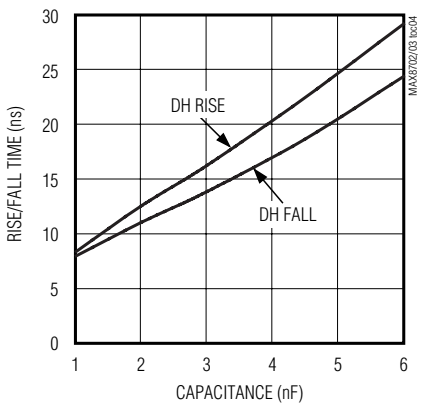
POWER DISSIPATION vs. CAPACITIVE LOAD (SINGLE PHASE, BOTH DRIVERS SWITCHING)



DL RISE/FALL TIME vs. CAPACITIVE LOAD



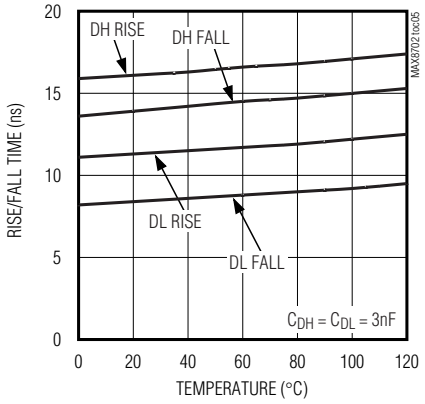
DH RISE/FALL TIME vs. CAPACITIVE LOAD



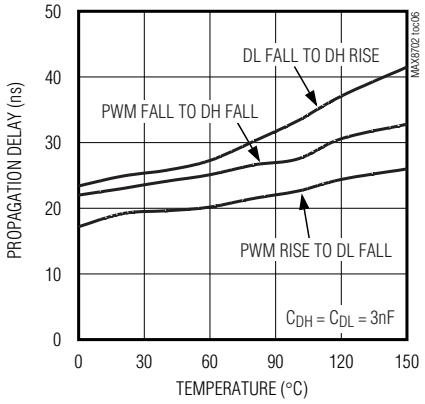
Typical Operating Characteristics (continued)

(Circuit of Figure 2. V_{IN} = 12V, V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = 5V, T_A = +25°C unless otherwise noted.)

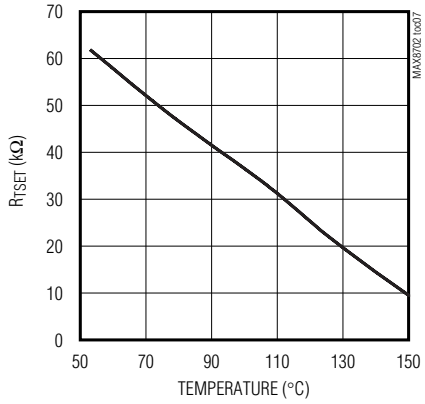
DH/DL RISE/FALL TIMES vs. TEMPERATURE



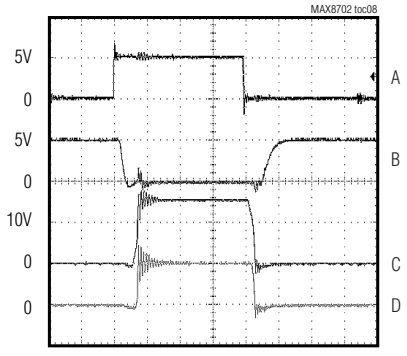
PROPAGATION DELAY vs. TEMPERATURE



R_{TSET} vs. TEMPERATURE



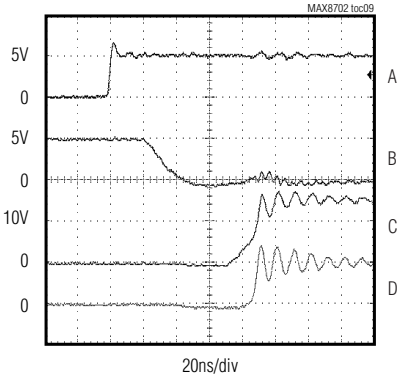
TYPICAL SWITCHING WAVEFORMS



125ns/div

A. PWM, 5V/div C. DH, 10V/div
B. DL, 5V/div D. LX, 10V/div

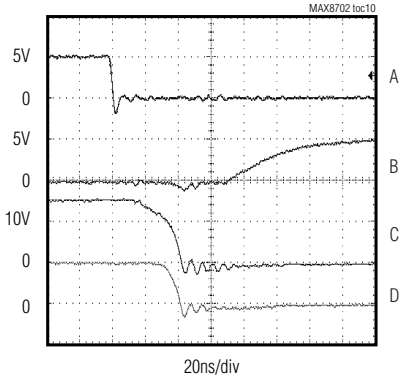
DH RISE AND DL FALL WAVEFORMS



20ns/div

A. PWM, 5V/div C. DH, 10V/div
B. DL, 5V/div D. LX, 10V/div

DH FALL AND DL RISE WAVEFORMS



20ns/div

A. PWM, 5V/div C. DH, 10V/div
B. DL, 5V/div D. LX, 10V/div

Dual-Phase MOSFET Drivers with Temperature Sensor

Pin Description

PIN		NAME	FUNCTION
MAX8702	MAX8703		
1	1	PWM1	Phase 1 PWM Logic Input. DH1 is high when PWM1 is high; DL1 is high when PWM1 is low.
2	2	PWM2	Phase 2 PWM Logic Input. DH2 is high when PWM2 is high; DL2 is high when PWM2 is low.
3	3	AGND	Analog Ground. The AGND and PGND_ pins must be connected externally at one point close to the IC. Connect the device's exposed backside pad to AGND.
4	—	TSET	Temperature-Set Input. Connect an external 1% resistor from TSET to AGND to set the trip point. R_{TSET} = 85,210 / T - 745,200 / T^2 - 195, where R_{TSET} is the temperature-setting resistor in kΩ and T is the trip temperature in Kelvin.
5	—	$\overline{DRHOT}$	Driver-Hot-Indicator Output. $\overline{DRHOT}$ is an open-drain output. Pull up with an external resistor. When the device's temperature exceeds the programmed set point, $\overline{DRHOT}$ is pulled low.
6	—	I.C.	Internally Connected. Connect to AGND.
7	7	V_{CC}	Internal Control Circuitry Supply Input. The input voltage range is from 4.5V to 5.5V. Bypass V_{CC} to AGND with a 1µF ceramic capacitor. The maximum resistance between V_{CC} and V_{DD} should be 10Ω.
8	8	BST2	Phase 2 Bootstrap Flying-Capacitor Connection. An optional resistor in series with BST2 allows the DH2 pullup current to be adjusted.
9	9	DH2	Phase 2 High-Side Gate-Driver Output. DH2 swings between LX2 and BST2.
10	10	LX2	Phase 2 Inductor Switching Node Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. LX2 is also the input to the skip-mode zero-crossing comparator.
11	11	PGND2	Phase 2 Power Ground. PGND2 is the internal lower supply rail for the DL2 low-side gate driver.
12	12	DL2	Phase 2 Low-Side Gate-Driver Output. DL2 swings between PGND2 and V_{DD}. DL2 is high in shutdown.
13	13	V_{DD}	DL_ Gate-Driver Supply Input. The input voltage range is from 4.5V to 5.5V. Bypass V_{DD} to the power ground with a 2.2µF ceramic capacitor.
14	14	DL1	Phase 1 Low-Side Gate-Driver Output. DL1 swings between PGND1 and V_{DD}. DL1 is high in shutdown.
15	15	PGND1	Phase 1 Power Ground. PGND1 is the internal lower supply rail for the DL1 low-side gate driver.
16	16	LX1	Phase 1 Inductor Switching Node Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. LX1 is also the input to the skip-mode zero-crossing comparator.
17	17	DH1	Phase 1 High-Side Gate-Driver Output. DH1 swings between LX1 and BST1.
18	18	BST1	Phase 1 Bootstrap Flying-Capacitor Connection. An optional resistor in series with BST1 allows the DH1 pullup current to be adjusted.
19	19	$\overline{SKIP}$	Pulse-Skipping-Mode Control Input. The pulse-skipping mode is enabled when $\overline{SKIP}$ is low. When $\overline{SKIP}$ is high, both drivers operate in PWM mode (i.e., except during dead times, DL_ is the complement of DH_).
20	20	$\overline{SHDN}$	Shutdown Control Input. When $\overline{SHDN}$ and $\overline{SKIP}$ are low, DH_ is forced low, DL_ forced high, and the device enters into a low-power shutdown state. Temperature sensing is disabled in shutdown.
—	4, 5, 6	N. C.	No Connection. Not internally connected.

Typical Operating Circuit

The typical operating circuit of the MAX8702 (Figure 2) shows the power-stage and gate-driver circuitry of a dual-phase CPU core supply operating at 300kHz, with each phase capable of supplying 20A of load current. Table 1 lists recommended component options, and Table 2 lists the component suppliers' contact information.

Detailed Description

The MAX8702/MAX8703 dual-phase noninverting MOSFET drivers are intended to work with PWM controller ICs in CPU core and other multiphase switching regulators. Each MOSFET driver is capable of driving 3nF capacitive loads with only 19ns propagation delay and 8ns typical rise and fall times. Larger capacitive loads are allowable but result in longer propagation and transition times. Adaptive dead-time control prevents shoot-through currents and maximizes converter

Table 1. Component List

DESIGNATION	DESCRIPTION
Total Input Capacitance (C_{IN})	(4) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Total Output Capacitance (C_{OUT})	(4) 330µF, 2.5V, 9mΩ low-ESR polymer capacitor (D case) Sanyo 2R5TPE330M9
Schottky Diode (per phase)	3A Schottky diode Central Semiconductor CMSH3-40
Inductor (per phase)	0.6µH Panasonic ETQP1H0R6BFA or Sumida CDEP134H-0R6
High-Side MOSFET (NH, per phase)	Siliconix (1) Si7892DP or International Rectifier (2) IRF6604
Low-Side MOSFET (NL, per phase)	Siliconix (2) Si7442DP or International Rectifier (2) IRF6603

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Central Semiconductor	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
Panasonic	www.panasonic.com
Sanyo	www.secc.co.jp
Siliconix (Vishay)	www.vishay.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com

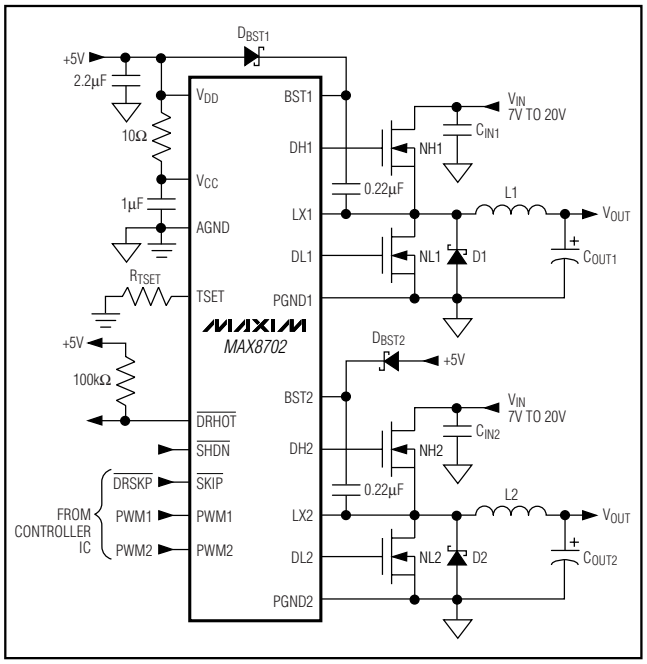


Figure 2. MAX8702 Typical Operating Circuit

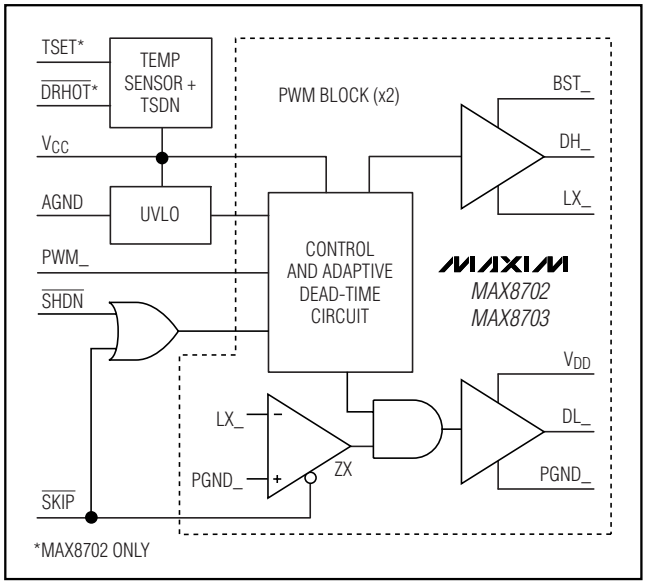


Figure 3. MAX8702 Functional Diagram

Dual-Phase MOSFET Drivers with Temperature Sensor

efficiency while allowing operation with a variety of MOSFETs and PWM controllers. A UVLO circuit allows proper power-on sequencing. The PWM control inputs are both TTL and CMOS compatible.

The MAX8702 integrates a resistor-programmable temperature sensor. An open-drain output ($\overline{DRHOT}$) signals to the system when the die temperature of the driver exceeds the set temperature. See the *Temperature Sensor* section.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderately sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in the notebook CPU environment, where a large V_{IN} - V_{OUT} differential exists. Two adaptive dead-time circuits monitor the DH and DL outputs and prevent the opposite-side FET from turning on until DH or DL is fully off. There must be a low-resistance, low-inductance path from the DH and DL drivers to the MOSFET gates for the adaptive dead-time circuits to work properly. Otherwise, the sense circuitry interprets the MOSFET gate as "off" while there is actually still charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 to 100 mils wide if the MOSFET is 1in from the device).

The internal pulldown transistor that drives DL low is robust, with a 0.35Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain-to-gate capacitance of the low-side synchronous-rectifier MOSFETs when LX switches from ground to V_{IN}. Applications with high input voltages and long, inductive DL traces may require additional gate-to-source capacitance to ensure fast-rising LX edges do not pull up the low-side MOSFET's gate voltage, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the minimum threshold voltage:

$$V_{GS(TH)} < V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage can cause problems in marginal designs. Typically, adding a 4700pF capacitor between DL and power ground, close to the low-side MOSFETs, greatly reduces coupling. To prevent excessive turn-off delays, do not exceed 22nF of total gate capacitance.

Alternatively, shoot-through currents may be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFETs is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor of less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 4). Slowing down the high-side MOSFETs also reduces the LX node rise time, thereby reducing the EMI and high-frequency coupling responsible for switching noise.

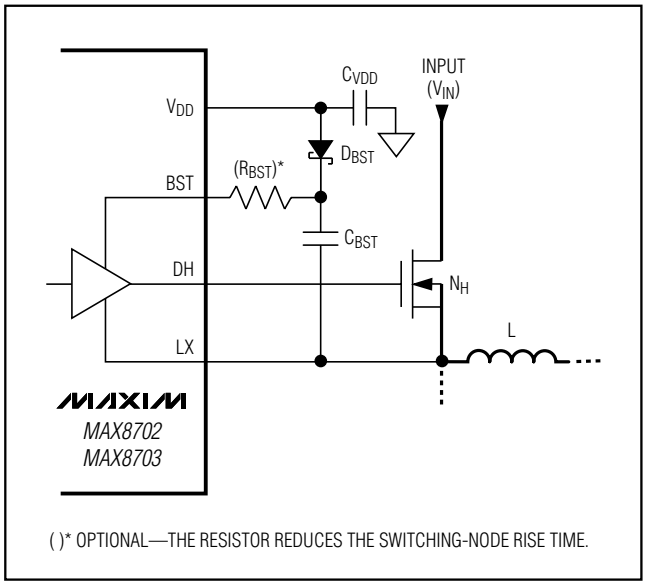


Figure 4. High-Side Gate-Driver Boost Circuitry

Boost Capacitor Selection

The MAX8702/MAX8703 use a bootstrap circuit to generate the floating supply voltages for the high-side drivers (DH). The boost capacitors (C_{BST}) selected must be large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFET's gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one phase and Q_{GATE} is the total gate charge specified in the MOSFET's data sheet. For example, assume

(2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance is:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

5V Bias Supply (V_{CC} and V_{DD})

V_{DD} provides the supply voltages for the low-side drivers (DL). The decoupling capacitor at V_{DD} also charges the BST capacitors during the time period when DL is high. Therefore, the V_{DD} capacitor should be large enough to minimize the ripple voltage during switching transitions. C_{VDD} should be chosen according to the following equation:

$$C_{VDD} = 10 \times C_{BST}$$

In the example above, a 0.22µF capacitor is used for C_{BST}, so the V_{DD} capacitor should be 2.2µF.

V_{CC} provides the supply voltage for the internal logic circuit and temperature sensor. To avoid switching noise from coupling into the sensitive internal circuit, an RC filter is recommended for the V_{CC} pin. Place a 10Ω resistor from the supply voltage to the V_{CC} pin and a 1µF capacitor from the V_{CC} pin to AGND.

The total bias current I_{BIAS} from the 5V supply can be calculated using the following equation:

$$I_{BIAS} = I_{DD} + I_{CC}$$

$$I_{DD} = n_{PHASE} \times f_{SW} \times (n_{NH} \times Q_{G(NH)} + n_{NL} \times Q_{G(NL)})$$

where n_{PHASE} is the number of phases, f_{SW} is the switching frequency, $Q_{G(NH)}$ and $Q_{G(NL)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V, n_{NH} is the total number of high-side MOSFETs in parallel, n_{NL} is the total number of low-side MOSFETs in parallel, and I_{CC} is the V_{CC} supply current.

Undervoltage Lockout (UVLO)

When V_{CC} is below the UVLO threshold (3.85V typ) and $\overline{SHDN}$ and $\overline{SKIP}$ are low, DL is kept high and DH is held low. This provides output overvoltage protection as soon as the supply voltage is applied. Once V_{CC} is above the UVLO threshold and $\overline{SHDN}$ is high, DL and DH levels depend on the PWM signal applied. If V_{CC} falls below the UVLO threshold while $\overline{SHDN}$ is high, both DL and DH are immediately forced low. This prevents negative undershoots on the output when the system power is removed without going through the proper shutdown sequence.

Low-Power Pulse Skipping

The MAX8702/MAX8703 enter into low-power pulse-skipping mode when $\overline{SKIP}$ is pulled low. In skip mode, an inherent automatic switchover to pulse frequency modulation (PFM) takes place at light loads. A zero-crossing comparator truncates the low-side switch on-time at the inductor current's zero-crossing. The comparator senses the voltage across LX and PGND. Once V_{LX} - V_{PGND} drops below the zero-crossing comparator threshold (see the *Electrical Characteristics*), the comparator forces DL low. This mechanism causes the threshold between pulse-skipping PFM and non-skipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation. The PFM/PWM crossover occurs when the load current of each phase is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value. For a battery input range of 7V to 20V, this threshold is relatively constant, with only a minor dependence on the input voltage due to the typically low duty cycles. The switching waveforms may appear noisy and asynchronous when light loading activates the pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency.

Shutdown

The MAX8702/MAX8703 feature a low-power shutdown mode that reduces the V_{CC} quiescent current drawn to 2µA (typ). Driving $\overline{SHDN}$ and $\overline{SKIP}$ low sets DH low and DL high. Temperature sensing is disabled in shutdown.

Temperature Sensor (MAX8702 Only)

The MAX8702 includes a fully integrated resistor-programmable temperature sensor. The sensor incorporates two temperature-dependent reference signals and one comparator. One signal exhibits a characteristic that is proportional to temperature, and the other is complementary to temperature. The temperature at which the two signals are equal determines the thermal trip point. When the temperature of the device exceeds the trip point, the open-drain output $\overline{DRHOT}$ pulls low.

Table 3. Modes of Operation

$\overline{SHDN}$	$\overline{SKIP}$	MODE OF OPERATION
L	L	Low-power shutdown state; temperature sensing disabled
L	H	PWM operation
H	L	Pulse-skipping operation
H	H	PWM operation

Dual-Phase MOSFET Drivers with Temperature Sensor

A 10°C hysteresis keeps the output from oscillating when the temperature is close to the threshold. The thermal trip point is programmable up to +160°C through an external resistor between TSET and AGND. Use the following equation to determine the value of the resistor:

$$R_{TSET} = (85{,}210 / T) - (745{,}200 / T^2) - 195$$

where R_{TSET} is the value of the set-point resistor in kΩ and T is the trip-point temperature in Kelvin.

The MAX8702 and MAX8703 include a thermal-shutdown circuit that is independent of the temperature sensor. The thermal shutdown has a fixed threshold of +160°C (typ) with 10°C of thermal hysteresis. When the die temperature exceeds +160°C, DH is pulled low and DL is pulled high. The driver automatically resets when the die temperature drops by +10°C.

Applications Information

Power MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (>20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both of these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but increasing C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ but reducing C_{GATE}). If V_{IN} does not vary over a wide range, the minimum power dissipation occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two SO-8s, DPAK, or D^2PAK), and is reasonably priced. Ensure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems can occur.

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD(N_H RESISTIVE) = \left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{I_{LOAD}}{n_{TOTAL}}\right)^2 R_{DS(ON)}$$

where n_{TOTAL} is the total number of phases.

Generally, a small high-side MOSFET is desired to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power dissipation often limits how small the MOSFETs can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PC board layout characteristics. The following switching-loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H SWITCHING) = (V_{IN(MAX)})^2\left(\frac{C_{RSS} f_{SW}}{I_{GATE}}\right)\left(\frac{I_{LOAD}}{n_{TOTAL}}\right)$$

where C_{RSS} is the reverse transfer capacitance of N_H and I_{GATE} is the peak gate-drive source/sink current (5A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the $C \times V_{IN}^2 \times f_{SW}$ switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at the maximum input voltage:

$$PD(N_L RESISTIVE) = \left[1-\left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right]\left(\frac{I_{LOAD}}{n_{TOTAL}}\right)^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$ but are not quite high enough to exceed

the current limit and cause the fault latch to trip. The MOSFETs must have a good-sized heatsink to handle the overload power dissipation. The heat sink can be a large copper field on the PC board or an externally mounted device.

The Schottky diode only conducts during the dead time when both the high-side and low-side MOSFETs are off. Choose a Schottky diode with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time, and a peak current rating higher than the peak inductor current. The Schottky diode must be rated to handle the average power dissipation per switching cycle. This diode is optional and can be removed if efficiency is not critical.

IC Power Dissipation and Thermal Considerations

Power dissipation in the IC package comes mainly from driving the MOSFETs. Therefore, it is a function of both switching frequency and the total gate charge of the selected MOSFETs. The total power dissipation when both drivers are switching is given by:

$$PD(IC) = I_{BIAS} \times 5V$$

where I_{BIAS} is the bias current of the 5V supply calculated in the *5V Bias Supply (V_{DD} and V_{CC})* section .

The rise in die temperature due to self-heating is given by the following formula:

$$\Delta T_J = PD(IC) \times \theta_{JA}$$

where PD(IC) is the power dissipated by the device, and θ_{JA} is the package's thermal resistance. The typical thermal resistance is 59.3°C/W for the 4mm x 4mm thin QFN package. For example, if the MAX8702 dissipates 500mW of power within the IC, this corresponds to a 30°C shift in the die temperature in the thin QFN package.

PC Board Layout Considerations

The MAX8702/MAX8703 MOSFET drivers source and sink large currents to drive MOSFETs at high switching speeds. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following PC board layout guidelines are recommended when designing with the device:

1) Place V_{CC} and V_{DD} decoupling capacitors as close to their respective pins as possible.
2) Minimize the high-current loops from the input capacitor, upper-switching MOSFET, and low-side MOSFET back to the input capacitor negative terminal.
3) Provide enough copper area at and around the switching MOSFETs and inductors to aid in thermal dissipation.
4) Connect the PGND1 and PGND2 pins as close as possible to the source of the low-side MOSFETs.
5) Keep LX traces away from sensitive analog components and nodes. Place the IC and analog components on the opposite side of the board from the power-switching node if possible.
6) Use two or more vias for DL and DH traces when changing layers to reduce via inductance.

Figure 5 shows a PC board layout example.

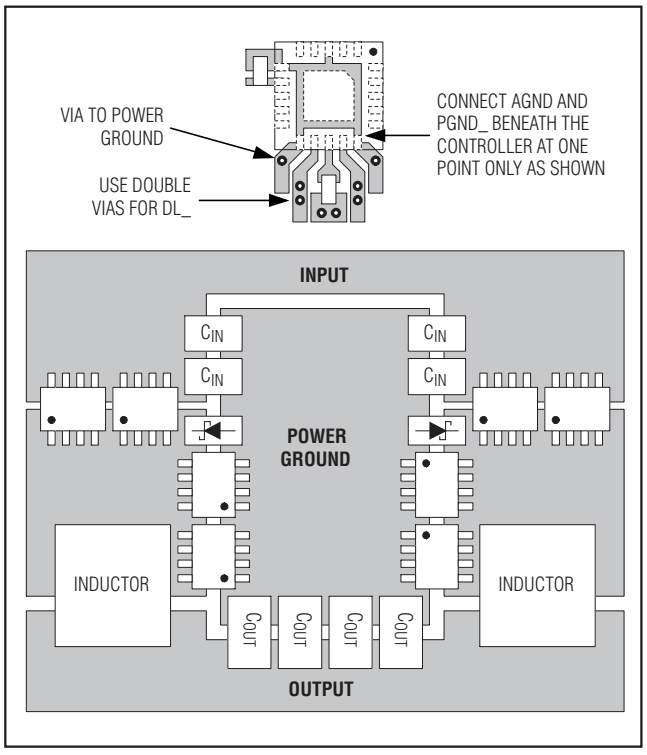
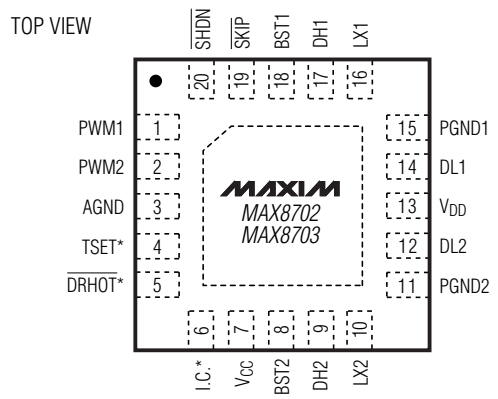


Figure 5. PC Board Layout Example

Dual-Phase MOSFET Drivers with Temperature Sensor

Pin Configuration



THIN QFN
(4mm x 4mm)

*THESE PINS ARE N.C. ON THE MAX8703

Chip Information

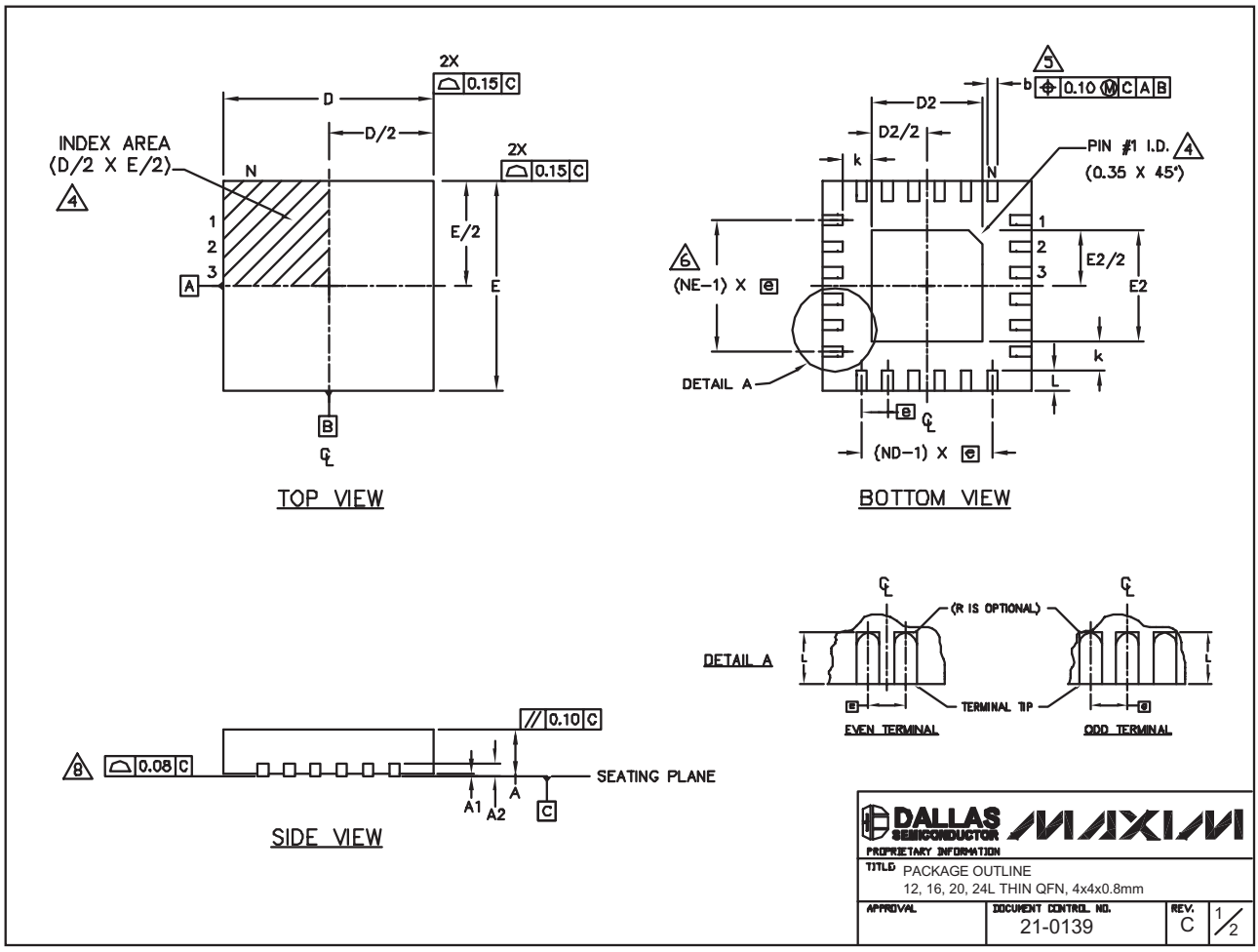
TRANSISTOR COUNT: 1100

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

24L QFN THIN.EPS



Dual-Phase MOSFET Drivers with Temperature Sensor

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS												
PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16			20			24		
ND	3			4			5			6		
NE	3			4			5			6		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2		

EXPOSED PAD VARIATIONS							
PKG. CODES	D2			E2			DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T1244-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-2	1.95	2.10	2.25	1.95	2.10	2.25	NO
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25	YES
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-1	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25	NO
T2444-1	2.45	2.60	2.63	2.45	2.60	2.63	NO
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25	YES
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63	YES
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
12, 16, 20, 24L THIN QFN, 4x4x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	C	2/2