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19-3321; Rev 0; 6/04

EVALUATION KIT AVAILABLE

Low-Cost CCFL Backlight Controller

General Description

The MAX8722 integrated backlight controller is optimized to drive cold-cathode fluorescent lamps (CCFLs) using a full-bridge resonant inverter architecture. Resonant operation maximizes striking capability and provides near-sinusoidal waveforms over the entire input range to improve CCFL lifetime. The controller operates over a wide input voltage range (4.6V to 28V) with high power to light efficiency. The device also includes safety features that effectively protect against many single-point fault conditions including lamp-out and short-circuit faults.

The MAX8722 achieves 10:1 dimming range by "chopping" the lamp current on and off using a digital pulse-width modulation (DPWM) method. The DPWM frequency can be accurately adjusted with a resistor or synchronized to an external signal. The brightness is controlled by an analog voltage on the CNTL pin. The device directly drives the four external n-channel power MOSFETs of the full-bridge inverter. An internal 5.3V linear regulator powers the MOSFET drivers, the DPWM oscillator, and most of the internal circuitry. The MAX8722 is available in a low-cost, 24-pin QSOP package and operates over a -40°C to +85°C temperature range.

Applications

Notebook Computer Displays

LCD Monitors

LCD TVs

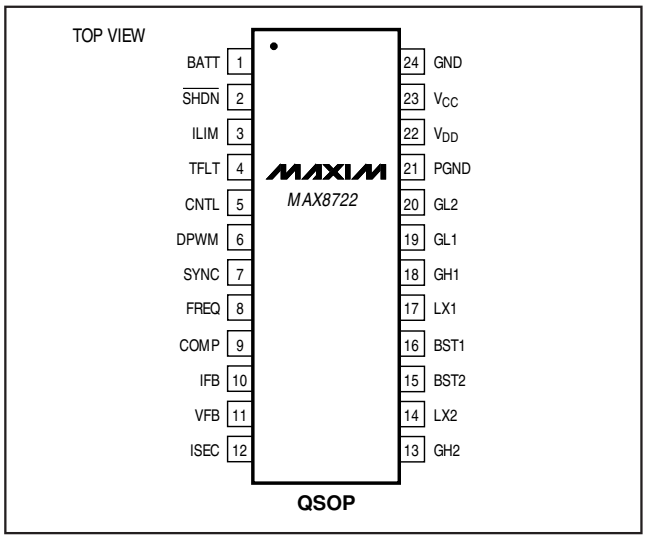
Features

- **Synchronized to Resonant Frequency**
  - **Longer Lamp Life**
  - **Guaranteed Striking Capability**
  - **High Power to Light Efficiency**
- **Wide Input Voltage Range (4.6V to 28V)**
- **Input-Voltage Feed-Forward for Excellent Line Rejection**
- **Accurate Dimming Control with Analog Interface**
- **10:1 Dimming Range**
- **Adjustable Accurate DPWM Frequency with Sync Function**
- **Adjustable Lamp Current Rise and Fall Time**
- **Secondary Voltage Limit Reduces Transformer Stress**
- **Lamp-Out Protection with Adjustable Timeout**
- **Secondary Overcurrent Protection with Adjustable Timeout**
- **Low-Cost 24-Pin QSOP Package**

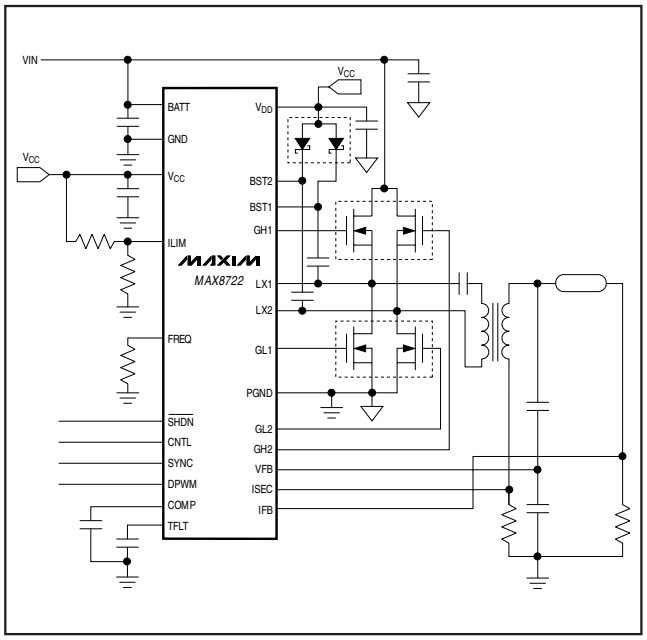
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8722EEG	-40°C to +85°C	24 QSOP

Pin Configuration



Minimal Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low-Cost CCFL Backlight Controller

ABSOLUTE MAXIMUM RATINGS

BATT to GND .....-0.3V to +30V
BST1, BST2 to GND .....-0.3V to +36V
BST1 to LX1, BST2 to LX2 .....-0.3V to +6V
CNTL, FREQ, SYNC, V_{CC}, V_{DD} to GND .....-0.3V to +6V
COMP, DPWM, ILIM, TFLT to GND .....-0.3V to (V_{CC} + 0.3V)
GH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
GH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
GL1, GL2 to GND .....-0.3V to (V_{DD} + 0.3V)
IFB, ISEC, VFB to GND.....-3V to +6V
$\overline{SHDN}$ to GND.....-0.3V to +6V
PGND to GND .....-0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
24-Pin QSOP (derate 9.5mW/°C above +70°C).....761.9mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Input Voltage Range	V_{CC} = V_{DD} = V_{BATT}		4.6		5.5	V
	V_{CC} = V_{DD} = open		5.5		28.0	
BATT Quiescent Current	$V_{\overline{SHDN}}$ = V_{CC}, V_{IFB} = 1V	V_{BATT} = 28V		1	2	mA
		V_{BATT} = V_{CC} = 5V			2	
BATT Quiescent Current, Shutdown	$\overline{SHDN}$ = GND			6	20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.5V, 6V < V_{BATT} < 28V, 0 < I_{LOAD} < 10mA		5.25	5.40	5.55	V
V_{CC} Output Voltage, Shutdown	$\overline{SHDN}$ = GND, no load		3.5	4.6	5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising (leaving lockout)				4.58	V
	V_{CC} falling (entering lockout)		4.0			
V_{CC} Undervoltage-Lockout Hysteresis				200		mV
GH1, GH2, GL1, GL2 On-Resistance, High	I_{TEST} = 10mA, V_{CC} = V_{DD} = 5.3V			20	37	Ω
GH1, GH2, GL1, GL2 On-Resistance, Low	I_{TEST} = 10mA, V_{CC} = V_{DD} = 5.3V			10	20	Ω
GH1, GH2, GL1, GL2 Maximum Output Current				0.3		A
BST1, BST2 Leakage Current	$V_{BST\_}$ = 12V, $V_{LX\_}$ = 7V				5	µA
Resonant Frequency Range	Guaranteed by design		30		80	kHz
Minimum Off-Time			340	470	600	ns
Maximum Off-Time			24	33	43	µs
Current-Limit Threshold LX1 to PGND, LX2 to PGND (Fixed)	ILIM = V_{CC}		180	200	220	mV
Current-Limit Threshold LX1 to PGND, LX2 to PGND (Adjustable)	V_{ILIM} = 0.5V		80	100	120	mV
	V_{ILIM} = 2.0V		370	400	430	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero-Current Crossing Threshold LX1 to GND, LX2 to GND		1	6	12	mV
Current-Limit Leading Edge Blanking		240	350	460	ns
IFB Input Voltage Range		-2		+2	V
IFB Regulation Point		770	790	810	mV
IFB Input Bias Current	$0 < V_{IFB} < 2V$	-2		+2	µA
	$-2V < V_{IFB} < 0$	-150			
IFB Lamp-Out Threshold		560	600	640	mV
IFB to COMP Transconductance	$0.5V < V_{COMP} < 4V$	60	100	160	µS
COMP Output Impedance		7	10	18	MΩ
COMP Discharge Current During Overvoltage or Overcurrent Fault	V_{IFB} = 800mV, V_{ISEC} = 2V		400		µA
COMP Discharge Current During DPWM Off-Time	CNTL = GND, V_{COMP} = 2V		100		µA
DPWM Rising to Falling Ratio	V_{IFB} = 0		2.5		
ISEC Overcurrent Threshold		1.15	1.21	1.28	V
ISEC Input Bias Current	$0 < V_{ISEC} < 2V$	-0.3		+0.3	µA
VFB Input Bias Current	V_{VFB} = 0.5V	-0.3		+0.3	µA
VFB Overvoltage Threshold		2.2	2.3	2.4	V
DPWM Chopping Frequency	R_{FREQ} = 100kΩ		343		Hz
	R_{FREQ} = 169kΩ	204	209	214	
	R_{FREQ} = 340kΩ		106		
DPWM Input Low Voltage	SYNC = V_{CC}, R_{FREQ} = 169kΩ			0.8	V
DPWM Input High Voltage	SYNC = V_{CC}, R_{FREQ} = 169kΩ	2.1			V
DPWM Input Hysteresis	SYNC = V_{CC}, R_{FREQ} = 169kΩ		100		mV
DPWM Input Bias Current	SYNC = V_{CC}, R_{FREQ} = 169kΩ	-0.3		+0.3	µA
DPWM Output Low Resistance	SYNC = GND, FREQ = V_{CC}			2.4	kΩ
DPWM Output High Resistance	SYNC = V_{CC}, FREQ = V_{CC}			2.4	kΩ
SYNC Input Low Voltage				0.8	V
SYNC Input High Voltage		2.1			V
SYNC Input Hysteresis			100		mV
SYNC Input Bias Current	V_{SYNC} = 2V	-0.3		+0.3	µA
SYNC Input Frequency Range		10		50	kHz
CNTL Minimum Duty-Cycle Threshold		0.20	0.23	0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9	2.0	2.1	V
CNTL Input Current	$0 < V_{CNTL} < V_{CC}$	-0.1		+0.1	µA
DPWM ADC Resolution	Guaranteed monotonic		5		Bits

Low-Cost CCFL Backlight Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		2.1			V
$\overline{SHDN}$ Input Bias Current		-1		+1	µA
FREQ Dual Mode™ Input High Level		V_{CC} - 0.35			V
FREQ Input Regulation Level			V_{CC} / 2		V
FREQ Input Bias Current	FREQ = V_{CC}		230		µA
TFLT Charge Current	V_{ISEC} < 1.25V and V_{IFB} < 600mV; V_{FLT} = 2V	0.95	1.00	1.05	µA
	V_{ISEC} < 1.25V and V_{IFB} > 600mV; V_{FLT} = 2V		-1		
	V_{ISEC} > 1.25V and V_{IFB} < 600mV; V_{FLT} = 2V		116		
TFLT Trip Threshold		3.95	4.10	4.20	V

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTIC

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Input Voltage Range	V_{CC} = V_{DD} = V_{BATT}		4.6		5.5	V
	V_{CC} = V_{DD} = open		5.5		28.0	
BATT Quiescent Current	$V_{\overline{SHDN}}$ = V_{CC}, V_{IFB} = 1V	V_{BATT} = 28V			2	mA
		V_{BATT} = V_{CC} = 5V			2	
BATT Quiescent Current, Shutdown	$\overline{SHDN}$ = GND				20	µA
V_{CC} Output Voltage, Normal Operation	$V_{\overline{SHDN}}$ = 5.5V, 6V < V_{BATT} < 28V 0 < I_{LOAD} < 20mA		5.25		5.55	V
V_{CC} Output Voltage, Shutdown	$\overline{SHDN}$ = GND, no load		3.5		5.5	V
V_{CC} Undervoltage-Lockout Threshold	V_{CC} rising (leaving lockout)				4.58	V
	V_{CC} falling (entering lockout)		4.0			
GH1, GH2, GL1, GL2 On-Resistance, High	I_{TEST} =10mA, V_{CC} = V_{DD} = 5.3V				37	Ω
GH1, GH2, GL1, GL2 On-Resistance, Low	I_{TEST} =10mA, V_{CC} = V_{DD} = 5.3V				20	Ω
BST1, BST2 Leakage Current	$V_{BST\_}$ = 12V, $V_{LX\_}$ = 7V				5	µA
Resonant Frequency Range	Guaranteed by design		30		80	kHz
Minimum Off-Time			340		600	ns
Maximum Off-Time			24		43	µs
Current-Limit Threshold LX1 - PGND, LX2 - PGND (Fixed)	ILIM = V_{CC}		180		220	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Limit Threshold LX1 - PGND, LX2 - PGND (Adjustable)	V_{ILIM} = 0.5V	80		120	mV
	V_{ILIM} = 2.0V	370		430	
Zero-Current Crossing Threshold LX1 - GND, LX2 - GND		1		12	mV
Current-Limit Leading Edge Blanking		240		460	ns
IFB Input Voltage Range		-2		+2	V
IFB Regulation Point		770		810	mV
IFB Input Bias Current	0 < V_{IFB} < 2V	-2		+2	µA
	-2V < V_{IFB} < 0	-150			
IFB Lamp-Out Threshold		560		640	mV
IFB to COMP Transconductance	0.5V < V_{COMP} < 4V	60		160	µS
COMP Output Impedance		7		18	MΩ
ISEC Overcurrent Threshold		1.15		1.28	V
VFB Overvoltage Threshold		2.2		2.4	V
DPWM Chopping Frequency	R_{FREQ} = 169kΩ	200		218	Hz
DPWM Input Low Voltage	SYNC = V_{CC}, R_{FREQ} = 169kΩ			0.8	V
DPWM Input High Voltage	SYNC = V_{CC}, R_{FREQ} = 169kΩ	2.1			V
DPWM Output Low Resistance	SYNC = GND, FREQ = V_{CC}			2.4	kΩ
DPWM Output High Resistance	SYNC = V_{CC}, FREQ = V_{CC}			2.4	kΩ
SYNC Input Low Voltage				0.8	V
SYNC Input High Voltage		2.1			V
SYNC Input Bias Current	V_{SYNC} = 2V	-0.3		+0.3	µA
SYNC Input Frequency Range		10		50	kHz
CNTL Minimum Duty-Cycle Threshold		0.20		0.26	V
CNTL Maximum Duty-Cycle Threshold		1.9		2.1	V
$\overline{SHDN}$ Input Low Voltage				0.8	V
$\overline{SHDN}$ Input High Voltage		2.1			V
FREQ Dual-Mode Input High Level		V_{CC} - 0.35			V
TFLT Trip Threshold		3.95		4.20	V

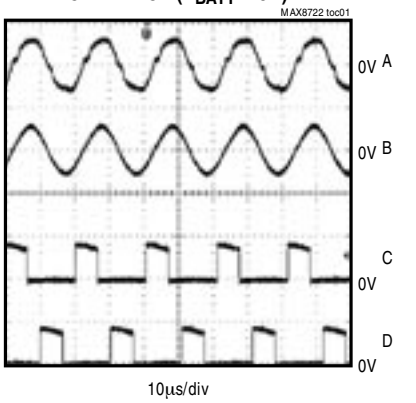
Note 1: Specifications to -40°C are guaranteed by design based on final characterization results.

Low-Cost CCFL Backlight Controller

Typical Operating Characteristics

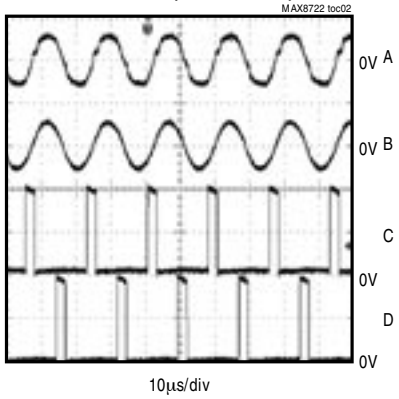
(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, T_A = +25°C, unless otherwise noted.)

LOW INPUT-VOLTAGE OPERATION (V_{BATT} = 8V)



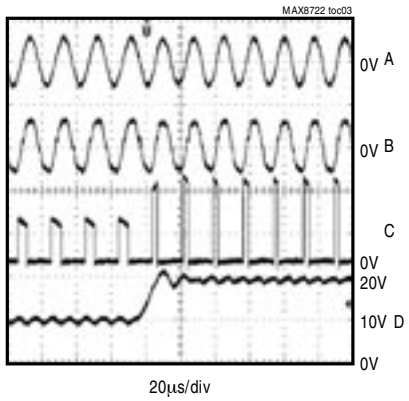
A: V_{IFB}, 2V/div C: V_{LX1}, 10V/div
B: V_{VFB}, 2V/div D: V_{LX2}, 10V/div

HIGH INPUT-VOLTAGE OPERATION (V_{BATT} = 20V)



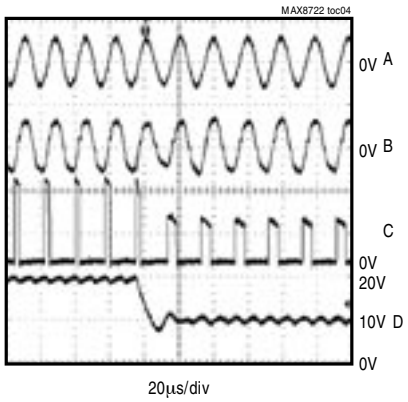
A: V_{IFB}, 2V/div C: V_{LX1}, 10V/div
B: V_{VFB}, 2V/div D: V_{LX2}, 10V/div

LINE-TRANSIENT RESPONSE



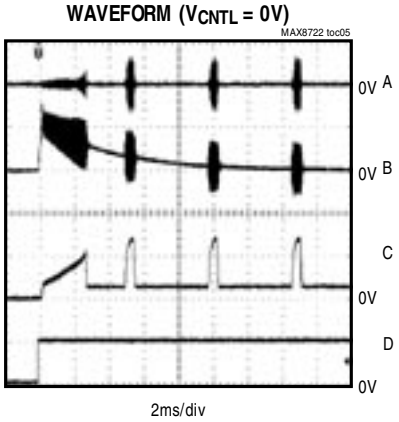
A: V_{VFB}, 2V/div C: V_{LX1}, 10V/div
B: V_{IFB}, 2V/div D: V_{BATT}, 10V/div

LINE-TRANSIENT RESPONSE



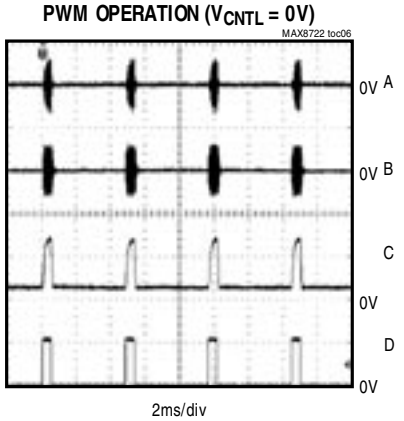
A: V_{VFB}, 2V/div C: V_{LX1}, 10V/div
B: V_{IFB}, 2V/div D: V_{BATT}, 10V/div

MINIMUM BRIGHTNESS STARTUP WAVEFORM (V_{CNTL} = 0V)



A: V_{IFB}, 2V/div C: V_{COMP}, 1V/div
B: V_{VFB}, 2V/div D: $V_{\overline{SHDN}}$, 5V/div

MINIMUM BRIGHTNESS DIGITAL PWM OPERATION (V_{CNTL} = 0V)

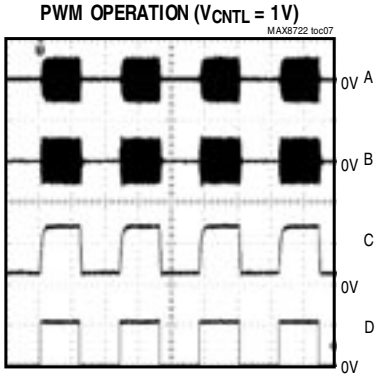


A: V_{IFB}, 2V/div C: V_{COMP}, 1V/div
B: V_{VFB}, 2V/div D: V_{DPWM}, 5V/div

Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, T_A = +25°C, unless otherwise noted.)

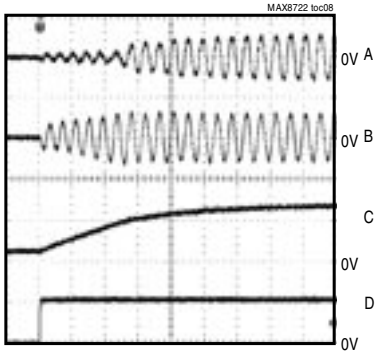
50% BRIGHTNESS DIGITAL PWM OPERATION (V_{CNTL} = 1V)



2ms/div

A: V_{IFB}, 2V/div
B: V_{VFB}, 2V/div
C: V_{COMP}, 1V/div
D: V_{DPWM}, 5V/div

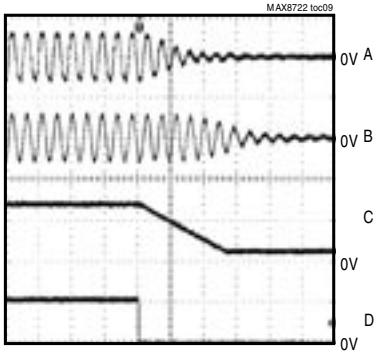
DIGITAL PWM SOFT-START



40µs/div

A: V_{IFB}, 2V/div
B: V_{VFB}, 2V/div
C: V_{COMP}, 1V/div
D: V_{DPWM}, 5V/div

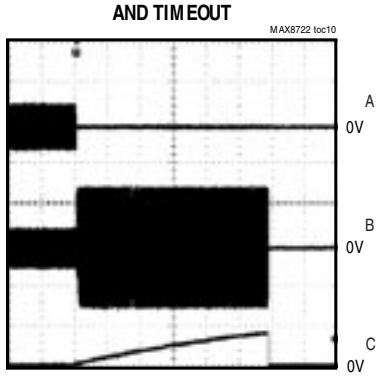
DIGITAL PWM SOFT-STOP



40µs/div

A: V_{IFB}, 2V/div
B: V_{VFB}, 2V/div
C: V_{COMP}, 1V/div
D: V_{DPWM}, 5V/div

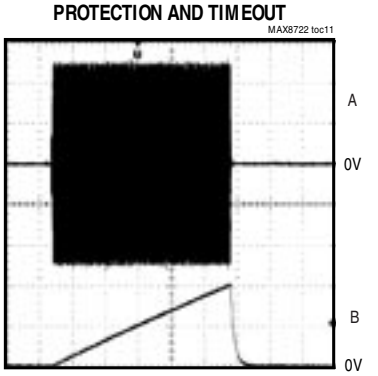
LAMP-OUT VOLTAGE LIMITING AND TIMEOUT



200ms/div

A: V_{IFB}, 2V/div
B: V_{VFB}, 2V/div
C: V_{TFLT}, 5V/div

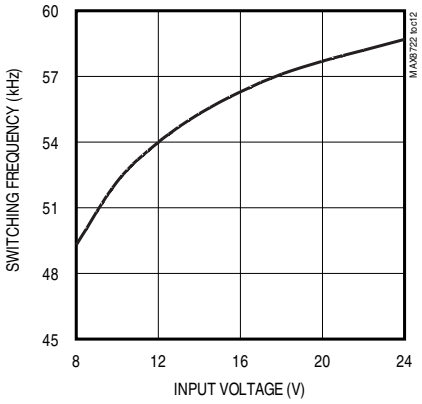
SECONDARY OVERCURRENT PROTECTION AND TIMEOUT



4ms/div

A: V_{ISEC}, 500mV/div
B: V_{TFLT}, 2V/div

SWITCHING FREQUENCY vs. INPUT VOLTAGE

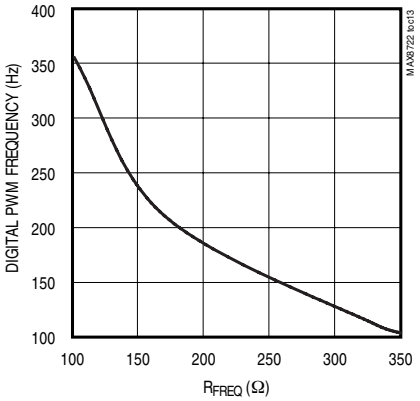


Low-Cost CCFL Backlight Controller

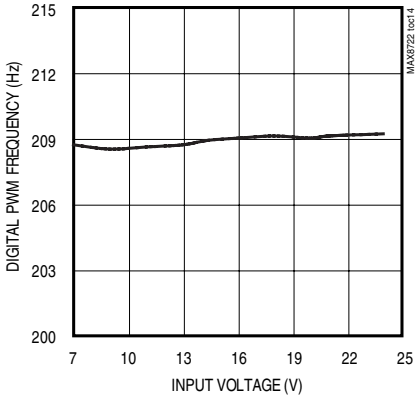
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{BATT} = 12V, V_{CC} = V_{DD}, $V_{\overline{SHDN}}$ = 5.3V, T_A = +25°C, unless otherwise noted.)

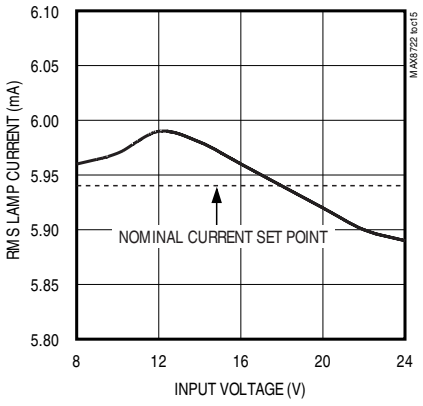
DIGITAL PWM FREQUENCY vs. R_{FREQ}



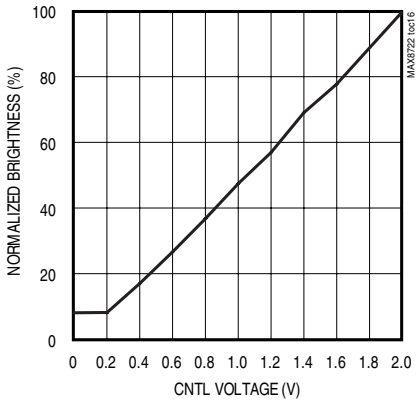
DIGITAL PWM FREQUENCY vs. INPUT VOLTAGE



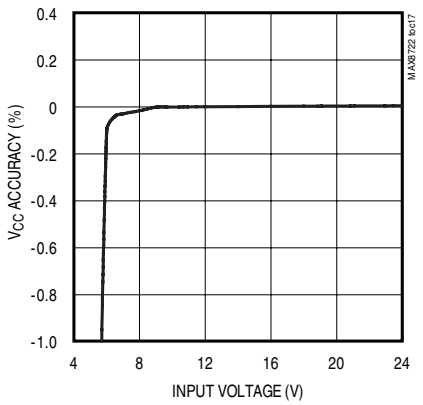
RMS LAMP CURRENT vs. INPUT VOLTAGE



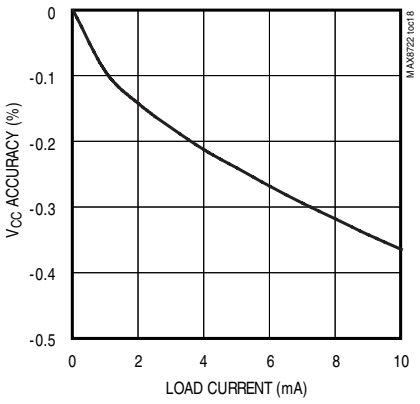
NORMALIZED BRIGHTNESS vs. CNTL VOLTAGE



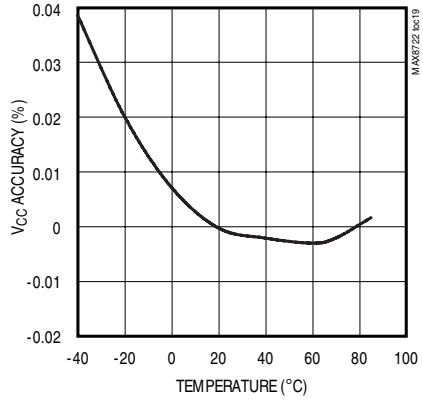
V_{CC} LINE REGULATION



V_{CC} LOAD REGULATION



V_{CC} ACCURACY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	BATT	Supply Input. BATT is the input to the internal 5.4V linear regulator that powers the device. Bypass BATT to GND with a 0.1µF ceramic capacitor.
2	$\overline{SHDN}$	Shutdown Control Input. The device shuts down when $\overline{SHDN}$ is pulled to GND.
3	ILIM	Primary Current-Limit Adjustment Input. Connect a resistive voltage-divider between V_{CC} and GND to set the primary current limit. The current-limit threshold is 1/5 of the voltage at ILIM. Connect it to V_{CC} with a pullup resistor to select the default current-limit threshold of 0.2V.
4	TFLT	Fault Timer Adjustment Pin. Connect a capacitor from TFLT to GND to set the timeout periods for open-lamp and secondary overcurrent faults.
5	CNTL	Brightness Control Input. Varying V_{CNTL} between 0 and 2V varies the DPWM duty cycle (brightness) between 10% (minimum) and 100% (maximum). The brightness remains at maximum for V_{CNTL} greater than 2V.
6	DPWM	Dual-Function DPWM Signal Pin. The DPWM pin can be used either as the DPWM signal output or as a low-frequency sync input. See the *Digital PWM Dimming Control* and *Digital PWM Frequency Setting* sections.
7	SYNC	DPWM High-Frequency Sync Input. The DPWM chopping frequency can be synchronized to an external high-frequency signal by connecting FREQ to V_{CC} and SYNC to the external signal source. The DPWM chopping frequency is 1/128 of the frequency of the external signal.
8	FREQ	DPWM Frequency Dual-Mode Adjustment Pin. Connect a resistor from FREQ to GND to set the DPWM frequency. Connect FREQ to V_{CC} to set DPWM frequency using SYNC. f_{DPWM} = 209Hz x 169kΩ / R_{FREQ}
9	COMP	Transconductance Error-Amplifier Output. A compensation capacitor connected between COMP and GND sets the rise and fall time of the lamp current in DPWM operation.
10	IFB	Lamp-Current Feedback Input. The average voltage on IFB is regulated to 0.8V by controlling the on-time of high-side switches. If V_{IFB} falls below 0.6V for a period longer than the timeout period set by TFLT, the MAX8722 activates the fault latch.
11	VFB	Transformer Secondary Voltage Feedback Input. A capacitive voltage-divider between the high-voltage terminal of the CCFL tube and GND sets the maximum average lamp voltage during lamp strike and open-lamp conditions. When the average voltage on VFB exceeds the internal overvoltage threshold, the controller turns on an internal current sink discharging the COMP capacitor.
12	ISEC	Transformer Secondary Current Feedback Input. A current-sense resistor connected between the low-voltage end of the transformer secondary and ground sets the maximum secondary current during faults. When the average voltage on ISEC exceeds the internal overcurrent threshold, the controller turns on an internal current sink discharging the COMP capacitor.
13	GH2	High-Side MOSFET NH2 Gate-Driver Output
14	LX2	GH2 Gate-Driver Return. LX2 is the input to the current-limit and zero-crossing comparators. The device senses the voltage across the low-side MOSFET NL2 to detect primary current zero-crossing and primary overcurrent.
15	BST2	GH2 Gate-Driver Supply Input. Connect a 0.1µF capacitor from LX2 to BST2 and a diode from V_{DD} to BST2 to form a bootstrap circuit.
16	BST1	GH1 Gate-Driver Supply Input. Connect a 0.1µF capacitor from LX1 to BST1 and a diode from V_{DD} to BST1 to form a bootstrap circuit.
17	LX1	GH1 Gate-Driver Return. LX1 is the input to the current-limit and zero-crossing comparators. The device senses the voltage across the low-side MOSFET NL1 to detect primary current zero-crossing and primary overcurrent.

Low-Cost CCFL Backlight Controller

Pin Description (continued)

PIN	NAME	FUNCTION
18	GH1	High-Side MOSFET NH1 Gate-Driver Output
19	GL1	Low-Side MOSFET NL1 Gate-Driver Output
20	GL2	Low-Side MOSFET NL2 Gate-Driver Output
21	PGND	Power Ground. PGND is the return for the GL1 and GL2 gate drivers.
22	V_{DD}	Low-Side Gate-Driver Supply Input. Connect V_{DD} to the output of the internal linear regulator (V_{CC}). Bypass V_{DD} with a 0.1µF capacitor to PGND.
23	V_{CC}	5.3V/10mA Internal Linear-Regulator Output. V_{CC} is the supply voltage for the device. Bypass V_{CC} with a 1µF ceramic capacitor to GND.
24	GND	Analog Ground. The ground return for V_{CC}, REF, and other analog circuitry. Connect GND to PGND under the IC at the IC's backside exposed metal pad.

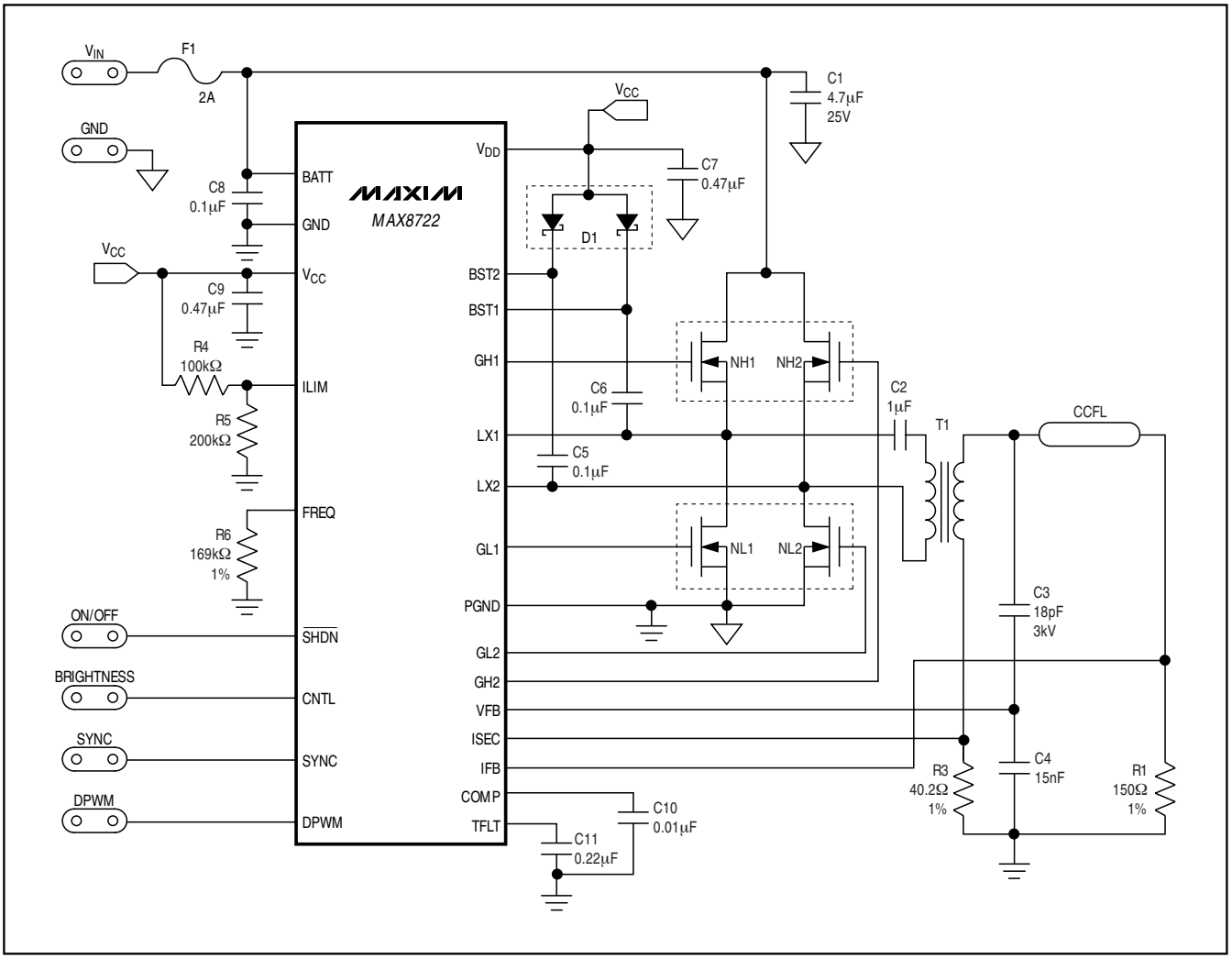


Figure 1. Typical Operating Circuit of the MAX8722

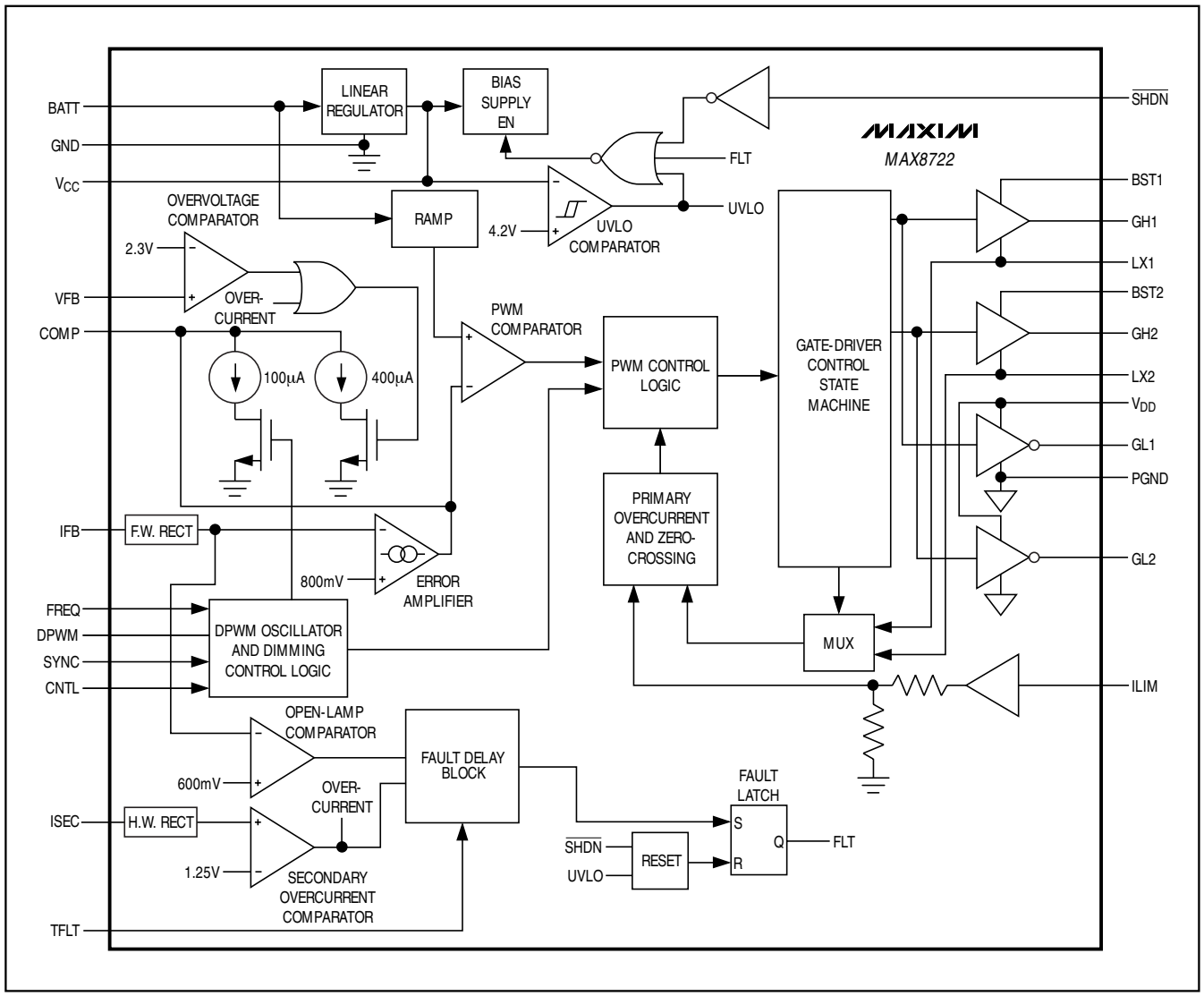


Figure 2. MAX8722 Functional Diagram

Low-Cost CCFL Backlight Controller

Typical Operating Circuit

The typical operating circuit of the MAX8722 (Figure 1) is a complete CCFL backlight inverter for TFT-LCD panels. The input voltage range of the circuit is from 8V to 24V. The maximum RMS lamp current is set to 6mA, and the maximum RMS striking voltage is set to 1600V. Table 1 lists some important components, and Table 2 lists the component suppliers' contact information.

Detailed Description

The MAX8722 controls a full-bridge resonant inverter to convert an unregulated DC input into a near-sinusoidal, high-frequency AC output for powering CCFLs. The lamp brightness is adjusted by turning the lamp on and off with a digital pulse-width-modulation (DPWM) signal. The brightness of the lamp is proportional to the duty cycle of the DPWM signal, which is set through an analog voltage on the CNTL pin. Figure 2 shows the functional diagram of the MAX8722.

Table 1. List of Important Components

DESIGNATION	DESCRIPTION
C1	4.7µF ±20%, 25V X5R ceramic capacitor Murata GRM32RR61E475K Taiyo Yuden TMK325BJ475MN TDK C3225X7R1E475M
C2	1µF ±10%, 25V X7R ceramic capacitor
C3	18pF ±1pF, 3kV, high-voltage ceramic capacitor Murata GRM42D1X3F180J TDK C4520C0G3F180F
D1	Dual silicon switching diode, common anode, SOT-323 Central Semiconductor CMSD2836 Diodes, Inc. BAW56W
NH1/2, NL1/2	Dual n-channel MOSFETs, 30V, 0.095, SOT23-6 Fairchild FDC6561AN
T1	CCFL transformer, 1:93 turns ratio TOKO T912MG-1018

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Central Semiconductor	www.centralsemi.com
Diodes Inc.	www.diodes.com
Fairchild Semiconductor	www.fairchildsemi.com
Murata	www.murata.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.components.tdk.com
TOKO	www.tokoam.com

Resonant Operation

The MAX8722 drives the four n-channel power MOSFETs that make up the zero-voltage-switching (ZVS) full-bridge inverter as shown in Figure 3. Assume that NH1 and NL2 are turned on at the beginning of a switching cycle as shown in Figure 3(a). The primary current flows through MOSFET NH1, DC blocking capacitor C2, the primary side of transformer T1, and MOSFET NL2. During this interval, the primary current ramps up until the controller turns off NH1. When NH1 turns off, the primary current forward biases the body diode of NL1, which clamps the LX1 voltage just below ground as shown in Figure 3(b). When the controller turns on NL1, its drain-to-source voltage is near zero because its forward-biased body diode clamps the drain. Since NL2 is still on, the primary current flows through NL1, C2, the primary side of T1, and NL2. Once the primary current drops to the minimum current threshold ($6mV/R_{DS(ON)}$), the controller turns off NL2. The remaining energy in T1 charges up the LX2 node until the body diode of NH2 is forward biased. When NH2 turns on, it does so with near-zero drain-to-source voltage. The primary current reverses polarity as shown in Figure 3(c), beginning a new cycle with the current flowing in the opposite direction, with NH2 and NL1 on. The primary current ramps up until the controller turns off NH2. When NH2 turns off, the primary current forward biases the body diode of NL2, which clamps the LX2 voltage just below ground as shown in Figure 3(d). After the LX2 node goes low, the controller losslessly turns on NL2. Once the primary current drops to the minimum current threshold, the controller turns off NL1. The remaining energy charges up the LX1 node until the body diode of NH1 is forward biased. Finally, NH1 losslessly turns on, beginning a new cycle as shown in Figure 3(a). Note that switching transitions on all four power MOSFETs occur under ZVS condition, which reduces transient power losses and EMI.

A simplified CCFL inverter circuit is shown in Figure 4(a). The full-bridge power stage is simplified and represented as a square-wave AC source. The resonant tank circuit can be further simplified to Figure 4(b) by removing the transformer. C_S is the primary series capacitor, C'_S is the series capacitance reflected to the secondary, C_P is the secondary parallel capacitor, N is the transformer turns ratio, L is the transformer secondary leakage inductance, and R_L is an idealized resistance that models the CCFL in normal operation.

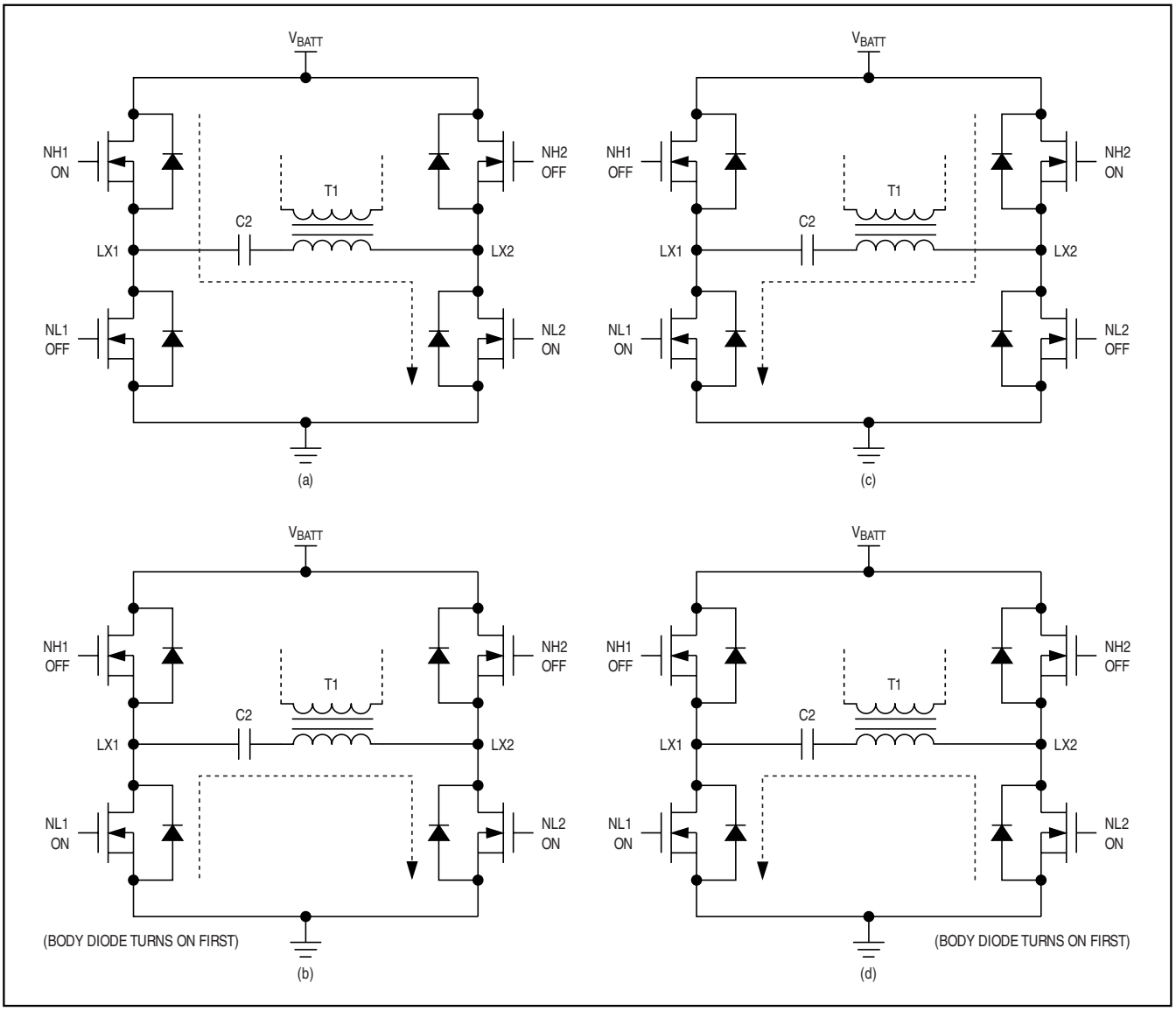


Figure 3. Resonant Operation

Low-Cost CCFL Backlight Controller

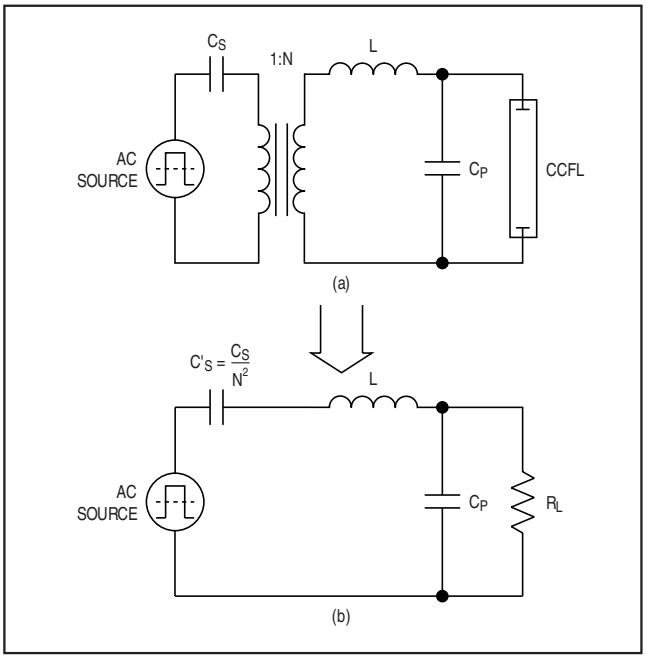


Figure 4. Equivalent Resonant Tank Circuit

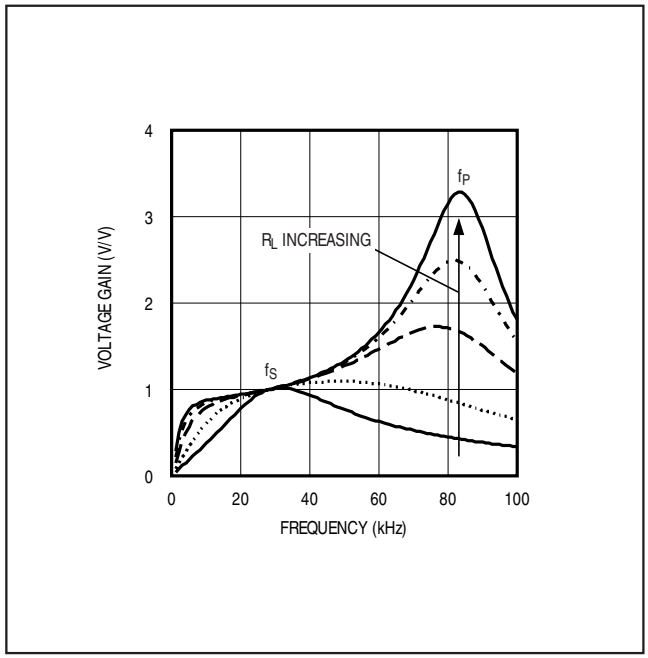


Figure 5. Frequency Response of the Resonant Tank

Figure 5 shows the frequency response of the resonant tank's voltage gain under different load conditions. The primary series capacitor is 1µF, the secondary parallel capacitor is 15pF, the transformer turns ratio is 1:93, and the secondary leakage inductance is 260mH. Notice that there are two peaks, f_S and f_P, in the frequency response. The first peak, f_S, is the series resonant peak determined by the secondary leakage inductance (L) and the series capacitor reflected to the secondary (C'_S):

$$f_S = \frac{1}{2\pi\sqrt{LC'_S}}$$

The second peak, f_P, is the parallel resonant peak determined by the secondary leakage inductance (L), the parallel capacitor (C_P), and the series capacitor reflected to the secondary (C'_S):

$$f_P = \frac{1}{2\pi\sqrt{L\frac{C'_S C_P}{C'_S + C_P}}}$$

The inverter is designed to operate between these two resonant peaks. When the lamp is off, the operating point of the resonant tank is close to the parallel resonant peak due to the lamp's infinite impedance. The circuit displays the characteristics of a parallel-loaded resonant converter. While in parallel-loaded resonant operation, the inverter behaves like a voltage source to generate the necessary striking voltage. Theoretically, the output voltage of the resonant converter will increase until the lamp is ionized or until it reaches the IC's secondary voltage limit, without regard to the transformer turns ratio or the input voltage level. Once the lamp is ionized, the equivalent load resistance decreases rapidly and the operating point moves toward the series resonant peak. While in series resonant operation, the inverter behaves like a current source.

Lamp-Current Regulation

The MAX8722 uses a lamp-current control loop to regulate the current delivered to the CCFL. The heart of the control loop is a transconductance error amplifier. The AC lamp current is sensed with a resistor connected in series with the low-voltage terminal of the lamp. The voltage across this resistor is fed to the IFB input and is internally full-wave rectified. The transconductance error amplifier compares the rectified IFB voltage with a 790mV (typ) internal threshold to generate an error current. The error current charges and discharges a capacitor connected between COMP and ground to create an error voltage (V_{COMP}). V_{COMP} is then compared with an internal ramp signal to set the high-side MOSFET switch on-time (t_{ON}).

Transformer Secondary Voltage Limiting

The MAX8722 reduces the voltage stress on the transformer's secondary winding by limiting the secondary voltage during startup and open-lamp faults. The AC voltage across the transformer secondary winding is sensed through a capacitive voltage-divider. The small voltage across the larger capacitor of the divider is fed to the VFB input and is internally half-wave rectified. An overvoltage comparator compares the VFB voltage with a 2.3V (typ) internal threshold. Once the sense voltage exceeds the overvoltage threshold, the MAX8722 turns on a 400µA current source that discharges the COMP capacitor. The high-side MOSFET on-time shortens as the COMP voltage decreases, reducing the transformer secondary's peak voltage below the threshold set by the capacitive voltage-divider.

Lamp Startup

A CCFL is a gas discharge lamp that is normally driven in the avalanche mode. To start ionization in a nonionized lamp, the applied voltage (striking voltage) must be increased to the level required for the start of avalanche. At low temperatures, the striking voltage can be several times the typical operating voltage.

Because of the MAX8722's resonant topology, the striking voltage is guaranteed. Before the lamp is ionized, the lamp impedance is infinite. The transformer secondary leakage inductance and the high-voltage parallel capacitor determine the unloaded resonant frequency. Since the unloaded resonant circuit has a high Q, it can generate very high voltages across the lamp.

Upon power-up, two soft-start features acting together smooth the startup behavior. First, V_{COMP} slowly rises, increasing the duty cycle of the high-side MOSFET switches and providing a measure of soft-start. Second, the MAX8722 charges VFB to the overvoltage threshold (2.3V typ) immediately after the device is enabled. The DC voltage on VFB is gradually discharged through an internal 300kΩ (typ) resistor during startup. This feature is equivalent to slowly raising the overvoltage threshold during startup, so it further improves the soft-start behavior.

Feed-Forward Control and Dropout Operation

The MAX8722 is designed to maintain tight control of the lamp current under all transient conditions. The feed-forward control instantaneously adjusts the on-time for changes in input voltage (V_{BATT}). This feature provides immunity to input-voltage variations and simplifies loop compensation over wide input voltage ranges. The feed-forward control also improves the line regulation for short on-times and makes startup transients less dependent on the input voltage.

Feed-forward control is implemented by increasing the internal voltage ramp rate for higher V_{BATT}. This has the effect of varying t_{ON} as a function of the input voltage while maintaining approximately the same signal levels at V_{COMP}. Since the required voltage change across the compensation capacitor is minimal, the controller's response to input voltage changes is essentially instantaneous.

Digital PWM Dimming Control

The MAX8722 controls the brightness of the CCFL by chopping the lamp current on and off using a low-frequency (between 100Hz and 350Hz) digital PWM signal either from the internal oscillator or from an external signal source. The CCFL brightness is proportional to the digital PWM duty cycle, which can be adjusted from 9.375% to 100% by the CNTL pin. CNTL is an analog input with a usable input voltage range between 0 and 2000mV, which is digitized to select one of 128 brightness levels. As shown in Figure 6, the MAX8722 ignores the first twelve steps, so the first twelve steps all represent the same brightness. When V_{CNTL} is between 0 and 187.5mV, the digital PWM duty cycle is always 9.375%. When V_{CNTL} is above 187.5mV, a 15.625mV change on CNTL results in a 0.78125% change in the digital PWM duty cycle. When V_{CNTL} is equal to or above 2000mV, the digital PWM duty cycle is always 100%.

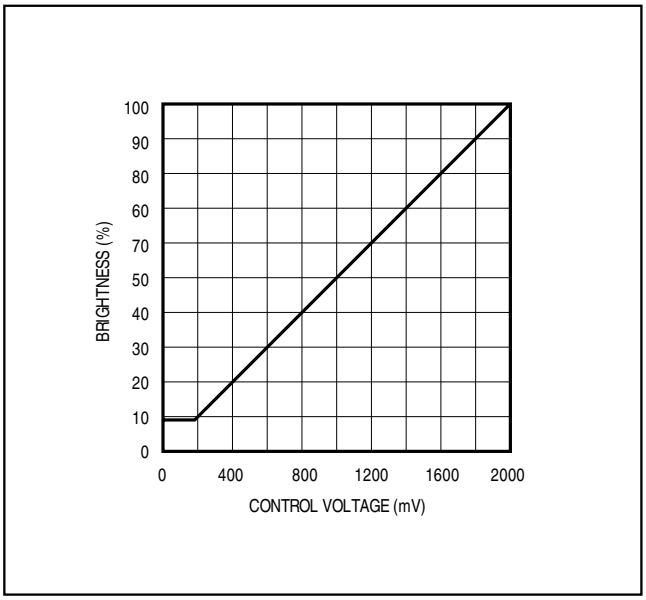


Figure 6. Theoretical Brightness vs. Control Voltage

In digital PWM operation, COMP controls the rise and fall time of the lamp-current envelope. At the beginning of the digital PWM on-cycle, V_{COMP} rises linearly, gradually increasing t_{ON}, which provides soft-start. At the end of the digital PWM on-cycle, the COMP capacitor discharges linearly, gradually decreasing t_{ON} and providing soft-stop.

Digital PWM Frequency Setting

There are three ways to set the digital PWM frequency.

1) The digital PWM frequency can be set with an external resistor. Connect SYNC to GND and connect a resistor between FREQ and GND. The digital PWM frequency is given by the following equation:

$$f_{DPWM} = 209Hz \times 169k\Omega / R_{FREQ}$$

The adjustable range of the digital PWM frequency is between 100Hz and 350Hz (R_{FREQ} is between 353kΩ and 101kΩ). CNTL controls the digital PWM duty cycle.

2) The digital PWM frequency can be clocked by an external high-frequency signal. Connect FREQ to V_{CC} and connect SYNC to the external high-frequency signal. The digital PWM frequency is 1/128 of the frequency of the external signal:

$$f_{DPWM} = \frac{f_{EXT}}{128}$$

where f_{EXT} is the frequency of the external signal. The frequency range of the external signal should be between 13kHz and 45kHz, resulting in a digital PWM frequency range between 100Hz and 350Hz. CNTL controls the DPWM duty cycle.

3) The digital PWM frequency can be synchronized to an external low-frequency signal. To enable this mode, connect SYNC to V_{CC}, connect FREQ to GND through a 100kΩ resistor, and connect DPWM to the external low-frequency signal. The digital PWM frequency and duty cycle are equal to those of the external signal.

The frequency range of the external signal is between 100Hz and 350Hz. In this mode, the brightness control input CNTL is disabled, and the brightness is proportional to the duty cycle of the external signal.

Table 3 summarizes the three ways of setting the digital PWM frequency.

UVLO

The MAX8722 includes an undervoltage-lockout (UVLO) circuit. The UVLO circuit monitors the V_{CC} voltage. When V_{CC} is below 4.2V (typ), the MAX8722 disables both high-side and low-side MOSFET drivers and resets the fault latch.

Low-Power Shutdown

When the MAX8722 is placed in shutdown, all functions of the IC are turned off except for the 5.4V linear regulator. In shutdown, the linear-regulator output voltage drops to about 4.5V and the supply current is 6µA (typ). While in shutdown, the fault latch is reset. The device can be placed into shutdown by pulling $\overline{SHDN}$ to its logic-low level.

Lamp-Out Protection

For safety, the MAX8722 monitors the lamp-current feedback (IFB) to detect faulty or open CCFL tubes and secondary short circuits in the lamp and IFB sense resistor. As described in the *Lamp-Current Regulation* section, the voltage on IFB is internally full-wave rectified. If the rectified IFB voltage is below 600mV, the MAX8722 charges the TFLT capacitor with 1µA. The

Table 3. Digital PWM Frequency Setting

FREQ	SYNC	DPWM	DIGITAL PWM FREQUENCY/DUTY CYCLE
Connect FREQ to GND through an external resistor.	Connect SYNC to GND.	DPWM is used as the digital PWM signal output.	The resistor value sets the frequency. CNTL controls the duty cycle.
Connect FREQ to V_{CC}.	Connect SYNC to an external high-frequency signal.	DPWM is used as the digital PWM signal output.	The frequency is 1/128 of the frequency of the external signal. CNTL controls the duty cycle.
Connect FREQ to GND through a 100kΩ resistor.	Connect SYNC to V_{CC}.	Connect DPWM to an external low-frequency signal.	The frequency and duty cycle are equal to those of the external signal.

MAX8722 latches off if the voltage on TFLT exceeds 4V. Unlike the normal shutdown mode, the linear-regulator output (V_{CC}) remains at 5.4V. Toggling $\overline{SHDN}$ or cycling the input power reactivates the device.

During the delay period, the current control loop tries to maintain lamp-current regulation by increasing the high-side MOSFET on-time. Because the open-circuit lamp impedance is very high, the transformer secondary voltage rises as a result of the high Q-factor of the resonant tank. Once the secondary voltage exceeds the overvoltage threshold, the MAX8722 turns on a 400µA current source that discharges the COMP capacitor. The on-time of the high-side MOSFET is reduced, lowering the secondary voltage, as the COMP voltage decreases. Therefore, the peak voltage of the transformer secondary winding never exceeds the limit set by a capacitive voltage-divider during the lamp-out delay period.

Primary Overcurrent Protection (ILIM)

The MAX8722 senses transformer primary current in each switching cycle. When the regulator turns on the low-side MOSFET, a comparator monitors the voltage drop from LX_ to GND. If the voltage exceeds the current-limit threshold, the regulator turns off the high-side switch at the opposite side of the primary to prevent further increasing the transformer primary current.

The current-limit threshold can be adjusted using the ILIM input. Connect a resistive voltage-divider between V_{CC} and GND with the midpoint connected to ILIM. The current-limit threshold measured between LX_ and GND is 1/5 of the voltage at ILIM. The ILIM adjustment range is 0 to 3V. Connect ILIM to V_{CC} to select the default current-limit threshold of 0.2V.

Secondary Current Limit (ISEC)

The secondary current limit provides fail-safe current limiting in case a failure, such as a short circuit or leakage from the lamp high-voltage terminal to ground, prevents the current control loop from functioning properly. ISEC monitors the voltage across a sense resistor placed between the transformer's low-voltage secondary terminal and ground. The ISEC voltage is internally half-wave rectified and continuously compared to the ISEC regulation threshold (1.25V typ). Any time the ISEC voltage exceeds the threshold, a controlled current is drawn from COMP to reduce the on-time of the bridge's high-side switches. At the same time, the MAX8722 charges the TFLT capacitor with a 116µA current source. The MAX8722 latches off when the voltage on TFLT exceeds 4V. Unlike the normal shutdown mode, the linear-regulator output (V_{CC}) remains at 5.3V. Toggling $\overline{SHDN}$ or cycling the input power reactivates the device.

Linear-Regulator Output (V_{CC})

The internal linear regulator steps down the DC input voltage to 5.4V (typ). The linear regulator supplies power to the internal control circuitry of the MAX8722 and is also used to power the MOSFET drivers by connecting V_{CC} to V_{DD}. The V_{CC} voltage drops to 4.5V in shutdown.

Applications Information

MOSFETs

The MAX8722 requires four external n-channel power MOSFETs NL1, NL2, NH1, and NH2 to form a full-bridge inverter circuit to drive the transformer primary. The regulator senses the on-state drain-to-source voltage of the two low-side MOSFETs NL1 and NL2 to detect the transformer primary current, so the $R_{DS(ON)}$ of NL1 and NL2 should be matched. For instance, if dual MOSFETs are used to form the full bridge, NL1 and NL2 should be in one package. Since the MAX8722 uses the low-side MOSFET $R_{DS(ON)}$ for primary overcurrent protection, the lower the MOSFET $R_{DS(ON)}$, the higher the current limit. Therefore, the user should select a dual, logic-level n-channel MOSFET with low $R_{DS(ON)}$ to minimize conduction loss, and keep the primary current limit at a reasonable level.

The regulator uses zero-voltage switching (ZVS) to softly turn on each of the four switches in the full bridge. ZVS occurs when the external power MOSFETs are turned on when their respective drain-to-source voltages are near 0V (see the *Resonant Operation* section). ZVS effectively eliminates the instantaneous turn-on loss of MOSFETs caused by C_{OSS} (drain-to-source capacitance) and parasitic capacitance discharge, and improves efficiency and reduces switching-related EMI.

Setting the Lamp Current

The MAX8722 senses the lamp current flowing through resistor R1 (Figure 1) connected between the low-voltage terminal of the lamp and ground. The voltage across R1 is fed to IFB and is internally full-wave rectified. The MAX8722 controls the desired lamp current by regulating the average of the rectified IFB voltage. To set the RMS lamp current, determine R1 as follows:

$$R1 = \frac{\pi \times 790mV}{2\sqrt{2} \times I_{LAMP(RMS)}}$$

where $I_{LAMP(RMS)}$ is the desired RMS lamp current and 790mV is the typical value of the IFB regulation point

specified in the *Electrical Characteristics* table. To set the RMS lamp current to 6mA, the value of R1 should be 148Ω. The closest standard 1% resistors are 147Ω and 150Ω. The precise shape of the lamp-current waveform, which is dependent on lamp parasitics, influences the actual RMS lamp current. Use a true RMS current meter connected between the R1/IFB junction and the low-voltage side of the lamp to make final adjustments to R1.

Setting the Secondary Voltage Limit

The MAX8722 limits the transformer secondary voltage during startup and lamp-out faults. The secondary voltage is sensed through the capacitive voltage-divider formed by C3 and C4 (Figure 1). The voltage on VFB is proportional to the CCFL voltage. The selection of the parallel resonant capacitor C3 is described in the *Transformer Design and Resonant Component Selection* section. C3 is usually between 10pF and 22pF. After the value of C3 is determined, select C4 using the following equation to set the desired maximum RMS secondary voltage $V_{LAMP(RMS)\_MAX}$:

$$C4 = \frac{\sqrt{2} \times V_{LAMP(RMS)\_MAX}}{2.3V} \times C3$$

where 2.3V is the typical value of the VFB overvoltage threshold specified in the *Electrical Characteristics* table. To set the maximum RMS secondary voltage to 1600V using 18pF for C3, use approximately 15nF for C4.

Setting the Secondary Current Limit

The MAX8722 limits the secondary current even if the IFB sense resistor (R1) is shorted or transformer secondary current finds its way to ground without passing through R1. ISEC monitors the voltage across the sense resistor R3, connected between the low-voltage terminal of the transformer secondary winding and ground. Determine the value of R3 using the following equation:

$$R3 = \frac{1.217V}{\sqrt{2} \times I_{SEC(RMS)\_MAX}}$$

where $I_{SEC(RMS)\_MAX}$ is the desired maximum RMS transformer secondary current during fault conditions, and 1.217V is the typical value of the ISEC regulation point specified in the *Electrical Characteristics* table. To set the maximum RMS secondary current in the circuit of Figure 1 to 22mA, use approximately 40.2Ω for R3.

Transformer Design and Resonant Component Selection

The transformer is the most important component of the resonant tank circuit. The first step in designing the transformer is to determine the turns ratio (N). The ratio must be high enough to support the CCFL operating voltage at the minimum supply voltage. N can be calculated as follows:

$$N \geq \frac{V_{LAMP(RMS)}}{0.9 \times V_{IN(MIN)}}$$

where $V_{LAMP(RMS)}$ is the maximum RMS lamp voltage in normal operation, and $V_{IN(MIN)}$ is the minimum DC input voltage. If the maximum RMS lamp voltage in normal operation is 650V and the minimum DC input voltage is 8V, the turns ratio should be greater than 90. The turns ratio of the transformer used in the circuit of Figure 1 is 93.

The next step in the design procedure is to determine the desired operating frequency range. The MAX8722 is synchronized to the natural resonant frequency of the resonant tank. The resonant frequency changes with operating conditions, such as the input voltage, lamp impedance, etc.; therefore, the switching frequency varies over a certain range. To ensure reliable operation, the resonant frequency range must be within the operating frequency range specified by the CCFL transformer manufacturer. As discussed in the *Resonant Operation* section, the resonant frequency range is determined by the transformer secondary leakage inductance L, the primary series DC blocking capacitor C2, and the secondary parallel resonant capacitor C3. Since it is difficult to control the transformer leakage inductance, the resonant tank design should be based on the existing secondary leakage inductance of the selected CCFL transformer. Leakage-inductance values can have large tolerance and significant variations among different batches, so it is best to work directly with transformer vendors on leakage-inductance requirements. The MAX8722 works best when the secondary leakage inductance is between 250mH and 350mH. The series capacitor C2 sets the minimum operating frequency, which is approximately two times the series resonant peak frequency. Choose:

$$C2 \leq \frac{N^2}{\pi^2 \times f_{MIN}^{\ 2} \times L}$$

where f_{MIN} is the minimum operating frequency range. In the circuit of Figure 1, the transformer's turns ratio is 93 and its secondary leakage inductance is approximately 300mH. To set the minimum operating frequency to 45kHz, use 1µF for C2.

The parallel capacitor C3 sets the maximum operating frequency, which is also the parallel resonant peak frequency. Choose C3 with the following equation:

$$C3 \geq \frac{C2}{(4\pi^2 \times f_{MAX}^2 \times L \times C2) - N^2}$$

In the circuit of Figure 1, to set the maximum operating frequency to 65kHz, use 18pF for C3.

The transformer core saturation should also be considered when selecting the operating frequency. The primary winding should have enough turns to prevent transformer saturation under all operating conditions. Use the following expression to calculate the minimum number of turns N1 of the primary winding:

$$N1 > \frac{D_{MAX} \times V_{IN(MAX)}}{B_S \times S \times f_{MIN}}$$

where D_{MAX} is the maximum duty cycle (approximately 0.8) of the high-side switches, $V_{IN(MAX)}$ is the maximum DC input voltage, B_S is the saturation flux density of the core, and S is the minimal cross-section area of the core.

COMP Capacitor Selection

The COMP capacitor sets the speed of the current loop that is used during startup, while maintaining lamp current regulation, and during transients caused by changing the input voltage. The typical COMP capacitor value is 0.01µF. Larger values increase the transient-response delays. Smaller values speed up transient response, but extremely small values can cause loop instability.

Other Components

The external bootstrap circuits formed by D1 and C5/C6 in Figure 1 power the high-side MOSFET drivers. Connect V_{DD} to BST1/BST2 through dual-diode D1 and couple BST1/BST2 to LX1/LX2 through C5 and C6. C5 = C6 = 0.1µF or greater.

Layout Guidelines

Careful PC board layout is important to achieve stable operation. The high-voltage section and the switching section of the circuit require particular attention. The high-voltage sections of the layout need to be well separated from the control circuit. Most layouts for single-lamp notebook displays are constrained to long and narrow form factors, so this separation occurs naturally. Follow these guidelines for good PC board layout:

1) Keep the high-current paths short and wide, especially at the ground terminals. This is essential for stable, jitter-free operation and high efficiency.
2) Use a star-ground configuration for power and analog grounds. The power and analog grounds should be completely isolated—meeting only at the center of the star. The center should be placed at the analog ground pin (GND). Using separate copper islands for these grounds may simplify this task. Quiet analog ground is used for V_{CC}, COMP, FREQ, TFLT, and ILIM (if a resistive voltage-divider is used).
3) Route high-speed switching nodes away from sensitive analog areas (V_{CC}, COMP, FREQ, TFLT, and ILIM). Make all pin-strap control input connections (ILIM, etc.) to analog ground or V_{CC} rather than power ground or V_{DD}.
4) Mount the decoupling capacitor from V_{CC} to GND as close as possible to the IC with dedicated traces that are not shared with other signal paths.
5) The current-sense paths for LX1 and LX2 to GND must be made using Kelvin sense connections to guarantee the current-limit accuracy.
6) Ensure the feedback connections are short and direct. To the extent possible, IFB, VFB, and ISEC connections should be far away from the high-voltage traces and the transformer.
7) To the extent possible, high-voltage trace clearance on the transformer's secondary should be widely separated. The high-voltage traces should also be separated from adjacent ground planes to prevent lossy capacitive coupling.
8) The traces to the capacitive voltage-divider on the transformer's secondary need to be widely separated to prevent arcing. Moving these traces to opposite sides of the board can be beneficial in some cases.

Chip Information

TRANSISTOR COUNT: 2985

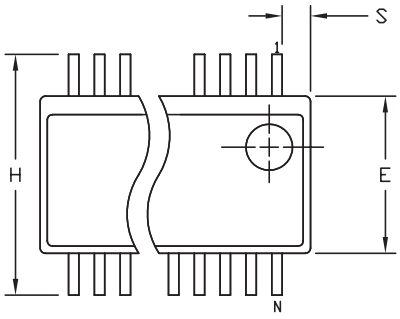
PROCESS: BiCMOS

Low-Cost CCFL Backlight Controller

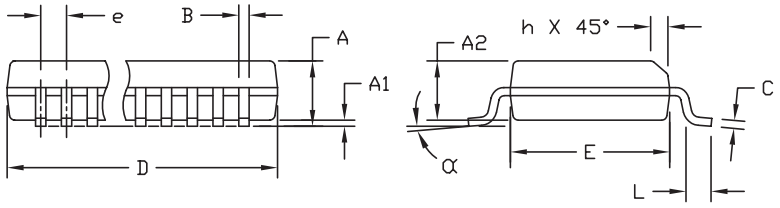
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QSOP.EPS



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.30
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
α	0°	8°	0°	8°



VARIATIONS:

	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.	N	
D	.189	.196	4.80	4.98	16	AB
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AD
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AE
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AF
S	.0250	.0300	0.635	0.762		

NOTES:
1). D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2). MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3). CONTROLLING DIMENSIONS: INCHES.
4). MEETS JEDEC MO137.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	E	1/1

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