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High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

General Description

The MAX8732A/MAX8733A/MAX8734A dual step-down, switch-mode power-supply (SMPS) controllers generate logic-supply voltages in battery-powered systems. The MAX8732A/MAX8733A/MAX8734A include two pulse-width modulation (PWM) controllers, adjustable from 2V to 5.5V or fixed at 5V and 3.3V. These devices feature two linear regulators providing 5V and 3.3V always-on outputs. Each linear regulator provides up to 100mA output current with automatic linear-regulator bootstrapping to the main SMPS outputs. The MAX8732A/MAX8733A/MAX8734A include on-board power-up sequencing, a power-good (PGOOD) output, digital soft-start, and internal soft-stop output discharge that prevents negative voltages on shutdown. Additionally, the outputs are high impedance when V_{CC} falls below its UVLO set point while the outputs are enabled.

Maxim's proprietary Quick-PWM™ quick-response, constant on-time PWM control scheme operates without sense resistors and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The unique ultrasonic pulse-skipping mode maintains the switching frequency above 25kHz, which eliminates noise in audio applications. Other features include pulse skipping, which maximizes efficiency in light-load applications, and fixed-frequency PWM mode, which reduces RF interference in sensitive applications.

The MAX8732A features a 200kHz/5V and 300kHz/3.3V SMPS for highest efficiency, while the MAX8733A features a 400kHz/5V and 500kHz/3.3V SMPS for "thin and light" applications. The MAX8734A provides a pin-selectable switching frequency, allowing either 200kHz/300kHz or 400kHz/500kHz operation of the 5V/3.3V SMPSs, respectively. The MAX8732A/MAX8733A/MAX8734A are available in 28-pin QSOP packages and operate over the extended temperature range (-40°C to +85°C).

The MAX8732A/MAX8733A/MAX8734A are pin-for-pin upgrades to the MAX1777/MAX1977/MAX1999. The MAX1999 evaluation kit (EV kit) can be used to evaluate the MAX8732A/MAX8733A/MAX8734A.

Applications

- Notebook and Subnotebook Computers
- PDA's and Mobile Communication Devices
- 3- and 4-Cell Li+ Battery-Powered Devices

Quick-PWM and Dual Mode are trademarks of Maxim Integrated Products, Inc.

Features

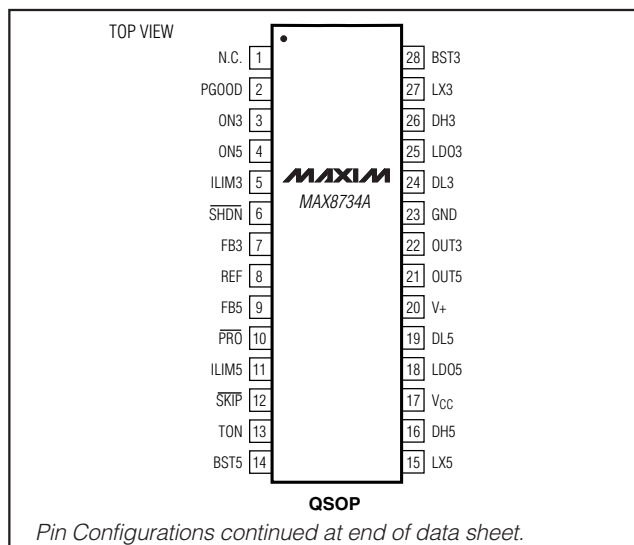
- ◆ No Current-Sense Resistor Needed (MAX8734A)
- ◆ Accurate Current Sense with Current-Sense Resistor (MAX8732A/MAX8733A)
- ◆ 1.5% Output Voltage Accuracy
- ◆ 3.3V and 5V 100mA Bootstrapped Linear Regulators
- ◆ Internal Soft-Start and Soft-Stop Output Discharge
- ◆ Quick-PWM with 100ns Load Step Response
- ◆ 3.3V and 5V Fixed or Adjustable Outputs (Dual Mode™)
- ◆ 4.5V to 24V Input Voltage Range
- ◆ Enhanced Ultrasonic Pulse-Skipping Mode (25kHz min)
- ◆ Power-Good (PGOOD) Signal
- ◆ Overvoltage Protection Enable/Disable

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	5V/3.3V SWITCHING FREQUENCY (kHz)
MAX8732AEEI+	-40°C to +85°C	28 QSOP	200/300
MAX8732AEEI	-40°C to +85°C	28 QSOP	200/300
MAX8733AEEI+	-40°C to +85°C	28 QSOP	400/500
MAX8733AEEI	-40°C to +85°C	28 QSOP	400/500

Ordering Information continued at end of data sheet.
+Denotes lead-free package.

Pin Configurations



MAX8732A/MAX8733A/MAX8734A



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ABSOLUTE MAXIMUM RATINGS

V+, $\overline{\text{SHDN}}$ to GND	-0.3V to +25V
BST_ to GND	-0.3V to +30V
LX_ to BST_	-6V to +0.3V
CS_ to GND (MAX8732A/MAX8733A only)	-2V to +6V
V _{CC} , LDO5, LDO3, OUT3, OUT5, ON3, ON5, REF, FB3, FB5, $\overline{\text{SKIP}}$, $\overline{\text{PRO}}$, PGOOD to GND	-0.3V to +6V
DH3 to LX3	-0.3V to (V _{BST3} + 0.3V)
DH5 to LX5	-0.3V to (V _{BST5} + 0.3V)
ILIM3, ILIM5 to GND	-0.3V to (V _{CC} + 0.3V)
DL3, DL5 to GND	-0.3V to (V _{LDO5} + 0.3V)
TON to GND (MAX8734A only)	-0.3V to +6V

LDO3, LDO5, REF Short Circuit to GND	Momentary
LDO3 Current (internal regulator) Continuous	+100mA
LDO3 Current (switched over to OUT3) Continuous	+200mA
LDO5 Current (internal regulator) Continuous	+100mA
LDO5 Current (switched over to OUT5) Continuous	+200mA
Continuous Power Dissipation (T _A = +70°C)	28-Pin QSOP (derate 10.8mW/°C above +70°C).....860mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, V₊ = 12V, ON3 = ON5 = V_{CC}, V $\overline{\text{SHDN}}$ = 5V, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
MAIN SMPS CONTROLLERS						
V ₊ Input Voltage Range	LDO5 in regulation	6		24	V	
	V ₊ = LDO5, V _{OUT5} < 4.43V	4.5		5.5		
3.3V Output Voltage in Fixed Mode	V ₊ = 6V to 24V, FB3 = GND, V $\overline{\text{SKIP}}$ = 5V	3.285	3.330	3.375	V	
5V Output Voltage in Fixed Mode	V ₊ = 6V to 24V, FB5 = GND, V $\overline{\text{SKIP}}$ = 5V, MAX8732A/MAX8734A (TON = V _{CC})	4.975	5.050	5.125	V	
	V ₊ = 7V to 24V, FB5 = GND, V $\overline{\text{SKIP}}$ = 5V, MAX8733A/MAX8734A (TON = GND)					
Output Voltage in Adjustable Mode	V ₊ = 6V to 24V, either SMPS	1.975	2.00	2.025	V	
Output Voltage Adjust Range	Either SMPS	2.0		5.5	V	
FB3, FB5 Adjustable-Mode Threshold Voltage	Dual-Mode comparator	0.1		0.2	V	
DC Load Regulation	Either SMPS, V $\overline{\text{SKIP}}$ = 5V, 0 to 5A		-0.1		%	
	Either SMPS, $\overline{\text{SKIP}}$ = GND, 0 to 5A		-1.5			
	Either SMPS, V $\overline{\text{SKIP}}$ = 2V, 0 to 5A		-1.7			
Line Regulation	Either SMPS, 6V < V ₊ < 24V		0.005		%/V	
Current-Limit Threshold (Positive, Default)	ILIM_ = V _{CC} , GND - CS_ (MAX8732A/MAX8733A), GND - LX_ (MAX8734A)	93	100	107	mV	
Current-Limit Threshold (Positive, Adjustable)	GND - CS_ (MAX8732A/MAX8733A), GND - LX_ (MAX8734A)	V _{ILIM_} = 0.5V	40	50	60	mV
		V _{ILIM_} = 1V	93	100	107	
		V _{ILIM_} = 2V	185	200	215	
Zero-Current Threshold	$\overline{\text{SKIP}}$ = GND, ILIM_ = V _{CC} , GND - CS_ (MAX8732A/MAX8733A), GND - LX_ (MAX8734A)		3		mV	
Current-Limit Threshold (Negative, Default)	$\overline{\text{SKIP}}$ = ILIM_ = V _{CC} , GND - CS_ (MAX8732A/MAX8733A), GND - LX_ (MAX8734A)		-120		mV	
Soft-Start Ramp Time	Zero to full limit		1.7		ms	

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

MAX8732A/MAX8733A/MAX8734A

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $V_{SHDN} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Frequency	MAX8732A or MAX8734A ($V_{TON} = 5V$), $\overline{SKIP} = V_{CC}$	5V SMPS	200		kHz	
		3.3V SMPS	300			
	MAX8733A or MAX8734A ($V_{TON} = 0$), $\overline{SKIP} = V_{CC}$	5V SMPS	400			
		3.3V SMPS	500			
	SKIP = REF	25	36			
On-Time Pulse Width	MAX8732A or MAX8734A ($V_{TON} = 5V$)	$V_{OUT5} = 5.05V$	1.895	2.105	2.315	μs
		$V_{OUT3} = 3.33V$	0.833	0.925	1.017	
	MAX8733A or MAX8734A ($V_{TON} = 0$)	$V_{OUT5} = 5.05V$	0.895	1.052	1.209	
		$V_{OUT3} = 3.33V$	0.475	0.555	0.635	
Minimum Off-Time		250	300	350	ns	
Maximum Duty Cycle	MAX8732A or MAX8734A ($V_{TON} = 5V$)	$V_{OUT5} = 5.05V$	94		%	
		$V_{OUT3} = 3.33V$	91			
	MAX8733A or MAX8734A ($V_{TON} = 0$)	$V_{OUT5} = 5.05V$	88			
		$V_{OUT3} = 3.33V$	85			
INTERNAL REGULATOR AND REFERENCE						
LDO5 Output Voltage	$ON3 = ON5 = GND$, $6V < V_+ < 24V$, $0 < I_{LDO5} < 100mA$	4.90	5.00	5.10	V	
LDO5 Short-Circuit Current	LDO5 = GND	190			mA	
LDO5 Undervoltage-Lockout Fault Threshold	Falling edge of LDO5, hysteresis = 1%	3.7	4.0	4.3	V	
LDO5 Bootstrap Switch Threshold	Falling edge of OUT5, rising edge at OUT5 regulation point	4.43	4.56	4.69	V	
LDO5 Bootstrap Switch Resistance	LDO5 to OUT5, $V_{OUT5} = 5V$		1.4	3.2	Ω	
LDO3 Output Voltage	$ON3 = ON5 = GND$, $6V < V_+ < 24V$, $0 < I_{LDO3} < 100mA$	3.28	3.35	3.42	V	
LDO3 Short-Circuit Current	LDO3 = GND	180			mA	
LDO3 Bootstrap Switch Threshold	Falling edge of OUT3, rising edge at OUT3 regulation point	2.80	2.91	3.02	V	
LDO3 Bootstrap Switch Resistance	LDO3 to OUT3, $V_{OUT3} = 3.2V$		1.5	3.5	Ω	
REF Output Voltage	No external load	1.980	2.000	2.020	V	
REF Load Regulation	$0 < I_{LOAD} < 50\mu A$			10	mV	
REF Sink Current	REF in regulation	10			μA	
V_+ Operating Supply Current	LDO5 switched over to OUT5, 5V SMPS		25	50	μA	
V_+ Standby Supply Current	$V_+ = 6V$ to $24V$, both SMPSs off, includes I_{SHDN}		150	250	μA	
V_+ Shutdown Supply Current	$V_+ = 4.5V$ to $24V$		6	15	μA	
Quiescent Power Consumption	Both SMPSs on, $FB3 = FB5 = \overline{SKIP} = GND$, $V_{OUT3} = 3.5V$, $V_{OUT5} = 5.3V$		3	4.5	mW	
FAULT DETECTION						
Overvoltage Trip Threshold	FB3 or FB5 with respect to nominal regulation point	+8	+11	+14	%	

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $V_{\overline{SHDN}} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Fault Propagation Delay	FB3 or FB5 delay with 50mV overdrive		10		μs
PGOOD Threshold	FB3 or FB5 with respect to nominal output, falling edge, typical hysteresis = 1%	-12	-9.5	-7	%
PGOOD Propagation Delay	Falling edge, 50mV overdrive		10		μs
PGOOD Output Low Voltage	$I_{SINK} = 4mA$			0.3	V
PGOOD Leakage Current	High state, forced to 5.5V			1	μA
Thermal-Shutdown Threshold			+160		$^\circ C$
Output Undervoltage Shutdown Threshold	FB3 or FB5 with respect to nominal output voltage	65	70	75	%
Output Undervoltage Shutdown Blanking Time	From ON_+ signal	10	22	35	ms
INPUTS AND OUTPUTS					
Feedback Input Leakage Current	$V_{FB3} = V_{FB5} = 2.2V$	-200	+40	+200	nA
\overline{PRO} Input Voltage	Low level			0.6	V
	High level	1.5			
\overline{SKIP} Input Voltage	Low level			0.8	V
	Float level	1.7		2.3	
	High level	2.4			
TON Input Voltage	Low level			0.8	V
	High level	2.4			
ON3, ON5 Input Voltage	Clear fault level/SMPS off level			0.8	V
	Delay start level	1.7		2.3	
	SMPS on level	2.4			
Input Leakage Current	$V_{\overline{PRO}}$ or $V_{TON} = 0$ or 5V	-1		+1	μA
	$V_{ON_+} = 0$ or 5V	-2		+2	
	$V_{\overline{SKIP}} = 0$ or 5V	-1		+1	
	$V_{\overline{SHDN}} = 0$ or 24V	-1		+1	
	$V_{CS_+} = 0$ or 5V	-2		+2	
	$V_{ILIM3}, V_{ILIM5} = 0$ or 2V	-0.2		+0.2	
\overline{SHDN} Input Trip Level	Rising edge	1.2	1.6	2.0	V
	Falling edge	0.96	1.00	1.04	
DH_ Gate-Driver Sink/Source Current	DH3, DH5 forced to 2V		2		A
DL_ Gate-Driver Source Current	DL3 (source), DL5 (source), forced to 2V		1.7		A
DL_ Gate-Driver Sink Current	DL3 (sink), DL5 (sink), forced to 2V		3.3		A
DH_ Gate-Driver On-Resistance	BST - LX_ forced to 5V		1.5	4.0	Ω
DL_ Gate-Driver On-Resistance	DL_, high state (pullup)		2.2	5.0	Ω
	DL_, low state (pulldown)		0.6	1.5	

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

MAX8732A/MAX8733A/MAX8734A

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $V_{SHDN} = 5V$, $T_A = 0^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUT3, OUT5 Discharge-Mode On-Resistance			12	40	Ω
OUT3, OUT5 Discharge-Mode Synchronous Rectifier Turn-On Level		0.2	0.3	0.4	V

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $V_{SHDN} = 5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS					
V+ Input Voltage Range	LDO5 in regulation	6		24	V
	$V_+ = LDO5$, $V_{OUT5} < 4.41V$	4.5		5.5	
3.3V Output Voltage in Fixed Mode	$V_+ = 6V$ to $24V$, $FB3 = GND$, $V_{SKIP} = 5V$	3.27		3.39	V
5V Output Voltage in Fixed Mode	$V_+ = 6V$ to $24V$, $FB5 = GND$, $V_{SKIP} = 5V$, MAX8732A/MAX8734A ($T_{ON} = V_{CC}$)	4.95		5.15	V
	$V_+ = 7V$ to $24V$, $FB5 = GND$, $V_{SKIP} = 5V$, MAX8733A/MAX8734A ($T_{ON} = GND$)				
Output Voltage in Adjustable Mode	$V_+ = 6V$ to $24V$, either SMPS	1.97		2.03	V
Output Voltage Adjust Range	Either SMPS	2.0		5.5	V
FB3, FB5 Adjustable-Mode Threshold Voltage	Dual-Mode comparator	0.1		0.2	V
Current-Limit Threshold (Positive, Default)	$ILIM_- = V_{CC}$, $GND - CS_-$ (MAX8732A/MAX8733A), $GND - LX_-$ (MAX8734A)	90		110	mV
Current-Limit Threshold (Positive, Adjustable)	$GND - CS_-$ (MAX8732A/MAX8733A), $GND - LX_-$ (MAX8734A)	$V_{ILIM_-} = 0.5V$	40	60	mV
		$V_{ILIM_-} = 1V$	90	110	
		$V_{ILIM_-} = 2V$	180	220	
On-Time Pulse Width	MAX8732A or MAX8734A ($V_{TON} = 5V$)	$V_{OUT5} = 5.05V$	1.895	2.315	μs
		$V_{OUT3} = 3.33V$	0.833	1.017	
	MAX8733A or MAX8734A ($V_{TON} = 0$)	$V_{OUT5} = 5.05V$	0.895	1.209	
		$V_{OUT3} = 3.33V$	0.475	0.635	
Minimum Off-Time		200		400	ns
INTERNAL REGULATOR AND REFERENCE					
LDO5 Output Voltage	$ON3 = ON5 = GND$, $6V < V_+ < 24V$, $0 < I_{LDO5} < 100mA$	4.90		5.10	V
LDO5 Undervoltage-Lockout Fault Threshold	Falling edge of LDO5, hysteresis = 1%	3.7		4.3	V

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12.0\text{V}$, $ON3 = ON5 = V_{CC}$, $V_{\overline{SHDN}} = 5\text{V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LDO5 Bootstrap Switch Threshold	Falling edge of OUT5, rising edge at OUT5 regulation point	4.43		4.69	V
LDO5 Bootstrap Switch Resistance	LDO5 to OUT5, $V_{OUT5} = 5\text{V}$			3.2	Ω
LDO3 Output Voltage	$ON3 = ON5 = \text{GND}$, $6\text{V} < V_+ < 24\text{V}$, $0 < I_{LDO3} < 100\text{mA}$	3.27		3.43	V
LDO3 Bootstrap Switch Threshold	Falling edge of OUT3, rising edge at OUT3 regulation point	2.80		3.02	V
LDO3 Bootstrap Switch Resistance	LDO3 to OUT3, $V_{OUT3} = 3.2\text{V}$			3.5	Ω
REF Output Voltage	No external load	1.975		2.025	V
REF Load Regulation	$0 < I_{LOAD} < 50\mu\text{A}$			10	mV
REF Sink Current	REF in regulation	10			μA
V_+ Operating Supply Current	LDO5 switched over to OUT5, 5V SMPS			50	μA
V_+ Standby Supply Current	$V_+ = 6\text{V}$ to 24V , both SMPSs off, includes $I_{\overline{SHDN}}$			300	μA
V_+ Shutdown Supply Current	$V_+ = 4.5\text{V}$ to 24V			15	μA
Quiescent Power Consumption	Both SMPSs on, $FB3 = FB5 = \overline{\text{SKIP}} = \text{GND}$, $V_{OUT3} = 3.5\text{V}$, $V_{OUT5} = 5.3\text{V}$			4.5	mW
FAULT DETECTION					
Overvoltage Trip Threshold	FB3 or FB5 with respect to nominal regulation point	+8		+14	%
PGOOD Threshold	FB3 or FB5 with respect to nominal output, falling edge, typical hysteresis = 1%	-12		-7	%
PGOOD Output Low Voltage	$I_{\text{SINK}} = 4\text{mA}$			0.3	V
PGOOD Leakage Current	High state, forced to 5.5V			1	μA
Output Undervoltage Shutdown Threshold	FB3 or FB5 with respect to nominal output voltage	65		75	%
Output Undervoltage Shutdown Blanking Time	From ON_+ signal	10		40	ms
INPUTS AND OUTPUTS					
Feedback Input Leakage Current	$V_{FB3} = V_{FB5} = 2.2\text{V}$	-200		+200	nA
$\overline{\text{PRO}}$ Input Voltage	Low level			0.6	V
	High level	1.5			
$\overline{\text{SKIP}}$ Input Voltage	Low level			0.8	V
	Float level	1.7		2.3	
	High level	2.4			
TON Input Voltage	Low level			0.8	V
	High level	2.4			

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12.0V$, $ON3 = ON5 = V_{CC}$, $V_{\overline{SHDN}} = 5V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ON3, ON5 Input Voltage	Clear fault level/SMPS off level			0.8	V
	Delay start level	1.7		2.3	
	SMPS on level	2.4			
Input Leakage Current	$V_{\overline{PRO}}$ or $V_{TON} = 0$ or $5V$	-1		+1	μA
	$V_{ON_} = 0$ or $5V$	-1		+1	
	$V_{\overline{SKIP}} = 0$ or $5V$	-2		+2	
	$V_{\overline{SHDN}} = 0$ or $24V$	-1		+1	
	$V_{CS_} = 0$ or $5V$	-2		+2	
	$V_{ILIM3}, V_{ILIM5} = 0$ or $2V$	-0.2		+0.2	
\overline{SHDN} Input Trip Level	Rising edge	1.2		2.0	V
	Falling edge	0.96		1.04	
DH_ Gate-Driver On-Resistance	BST - LX_ forced to 5V			4.0	Ω
DL_ Gate-Driver On-Resistance	DL_, high state (pullup)			5.0	Ω
	DL_, low state (pulldown)			1.5	
OUT3, OUT5 Discharge-Mode On-Resistance				40	Ω
OUT3, OUT5 Discharge-Mode Synchronous Rectifier Turn-On Level		0.2		0.4	V

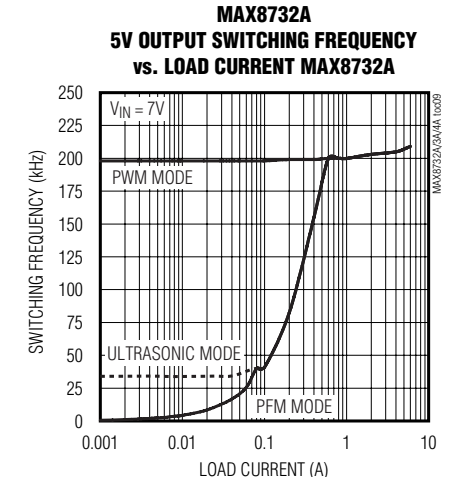
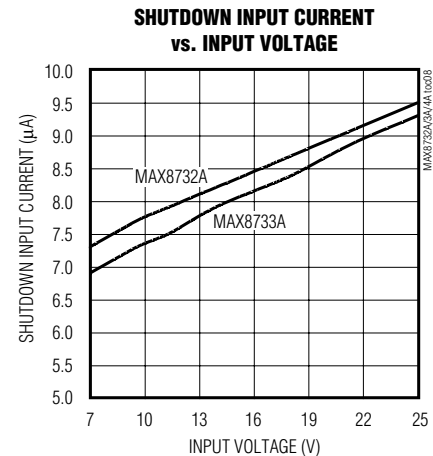
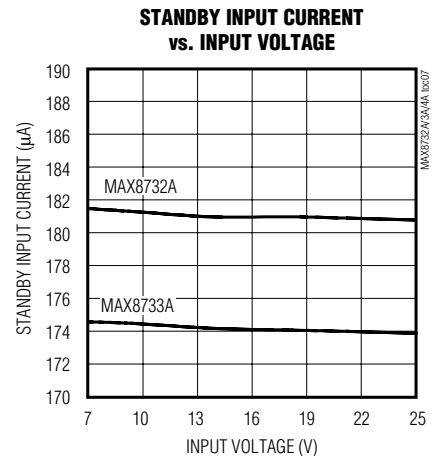
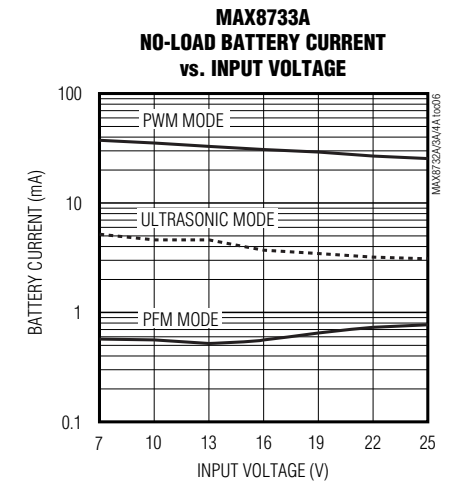
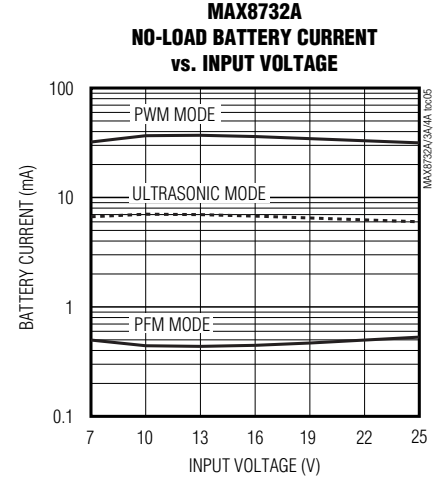
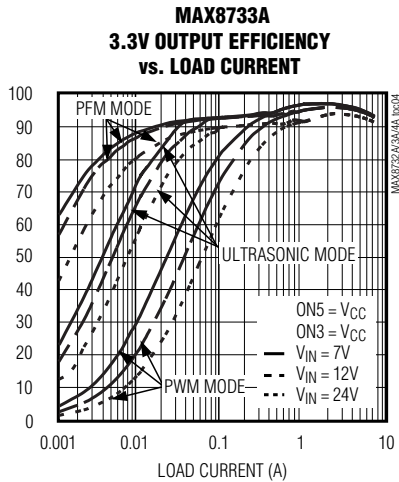
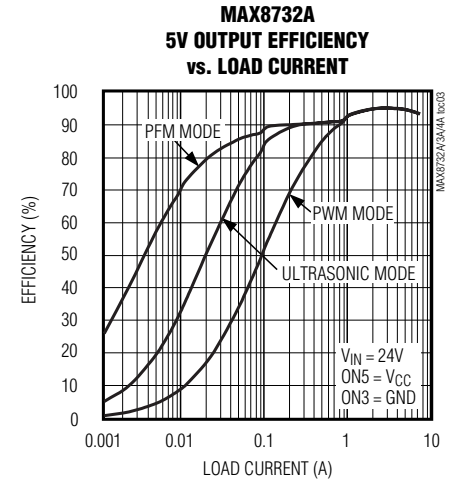
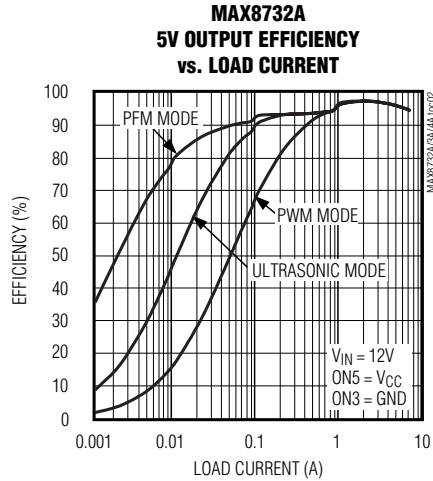
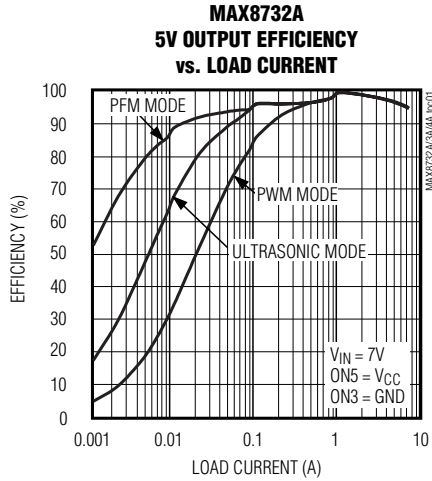
Note 1: Specifications to $-40^\circ C$ are guaranteed by design, not production tested.

MAX8732A/MAX8733A/MAX8734A

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $\overline{SHDN} = V_+$, $R_{CS} = 7m\Omega$, $V_{ILIM-} = 0.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

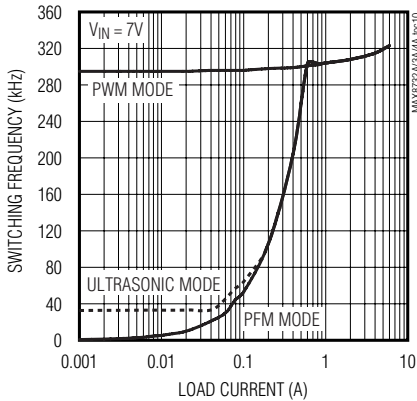


High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

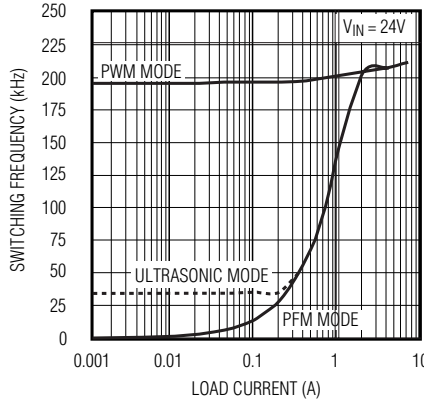
Typical Operating Characteristics (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $SHDN = V_+$, $R_{CS} = 7m\Omega$, $V_{LIML} = 0.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

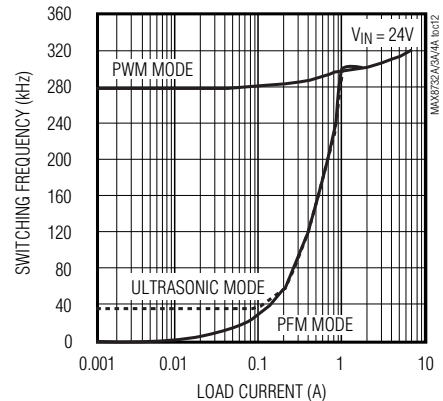
MAX8732A
3.3V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT (MAX8732A)



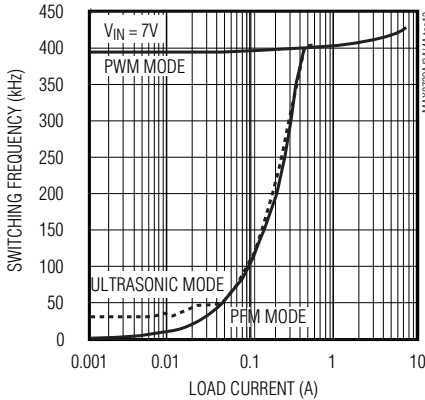
MAX8732A
5V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT



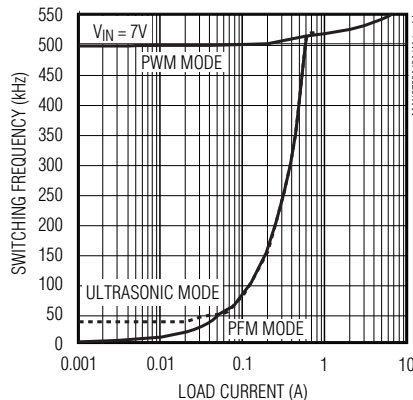
MAX8732A
3.3V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT



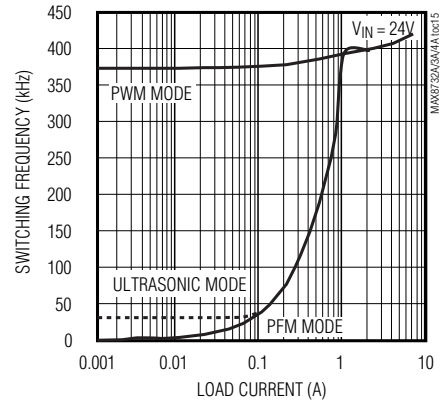
MAX8733A
5V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT



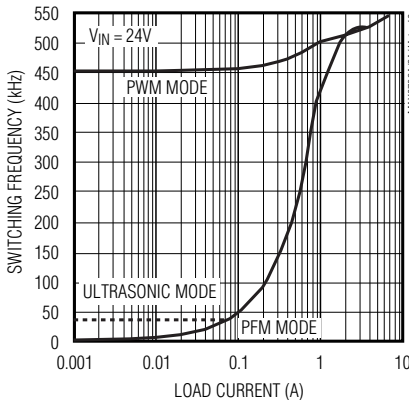
MAX8733A
3.3V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT



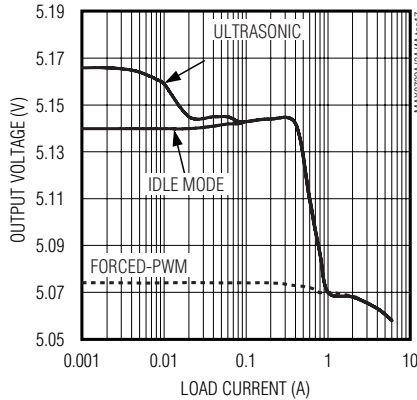
MAX8733A
5V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT



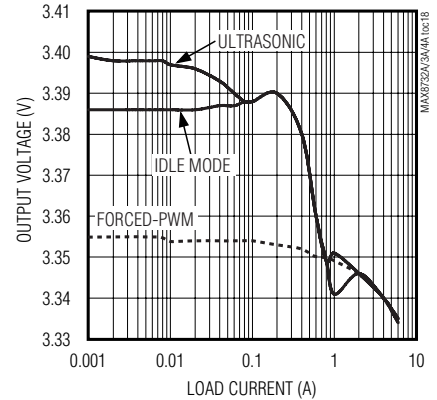
MAX8733A
3.3V OUTPUT SWITCHING
FREQUENCY vs. LOAD CURRENT



MAX8732A
OUT5 VOLTAGE REGULATION
vs. LOAD CURRENT



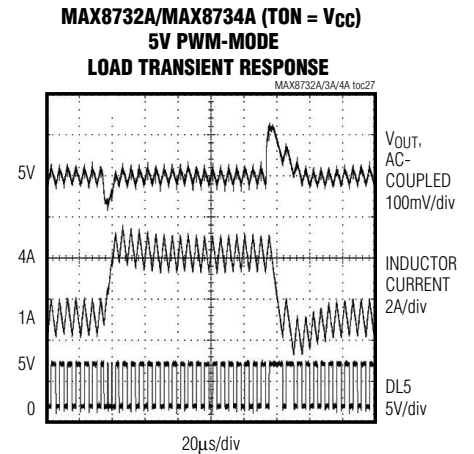
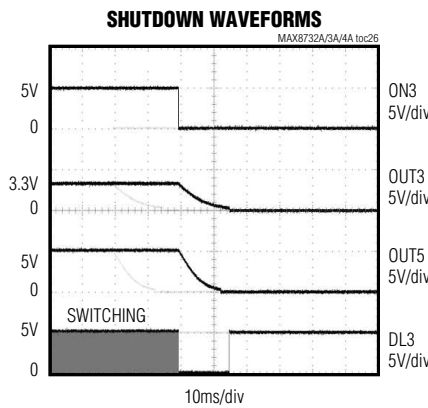
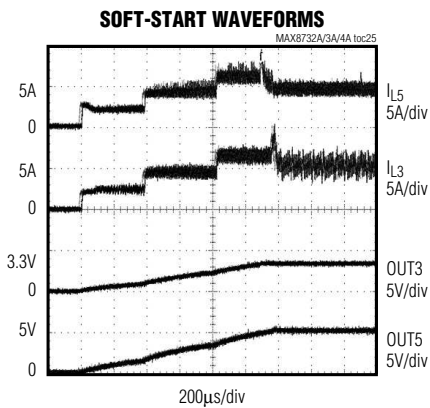
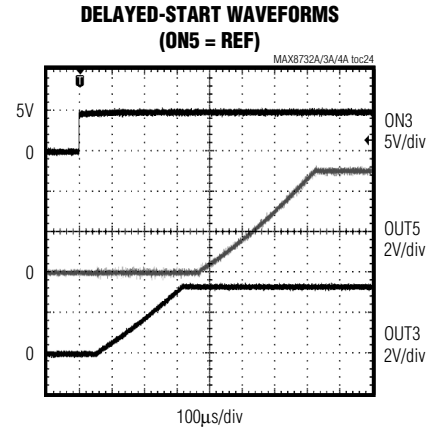
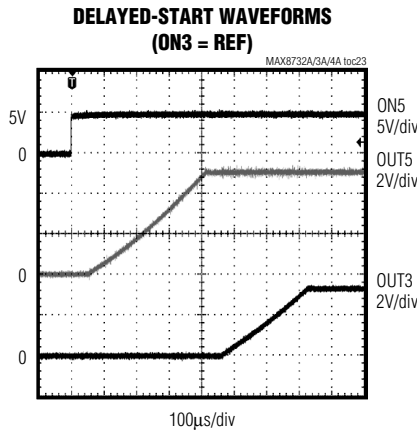
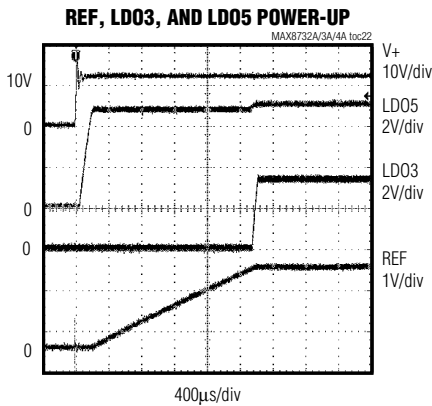
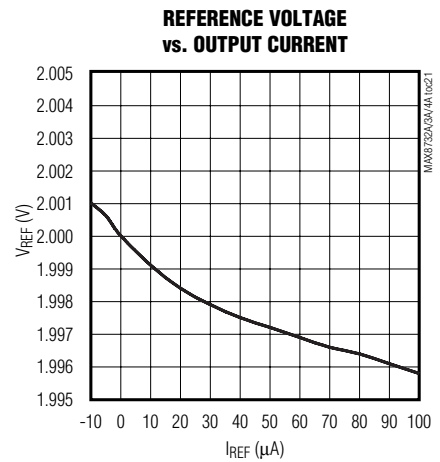
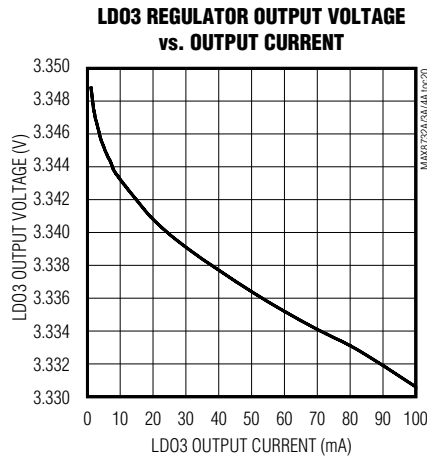
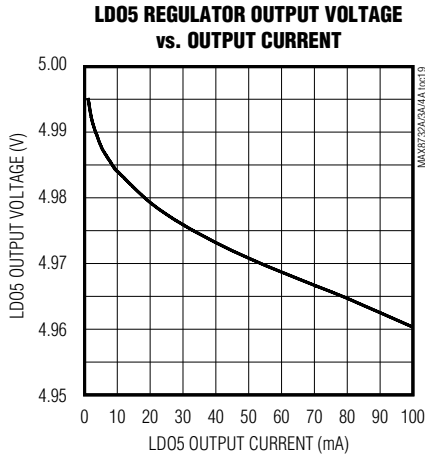
MAX8732A
OUT3 VOLTAGE REGULATION
vs. LOAD CURRENT



High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $\overline{SHDN} = V_+$, $R_{CS} = 7m\Omega$, $V_{LIM_} = 0.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

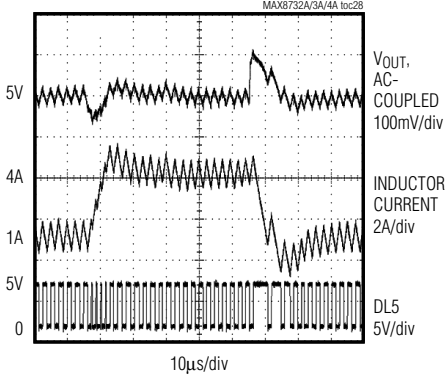


High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

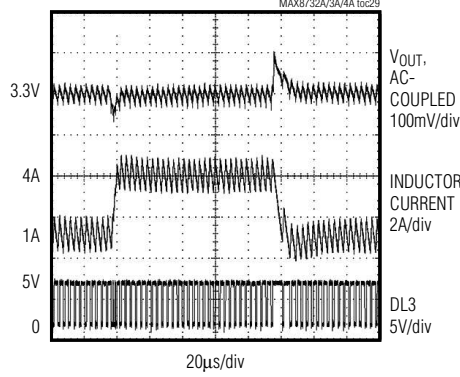
Typical Operating Characteristics (continued)

(Circuit of Figure 1 and Figure 2, no load on LDO5, LDO3, OUT3, OUT5, and REF, $V_+ = 12V$, $ON3 = ON5 = V_{CC}$, $\overline{SHDN} = V_+$, $R_{CS} = 7m\Omega$, $V_{LIM_} = 0.5V$, $T_A = +25^\circ C$, unless otherwise noted.)

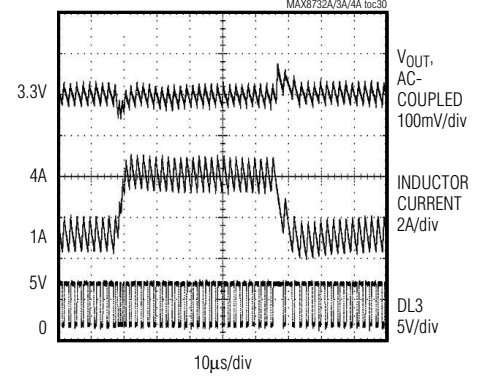
**MAX8733A/MAX8734A (TON = GND)
5V PWM-MODE
LOAD TRANSIENT RESPONSE**



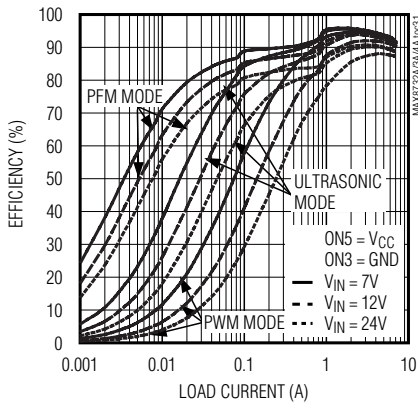
**MAX8732A/MAX8734A (TON = Vcc)
3.3V PWM-MODE
LOAD TRANSIENT RESPONSE**



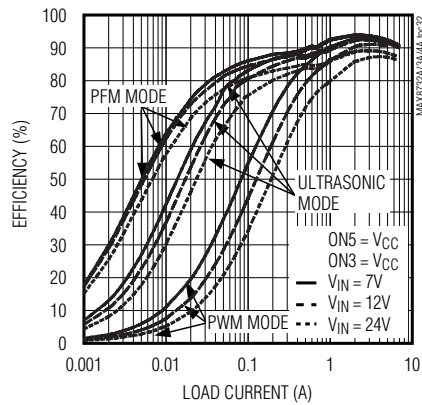
**MAX8733A/MAX8734A (TON = GND)
3.3V PWM-MODE
LOAD TRANSIENT RESPONSE**



**MAX8733A
5V OUTPUT EFFICIENCY
vs. LOAD CURRENT**



**MAX8733A
3.3V OUTPUT EFFICIENCY
vs. LOAD CURRENT**



MAX8732A/MAX8733A/MAX8734A

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Pin Description

MAX8732A/MAX8733A/MAX8734A

PIN		NAME	FUNCTION
MAX8732A MAX8733A	MAX8734A		
1	—	CS3	3.3V SMPS Current-Sense Input. Connect CS3 to a current-sensing resistor from the source of the synchronous rectifier to GND. The voltage at ILIM3 determines the current-limit threshold (see the <i>Current-Limit Circuit (ILIM_)</i> section).
—	1	N.C.	No Connection. Not internally connected.
2	2	PGOOD	Power-Good Output. PGOOD is an open-drain output that is pulled low if either output is disabled or is more than 10% below its nominal value.
3	3	ON3	3.3V SMPS Enable Input. The 3.3V SMPS is enabled if ON3 is greater than the SMPS on level and disabled if ON3 is less than the SMPS off level. If ON3 is connected to REF, the 3.3V SMPS starts after the 5V SMPS reaches regulation (delay start). Drive ON3 below the clear fault level to reset the fault latches.
4	4	ON5	5V SMPS Enable Input. The 5V SMPS is enabled if ON5 is greater than the SMPS on level and disabled if ON5 is less than the SMPS off level. If ON5 is connected to REF, the 5V SMPS starts after the 3.3V SMPS reaches regulation (delay start). Drive ON5 below the clear fault level to reset the fault latches.
5	5	ILIM3	3.3V SMPS Current-Limit Adjustment. The GND-LX current-limit threshold defaults to 100mV if ILIM3 is connected to V _{CC} . In adjustable mode, the current-limit threshold is 1/10 the voltage seen at ILIM3 over a 0.5V to 3V range. The logic threshold for switchover to the 100mV default value is approximately V _{CC} - 1V. Connect ILIM3 to REF for a fixed 200mV threshold.
6	6	$\overline{\text{SHDN}}$	Shutdown Control Input. The device enters its 6 μ A supply current shutdown mode if V _{SHDN} is less than the $\overline{\text{SHDN}}$ input falling-edge trip level and does not restart until V _{SHDN} is greater than the $\overline{\text{SHDN}}$ input rising-edge trip level. Connect $\overline{\text{SHDN}}$ to V+ for automatic startup. $\overline{\text{SHDN}}$ can be connected to V+ through a resistive voltage-divider to implement a programmable undervoltage lockout.
7	7	FB3	3.3V SMPS Feedback Input. Connect FB3 to GND for fixed 3.3V operation. Connect FB3 to a resistive voltage-divider from OUT3 to GND to adjust the output from 2V to 5.5V.
8	8	REF	2V Reference Output. Bypass to GND with a 0.22 μ F (min) capacitor. REF can source up to 100 μ A for external loads. Loading REF degrades FB __ and output accuracy according to the REF load-regulation error.
9	9	FB5	5V SMPS Feedback Input. Connect FB5 to GND for fixed 5V operation. Connect FB5 to a resistive voltage-divider from OUT5 to GND to adjust the output from 2V to 5.5V.
10	10	$\overline{\text{PRO}}$	Overvoltage and Undervoltage Fault Protection Enable/Disable. Connect $\overline{\text{PRO}}$ to V _{CC} to disable undervoltage, overvoltage protection, and discharge mode (DL = low in shutdown). Connect $\overline{\text{PRO}}$ to GND to enable undervoltage and overvoltage protection (see the <i>Fault Protection</i> section), and output discharge mode.
11	11	ILIM5	5V SMPS Current-Limit Adjustment. The GND-LX current-limit threshold defaults to 100mV if ILIM5 is connected to V _{CC} . In adjustable mode, the current-limit threshold is 1/10 the voltage seen at ILIM5 over a 0.5V to 3V range. The logic threshold for switchover to the 100mV default value is approximately V _{CC} - 1V. Connect ILIM5 to REF for a fixed 200mV threshold.
12	12	$\overline{\text{SKIP}}$	Low-Noise Mode Control. Connect $\overline{\text{SKIP}}$ to GND for normal Idle-Mode (pulse-skipping) operation or to V _{CC} for PWM mode (fixed frequency). Connect to REF or leave floating for ultrasonic mode (pulse skipping, 25kHz min).

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Pin Description (continued)

PIN		NAME	FUNCTION
MAX8732A MAX8733A	MAX8734A		
13	—	CS5	5V SMPS Current-Sense Input. Connect CS5 to a current-sensing resistor from the source of the synchronous rectifier to GND. The voltage at ILIM5 determines the current-limit threshold (see the <i>Current-Limit Circuit (ILIM_)</i> section).
—	13	TON	Frequency Select Input. Connect to V _{CC} for 200kHz/300kHz operation and to GND for 400kHz/500kHz operation (5V/3.3V SMPS switching frequencies, respectively).
14	14	BST5	Boost Flying Capacitor Connection for 5V SMPS. Connect to an external capacitor and diode according to the typical application circuits (Figure 1 and Figure 2). See the <i>MOSFET Gate Drivers (DH_, DL_)</i> section.
15	15	LX5	Inductor Connection for 5V SMPS. LX5 is the internal lower supply rail for the DH5 high-side gate driver. LX5 is the current-sense input for the 5V SMPS (MAX8734A only).
16	16	DH5	High-Side MOSFET Floating Gate-Driver Output for 5V SMPS. DH5 swings from LX5 to BST5.
17	17	V _{CC}	Analog Supply Voltage Input for PWM Core. Connect V _{CC} to the system supply voltage with a series 50Ω resistor. Bypass to GND with a 1μF ceramic capacitor.
18	18	LDO5	5V Linear-Regulator Output. LDO5 is the gate-driver supply for the external MOSFETs. LDO5 can provide a total of 100mA, including MOSFET gate-drive requirements and external loads. The internal load depends on the choice of MOSFET and switching frequency (see the <i>Reference and Linear Regulators (REF, LDO5, and LDO3)</i> section). If OUT5 is greater than the LDO5 bootstrap switch threshold, the LDO5 regulator shuts down and the LDO5 pin connects to OUT5 through a 1.4Ω switch. Bypass LDO5 with a minimum of 4.7μF. Use an additional 1μF per 5mA of load.
19	19	DL5	5V SMPS Synchronous Rectifier Gate-Drive Output. DL5 swings between GND and LDO5.
20	20	V+	Power-Supply Input. V+ powers the LDO5/LDO3 linear regulators and is also used for the Quick-PWM on-time, one-shot circuits. Connect V+ to the battery input and bypass with a 0.1μF capacitor.
21	21	OUT5	5V SMPS Output Voltage-Sense Input. Connect to the 5V SMPS output. OUT5 is an input to the Quick-PWM on-time, one-shot circuit. It also serves as the 5V feedback input in fixed-voltage mode. If OUT5 is greater than the LDO5 bootstrap-switch threshold, the LDO5 linear regulator shuts down and LDO5 connects to OUT5 through a 1.4Ω switch.
22	22	OUT3	3.3V SMPS Output Voltage-Sense Input. Connect to the 3.3V SMPS output. OUT3 is an input to the Quick-PWM on-time, one-shot circuit. It also serves as the 3V feedback input in fixed-voltage mode. If OUT3 is greater than the LDO3 bootstrap-switch threshold, the LDO3 linear regulator shuts down and LDO3 connects to OUT3 through a 1.5Ω switch.
23	23	GND	Analog and Power Ground
24	24	DL3	3.3V SMPS Synchronous-Rectifier Gate-Drive Output. DL3 swings between GND and LDO5.
25	25	LDO3	3.3V Linear-Regulator Output. LDO3 powers up after REF is in regulation. LDO3 can provide a total of 100mA to external loads. If OUT3 is greater than the LDO3 bootstrap-switch threshold, the LDO3 regulator shuts down and the LDO3 pin connects to OUT3 through a 1.5Ω switch. Bypass LDO3 with a minimum of 4.7μF. Use an additional 1μF per 5mA of load.
26	26	DH3	High-Side MOSFET Floating Gate-Driver Output for 3.3V SMPS. DH3 swings from LX3 to BST3.
27	27	LX3	Inductor Connection for 3.3V SMPS. LX3 is the current-sense input for the 3.3V SMPS (MAX8734A only).
28	28	BST3	Boost Flying Capacitor Connection for 3.3V SMPS. Connect to an external capacitor and diode according to the typical application circuits (Figure 1 and Figure 2). See the <i>MOSFET Gate Drivers (DH_, DL_)</i> section.

MAX8732A/MAX8733A/MAX8734A

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Typical Application Circuits

The typical application circuits (Figures 1 and 2) generate the 5V/5A and 3.3V/5A main supplies in a notebook computer. The input supply range is 7V to 24V. Table 1 lists component suppliers.

Detailed Description

The MAX8732A/MAX8733A/MAX8734A dual-buck, BiCMOS, switch-mode power-supply controllers generate logic supply voltages for notebook computers. The MAX8732A/MAX8733A/MAX8734A are designed primarily for battery-powered applications where high efficiency and low-quiescent supply current are critical. The MAX8732A is optimized for highest efficiency with a 5V/200kHz SMPS and a 3.3V/300kHz SMPS, while the

Table 1. Component Suppliers

MANUFACTURER	PHONE	FAX
Central Semiconductor	516-435-1110	516-435-1824
Dale-Vishay	402-564-3131	402-563-6418
Fairchild	408-721-2181	408-721-1635
International Rectifier	310-322-3331	310-322-3332
NIEC (Nihon)	805-843-7500	847-843-2798
Sanyo	619-661-6835	619-661-1055
Sprague	603-224-1961	603-224-1430
Sumida	847-956-0666	847-956-0702
Taiyo Yuden	408-573-4150	408-573-4159
TDK	847-390-4461	847-390-4405

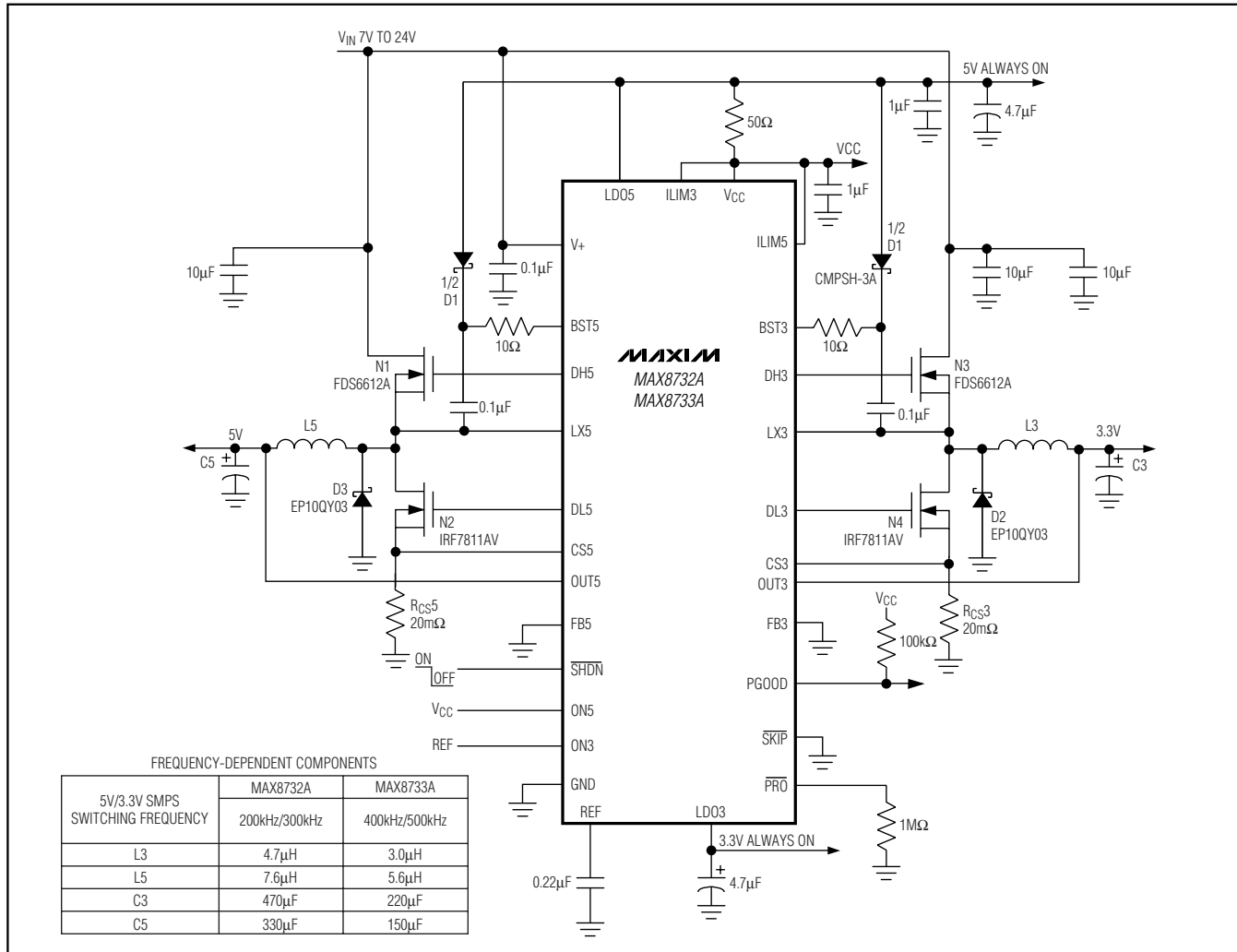
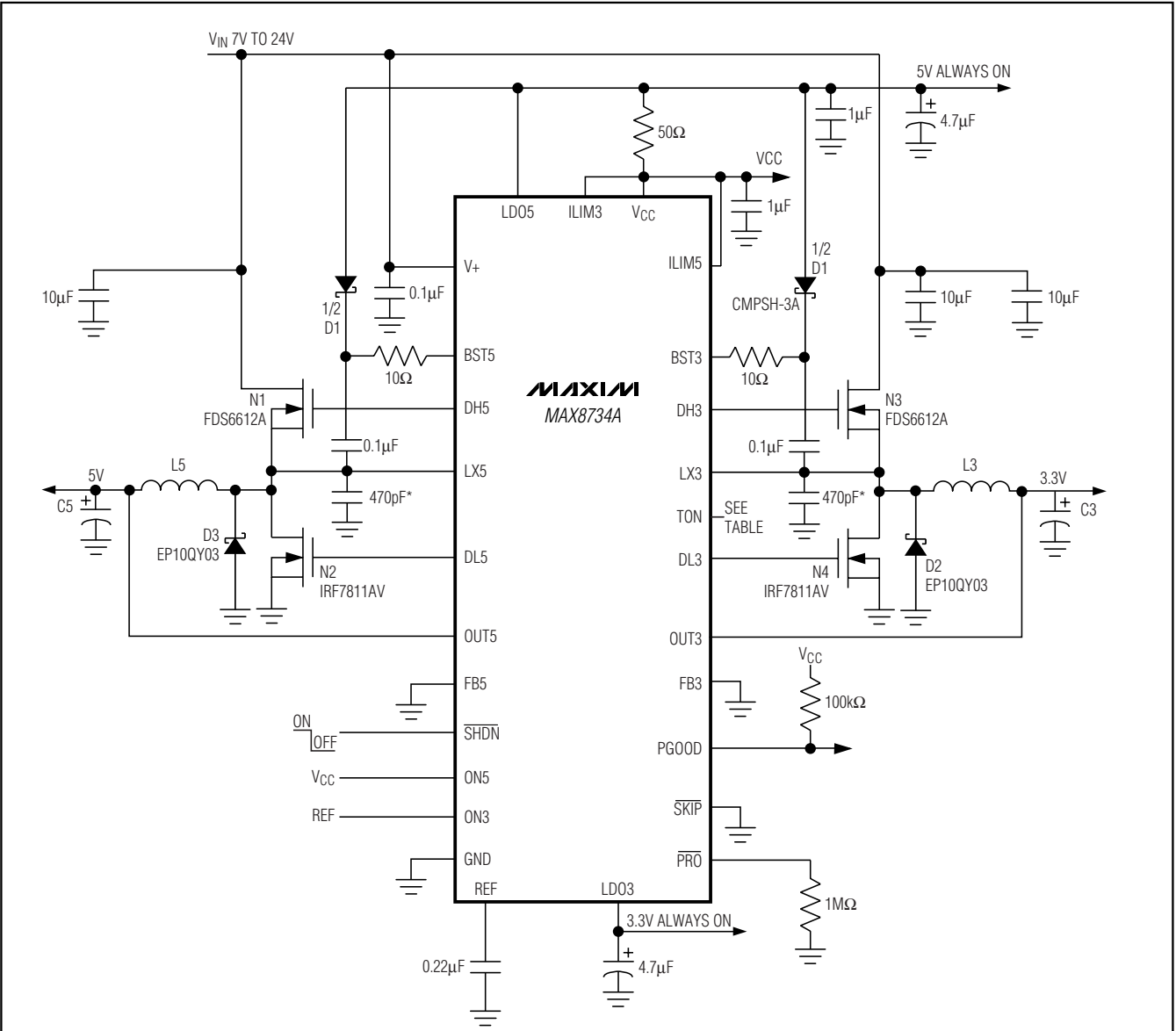


Figure 1. MAX8732A/MAX8733A Typical Application Circuit

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

MAX8732A/MAX8733A/MAX8734A



*OPTIONAL CAPACITANCE BETWEEN LX AND PGND (CLOSE TO THE IC) ONLY REQUIRED FOR ULTRASONIC MODE

FREQUENCY-DEPENDENT COMPONENTS

5V/3.3V SMPS SWITCHING FREQUENCY	TON = VCC	TON = GND
	200kHz/300kHz	400kHz/500kHz
L3	4.7μH	3.0μH
L5	7.6μH	5.6μH
C3	470μF	220μF
C5	330μF	150μF

Figure 2. MAX8734A Typical Application Circuit

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

MAX8733A is optimized for “thin and light” applications with a 5V/400kHz SMPS and a 3.3V/500kHz SMPS. The MAX8734A provides a pin-selectable switching frequency, allowing either 200kHz/300kHz or 400kHz/500kHz operation of the 5V/3.3V SMPSs, respectively.

Light-load efficiency is enhanced by automatic Idle-Mode operation, a variable-frequency pulse-skipping mode that reduces transition and gate-charge losses.

Each step-down, the power-switching circuit consists of two n-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the n-channel, high-side MOSFET must exceed the battery voltage, and is provided by a flying-capacitor boost circuit that uses a 100nF capacitor connected to BST_.

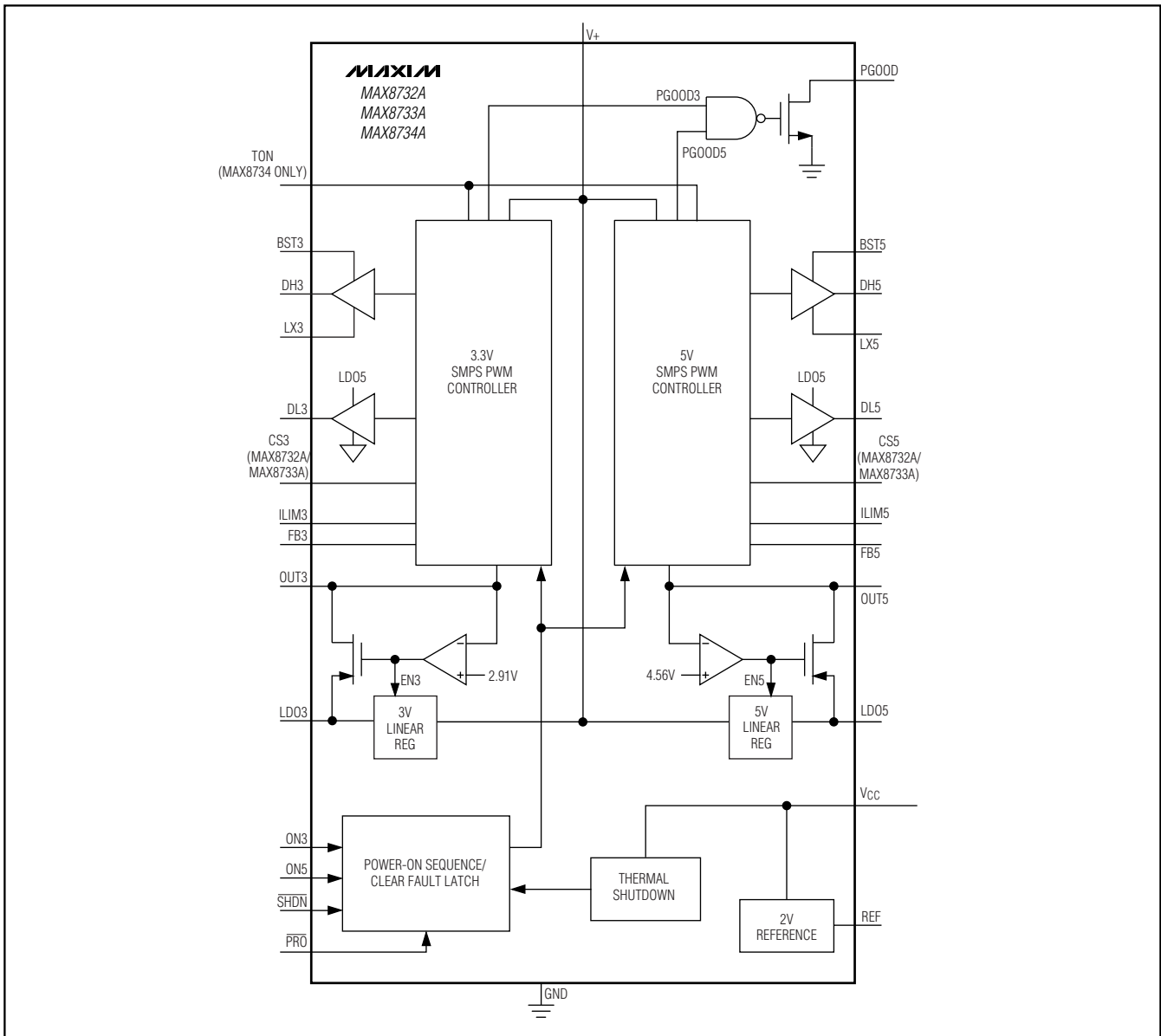


Figure 3. Detailed Functional Diagram

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Each PWM controller consists of a Dual-Mode feedback network and multiplexer, a multi-input PWM comparator, high-side and low-side gate drivers, and logic. The MAX8732A/MAX8733A/MAX8734A contain fault-protection circuits that monitor the main PWM outputs for undervoltage and overvoltage conditions. A power-on sequence

block controls the power-up timing of the main PWMs and monitors the outputs for undervoltage faults. The MAX8732A/MAX8733A/MAX8734A include 5V and 3.3V linear regulators. Bias generator blocks include the 5V (LDO5) linear regulator, 2V precision reference, and automatic bootstrap switchover circuit.

MAX8732A/MAX8733A/MAX8734A

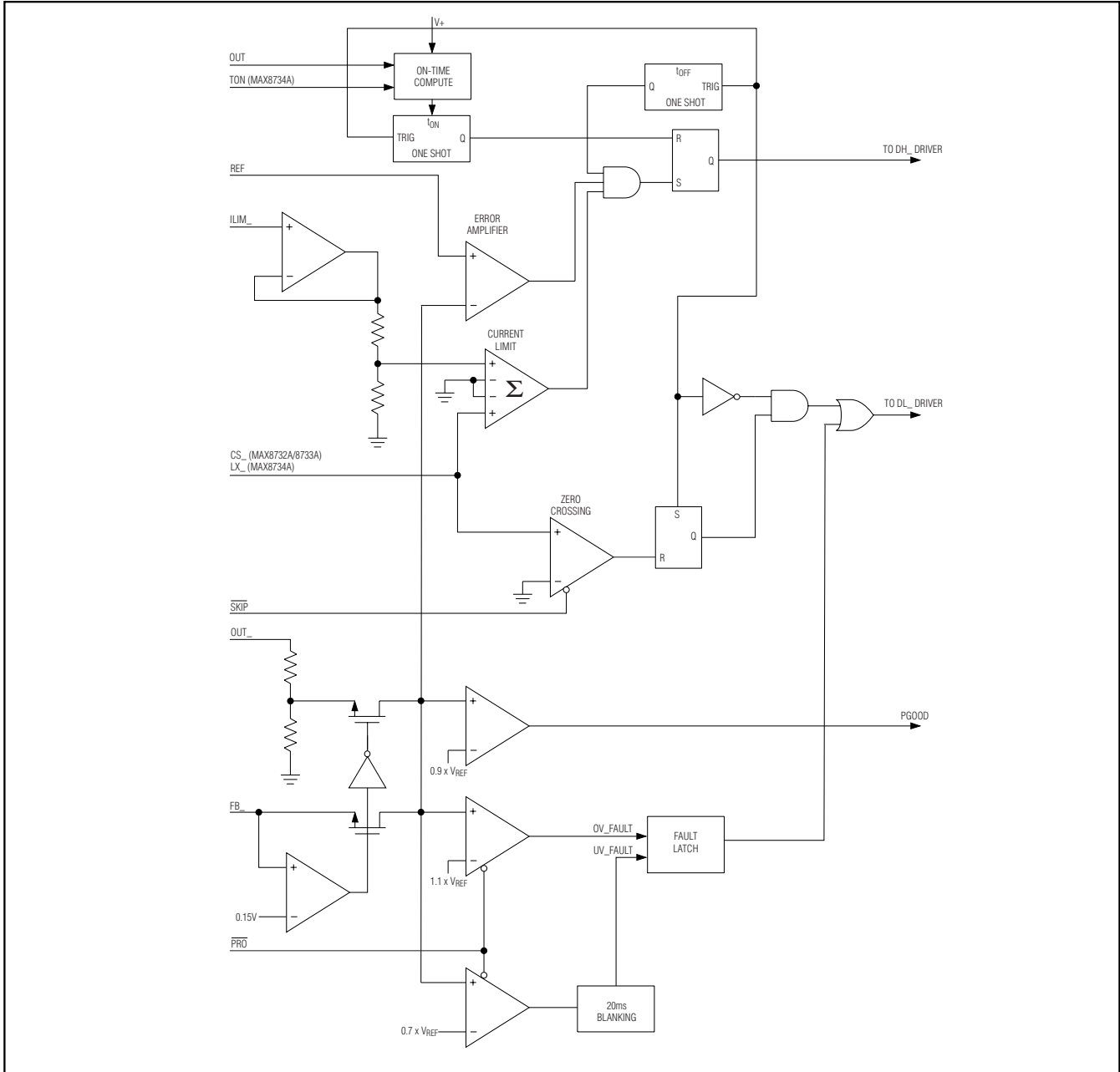


Figure 4. PWM Controller (One Side Only)

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

These internal blocks are not powered directly from the battery. Instead, the 5V (LDO5) linear regulator steps down the battery voltage to supply both internal circuitry and the gate drivers. The synchronous-switch gate drivers are directly powered from LDO5, while the high-side switch gate drivers are indirectly powered from LDO5 through an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the 5V linear regulator and powers the device from OUT5 when OUT5 is above 4.56V.

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode type with voltage feed-forward. The Quick-PWM control architecture relies on the output ripple voltage to provide the PWM ramp signal; thus, the output filter capacitor's ESR acts as a current-feedback resistor. The high-side switch on-time is determined by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (300ns typ). The on-time, one-shot triggers when the following conditions are met: the error comparator is low, the synchronous rectifier current is below the current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time, One-Shot (t_{ON})

Each PWM core includes a one-shot that sets the high-side switch on-time for each controller. Each fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as measured by the V+ input, and proportional to the output voltage. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefit of a constant switching frequency is the frequency can be selected to avoid noise-sensitive frequency regions:

$$t_{ON} = \frac{K(V_{OUT} + 0.075V)}{V+}$$

Table 2. Approximate K-Factor Errors

SMPS	SWITCHING FREQUENCY (kHz)	K-FACTOR (μ s)	APPROXIMATE K-FACTOR ERROR (%)
MAX8732A/MAX8734A ($t_{ON} = V_{CC}$), 5V	200	5.0	± 10
MAX8732A/MAX8734A ($t_{ON} = V_{CC}$), 3.3V	300	3.3	± 10
MAX8733A/MAX8734A ($t_{ON} = GND$), 5V	400	2.5	± 10
MAX8733A/MAX8734A ($t_{ON} = GND$), 3.3V	500	2.0	± 10

See Table 2 for approximate K-factors. The constant 0.075V is an approximation to account for the expected drop across the synchronous-rectifier switch. Switching frequency increases as a function of load current due to the increasing drop across the synchronous rectifier, which causes a faster inductor-current discharge ramp.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by switching delays in the external high-side power MOSFET. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only in PWM mode ($\overline{SKIP} = V_{CC}$) and during dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time.

For loads above the critical conduction point, the actual switching frequency is:

$$f = \frac{V_{OUT} + V_{DROP1}}{t_{ON}(V+ + V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{DROP2} is the sum of the parasitic voltage drops in the charging path, including high-side switch, inductor, and PC board resistances, and t_{ON} is the on-time calculated by the MAX8732A/MAX8733A/MAX8734A.

Automatic Pulse-Skipping Switchover (Idle Mode)

In Idle Mode ($\overline{SKIP} = GND$), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between con-

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

tinuous and discontinuous inductor-current operation (also known as the critical conduction point):

$$I_{LOAD(SKIP)} = \frac{K \times V_{OUT-}}{2 \times L} \left(\frac{V_+ - V_{OUT-}}{V_+} \right)$$

where K is the on-time scale factor (see the *On-Time One-Shot (t_{ON})* section). The load-current level at which PFM/PWM crossover occurs, I_{LOAD(SKIP)}, is equal to 1/2 the peak-to-peak ripple current, which is a function of the inductor value (Figure 5). For example, in the MAX8732A *Typical Application Circuit* with V_{OUT2} = 5V, V₊ = 12V, L = 7.6μH, and K = 5μs, switchover to pulse-skipping operation occurs at I_{LOAD} = 0.96A or about 1/5 full load. The crossover point occurs at an even lower value if a swinging (soft-saturation) inductor is used.

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

DC output accuracy specifications refer to the trip level of the error comparator. When the inductor is in continuous conduction, the output voltage has a DC regulation higher than the trip level by 50% of the ripple. In discontinuous conduction (SKIP = GND, light load), the output voltage has a DC regulation higher than the trip level by approximately 1.5% due to slope compensation.

Forced-PWM Mode

The low-noise, forced-PWM (SKIP = V_{CC}) mode disables the zero-crossing comparator, which controls the

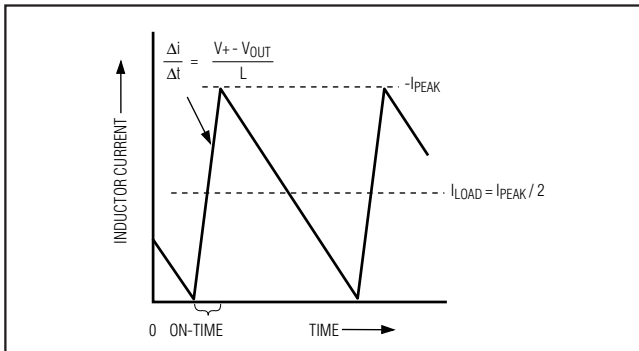


Figure 5. Pulse-Skipping/Discontinuous Crossover Point

low-side switch on-time. Disabling the zero-crossing detector causes the low-side, gate-drive waveform to become the complement of the high-side, gate-drive waveform. The inductor current reverses at light loads as the PWM loop strives to maintain a duty ratio of V_{OUT}/V₊. The benefit of forced-PWM mode is to keep the switching frequency fairly constant, but it comes at a cost: the no-load battery current can be 10mA to 50mA, depending on switching frequency and the external MOSFETs.

Forced-PWM mode is most useful for reducing audio-frequency noise, improving load-transient response, providing sink-current capability for dynamic output voltage adjustment, and improving the cross-regulation of multiple-output applications that use a flyback transformer or coupled inductor.

Enhanced Ultrasonic Mode (25kHz (min) Pulse Skipping)

Leaving SKIP unconnected or connecting SKIP to REF activates a unique pulse-skipping mode with a minimum switching frequency of 25kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point (I_{LOAD(SKIP)}) that occurs when normally pulse skipping.

An ultrasonic pulse occurs when the controller detects that no switching has occurred within the last 28μs. Once triggered, the ultrasonic controller pulls DL high, turning on the low-side MOSFET to induce a negative inductor current. After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the controller detects that the inductor current dropped below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equation:

$$V_{ISONIC} = I_L R_{ON} = (V_{REF} - V_{FB}) \times 0.58$$

where V_{FB} > V_{REF} and R_{ON} is the on-resistance of the synchronous rectifier (MAX8734A) or the current-sense resistor value (MAX8732A/MAX8733A).

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Reference and Linear Regulators (REF, LDO5, and LDO3)

The 2V reference (REF) is accurate to $\pm 1\%$ over temperature, making REF useful as a precision system reference. Bypass REF to GND with a $0.22\mu\text{F}$ (min) capacitor. REF can supply up to $100\mu\text{A}$ for external loads. However, if extremely accurate specifications for both the main output voltages and REF are essential, avoid loading REF. Loading REF reduces the LDO5, LDO3, OUT5, and OUT3 output voltages slightly because of the reference load-regulation error.

Two internal regulators produce 5V (LDO5) and 3.3V (LDO3). LDO5 provides gate drive for the external MOSFETs and powers the PWM controller, logic, reference, and other blocks within the device. The LDO5 regulator supplies a total of 100mA for internal and external loads, including MOSFET gate drive, which typically varies from 10mA to 50mA, depending on switching frequency and the external MOSFETs. LDO3 powers up when the reference (REF) is in regulation, and supplies up to 100mA for external loads. Bypass LDO5 and LDO3 with a minimum $4.7\mu\text{F}$ load; use an additional $1\mu\text{F}$ per 5mA of internal and external load.

When the 5V main output voltage is above the LDO5 bootstrap-switchover threshold, an internal 1.4Ω p-channel MOSFET switch connects OUT5 to LDO5 while simultaneously shutting down the LDO5 linear regulator. Similarly, when the 3.3V main output voltage is above the LDO3 bootstrap-switchover threshold, an internal 1.5Ω p-channel MOSFET switch connects OUT3 to LDO3 while simultaneously shutting down the LDO3 linear regulator. These actions bootstrap the device, powering the internal circuitry and external loads from the output SMPS voltages, rather than through linear regulators from the bat-

tery. Bootstrapping reduces power dissipation due to gate charge and quiescent losses by providing power from a 90%-efficient switch-mode source, rather than from a much-less-efficient linear regulator.

Current-Limit Circuit (ILIM_)

The current-limit circuit employs a “valley” current-sensing algorithm. The MAX8734A uses the on-resistance of the synchronous rectifier, while the MAX8732A/MAX8733A use a discrete resistor in series with the source of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at CS_ (MAX8732A/MAX8733A)/LX_ (MAX8734A) is above the current-limit threshold, the PWM is not allowed to initiate a new cycle (Figure 7). The actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-limit threshold, inductor value, and input and output voltage.

For the MAX8732A/MAX8733A, connect CS_ to the junction of the synchronous rectifier source and a current-sense resistor to GND. With a current-limit threshold of 100mV, the accuracy is approximately $\pm 7\%$. Using a lower current-sense threshold results in less accuracy. The current-sense resistor only dissipates power when the synchronous rectifier is on.

For lower power dissipation, the MAX8734A uses the on-resistance of the synchronous rectifier as the current-sense element. Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET data sheet, and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each $^{\circ}\text{C}$ of temperature rise. The current limit varies with the on-resistance of the synchronous rectifier. The reward for this uncertainty is robust, lossless overcurrent sensing. When combined with the

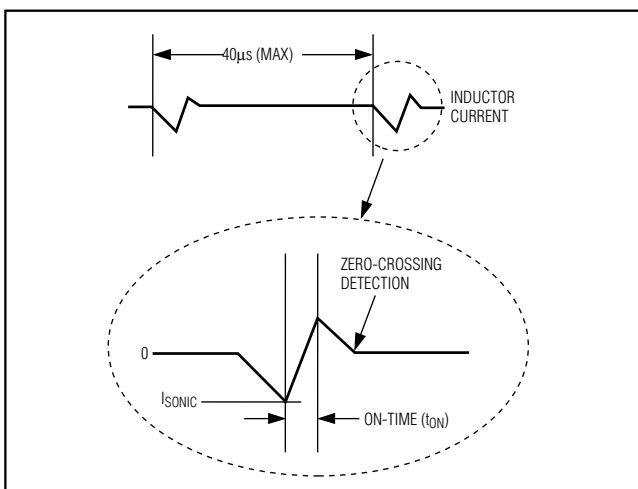


Figure 6. Ultrasonic Current Waveforms

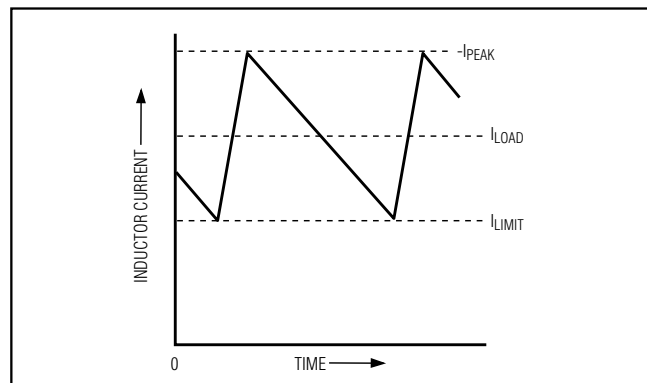


Figure 7. “Valley” Current-Limit Threshold Point

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

MAX8732A/MAX8733A/MAX8734A

undervoltage-protection circuit, this current-limit method is effective in almost every circumstance.

A negative current limit prevents excessive reverse inductor currents when V_{OUT} sinks current. The negative current-limit threshold is set to approximately 120% of the positive current limit and therefore tracks the positive current limit when $ILIM_{-}$ is adjusted.

The current-limit threshold is adjusted with an external voltage-divider at $ILIM_{-}$. The current-limit threshold adjustment range is from 50mV to 300mV. In the adjustable mode, the current-limit threshold voltage is precisely 1/10th the voltage at $ILIM_{-}$. The threshold defaults to 100mV when $ILIM_{-}$ is connected to V_{CC} .

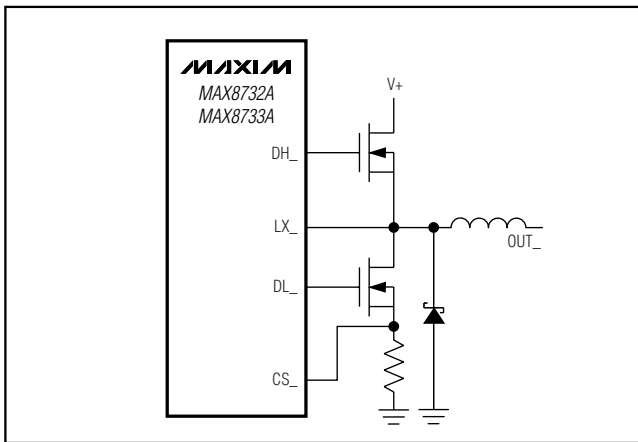


Figure 8. Current Sensing Using Sense Resistor (MAX8732A/MAX8733A)

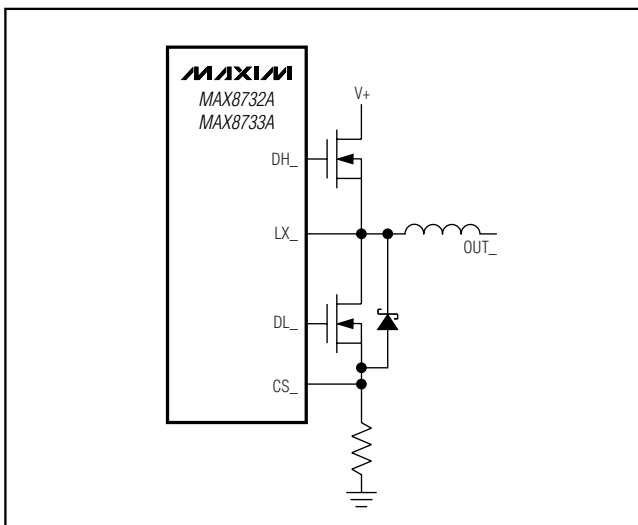


Figure 9. More Accurate Current Sensing with Adjusted Schottky Connection

The logic threshold for switchover to the 100mV default value is approximately $V_{CC} - 1V$.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals at CS_{-} . Mount or place the device close to the synchronous rectifier or sense resistor (whichever is used) with short, direct traces, making a Kelvin-sense connection to the sense resistor. The current-sense accuracy of Figure 8 is degraded if the Schottky diode conducts during the synchronous rectifier on-time. To ensure that all current passes through the sense resistor, connect the Schottky diode in parallel with only the synchronous rectifier (Figure 9) if the voltage drop across the synchronous rectifier and sense resistor exceeds the Schottky diode's forward voltage. Note that at high temperatures, the on-resistance of the synchronous rectifier increases and the forward voltage of the Schottky diode decreases.

MOSFET Gate Drivers (DH_{-} , DL_{-})

The DH_{-} and DL_{-} gate drivers sink 2.0A and 3.3A, respectively, of gate drive, ensuring robust gate drive for high-current applications. The DH_{-} floating high-side MOSFET drivers are powered by diode-capacitor charge pumps at BST_{-} . The DL_{-} synchronous-rectifier drivers are powered by $LDO5$.

The internal pulldown transistors that drive DL_{-} low have a 0.6Ω typical on-resistance. These low on-resistance pulldown transistors prevent DL_{-} from being pulled up during the fast rise time of the inductor nodes due to capacitive coupling from the drain to the gate of the low-side synchronous-rectifier MOSFETs. However, for high-current applications, some combinations of high- and low-side MOSFETs may cause excessive gate-drain coupling, which leads to poor efficiency and EMI-producing shoot-through currents. Adding a resistor in series with BST_{-} increases the turn-on time of the

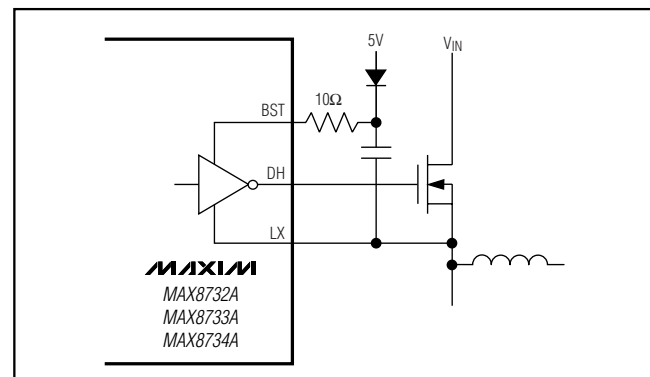


Figure 10. Reducing the Switching-Node Rise Time

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

high-side MOSFETs at the expense of efficiency, without degrading the turn-off time (Figure 10).

Adaptive dead-time circuits monitor the DL₋ and DH₋ drivers and prevent either FET from turning on until the other is fully off. This algorithm allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be low-resistance, low-inductance paths from the gate drivers to the MOSFET gates for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry interprets the MOSFET gate as “off” when there is actual charge left on the gate. Use very short, wide traces measuring 10 to 20 squares (50 mils to 100 mils wide if the MOSFET is 1in from the device).

POR, UVLO, and Internal Digital Soft-Start

Power-on reset (POR) occurs when V₊ rises above approximately 2.4V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. LDO5 undervoltage-lockout (UVLO) circuitry inhibits switching when LDO5 is below 4V (typ). DL₋ is low if $\overline{\text{PRO}}$ is disabled; DL₋ is high if $\overline{\text{PRO}}$ is enabled. The output voltages begin to ramp up once V_{CC} exceeds its 3.25V (typ) UVLO threshold and REF is in regulation. The internal digital soft-start timer begins to ramp up the maximum-allowed current limit during startup. The 1.7ms ramp occurs in five steps: 20%, 40%, 60%, 80%, and 100%.

When LDO5 falls below its 4V (typ) UVLO threshold, DH₋ and DL₋ are immediately forced low, and the outputs are high impedance. REF is turned off when V_{CC} falls below 3.25V (typ). DL₋ is forced high again when V_{CC} falls below its 1V (typ) POR threshold.

Power-Good Output (PGOOD)

The PGOOD comparator continuously monitors both output voltages for undervoltage conditions. PGOOD is actively held low in shutdown, standby, and soft-start. PGOOD releases and digital soft-start terminates when both outputs reach the error-comparator threshold. PGOOD goes low if EITHER output turns off or is 10% below its nominal regulation point. PGOOD is a true open-drain output. Note that PGOOD is independent of the state of $\overline{\text{PRO}}$.

Fault Protection

The MAX8732A/MAX8733A/MAX8734A provide over/undervoltage fault protection. Drive $\overline{\text{PRO}}$ low to activate fault protection. Drive $\overline{\text{PRO}}$ high to disable fault protection. Once activated, the devices continuously monitor for both undervoltage and overvoltage conditions.

Overvoltage Protection

When the output voltage is 11% above the set voltage, the overvoltage fault protection activates. The synchronous rectifier turns on 100% and the high-side MOSFET turns off. This rapidly discharges the output capacitors, decreasing the output voltage. The output voltage may dip below ground. For loads that cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. In practical applications, there is a fuse between the power source (battery) and the external high-side switches. If the overvoltage condition is caused by a short in the high-side switch, turning the synchronous rectifier on 100% creates an electrical short between the battery and GND, blowing the fuse and disconnecting the battery from the output. Once an overvoltage fault condition is set, it can only be reset by toggling $\overline{\text{SHDN}}$, ON₋, or cycling V₊ (POR).

Undervoltage Protection

When the output voltage is 30% below the set voltage for over 22ms (undervoltage shutdown blanking time), the undervoltage fault protection activates. Both SMPSs stop switching. The two outputs start to discharge (see the *Discharge Mode (Soft-Stop)* section). When the output voltage drops to 0.3V, the synchronous rectifiers turn on, clamping the outputs to GND. Toggle $\overline{\text{SHDN}}$ or ON₋, or cycle V₊ (POR) to clear the undervoltage fault latch.

Thermal Protection

The MAX8732A/MAX8733A/MAX8734A have thermal shutdown to protect the devices from overheating. Thermal shutdown occurs when the die temperature exceeds +160°C. All internal circuitry shuts down during thermal shutdown. The MAX8732A/MAX8733A/MAX8734A may trigger thermal shutdown if LDO₋ is not bootstrapped from OUT₋ while applying a high input voltage on V₊ and drawing the maximum current (including short circuit) from LDO₋. Even if LDO₋ is bootstrapped from OUT₋, overloading the LDO₋ causes large power dissipation on the bootstrap switches, which may result in thermal shutdown. Cycling $\overline{\text{SHDN}}$, ON3, ON5, or a V₊ (POR) ends the thermal-shutdown state.

Discharge Mode (Soft-Stop)

When $\overline{\text{PRO}}$ is low and a transition to standby or shutdown mode occurs, or the output undervoltage fault latch is set, the outputs discharge to GND through an internal 12Ω switch, until the output voltages decrease to 0.3V. The reference remains active to provide an accurate threshold and to provide overvoltage protection. When both SMPS outputs discharge to 0.3V, the DL₋ synchronous rectifier drivers are forced high. The

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

MAX8732A/MAX8733A/MAX8734A

Table 3. Operating-Mode Truth Table

MODE	CONDITION	COMMENT
Power-Up	LDO5 < UVLO threshold	Transitions to discharge mode after a V+ POR and after REF becomes valid. LDO5, LDO3, and REF remain active. DL_ is active if $\overline{P\overline{R}O}$ is low.
Run	$\overline{S\overline{H}D\overline{N}}$ = high, ON3 or ON5 enabled	Normal operation.
Overvoltage Protection	Either output > 111% of nominal level, $\overline{P\overline{R}O}$ = low	DL_ is forced high. LDO3, LDO5 active. Exited by a V+ POR or by toggling $\overline{S\overline{H}D\overline{N}}$, ON3, or ON5.
Undervoltage Protection	Either output < 70% of nominal after 22ms time-out expires and output is enabled, $\overline{P\overline{R}O}$ = low	If $\overline{P\overline{R}O}$ is low, DL_ is forced high after discharge mode terminates. LDO3, LDO5 active. Exited by a V+ POR or by toggling $\overline{S\overline{H}D\overline{N}}$, ON3, or ON5.
Discharge	$\overline{P\overline{R}O}$ is low and either SMPS output is still high in either standby mode or shutdown mode	Discharge switch (12 Ω) connects OUT_ to PGND. One output may still run while the other is in discharge mode. Activates when LDO_ is in UVLO, or transition to UVLO, standby, or shutdown has begun. LDO3, LDO5 active.
Standby	ON5, ON3 < startup threshold, $\overline{S\overline{H}D\overline{N}}$ = high	DL_ stays high if $\overline{P\overline{R}O}$ is low. LDO3, LDO5 active.
Shutdown	$\overline{S\overline{H}D\overline{N}}$ = low	All circuitry off.
Thermal Shutdown	T _J > +160°C	All circuitry off. Exited by V+ POR or cycling $\overline{S\overline{H}D\overline{N}}$, ON3, or ON5.

synchronous rectifier drivers clamp the SMPS outputs to GND. When $\overline{P\overline{R}O}$ is high, the SMPS outputs do not discharge and the DL_ synchronous rectifier drivers remain low.

Shutdown Mode

Drive $\overline{S\overline{H}D\overline{N}}$ below the precise $\overline{S\overline{H}D\overline{N}}$ input falling-edge trip level to place the MAX8732A/MAX8733A/MAX8734A in their low-power shutdown state. The MAX8732A/MAX8733A/MAX8734A consume only 6 μ A of quiescent current while in shutdown mode. When shutdown mode activates, the reference turns off, making the threshold to exit shutdown inaccurate. To guarantee startup,

drive $\overline{S\overline{H}D\overline{N}}$ above 2V ($\overline{S\overline{H}D\overline{N}}$ input rising-edge trip level). For automatic shutdown and startup, connect $\overline{S\overline{H}D\overline{N}}$ to V+. If $\overline{P\overline{R}O}$ is low, both SMPS outputs are discharged to 0.3V through a 12 Ω switch before entering true shutdown. The accurate 1V falling-edge threshold on $\overline{S\overline{H}D\overline{N}}$ can be used to detect a specific analog voltage level and shut down the device. Once in shutdown, the 1.6V rising-edge threshold activates, providing sufficient hysteresis for most applications. For additional hysteresis, the undervoltage threshold can be made dependent on REF or LDO_, which go to 0V in shutdown.

Table 4. Power-Up Sequencing

$\overline{S\overline{H}D\overline{N}}$ (V)	V _{ON3} (V)	V _{ON5} (V)	LDO5	LDO3	5V SMPS	3V SMPS
Low	X	X	Off	Off	Off	Off
"> 2.4" => High	Low	Low	On	On (after REF powers up)	Off	Off
"> 2.4" => High	High	High	On	On (after REF powers up)	On	On
"> 2.4" => High	High	Low	On	On (after REF powers up)	Off	On
"> 2.4" => High	Low	High	On	On (after REF powers up)	On	Off
"> 2.4" => High	High	REF	On	On (after REF powers up)	On (after 3V SMPS is up)	On
"> 2.4" => High	REF	High	On	On (after REF powers up)	On	On (after 5V SMPS is up)

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Power-Up Sequencing and On/Off Controls (ON3, ON5)

ON3 and ON5 control SMPS power-up sequencing. ON3 or ON5 rising above 2.4V enables the respective outputs. ON3 or ON5 falling below 1.6V disables the respective outputs.

Connecting ON3 or ON5 to REF forces the respective outputs off while the other output is below regulation and starts after that output regulates. The second SMPS remains on until the first SMPS turns off, the device shuts down, a fault occurs, or LDO5 goes into undervoltage lockout. Both supplies begin their power-down sequence immediately when the first supply turns off. Driving ON_ below 0.8V clears the overvoltage, undervoltage, and thermal fault latches.

Adjustable-Output Feedback (Dual-Mode FB)

Connect FB_ to GND to enable the fixed, preset SMPS output voltages (3.3V and 5V). Connect a resistive voltage-divider at FB_ between OUT_ and GND to adjust the respective output voltage between 2V and 5.5V (Figure 11). Choose R2 to be approximately 10k Ω , and solve for R1 using the equation:

$$R1 = R2 \times \left(\frac{V_{OUT_}}{V_{FB}} - 1 \right)$$

where $V_{FB} = 2V$ nominal.

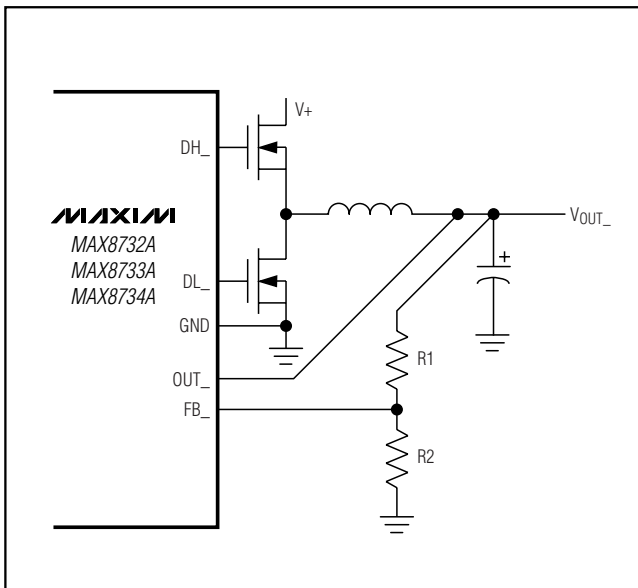


Figure 11. Setting $V_{OUT_}$ with a Resistor-Divider

When using the adjustable-output mode, set the 3.3V SMPS lower than the 5V SMPS. LDO5 connects to OUT5 through an internal switch only when OUT5 is above the LDO5 bootstrap-switch threshold (4.56V). LDO3 connects to OUT3 through an internal switch only when OUT3 is above the LDO3 bootstrap switch threshold (2.91V). Bootstrapping is most effective when the fixed output voltages are used. Once LDO_ is bootstrapped from OUT_, the internal linear regulator turns off. This reduces internal power dissipation and improves efficiency when LDO_ is powered with a high input voltage.

Design Procedure

Establish the input voltage range and maximum load current before choosing an inductor and its associated ripple-current ratio (LIR). The following four factors dictate the rest of the design:

- 1) **Input Voltage Range.** The maximum value ($V_{+(MAX)}$) must accommodate the maximum AC adapter voltage. The minimum value ($V_{+(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. Lower input voltages result in better efficiency.
- 2) **Maximum Load Current.** The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stress and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stress and drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- 3) **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage and MOSFET switching losses. The MAX8732A has a nominal switching frequency of 200kHz for the 5V SMPS and 300kHz for the 3.3V SMPS. The MAX8733A has a nominal switching frequency of 400kHz for the 5V SMPS and 500kHz for the 3.3V SMPS. The MAX8734A has a pin-selectable switching frequency.
- 4) **Inductor Ripple Current Ratio (LIR).** LIR is the ratio of the peak-to-peak ripple current to the average inductor current. Size and efficiency trade-offs must be considered when setting the inductor ripple current ratio. Low inductor values cause large ripple currents, resulting in the smallest size, but poor efficiency and high output noise. The minimum practical inductor value is one that causes the circuit to operate at critical conduction (where the inductor current just touches zero with every cycle

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

at maximum load). Inductor values lower than this grant no further size-reduction benefit.

The MAX8732A/MAX8733A/MAX8734As' pulse-skipping algorithm (SKIP = GND) initiates skip mode at the critical conduction point, so the inductor's operating point also determines the load current at which PWM/PFM switchover occurs. The optimum point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency (on-time) and operating point (% ripple or LIR) determine the inductor value as follows:

$$L = \frac{V_{OUT_}(V_{+} - V_{OUT_})}{V_{+} \times f \times LIR \times I_{LOAD(MAX)}}$$

Example: $I_{LOAD(MAX)} = 5A$, $V_{+} = 12V$, $V_{OUT5} = 5V$, $f = 200kHz$, 35% ripple current or $LIR = 0.35$:

$$L = \frac{5V(12V - 5V)}{12V \times 200kHz \times 0.35 \times 5A} = 8.3\mu H$$

Find a low-loss inductor with the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + [(LIR / 2) \times I_{LOAD(MAX)}]$$

The inductor ripple current also impacts transient-response performance, especially at low $V_{+} - V_{OUT_}$ differences. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The peak amplitude of the output transient (V_{SAG}) is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time:

$$V_{SAG} = \frac{(\Delta I_{LOAD(MAX)})^2 \times L \left(K \frac{V_{OUT_}}{V_{+}} + t_{OFF(MIN)} \right)}{2 \times C_{OUT} \times V_{OUT_} \left[K \left(\frac{V_{+} - V_{OUT_}}{V_{+}} \right) - t_{OFF(MIN)} \right]}$$

where minimum off-time = $0.350\mu s$ (max) and K is from Table 2.

Determining the Current Limit

The minimum current-limit threshold must be great enough to support the maximum load current when the current limit is at the minimum tolerance value. The val-

ley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half of the ripple current; therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - [(LIR / 2) \times I_{LOAD(MAX)}]$$

where $I_{LIMIT(LOW)}$ = minimum current-limit threshold voltage divided by the $R_{DS(ON)}$ of N2/N4 (MAX8734A). For the MAX8732A/MAX8733A/MAX8734A, the minimum current-limit threshold voltage is 93mV ($I_{LIM_} = V_{CC}$). Use the worst-case maximum value for $R_{DS(ON)}$ from the MOSFET N2/N4 data sheet and add some margin for the rise in $R_{DS(ON)}$ with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise.

Examining the 5A circuit example with a maximum $R_{DS(ON)} = 12m\Omega$ at high temperature reveals the following:

$$I_{LIMIT(LOW)} = 93mV / 12m\Omega > 5A - (0.35 / 2) 5A$$

$$7.75A > 4.125A$$

7.75A is greater than the valley current of 4.125A, so the circuit can easily deliver the full-rated 5A using the fixed 100mV nominal current-limit threshold voltage.

Connect the source of the synchronous rectifier to a current-sense resistor to GND (MAX8732A/MAX8733A), and connect CS_{-} to that junction to set the current limit for the device. The MAX8732A/MAX8733A/MAX8734A limit the current with the sense resistor instead of the $R_{DS(ON)}$ of N2/N4. The maximum value of the sense resistor can be calculated with the equation:

$$I_{LIM_} = 93mV / R_{SENSE}$$

Output-Capacitor Selection

The output filter capacitor must have low enough equivalent series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements. The output capacitance must also be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions without tripping the overvoltage fault latch. In applications where the output is subject to large load transients, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$R_{ESR} \leq \frac{V_{DIP}}{I_{LOAD(MAX)}}$$

where V_{DIP} is the maximum-tolerable transient voltage drop. In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain an acceptable level of output voltage ripple: