Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-0839; Rev 0; 6/07

EVALUATION KIT AVAILABLE

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

General Description

The MAX8744A/MAX8745A are dual step-down, switch-mode, power-supply (SMPS) controllers with synchronous rectification, intended for main 5V/3.3V power generation in battery-powered systems. Fixed-frequency operation with optimal interleaving minimizes input ripple current from the lowest input voltages up to the 26V maximum input. Optimal 40/60 interleaving allows the input voltage to go down to 8.3V before duty-cycle overlap occurs, compared to 180° out-of-phase regulators where the duty-cycle overlap occurs when the input drops below 10V.

Output current sensing provides peak current-limit protection, using either an accurate sense resistor or using lossless inductor DCR current sensing. A low-noise mode maintains high light-load efficiency while keeping the switching frequency out of the audible range.

An internal, fixed 5V, 100mA linear regulator powers up the MAX8744A/MAX8745A and their gate drivers, as well as external keep-alive loads. When the main PWM regulator is in regulation, an automatic bootstrap switch bypasses the internal linear regulator, providing current up to 200mA. An additional adjustable linear-regulator driver with an external pnp transistor can be used with a secondary winding to provide a 12V supply, or powered directly from the main outputs to generate low-voltage outputs as low as 1V.

Independent enable controls and power-good signals allow flexible power sequencing. Voltage soft-start gradually ramps up the output voltage and reduces inrush current, while soft-shutdown gradually ramps the output voltage down, preventing negative voltage dips. The MAX8744A/MAX8745A feature output undervoltage and thermal-fault protection. The MAX8744A also includes output overvoltage-fault protection.

The MAX8744A/MAX8745A are available in a 32-pin, 5mm x 5mm, thin QFN package. The exposed backside pad improves thermal characteristics for demanding linear keep-alive applications.

Applications

Main Power Supplies

2 to 4 Li+ Cell Battery-Powered Devices

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Dual Mode is a trademark of Maxim Integrated Products, Inc.

Features

- ♦ Fixed-Frequency, Current-Mode Control
- ♦ 40/60 Optimal Interleaving
- ♦ Internal BST Switches
- ♦ Internal 5V, 100mA Linear Regulator
- ♦ Auxiliary Linear-Regulator Driver (12V or Adjustable Down to 1V)
- ♦ Dual Mode™ Feedback—3.3V/5V Fixed or Adjustable Output Voltages
- ♦ 200kHz/300kHz/500kHz Switching Frequency
- ♦ Undervoltage and Thermal-Fault Protection
- ♦ Overvoltage-Fault Protection (MAX8744A Only)
- ♦ 6V to 26V Input Range
- ♦ 2V ±0.75% Reference Output
- ♦ Independent Enable Inputs and Power-Good Outputs
- ♦ Soft-Start and Soft-Shutdown (Voltage Ramp)
- ♦ 8µA (typ) Shutdown Current

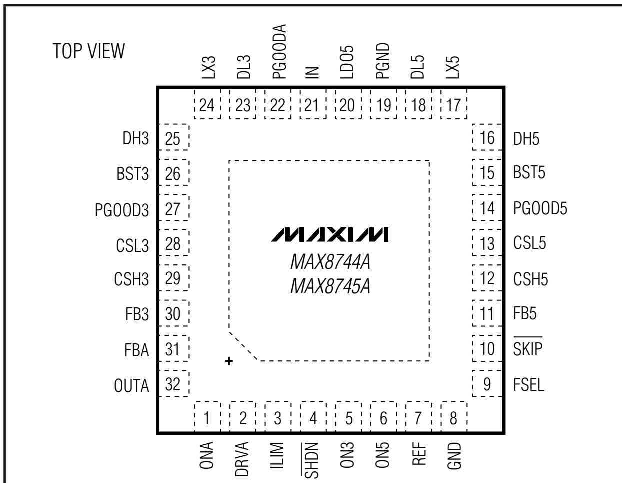
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8744AETJ+	-40°C to +85°C	32 Thin QFN (5mm x 5mm)	T3255-4
MAX8745AETJ+*	-40°C to +85°C	32 Thin QFN (5mm x 5mm)	T3255-4

+Denotes a lead-free package.

**Future product—contact factory for availability.*

Pin Configuration



THIN QFN 5mm x 5mm

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, DRVA, OUTA to GND...........................-0.3V to +28V
LDO5, ON3, ON5, ONA to GND ....-0.3V to +6V
PGOODA, PGOOD3, PGOOD5 to GND..................-0.3V to +6V
CSL3, CSH3, CSL5, CSH5 to GND ....-0.3V to +6V
$\overline{REF}$, FB3, FB5, FBA to GND..................-0.3V to (V_{LDO5} + 0.3V)
$\overline{SKIP}$, FSEL, ILIM to GND.......................-0.3V to (V_{LDO5} + 0.3V)
DL3, DL5 to PGND................................-0.3V to (V_{LDO5} + 0.3V)
BST3, BST5 to PGND ....-0.3V to +34V
BST3 to LX3...-0.3V to +6V
DH3 to LX3 ....-0.3V to (V_{BST3} + 0.3V)
BST5 to LX5...-0.3V to +6V
DH5 to LX5 ....-0.3V to (V_{BST5} + 0.3V)
GND to PGND ....-0.3V to +0.3V
BST3, BST5 to LDO5...-0.3V to +0.3V
LDO Short Circuit to GND ....Momentary
REF Short Circuit to GND ....Momentary
DRVA Current (Sinking) 30mA
OUTA Shunt Current 30mA
Continuous Power Dissipation (T_A = +70°C)
Multilayer PCB
32-Pin, 5mm x 5mm TQFN
(derated 34.5mW/°C above +70°C) 2459mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature..+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES (Note 1)						
V_{IN} Input Voltage Range	V_{IN}	LDO5 in regulation	5.4		26.0	V
		IN = LDO5, V_{CSL5} < 4.4V	4.5		5.5	
V_{IN} Operating Supply Current	I_{IN}	LDO5 switched over to CSL5, either SMPS on		20	36	µA
V_{IN} Standby Supply Current	$I_{IN(STBY)}$	V_{IN} = 6V to 26V, both SMPS off, includes $I_{\overline{SHDN}}$		65	120	µA
V_{IN} Shutdown Supply Current	$I_{IN(SHDN)}$	V_{IN} = 6V to 26V		8	20	µA
Quiescent Power Consumption	P_Q	Both SMPS on, FB3 = FB5 = LDO5, $\overline{SKIP}$ = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V, V_{OUTA} = 15V, P_{IN} + P_{CSL3} + P_{CSL5} + P_{OUTA}		3.5	4.5	mW
MAIN SMPS CONTROLLERS						
3.3V Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB3 = LDO5, 0 < V_{CSH3} - V_{CSL3} < 50mV (Note 2)	3.265	3.315	3.365	V
5V Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB5 = LDO5, 0 < V_{CSH5} - V_{CSL5} < 50mV (Note 2)	4.94	5.015	5.09	V
Feedback Voltage in Adjustable Mode (Note 2)	$V_{FB\_}$	V_{IN} = 6V to 26V, FB3 or FB5 duty factor = 20% to 80%	1.980	2.010	2.040	V
		V_{IN} = 6V to 26V, FB3 or FB5 duty factor = 50%	1.990	2.010	2.030	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{\text{SKIP}}$ = GND, ILIM = LDO5, FBA = LDO5, $I_{REF} = I_{LDO5} = I_{OUTA}$ = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Adjust Range		Either SMPS		2.0		5.5	V
FB3, FB5 Dual Mode Threshold				3.0	V_{LOO5} - 1.0	V_{LOO5} - 0.4	V
Feedback Input Leakage Current		$V_{FB3} = V_{FB5}$ = 2.1V		-0.1		+0.1	µA
DC Load Regulation		Either SMPS, $\overline{\text{SKIP}}$ = LDO5, 0 < $V_{CSH\_}$ - $V_{CSL\_}$ < 50mV			-0.1		%
Line Regulation Error		Either SMPS, 6V < V_{IN} < 26V			0.03		%/V
Operating Frequency (Note 1)	f_{OSC}	FSEL = GND		170	200	230	kHz
		FSEL = REF		270	300	330	
		FSEL = LDO5		425	500	575	
Maximum Duty Factor	D_{MAX}	(Note 1)		97.5	99		%
Minimum On-Time	t_{ONMIN}				100		ns
SMPS3-to-SMPS5 Phase Shift		SMPS5 starts after SMPS3			40		%
					144		Deg
CURRENT LIMIT							
ILIM Adjustment Range				0.5		V_{REF}	V
Current-Sense Input Leakage Current		CSH3 = CSH5 = GND or LDO5		-1		+1	µA
Current-Limit Threshold (Fixed)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM = LDO5		45	50	55	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	V_{ILIM} = 2.00V	185	200	215	mV
			V_{ILIM} = 1.00V	94	100	106	
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{\text{SKIP}}$ = ILIM = LDO5		-67	-60	-53	mV
		$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{\text{SKIP}}$ = LDO5, adjustable mode, percent of current limit			-120		%
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{\text{SKIP}}$ = GND, ILIM = LDO5		0	3	6	mV
Idle Mode™ Threshold	V_{IDLE}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{\text{SKIP}}$ = GND	ILIM = LDO5	6	10	14	mV
			With respect to current-limit threshold (V_{LIMIT})		20		%
Idle Mode Threshold (Low Audible-Noise Mode)	V_{IDLE}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{\text{SKIP}}$ = REF	ILIM = LDO5	2.5	5	7.5	mV
			With respect to current-limit threshold (V_{LIMIT})		10		%
ILIM Leakage Current		ILIM = GND or REF		-1		+1	µA

Idle Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Ramp Time	t_{SSTART}	Measured from the rising edge of ON_ to full scale		2		ms
Soft-Stop Ramp Time	t_{SSTOP}	Measured from the falling edge of ON_ to full scale		4		ms
INTERNAL FIXED LINEAR REGULATORS						
LDO5 Output Voltage	V_{LDO5}	ON5 = GND, 6V < V_{IN} < 26V, 0 < I_{LDO5} < 100mA	4.85	4.95	5.10	V
LDO5 Undervoltage-Lockout Fault		Rising edge, hysteresis = 1%	3.7	4.0	4.1	V
Short-Circuit Current (Switched Over to CSL5)		LDO5 = GND, V_{CSL5} > 4.7V	200	425		mA
AUXILIARY LINEAR REGULATOR						
DRVA Voltage Range	V_{DRVA}		0.5		26.0	V
DRVA Drive Current		V_{FBA} = 1.05V, V_{DRVA} = 5V			0.4	mA
		V_{FBA} = 0.965V, V_{DRVA} = 5V	10			
FBA Regulation Threshold	V_{FBA}	V_{DRVA} = 5V, I_{DRVA} = 1mA (sink)	0.98	1.00	1.02	V
FBA Load Regulation		V_{DRA} = 5V, I_{DRVA} = 0.5mA to 5mA		-1.2	-2.2	%
OUTA Shunt Trip Level		Rising edge	25	26	27	V
FBA Leakage Current		V_{FBA} = 1.035V	-0.1		+0.1	µA
Secondary Feedback Regulation Threshold		V_{DRVA} - V_{OUTA}		0		V
DL5 Pulse Width				1/ $3f_{OSC}$		µs
OUTA Leakage Current	I_{OUTA}	V_{DRVA} = V_{OUTA} = 25V			50	µA
REFERENCE (REF)						
Reference Voltage	V_{REF}	LDO5 in regulation, I_{REF} = 0	1.985	2.00	2.015	V
Reference Load-Regulation Error	ΔV_{REF}	I_{REF} = -5µA to +50µA	-10		+10	mV
REF Lockout Voltage	$V_{REF(UVLO)}$	Rising edge		1.8		V
FAULT DETECTION						
Output Overvoltage Trip Threshold (MAX8744A Only)		With respect to error-comparator threshold	8	11	14	%
Output Overvoltage Fault Propagation Delay (MAX8744A Only)	t_{OVP}	50mV overdrive		10		µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage Protection Trip Threshold		With respect to error-comparator threshold		65	70	75	%
Output Undevoltage Fault Propagation Delay	t_{UVP}	50mV overdrive			10		µs
Output Undervoltage Protection Blanking Time	t_{BLANK}	From rising edge of ON_ with respect to f_{SW}		5000	6144	7000	$1/f_{OSC}$
PGOOD_ Lower Trip Threshold		With respect to error-comparator threshold, hysteresis = 1% (typ)		-12	-10	-8	%
PGOOD_ Propagation Delay	$t_{PGOOD\_}$	Falling edge, 50mV overdrive			10		µs
		Rising edge, 50mV overdrive			1		
PGOOD_ Output Low Voltage		I_{SINK} = 1mA				0.4	V
PGOOD_ Leakage Current	$I_{PGOOD\_}$	High state, PGOOD_ forced to 5.5V				1	µA
Thermal-Shutdown Threshold	t_{SHDN}	Hysteresis = 15°C			+160		°C
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ – LX_ forced to 5V			1.3	5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state			1.7	5	Ω
		DL_, low state			0.6	3	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2		A
DL_ Gate-Driver Source Current	I_{DL}	DL_ forced to 2.5V			1.7		A
DL_ Gate-Driver Sink Current	$I_{DL\ (SINK)}$	DL_ forced to 2.5V			3.3		A
Dead Time	t_{DEAD}	DH_low to DL_high		15	45		ns
		DL_low to DH_high		15	44		
Internal BST_ Switch On-Resistance	R_{BST}	I_{BST} = 10mA			5		Ω
BST_ Leakage Current		$V_{BST\_}$ = 26V			2	20	µA
INPUTS AND OUTPUTS							
$\overline{SHDN}$ Input Trip Level		Rising trip level		1.1	1.6	2.2	V
		Falling trip level		0.96	1	1.04	
ONA Logic Input Voltage		Hysteresis = 600mV (typ)	High	2.4			V
			Low			0.8	
ON3, ON5 Input Voltage		SMPS off level/clear fault level				0.8	V
		Delay start level		1.9		2.1	
		SMPS on level		2.4			

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Tri-Level Input Logic		$\overline{SKIP}$, FSEL	High	V_{LDO5} - 0.4			V
			REF	1.65		2.35	
			GND			0.5	
Input Leakage Current		$\overline{SKIP}$, FSEL forced to GND or LDO5		-1		+1	µA
		$\overline{SHDN}$ forced to GND or 26V		-1		+1	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
INPUT SUPPLIES (Note 1)					
V_{IN} Input Voltage Range	V_{IN}	LDO5 in regulation	5.4	26.0	V
		IN = LDO5, V_{CSL5} < 4.4V	4.5	5.5	
V_{IN} Operating Supply Current	I_{IN}	LDO5 switched over to CSL5, either SMPS on		40	µA
V_{IN} Standby Supply Current	$I_{IN(STBY)}$	V_{IN} = 6V to 26V, both SMPS off, includes $I_{\overline{SHDN}}$		120	µA
V_{IN} Shutdown Supply Current	$I_{IN(SHDN)}$	V_{IN} = 6V to 26V		20	µA
Quiescent Power Consumption	P_Q	Both SMPS on, FB3 = FB5 = LDO5; $\overline{SKIP}$ = GND, V_{CSL3} = 3.5V, V_{CSL5} = 5.3V, V_{OUTA} = 15V, P_{IN} + P_{CSL3} + P_{CSL5} + P_{OUTA}		4.5	mW
MAIN SMPS CONTROLLERS					
3.3V Output Voltage in Fixed Mode	V_{OUT3}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB3 = LDO5, 0 < V_{CSH3} - V_{CSL3} < 50mV (Note 2)	3.255	3.375	V
5V Output Voltage in Fixed Mode	V_{OUT5}	V_{IN} = 6V to 26V, $\overline{SKIP}$ = FB5 = LDO5, 0 < V_{CSH5} - V_{CSL5} < 50mV (Note 2)	4.925	5.105	V
Feedback Voltage in Adjustable Mode	$V_{FB\_}$	V_{IN} = 6V to 26V, FB3 or FB5 duty factor = 20% to 80% (Note 2)	1.974	2.046	V
Output Voltage Adjust Range		Either SMPS	2.0	5.5	V
FB3, FB5 Dual Mode Threshold			3V	V_{LDO5} - 0.4	V
Operating Frequency (Note 1)	f_{OSC}	FSEL = GND	170	230	kHz
		FSEL = REF	270	330	
		FSEL = LDO5	425	575	
Maximum Duty Factor	D_{MAX}		97		%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
CURRENT LIMIT						
ILIM Adjustment Range				0.5	V_{REF}	V
Current-Limit Threshold (Fixed)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM = LDO5		44	56	mV
Current-Limit Threshold (Adjustable)	V_{LIMIT}	$V_{CSH\_}$ - $V_{CSL\_}$	V_{ILIM} = 2.00V	185	215	mV
			V_{ILIM} = 1.00V	93	107	
INTERNAL FIXED LINEAR REGULATORS						
LDO5 Output Voltage	V_{LDO5}	ON5 = GND, 6V < V_{IN} < 26V,		4.85	5.10	V
LDO5 Undervoltage-Lockout Fault Threshold		Rising edge, hysteresis = 1% (typ)		3.7	4.1	V
LDO5 Bootstrap Switch		Rising edge of CSL5, hysteresis = 1% (typ)		4.30	4.75	V
Short-Circuit Current		LDO5 = GND, ON5 = GND			450	mA
Short-Circuit Current (Switched over to CSL5)		LDO5 = GND, V_{CSL5} > 4.7V		200		mA
AUXILIARY LINEAR REGULATOR						
DRVA Voltage Range	V_{DRVA}			0.5	26.0	V
DRVA Drive Current		V_{FBA} = 1.05V, V_{DRVA} = 5V			0.4	mA
		V_{FBA} = 0.965V, V_{DRVA} = 5V		10		
FBA Regulation Threshold	V_{FBA}	V_{DRVA} = 5V, I_{DRVA} = 1mA (sink)		0.98	1.02	V
OUTA Shunt Trip Level				25	27	V
REFERENCE (REF)						
Reference Voltage	V_{REF}	LDO5 in regulation, I_{REF} = 0		1.980	2.020	V

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, both SMPS enabled, FSEL = REF, $\overline{SKIP}$ = GND, ILIM = LDO5, FBA = LDO5, I_{REF} = I_{LDO5} = I_{OUTA} = no load, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT DETECTION							
Output Overvoltage Trip Threshold (MAX8744A Only)		With respect to error comparator threshold		8		14	%
Output Undervoltage Protection		With respect to error comparator threshold		65		75	%
PGOOD_ Lower Trip Threshold		With respect to error comparator threshold, hysteresis = 1%		-12		-8	%
PGOOD_ Output Low Voltage		I_{SINK} = 1mA				0.4	V
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	R_{DH}	BST_ – LX_ forced to 5V				5	Ω
DL_ Gate-Driver On-Resistance	R_{DL}	DL_, high state				5	Ω
		DL_, low state				3	
INPUTS AND OUTPUTS							
$\overline{SHDN}$ Input Trip Level		Rising trip level		1.0		2.3	V
		Falling trip level		0.96		1.04	
ONA Logic Input Voltage		Hysteresis = 600mV	High	2.4			V
			Low			0.8	
ON3, ON5 Input Voltage		SMPS off level/clear fault level				0.8	V
		Delay start level		1.9		2.1	
		SMPS on level		2.4			
Tri-Level Input Logic		$\overline{SKIP}$, FSEL	High	V_{LDO5} - 0.4			V
			REF	1.65		2.35	
			GND			0.5	

Note 1: The MAX8744A/MAX8745A cannot operate over all combinations of frequency, input voltage (V_{IN}), and output voltage. For large input-to-output differentials and high switching-frequency settings, the required on-time may be too short to maintain the regulation specifications. Under these conditions, a lower operating frequency must be selected. The minimum on-time must be greater than 150ns, regardless of the selected switching frequency. On-time and off-time specifications are measured from 50% point to 50% point at the DH_ pin with LX_ = GND, $V_{BST\_}$ = 5V, and a 250pF capacitor connected from DH_ to LX_. Actual in-circuit times may differ due to MOSFET switching speeds.

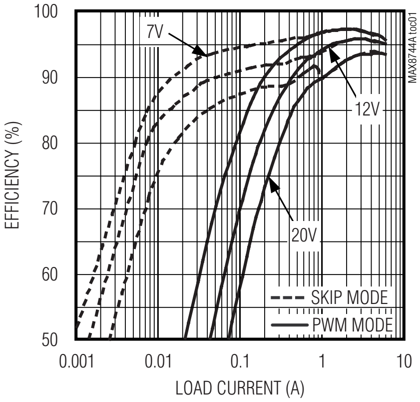
Note 2: When the inductor is in continuous conduction, the output voltage has a DC-regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction ($\overline{SKIP}$ = GND, light load), the output voltage has a DC regulation level higher than the trip level by approximately 1.1% due to slope compensation.

Note 3: Specifications from -40°C to +85°C are guaranteed by design, not production tested.

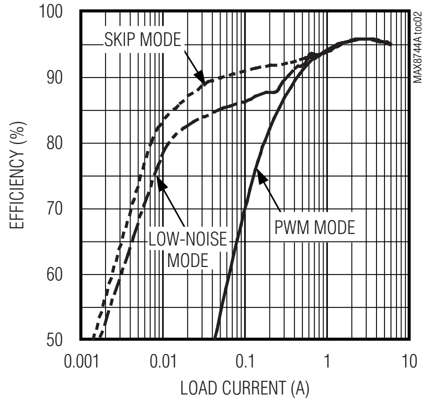
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

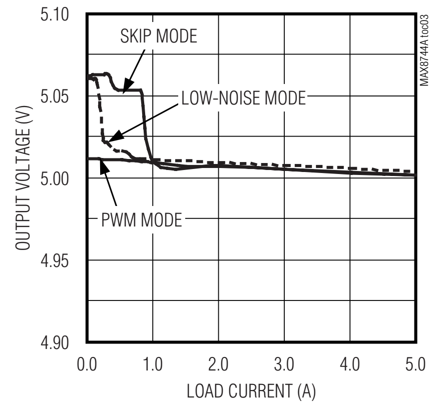
5V OUTPUT EFFICIENCY vs. LOAD CURRENT



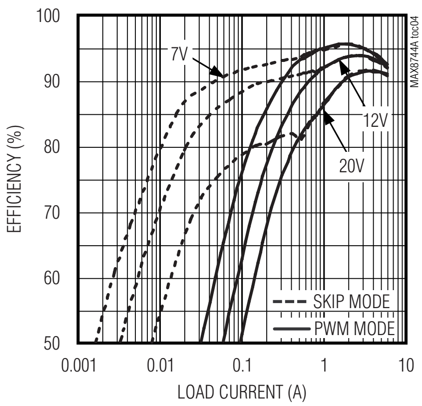
5V OUTPUT EFFICIENCY vs. LOAD CURRENT



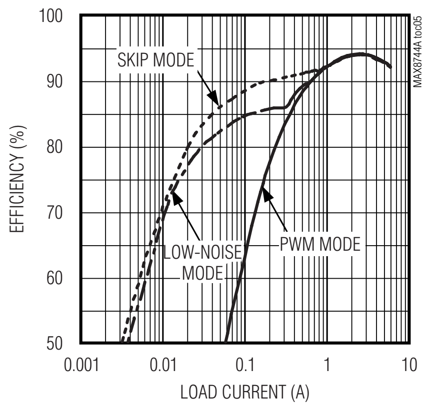
5V OUTPUT VOLTAGE vs. LOAD CURRENT



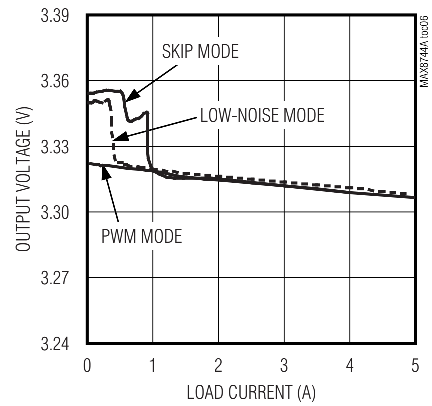
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



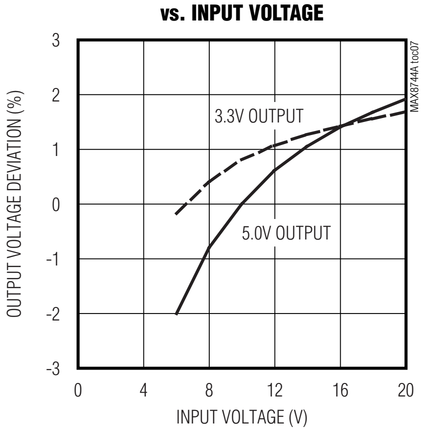
3.3V OUTPUT EFFICIENCY vs. LOAD CURRENT



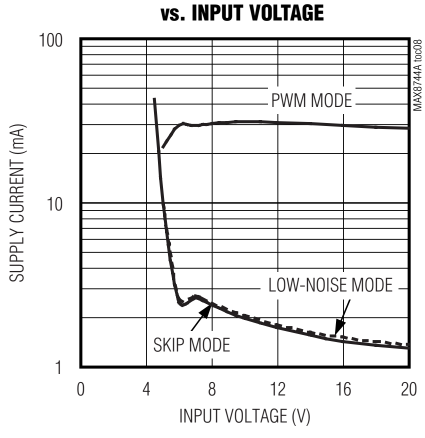
3.3V OUTPUT VOLTAGE vs. LOAD CURRENT



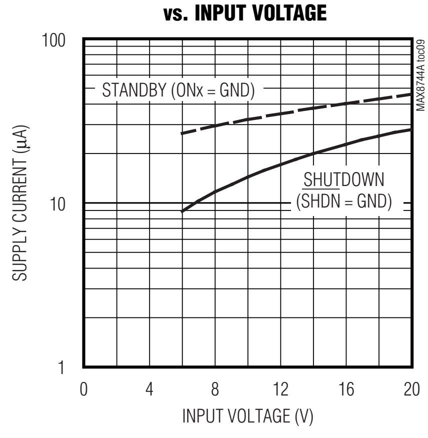
OUTPUT VOLTAGE DEVIATION vs. INPUT VOLTAGE



NO-LOAD INPUT SUPPLY CURRENT vs. INPUT VOLTAGE



STANDBY AND SHUTDOWN INPUT CURRENT vs. INPUT VOLTAGE

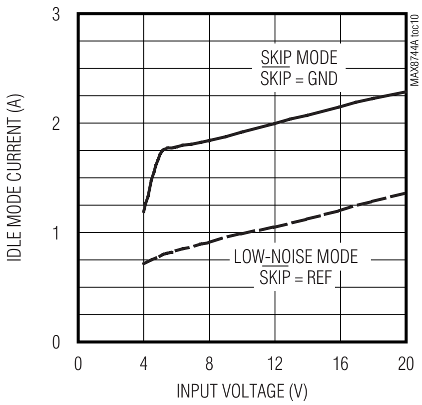


High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

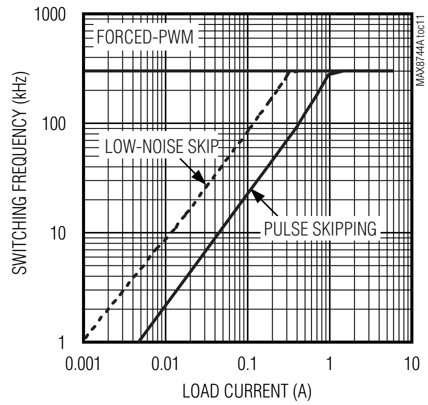
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

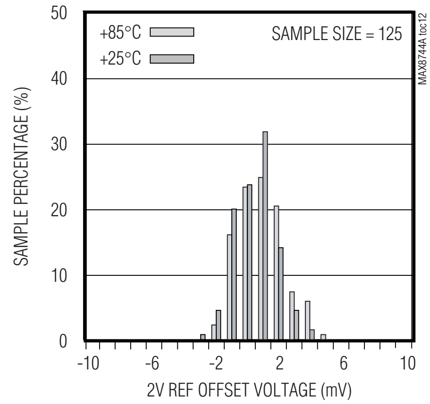
3.3V IDLE MODE CURRENT vs. INPUT VOLTAGE



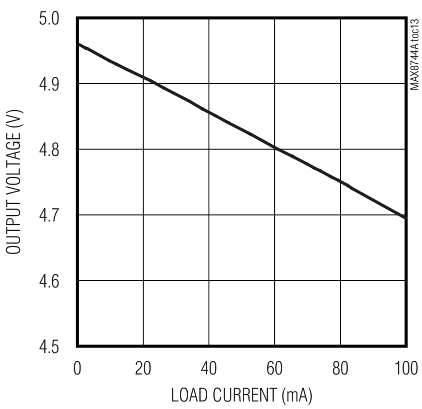
3.3V SWITCHING FREQUENCY vs. LOAD CURRENT



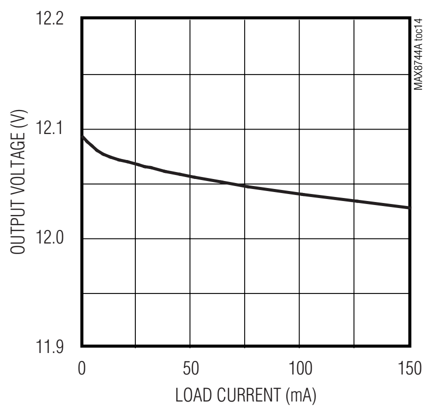
REFERENCE OFFSET VOLTAGE DISTRIBUTION



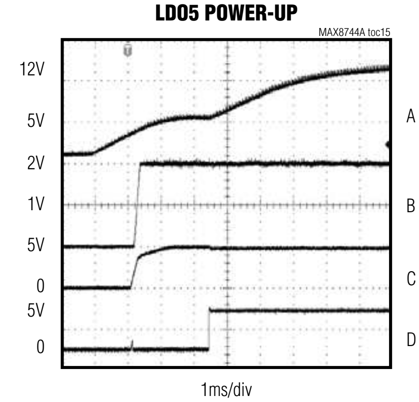
LDO5 OUTPUT VOLTAGE vs. LOAD CURRENT



OUTA OUTPUT VOLTAGE vs. LOAD CURRENT



LDO5 POWER-UP

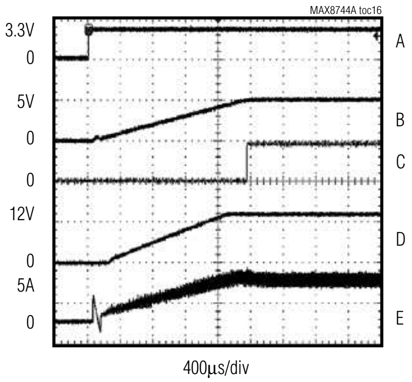


A. INPUT SUPPLY, 5V/div
B. REF, 2V/div
$\overline{SHDN}$ = IN
C. LDO5, 5V/div
D. PGOOD5, 5V/div

Typical Operating Characteristics (continued)

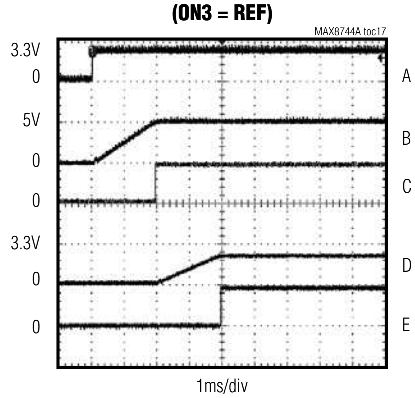
(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

SOFT-START WAVEFORM



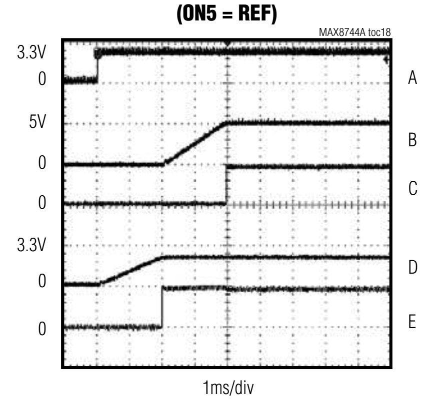
A. ON3 AND ON5, 5V/div
B. 5V OUTPUT (V_{OUT5}), 5V/div
C. PGOOD5, 5V/div
D. AUX LDO OUTPUT (V_{OUTA}), 10V/div
E. L5 INDUCTOR CURRENT, 5A/div

SMPS DELAYED STARTUP SEQUENCE (ON3 = REF)



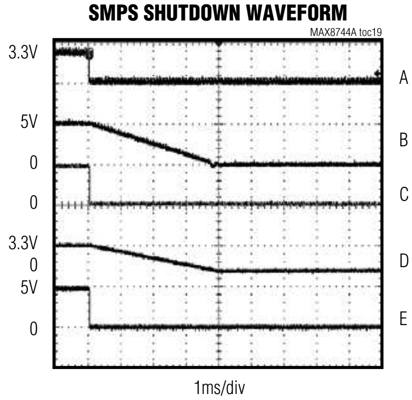
A. ON5, 5V/div
B. 5V OUTPUT (V_{OUT5}), 5V/div
C. PGOOD5, 5V/div
ON3 = REF
D. 3.3V OUTPUT (V_{OUT3}), 5V/div
E. PGOOD3, 5V/div

SMPS DELAYED STARTUP SEQUENCE (ON5 = REF)



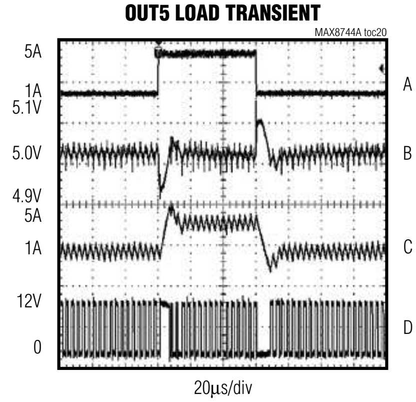
A. ON3, 5V/div
B. 5V OUTPUT (V_{OUT5}), 5V/div
C. PGOOD5, 5V/div
ON5 = REF
D. 3.3V OUTPUT (V_{OUT3}), 5V/div
E. PGOOD3, 5V/div

SMPS SHUTDOWN WAVEFORM



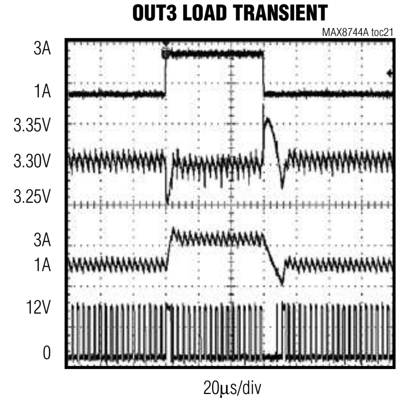
A. $\overline{SHDN}$, 5V/div
B. 5V OUTPUT (V_{OUT5}), 5V/div
C. PGOOD5, 5V/div
NO LOAD
D. 3.3V OUTPUT (V_{OUT3}), 5V/div
E. PGOOD3, 5V/div

OUT5 LOAD TRANSIENT



A. I_{OUT5} = 1A TO 5A, 5A/div
B. V_{OUT5}, 50mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX5, 10V/div

OUT3 LOAD TRANSIENT



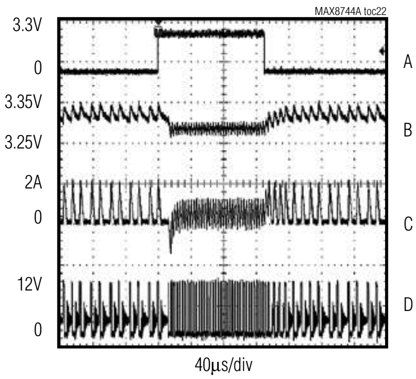
A. I_{OUT3} = 1A TO 3A, 5A/div
B. V_{OUT3}, 50mV/div
C. INDUCTOR CURRENT, 5A/div
D. LX3, 10V/div

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Typical Operating Characteristics (continued)

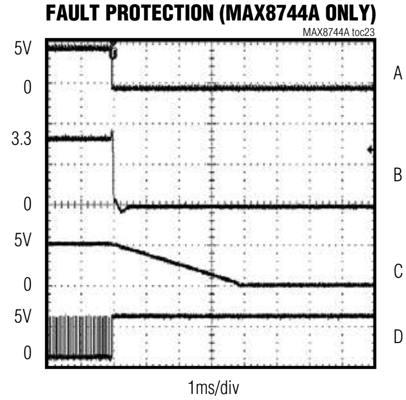
(Circuit of Figure 1, V_{IN} = 12V, $\overline{SKIP}$ = GND, FSEL = REF, T_A = +25°C, unless otherwise noted.)

$\overline{SKIP}$ TRANSITION



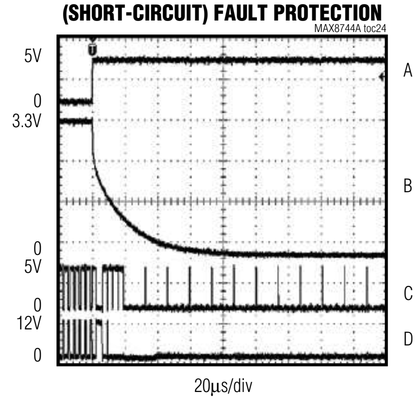
A. $\overline{SKIP}$, 5V/div
B. 3.3V OUTPUT (V_{OUT3}), 100mV/div
C. INDUCTOR CURRENT, 2A/div
D. LX3, 10V/div
0.5A LOAD

OUTPUT OVERVOLTAGE FAULT PROTECTION (MAX8744A ONLY)



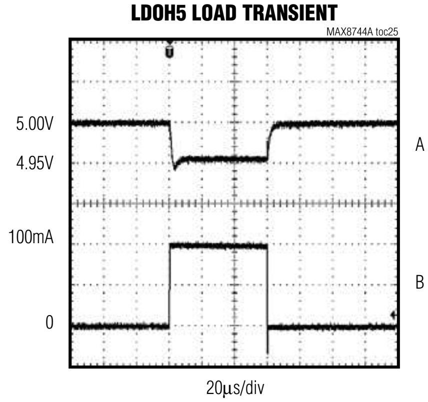
A. PGOOD3, 5V/div
B. 3.3V OUTPUT (V_{OUT3}), 2V/div
C. 5V OUTPUT (V_{OUT5}), 5V/div
D. DL3, 5V/div

OUTPUT UNDERVOLTAGE (SHORT-CIRCUIT) FAULT PROTECTION



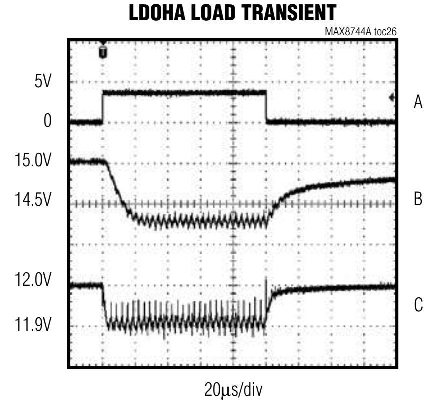
A. LOAD FET GATE, 5V/div
B. 3.3V OUTPUT (V_{OUT3}), 1V/div
C. DL3, 5V/div
D. DH3, 10V/div
30mΩ MOSFET

LDOH5 LOAD TRANSIENT



A. LDO5 OUTPUT, 50mV/div
B. LOAD CURRENT, 50mA/div

LDOHA LOAD TRANSIENT



A. LOAD FET GATE, 5V/div
B. AUX LDO INPUT, 0.5V/div
C. AUX LDO OUTPUT (V_{OUTA}), 0.1V/div
0 TO 150mA LOAD TRANSIENT

Pin Description

PIN	NAME	FUNCTION
1	ONA	Auxiliary LDO Enable Input. When ONA is pulled low, OUTA is high impedance and the secondary feedback control is disabled. When ONA is driven high, the controller enables the auxiliary LDO.
2	DRVA	Auxiliary LDO Transistor Base Driver. Connect DRVA to the base of a pnp power transistor. Add a 680Ω pullup resistor between the base and emitter.
3	ILIM	Peak Current-Limit Threshold Adjustment. The current-limit threshold defaults to 50mV if ILIM is pulled up to LDO5. In adjustable mode, the current-limit threshold across CSH_ and CSL_ is precisely 1/10 the voltage seen at ILIM over a 0.5V to 2.0V range. The logic threshold for switchover to the 50mV default value is approximately V_{LDO5} - 1V.
4	$\overline{\text{SHDN}}$	Shutdown Control Input. The device enters its 8µA supply-current shutdown mode if $V_{\overline{SHDN}}$ is less than the $\overline{\text{SHDN}}$ input falling edge trip level and does not restart until $V_{\overline{SHDN}}$ is greater than the $\overline{\text{SHDN}}$ input rising-edge trip level. Connect $\overline{\text{SHDN}}$ to V_{IN} for automatic startup. $\overline{\text{SHDN}}$ can be connected to V_{IN} through a resistive voltage-divider to implement a programmable undervoltage lockout.
5	ON3	3.3V SMPS Enable Input. Driving ON3 high enables the 3.3V SMPS, while pulling ON3 low disables the 3.3V SMPS. If ON3 is connected to REF, the 3.3V SMPS starts after the 5V SMPS reaches regulation (delayed start). Drive ON3 below the clear fault level to reset the fault latch.
6	ON5	5V SMPS Enable Input. Driving ON5 high enables the 5V SMPS, while pulling ON5 low disables the 5V SMPS. If ON5 is connected to REF, the 5V SMPS starts after the 3.3V SMPS reaches regulation (delayed start). Drive ON5 below the clear fault level to reset the fault latch.
7	REF	2.0V Reference Voltage Output. Bypass REF to analog ground with a 0.1µF or greater ceramic capacitor. The reference sources up to 50µA for external loads. Loading REF degrades output-voltage accuracy according to the REF load-regulation error. The reference shuts down when the system pulls $\overline{\text{SHDN}}$ low.
8	GND	Analog Ground. Connect the exposed backside pad to GND.
9	FSEL	Frequency Select Input. This three-level logic input sets the controllers' switching frequency. Connect to LDO5, REF, or GND to select the following typical switching frequencies: LDO5 = 500kHz, REF = 300kHz, GND = 200kHz.
10	$\overline{\text{SKIP}}$	Pulse-Skipping Control Input. Connect to LDO5 for low-noise, forced-PWM operation. Connect to REF for automatic, low-noise, pulse-skipping operation at light loads. Connect to GND for automatic, high-efficiency, pulse-skipping operation at light loads.
11	FB5	Feedback Input for the 5V SMPS. Connect to LDO5 for the preset 5V output. In adjustable mode, FB5 regulates to 2V.
12	CSH5	Positive Current-Sense Input for the 5V SMPS. Connect to the positive terminal of the current-sense element. Figure 7 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
13	CSL5	Output-Sense and Negative Current-Sense Input for the 5V SMPS. When using the internal preset 5V feedback-divider (FB5 = LDO5), the controller uses CSL5 to sense the output voltage. Connect to the negative terminal of the current-sense element. CSL5 also serves as the bootstrap input for LDO5.
14	PGOOD5	Open-Drain, Power-Good Output for the 5V SMPS. PGOOD5 is pulled low if CSL5 drops more than 10% (typ) below the normal regulation point. PGOOD5 is held low during soft-start and shutdown. PGOOD5 becomes high impedance when CSL5 is in regulation.

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Pin Description (continued)

PIN	NAME	FUNCTION
15	BST5	Boost Flying Capacitor Connection for the 5V SMPS. The MAX8744A/MAX8745A include an internal boost switch connected between LDO5 and BST5. Connect to an external capacitor as shown in Figure 1.
16	DH5	High-Side Gate-Driver Output for the 5V SMPS. DH5 swings from LX5 to BST5.
17	LX5	Inductor Connection for the 5V SMPS. Connect LX5 to the switched side of the inductor. LX5 serves as the lower supply rail for the DH5 high-side gate driver.
18	DL5	Low-Side Gate-Driver Output for the 5V SMPS. DL5 swings from PGND to LDO5.
19	PGND	Power Ground
20	LDO5	5V Internal Linear-Regulator Output. Bypass with 4.7µF minimum (1µF/25mA). Provides at least 100mA for the DL_ low-side gate drivers, the DH_ high-side drivers through the BST switches, the PWM controller, logic, reference, and external loads. If CSL5 is greater than 4.5V and soft-start is complete, the linear regulator shuts down, and LDO5 connects to CSL5 through a 1Ω switch rated for loads up to 200mA.
21	IN	Input of the Startup Circuitry and the LDO5 Internal 5V Linear Regulator. Bypass to PGND with a 0.22µF or greater ceramic capacitor close to the IC.
22	PGOODA	Open-Drain, Power-Good Output for the Auxiliary LDO. PGOODA is pulled low if FBA drops more than 10% (typ) below the normal regulation point, and when the auxiliary LDO is shut down. PGOODA becomes high impedance when FBA is in regulation.
23	DL3	Low-Side Gate-Driver Output for the 3.3V SMPS. DL3 swings from PGND to LDO5.
24	LX3	Inductor Connection for the 3.3V SMPS. Connect LX3 to the switched side of the inductor. LX3 serves as the lower supply rail for the DH3 high-side gate driver.
25	DH3	High-Side Gate-Driver Output for the 3.3V SMPS. DH3 swings from LX3 to BST3.
26	BST3	Boost Flying Capacitor Connection for the 3.3V SMPS. The MAX8744A/MAX8745A include an internal boost switch connected between LDO5 and BST3. Connect to an external capacitor as shown in Figure 1.
27	PGOOD3	Open-Drain, Power-Good Output for the 3.3V SMPS. PGOOD3 is pulled low if CSL3 drops more than 10% (typ) below the normal regulation point. PGOOD3 is held low during soft-start and shutdown. PGOOD3 becomes high impedance when CSL3 is in regulation.
28	CSL3	Output Sense and Negative Current Sense for the 3.3V SMPS. When using the internal preset 3.3V feedback divider (FB3 = LDO5), the controller uses CSL3 to sense the output voltage. Connect to the negative terminal of the current-sense element.
29	CSH3	Positive Current-Sense Input for the 3.3V SMPS. Connect to the positive terminal of the current-sense element. Figure 7 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
30	FB3	Feedback Input for the 3.3V SMPS. Connect to LDO5 for fixed 3.3V output. In adjustable mode, FB3 regulates to 2V.
31	FBA	Auxiliary LDO Feedback Input. Connect a resistive voltage-divider from OUTA to analog ground to adjust the auxiliary linear-regulator output voltage. FBA regulates at 1V.

Pin Description (continued)

PIN	NAME	FUNCTION
32	OUTA	Adjustable Auxiliary Linear-Regulator Output. Bypass OUTA to GND with 1µF or greater capacitor (1µF/25mA). When DRVA < OUTA, the secondary feedback control triggers the DL5 for 1µs forcing the controller to recharge the auxiliary storage capacitor. When DRVA exceeds 25V, the MAX8744A/MAX8745A enable a 10mA shunt on OUTA, preventing the storage capacitor from rising to unsafe levels due to the transformer's leakage inductance. Pulling ONA high enables the linear-regulator driver and the secondary feedback control.
EP	EP	Exposed Pad. **Connect the exposed backside pad to analog ground.**

Table 1. Component Selection for Standard Applications

COMPONENT	300kHz 5V AT 5A 3.3V AT 5A	500kHz 5V AT 3A 3.3V AT 5A
INPUT VOLTAGE	**V_{IN} = 7V TO 24V**	**V_{IN} = 7V TO 24V**
$C_{IN\_}$, Input Capacitor	(3) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(3) 10µF, 25V Taiyo Yuden TMK432BJ106KM
5V OUTPUT		
C_{OUT5}, Output Capacitor	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB
L5/T5 Inductor/Transformer	6.8µH, 6.4A, 18mΩ (max) 1:2 Sumida 4749-T132	—
N_{H5} High-Side MOSFET	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V
N_{L5} Low-Side MOSFET	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1
3V OUTPUT		
C_{OUT3}, Output Capacitor	2x 150µF, 4V, 35mΩ SANYO 4TPE150MAZB	2x 100µF, 6V, 35mΩ SANYO 6TPE100MAZB
L3, Inductor	5.8µH, 8.6A, 16.2mΩ Sumida CDRH127/LD-5R8NC	3.9µH, 6.5A, 15mΩ Sumida CDRH124-3R9NC
N_{H3} High-Side MOSFET	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V	Fairchild Semiconductor FDS6612A International Rectifier IRF7807V
N_{L3} Low-Side MOSFET	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1	Fairchild Semiconductor FDS6670S International Rectifier IRF7807VD1

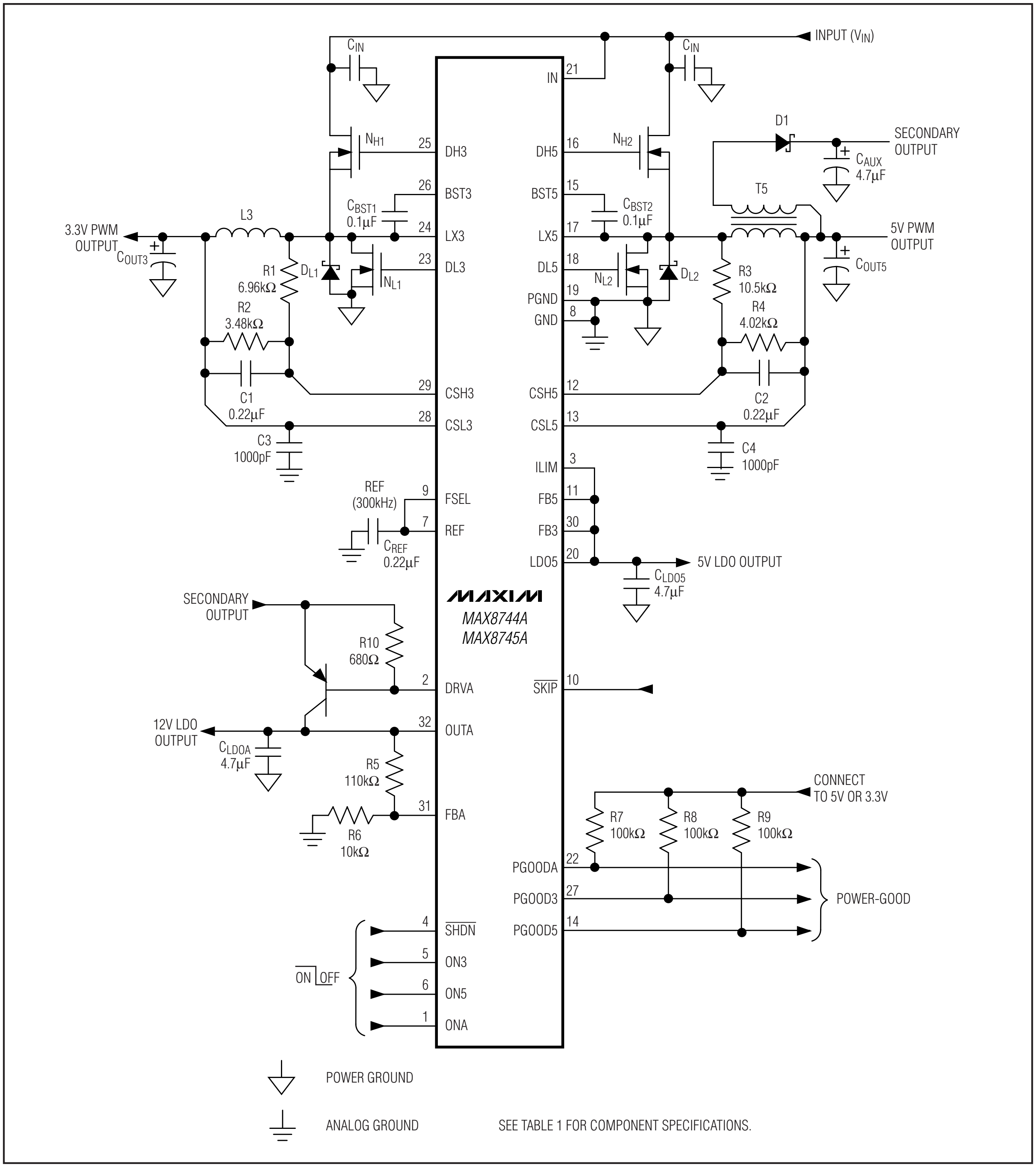


Figure 1. Standard Application Circuit

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX	www.avx.com
Central Semiconductor	www.centralsemi.com
Fairchild	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET	www.kemet.com
NEC/Tokin	www.nec-tokin.com
Panasonic	www.panasonic.com/industrial
Philips	www.philips.com
Pulse	www.pulseeng.com
Renesas	www.renesas.com
SANYO	www.edc.sanyo.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com

Detailed Description

The MAX8744A/MAX8745A standard application circuit (Figure 1) generates the 5V/5A and 3.3V/5A typical of the main supplies in a notebook computer. The input supply range is 7V to 24V. See Table 1 for component selections, while Table 2 lists the component manufacturers.

The MAX8744A/MAX8745A contain two interleaved, fixed-frequency, step-down controllers designed for low-voltage power supplies. The optimal interleaved architecture guarantees out-of-phase operation, reducing the input capacitor ripple. One internal LDO generates the keep-alive 5V power. The MAX8744A/MAX8745A have an auxiliary LDO with an adjustable output for generating either the 3.3V keep-alive supply or regulating the low-power 12V system supply.

Fixed 5V Linear Regulator (LDO5)

An internal linear regulator produces a preset 5V low-current output. LDO5 powers the gate drivers for the external MOSFETs, and provides the bias supply required for the SMPS analog controller, reference, and logic blocks. LDO5 supplies at least 100mA for external and internal loads, including the MOSFET gate drive, which typically varies from 5mA to 50mA, depending on the switching frequency and external MOSFETs selected. Bypass LDO5 with a 4.7µF or greater ceramic capacitor (1µF per 25mA of load) to guarantee stability under the full-load conditions.

The MAX8744A/MAX8745A switch-mode power supplies (SMPS) require a 5V bias supply in addition to the high-power input supply (battery or AC adapter). This 5V bias supply is generated by the controller's internal 5V linear regulator (LDO5). This bootstrapped LDO allows the controller to power up independently. The gate-driver input supply is connected to the fixed 5V linear-regulator output (LDO5). Therefore, the 5V LDO supply must provide LDO5 (PWM controller) and the gate-drive power, so the maximum supply current required is:

$$
\begin{aligned}
I_{BIAS} &= I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)}) \\
&= 5mA \text{ to } 50mA \text{ (typ)}
\end{aligned}
$$

where I_{CC} is 0.7mA (typ), f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

SMPS to LDO Bootstrap Switchover

When the 5V main output voltage is above the LDO5 bootstrap-switchover threshold and has completed soft-start, an internal 1Ω (typ) p-channel MOSFET shorts CSL5 to LDO5, while simultaneously shutting down the LDO5 linear regulator. This bootstraps the device, powering the internal circuitry and external loads from the 5V SMPS output (CSL5), rather than through the linear regulator from the battery. Bootstrapping reduces power dissipation due to gate charge and quiescent losses by providing power from a 90%-efficient switch-mode source, rather than from a much-less-efficient linear regulator. The current capability increases from 100mA to 200mA when the LDO5 output is switched over to CSL5. When ON5 is pulled low, the controller immediately disables the bootstrap switch and reenables the 5V LDO.

Reference (REF)

The 2V reference is accurate to ±1% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.1µF or greater ceramic capacitor. The reference sources up to 50µA and sinks 5µA to support external loads. If highly accurate specifications are required for the main SMPS output voltages, the reference should not be loaded. Loading the reference reduces the LDO5, CSL5 (OUT5), CSL3 (OUT3), and OUTA output voltages slightly because of the reference load-regulation error.

System Enable/Shutdown ($\overline{SHDN}$)

Drive $\overline{SHDN}$ below the precise $\overline{SHDN}$ input falling-edge trip level to place the MAX8744A/MAX8745A in its low-power shutdown state. The controller consumes only 8µA of quiescent current while in shutdown mode. When shutdown mode activates, the reference turns off after the controller completes the shutdown sequence

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

making the threshold to exit shutdown less accurate. To guarantee startup, drive $\overline{SHDN}$ above 2V ($\overline{SHDN}$ input rising-edge trip level). For automatic shutdown and startup, connect $\overline{SHDN}$ to V_{IN}. The accurate 1V falling-edge threshold on $\overline{SHDN}$ can be used to detect a specific input voltage level and shut the device down. Once in shutdown, the 1.6V rising-edge threshold activates, providing sufficient hysteresis for most applications.

SMPS POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when LDO5 rises above approximately 1V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. The POR circuit also ensures that the low-side drivers are pulled high until the SMPS controllers are activated. Figure 2 is the MAX8744A/MAX8745A block diagram.

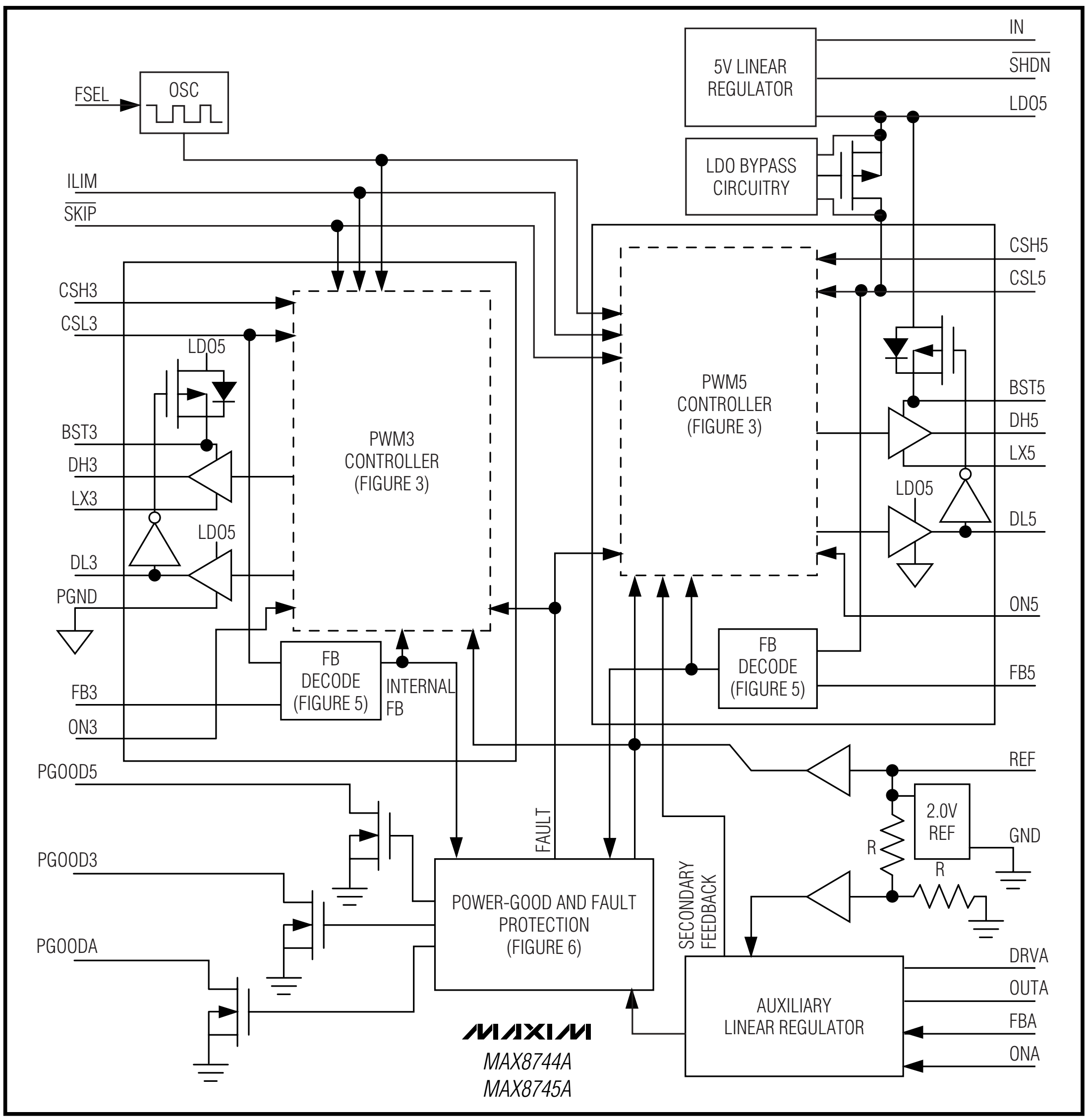


Figure 2. Block Diagram

Table 3. Operating Mode Truth Table

MODE	INPUTS*			OUTPUTS		
	$\overline{SHDN}$	ON5	ON3	LDO5	5V SMPS	3V SMPS
Shutdown Mode	Low	X	X	OFF	OFF	OFF
Standby Mode	High	Low	Low	ON	OFF	OFF
Normal Operation	High	High	High	ON	ON	ON
3.3V SMPS Active	High	Low	High	ON	OFF	ON
5V SMPS Active	High	High	Low	OFF LDO5 to CSL5 bypass switch enabled	ON	OFF
Normal Operation (Delayed 5V SMPS Startup)	High	Ref	High	OFF LDO5 to CSL5 bypass switch enabled	ON Power-up after 3.3V SMPS is in regulation	ON
Normal Operation (Delayed 3.3V SMPS Startup)	High	High	Ref	OFF LDO5 to CSL5 bypass switch enabled	ON	ON Power-up after 5V SMPS is in regulation

**$\overline{SHDN}$ is an accurate, low-voltage logic input with 1V falling-edge threshold voltage and 1.6V rising-edge threshold voltage. ON3 and ON5 are tri-level CMOS logic inputs, a logic-low voltage is less than 0.8V, a logic-high voltage is greater than 2.4V, and the middle-logic level is between 1.7V and 2.3V (see the* Electrical Characteristics *table).*

The LDO5 input undervoltage-lockout (UVLO) circuitry inhibits switching if the 5V bias supply (LDO5) is below its 4V UVLO threshold. Once the 5V bias supply (LDO5) rises above this input UVLO threshold and the SMPS controllers are enabled (ON_ driven high), the SMPS controllers start switching, and the output voltages begin to ramp up using soft-start. If the LDO5 voltage drops below the UVLO threshold, the controller stops switching and pulls the low-side gate drivers low until the LDO5 voltage recovers or drops below the POR threshold.

The internal soft-start gradually increases the feedback voltage with a 1V/ms slew rate. Therefore, the outputs reach their nominal regulation voltage 2ms after the SMPS controllers are enabled (see the Soft-Start Waveform in the *Typical Operating Characteristics*). This gradual slew rate effectively reduces the input surge current by minimizing the current required to charge the output capacitors ($I_{OUT} = I_{LOAD} + C_{OUT} \times V_{OUT(NOM)}/t_{SLEW}$).

SMPS Enable Controls (ON3, ON5)

ON3 and ON5 control SMPS power-up sequencing. ON3 or ON5 rising above 2.4V enables the respective outputs. ON3 or ON5 falling below 1.6V disables the respective outputs. Driving ON_ below 0.8V clears the overvoltage, undervoltage, and thermal fault latches.

SMPS Power-Up Sequencing

Connecting ON3 or ON5 to REF forces the respective outputs off while the other output is below regulation and starts after that output regulates. The second SMPS remains on until the first SMPS turns off, the device shuts down, a fault occurs, or LDO5 goes into UVLO. Both supplies begin their power-down sequence immediately when the first supply turns off.

Output Discharge (Soft-Shutdown)

When the switching regulators are disabled—when ON_ or $\overline{SHDN}$ is pulled low, or when an output undervoltage fault occurs—the internal soft-shutdown gradually decreases the feedback voltage with a 0.5V/ms slew rate. Therefore, the regulation voltage drops to 0V within 4ms after the SMPS controllers are disabled (see the SMPS Shutdown Waveform in the *Typical Operating Characteristics*). This slowly discharges the output capacitance, eliminating the negative output voltages caused by quickly discharging the output through the inductor and low-side MOSFET. When an SMPS target voltage discharges to 0.1V, its low-side driver (DL_) is forced high, clamping the respective SMPS output to GND. The reference remains active to provide an accurate threshold and to provide overvoltage protection. Both SMPS controllers contain separate soft-shutdown circuits.

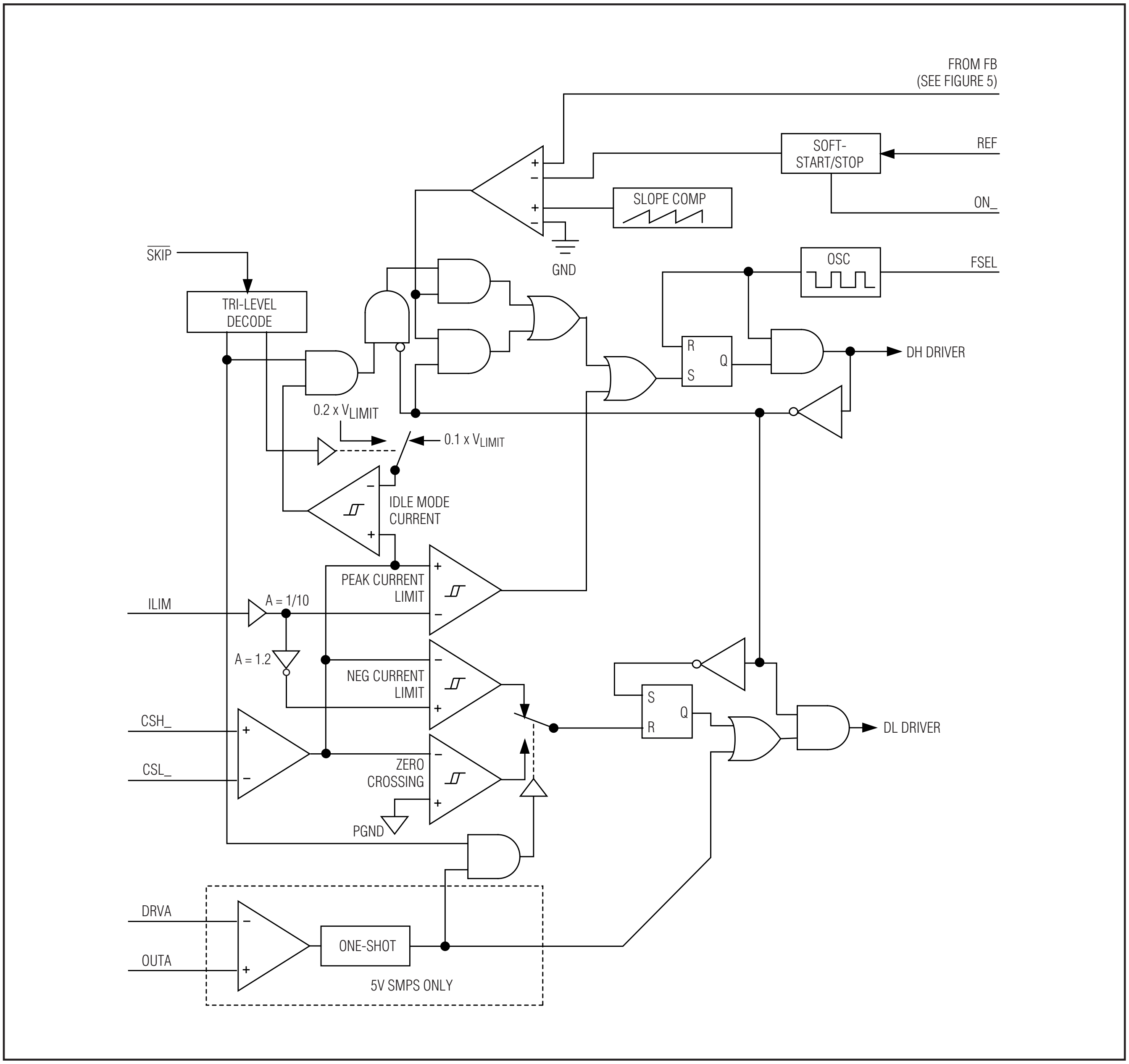


Figure 3. PWM Controller Functional Diagram

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums two signals: the output-voltage error signal with respect to the reference voltage and the slope-compensation ramp (Figure 3). The MAX8744A/MAX8745A use a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it.

Table 4. FSEL Configuration Table

FSEL	SWITCHING FREQUENCY (kHz)
LDO5	500
REF	300
GND	200

Frequency Selection (FSEL)

The FSEL input selects the PWM mode switching frequency. Table 4 shows the switching frequency based on FSEL connection. High-frequency (500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultraportable devices where the load currents are lower. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

Forced-PWM Mode

The low-noise forced-PWM mode ($\overline{SKIP}$ = LDO5) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to be constantly the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH_ maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V supply current remains between 20mA to 50mA, depending on the external MOSFETs and switching frequency.

Forced-PWM mode is most useful for avoiding audio-frequency noise and improving load-transient response. Since forced-PWM operation disables the zero-crossing comparator, the inductor current reverses under light loads.

Light-Load Operation Control ($\overline{SKIP}$)

The MAX8744A/MAX8745A include a light-load operating mode control input ($\overline{SKIP}$) used to enable or disable the zero-crossing comparator for both switching regulators. When the zero-crossing comparator is enabled, the regulator forces DL_ low when the current-sense inputs detect zero inductor current. This keeps the inductor from discharging the output capacitors and forces the regulator to skip pulses under light-load conditions to avoid overcharging the output. When the zero-crossing comparator is disabled, the regulator is forced to maintain PWM operation under light-load conditions (forced PWM).

Idle Mode Current-Sense Threshold

When pulse-skipping mode is enabled, the on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle mode current-sense threshold. Under light-load conditions, the on-time duration depends solely on the idle mode current-sense threshold, which is 20% ($\overline{SKIP}$ = GND) of the full-load current-limit threshold set by ILIM, or the low-noise current-sense threshold, which is 10% ($\overline{SKIP}$ = REF) of the full-load current-limit threshold set by ILIM. This forces the controller to source a minimum amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until the output voltage drops below the feedback threshold. Since the zero-crossing comparator prevents the switching regulator from sinking current, the controller must skip pulses. Therefore, the controller regulates the valley of the output ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads (Figure 4). This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current across CSH_ to CSL_. Once $V_{CSH\_}$ - $V_{CSL\_}$ drops below the 3mV zero-crossing, current-sense threshold, the comparator forces DL_ low (Figure 3). This mechanism causes the threshold between pulse-skipping PFM and nonskipping PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the "critical conduction" point). The load-current level at which PFM/PWM crossover occurs, $I_{LOAD(SKIP)}$, is given by:

$$I_{LOAD(SKIP)} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{2V_{IN}f_{OSC}L}$$

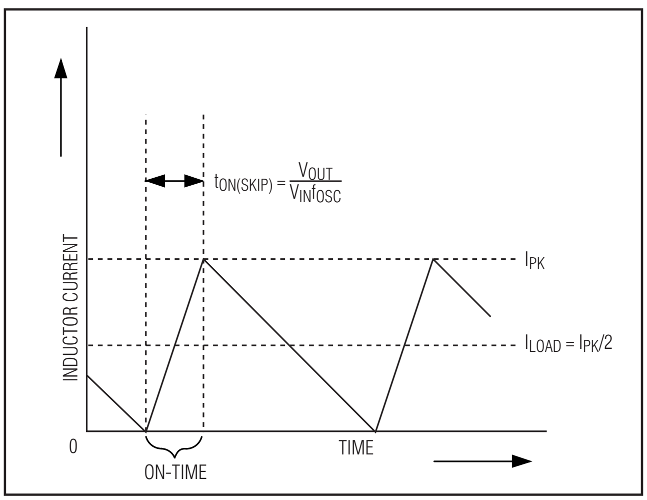


Figure 4. Pulse-Skipping/Discontinuous Crossover Point

The switching waveforms may appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output-voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

Output Voltage

DC output accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold. When the inductor continuously conducts, the MAX8744A/MAX8745A regulate the peak of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM}\left(1 - \frac{A_{SLOPE}V_{RIPPLE}}{V_{IN}}\right) - \left(\frac{V_{RIPPLE}}{2}\right)$$

where V_{NOM} is the nominal output voltage, A_{SLOPE} equals 1.1%, and V_{RIPPLE} is the output ripple voltage (V_{RIPPLE} = ESR x $\Delta I_{INDUCTOR}$, as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the MAX8744A/MAX8745A regulate the valley of the output ripple, so the output voltage has a DC regulation level higher than the error-comparator threshold. For PFM operation (discontinuous conduction), the output voltage is approximately defined by the following equation:

$$V_{OUT(PFM)} = V_{NOM} + \frac{1}{2}\left(\frac{f_{SW}}{f_{OSC}}\right)I_{IDLE}ESR$$

where V_{NOM} is the nominal output voltage, f_{OSC} is the maximum switching frequency set by the internal oscillator, f_{SW} is the actual switching frequency, and I_{IDLE} is the idle mode inductor current when pulse skipping.

Connect FB3 and FB5 to LDO5 to enable the fixed SMPS output voltages (3.3V and 5V, respectively), set by a preset, internal resistive voltage-divider connected between the output (CSL_) and analog ground. Connect a resistive voltage-divider at FB_ between the output (CSL_) and GND to adjust the respective output voltage between 2V and 5.5V (Figure 5). Choose R_{FBLO} (resistance from FB to GND) to be approximately 10kΩ

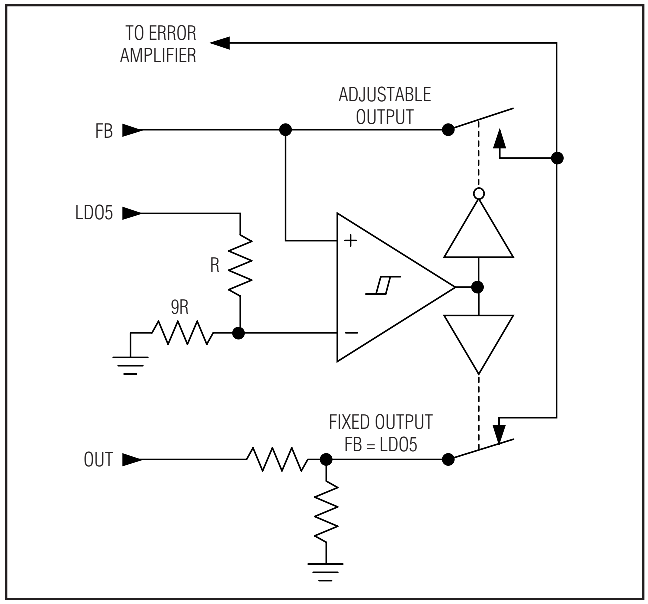


Figure 5. Dual Mode Feedback Decoder

and solve for R_{FBHI} (resistance from the output to FB) using the equation:

$$R_{FBHI} = R_{FBLO}\left(\frac{V_{OUT\_}}{V_{FB\_}} - 1\right)$$

where $V_{FB\_}$ = 2V nominal.

When adjusting both output voltages, set the 3.3V SMPS lower than the 5V SMPS. LDO5 connects to the 5V output (CSL5) through an internal switch only when CSL5 is above the LDO5 bootstrap threshold (4.5V) and the soft-start sequence for the CSL5 side has completed. Bootstrapping works most effectively when the fixed output voltages are used. Once LDO5 is bootstrapped from CSL5, the internal 5V linear regulator turns off. This reduces the internal power dissipation and improves efficiency at higher input voltages.

Current-Limit Protection (ILIM)

The current-limit circuit uses differential current-sense inputs (CSH_ and CSL_) to limit the peak inductor current. If the magnitude of the current-sense signal exceeds the current-limit threshold, the PWM controller turns off the high-side MOSFET (Figure 3). The actual maximum load current is less than the peak current-limit threshold by an amount equal to half of the inductor ripple current. Therefore, the maximum load capability is a function of the current-sense resistance, inductor value, switching frequency, and duty cycle (V_{OUT}/V_{IN}).

In forced-PWM mode, the MAX8744A/MAX8745A also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit and tracks the positive current limit when ILIM is adjusted.

Connect ILIM to LDO5 for the 50mV default threshold, or adjust the current-limit threshold with an external resistor-divider at ILIM. Use a 2µA to 20µA divider current for accuracy and noise immunity. The current-limit threshold adjustment range is from 50mV to 200mV. In the adjustable mode, the current-limit threshold voltage equals precisely 1/10 the voltage seen at ILIM. The logic threshold for switchover to the default value is approximately V_{LDO5} - 1V.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the differential current-sense signals seen by CSH_ and CSL_. Place the IC close to the sense resistor with short, direct traces, making a Kelvin-sense connection to the current-sense resistor.

MOSFET Gate Drivers (DH_, DL_)

The DH_ and DL_ drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate drivers (DH_) source and sink 2A, and the low-side gate drivers (DL_) source 1.7A and sink 3.3A. This ensures robust gate drive for high-current applications. The DH_ floating high-side MOSFET drivers are powered by charge pumps at BST_ while the DL_ synchronous-rectifier drivers are powered directly by the fixed 5V linear regulator (LDO5).

Adaptive dead-time circuits monitor the DL_ and DH_ drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead-time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. There must be a low-resistance, low-inductance path from the DL_ and DH_ drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX8744A/MAX8745A interprets the MOSFET gates as “off” while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL_ low is robust, with a 0.6Ω (typ) on-resistance. This helps prevent DL_ from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX_) quickly switches from ground to V_{IN}.

Applications with high input voltages and long inductive driver traces may require additional gate-to-source capacitance to ensure fast-rising LX_ edges do not pull up the low-side MOSFETs gate, causing shoot-through currents. The capacitive coupling between LX_ and DL_ created by the MOSFET’s gate-to-drain capacitance (C_{GD} = C_{RSS}), gate-to-source capacitance (C_{GS} = C_{ISS} - C_{GD}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Lot-to-lot variation of the threshold voltage may cause problems in marginal designs.

Power-Good Output (PGOOD_)

PGOOD_ is the open-drain output of a comparator that continuously monitors both SMPS output voltages and the auxiliary LDO output for undervoltage conditions. PGOOD_ is actively held low in shutdown ($\overline{SHDN}$ = GND), standby (ON3 = ON5 = ONA = GND), soft-start, and soft-shutdown. Once the soft-start sequence terminates, PGOOD_ becomes high impedance as long as the outputs are above 90% of the nominal regulation voltage set by FB_. PGOOD_ goes low once the respective output drops 10% below its nominal regulation point, an SMPS output overvoltage fault occurs, or ON_ or $\overline{SHDN}$ is low. For a logic-level PGOOD_ output voltage, connect an external pullup resistor between PGOOD_ and LDO5. A 100kΩ pullup resistor works well in most applications.

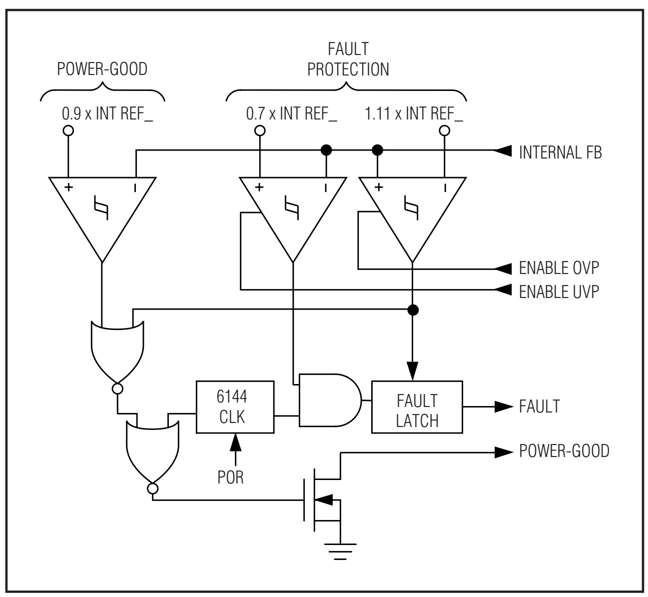


Figure 6. Power-Good and Fault Protection

High-Efficiency, Quad-Output, Main Power-Supply Controllers for Notebook Computers

Table 5. Operating Modes Truth Table

MODE	CONDITION	COMMENT
Power-Up	LDO5 < UVLO threshold	Transitions to discharge mode after V_{IN} POR and after REF becomes valid. LDO5, REF remain active. DL_ is active (high).
Run	$\overline{SHDN}$ = high, ON3 or ON5 enabled	Normal operation.
Output Overvoltage (OVP) Protection (MAX8744A)	Either output > 111% of nominal level	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.
Output Undervoltage Protection (UVP)	Either output < 70% of nominal level, UVP is enabled 6144 clock cycles ($1/f_{OSC}$) after the output is enabled	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.
Standby	ON5 and ON3 < startup threshold, $\overline{SHDN}$ = high	DL_ stays high. LDO5 active.
Shutdown	$\overline{SHDN}$ = low	All circuitry off.
Thermal Shutdown	T_J > +160°C	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5. DL3 and DL5 go high before LDO5 turns off. They remain high as long as possible thereafter.
Switchover Fault	Excessive current on LDO5 switchover transistors	Exited by POR or cycling $\overline{SHDN}$, ON3, or ON5.

Fault Protection

Output Overvoltage Protection (OVP)—MAX8744A Only

If the output voltage of either SMPS rises above 111% of its nominal regulation voltage and the OVP protection is enabled, the controller sets the fault latch, pulls PGOOD low, shuts down the SMPS controllers that tripped the fault, and immediately pulls DH_ low and forces DL_ high. This turns on the synchronous-rectifier MOSFETs with 100% duty, rapidly discharging the output capacitors and clamping both outputs to ground. However, immediately latching DL_ high typically causes slightly negative output voltages due to the energy stored in the output LC at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery blows. The other output is shut down using the soft-shutdown sequence. Cycle LDO5 below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the SMPS controllers.

Output Undervoltage Protection (UVP)

Each SMPS controller includes an output UVP protection circuit that begins to monitor the output 6144 clock cycles ($1/f_{OSC}$) after that output is enabled (ON_ pulled high). If either SMPS output voltage drops below 70% of its nominal regulation voltage and the UVP protection is enabled, the UVP circuit sets the fault latch, pulls PGOOD low, and shuts down both controllers using the soft-shutdown sequence. When an SMPS output voltage drops to 0.1V, its synchronous rectifier turns on, clamping the discharged output to GND. Cycle LDO5 below 1V or toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the SMPS controllers.

Thermal-Fault Protection

The MAX8744A/MAX8745A feature a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, and shuts down both SMPS controllers using the soft-shutdown sequence. When an SMPS output voltage drops to 0.1V, its synchronous rectifier turns on, clamping the discharged output to GND. Toggle either ON3, ON5, or $\overline{SHDN}$ to clear the fault latch and restart the controllers after the junction temperature cools by 15°C.

Auxiliary LDO Detailed Description

The MAX8744A/MAX8745A include an auxiliary linear regulator (OUTA) that can be configured for 12V, ideal for PCMCIA power requirements, and for biasing the gates of load switches in a portable device. OUTA can also be configured for outputs from 1V to 23V. The auxiliary regulator has an independent ON/OFF control, allowing it to be shut down when not needed, reducing power consumption when the system is in a low-power state.

A flyback-winding control loop regulates a secondary winding output, improving cross-regulation when the primary output is lightly loaded or when there is a low input-output differential voltage. If $V_{DRVA} < V_{OUTA}$, the low-side switch is turned on for a time equal to 33% of the switching period. This reverses the inductor (primary) current, pulling current from the output filter capacitor and causing the flyback transformer to operate in forward mode. The low impedance presented by the transformer secondary in forward mode dumps current into the secondary output, charging up the secondary capacitor and bringing V_{INA} - V_{OUTA} back into regulation. The secondary feedback loop does not improve secondary output accuracy in normal flyback mode, where the main (primary) output is heavily loaded. In this condition, secondary output accuracy is determined by the secondary rectifier drop, transformer turns ratio, and accuracy of the main output voltage.

SMPS Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high AC-adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point.** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping ($\overline{SKIP}$ low and light loads), the inductor value also determines the load-current value at which PFM/PWM switchover occurs.

Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}\left(V_{IN} - V_{OUT}\right)}{V_{IN} f_{OSC} I_{LOAD(MAX)} LIR}$$

For example: $I_{LOAD(MAX)}$ = 5A, V_{IN} = 12V, V_{OUT} = 5V, f_{OSC} = 300kHz, 30% ripple current or LIR = 0.3:

$$L = \frac{5V \times \left(12V - 5V\right)}{12V \times 300kHz \times 5A \times 0.3} = 6.50\mu H$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for non-standard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{OSC} L}$$