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EVALUATION KIT AVAILABLE

Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

General Description

The MAX8760 is a dual-phase, Quick-PWM™, step-down controller for 6-bit VID AMD Mobile Turion™ 64 CPU core supplies. Dual-phase operation reduces input ripple current requirements and output voltage ripple while easing component selection and layout difficulties. The Quick-PWM control scheme provides instantaneous response to fast-load current steps. The MAX8760 includes active voltage positioning with adjustable gain and offset, reducing power dissipation and bulk output capacitance requirements.

The MAX8760 is intended for two different notebook CPU core applications: stepping down the battery directly or stepping down the 5V system supply to create the core voltage. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at a higher switching frequency provides the minimum possible physical size.

The MAX8760 complies with AMD's desktop and mobile CPU specifications. The switching regulator features soft-start and power-up sequencing, and soft-shutdown. The MAX8760 also features independent four-level logic inputs for setting the suspend voltage (S0, S1).

The MAX8760 includes output undervoltage protection, thermal protection, and voltage regulator power-OK (VROK) output. When any of these protection features detect a fault, the controller shuts down.

The MAX8760 is available in a low-profile, 40-pin 6mm x 6mm thin QFN package. For other CPU platforms, refer to the pin-to-pin compatible MAX1544, MAX1519/MAX1545, and MAX1532/MAX1546/MAX1547 data sheets.

Applications

6-Bit VID AMD Mobile Turion 64 CPU

Multiphase CPU Core Supply

Voltage-Positioned Step-Down Converters

Servers/Desktop Computers

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Turion is a trademark of AMD.

Features

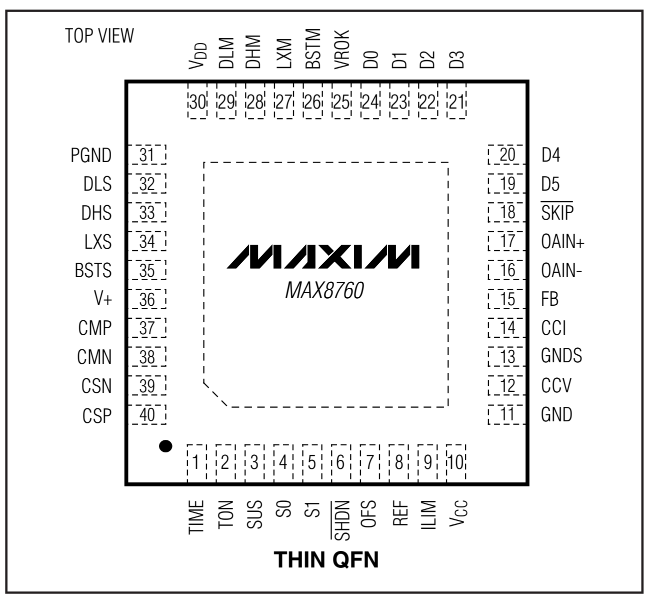
- ♦ Dual-Phase, Quick-PWM Controller
- ♦ ±0.75% V_{OUT} Accuracy Over Line, Load, and Temperature (1.3V)
- ♦ Active Voltage Positioning with Adjustable Gain and Offset
- ♦ 6-Bit On-Board DAC: 0.375V to 1.55V Output Adjust Range
- ♦ Selectable 100kHz/200kHz/300kHz/550kHz Switching Frequency
- ♦ 4V to 28V Battery Input Voltage Range
- ♦ Adjustable Slew-Rate Control
- ♦ Drives Large Synchronous Rectifier MOSFETs
- ♦ Undervoltage and Thermal-Fault Protection
- ♦ Power Sequencing and Timing
- ♦ Selectable Suspend Voltage
- ♦ Soft-Start and Soft-Shutdown
- ♦ Selectable Single- or Dual-Phase Pulse Skipping

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8760ETL	-40°C to +100°C	40 Thin QFN 6mm x 6mm
MAX8760ETL+	-40°C to +100°C	40 Thin QFN 6mm x 6mm

+Denotes lead-free package.

Pin Configuration



Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V+ to GND ....-0.3V to +30V
V_{CC} to GND ....-0.3V to +6V
V_{DD} to PGND ....-0.3V to +6V
$\overline{SKIP}$, SUS, D0–D5 to GND ....-0.3V to +6V
ILIM, FB, OFS, CCV, CCI, REF, OAIN+,
OAIN- to GND ....-0.3V to (V_{CC} + 0.3V)
CMP, CSP, CMN, CSN, GNDS to GND ......-0.3V to (V_{CC} + 0.3V)
TON, TIME, VROK, S0–S1 to GND ....-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 1) ....-0.3V to +18V
DLM, DLS to PGND ....-0.3V to (V_{DD} + 0.3V)
BSTM, BSTS to GND ....-0.3V to +36V
DHM to LXM ....-0.3V to (V_{BSTM} + 0.3V)
LXM to BSTM ....-6V to +0.3V
DHS to LXS ....-0.3V to (V_{BSTS} + 0.3V)
LXS to BSTS ....-6V to +0.3V
GND to PGND ....-0.3V to +0.3V
REF Short-Circuit Duration ....Continuous
Continuous Power Dissipation (T_A = +70°C)
40-Pin 6mm × 6mm Thin QFN
(derate 23.2mW/°C above +70°C) 1.860W
Operating Temperature Range ....-40°C to +100°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: $\overline{SHDN}$ may be forced to 12V for the purpose of debugging prototype boards using the no-fault test mode, which disables fault protection and overlapping operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		Battery voltage, V+		4		28	V
		V_{CC}, V_{DD}		4.5		5.5	
DC Output Voltage Accuracy (Note 2)		V+ = 4.5V to 28V, includes load regulation error	DAC codes ≥ 1V	-10		+10	mV
			DAC codes from 0.375V to 1V	-15		+15	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V+ = 4.5V to 28V			5		mV
Input Bias Current	I_{FB}, I_{GNDS}	FB, GNDS		-2		+2	µA
	I_{OFS}	OFS		-0.1		+0.1	
OFS Input Range				0		2	V
OFS Gain	A_{OFS}	$\Delta V_{OUT}/\Delta V_{OFS}$; ΔV_{OFS} = V_{OFS}, V_{OFS} = 0 to 1V		-0.129	-0.125	-0.117	V/V
		$\Delta V_{OUT}/\Delta V_{OFS}$; ΔV_{OFS} = V_{OFS} - V_{REF}, V_{OFS} = 1V to 2V		-0.129	-0.125	-0.117	
GNDS Input Range				-20		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	0.99	1.01	V/V
TIME Frequency Accuracy	f_{TIME}	1000kHz nominal, R_{TIME} = 15kΩ		900	1000	1100	kHz
		500kHz nominal, R_{TIME} = 30kΩ		460	500	540	
		250kHz nominal, R_{TIME} = 60kΩ		225	250	275	
		Startup and shutdown, R_{TIME} = 30kΩ			125		

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time (Note 3)	t_{ON}	V+ = 12V, V_{FB} = V_{CCI} = 1.2V	TON = GND (550kHz)	155	180	205	ns
			TON = REF (300kHz)	320	355	390	
			TON = open (200kHz)	475	525	575	
			TON = V_{CC} (100kHz)	920	1000	1140	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	TON = GND			300	375	ns
		TON = V_{CC}, open, or REF			400	480	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point, OAIN- = FB, V_{OAIN+} = 1.3V			1.70	3.20	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			<1	5	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+			25	40	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			4	10	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND			<1	5	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0V or 5V			<1	5	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.990	2.000	2.010	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -10µA to 100µA		-10		+10	mV
FAULT PROTECTION							
Output Overvoltage Protection Threshold	V_{OVP}				2.00		V
Output Overvoltage Propagation Delay	t_{OVP}	FB forced 2% above trip threshold			10		µs
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		67	70	73	%
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 2% below trip threshold			10		µs
VROK Threshold		Measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-12	-10	-8	%
			Upper threshold (overvoltage) $\overline{SKIP}$ = V_{CC}	+8	+10	+12	

Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage Fault and VROK Transition Blanking Time	t_{BLANK}	Measured from the time when FB reaches the voltage set by the DAC code; clock speed set by R_{TIME} (Note 4)			24		Clks
VROK Startup Delay		Measured from the time when FB first reaches the voltage set by the DAC code after startup		3	5	7	ms
VROK Delay	t_{VROK}	FB forced 2% outside the VROK trip threshold			10		µs
VROK Output Low Voltage		I_{SINK} = 3mA				0.4	V
VROK Leakage Current		High state, VROK forced to 5.5V				1	µA
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 90mV, PWM disabled below this level		4.0	4.25	4.4	V
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 10°C			+160		°C
CURRENT LIMIT AND BALANCE							
Current-Limit Threshold Voltage (Positive, Default)	V_{LIMIT}	CMP - CMN, CSP - CSN; ILIM = V_{CC}		28	30	32	mV
Current-Limit Threshold Voltage (Positive, Adjustable)	V_{LIMIT}	CMP - CMN, CSP - CSN	V_{ILIM} = 0.2V	8	10	12	mV
			V_{ILIM} = 1.5V	73	75	77	
Current-Limit Threshold Voltage (Negative)	$V_{LIMIT(NEG)}$	CMP - CMN, CSP - CSN; ILIM = V_{CC}, $\overline{SKIP}$ = V_{CC}		-41	-36	-31	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	CMP - CMN, CSP - CSN; $\overline{SKIP}$ = GND			1.5		mV
CMP, CMN, CSP, CSN Input Ranges				0		2	V
CMP, CMN, CSP, CSN Input Current		V_{CSP} = V_{CSN} = 0 to 5V		-2		+2	µA
Secondary Driver-Disable Threshold	V_{CSP}			3	V_{CC} - 1	V_{CC} - 0.4	V
ILIM Input Current	I_{ILIM}	V_{ILIM} = 0 to 5V			0.1	200	nA
Current-Limit Default Switchover Threshold	V_{ILIM}			3	V_{CC} - 1	V_{CC} - 0.4	V
Current-Balance Offset	$V_{OS(IBAL)}$	(V_{CMP} - V_{CMN}) - (V_{CSP} - V_{CSN}); I_{CCI} = 0, -20mV < (V_{CMP} - V_{CMN}) < 20mV, 1.0V < V_{CCI} < 2.0V		-2		+2	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Current-Balance Transconductance	$G_{m(IBAL)}$				400		µS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V			1.0	4.5	Ω
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			1.0	4.5	Ω
		Low start (pulldown)			0.4	2	
DH_ Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			1.6		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 5V			4		A
DL_ Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			1.6		A
Dead Time	t_{DEAD}	DL_ rising			35		ns
		DH_ rising			26		
VOLTAGE-POSITIONING AMPLIFIER							
Input Offset Voltage	V_{OS}			-1		+1	mV
Input Bias Current	I_{BIAS}	OAIN+, OAIN-			0.1	200	nA
Op Amp Disable Threshold	V_{OAIN-}			3	V_{CC} - 1	V_{CC} - 0.4	V
Common-Mode Input Voltage Range	V_{CM}	Guaranteed by CMRR test		0		2.5	V
Common-Mode Rejection Ratio	CMRR	V_{OAIN+} = V_{OAIN-} = 0 to 2.5V		70	115		dB
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V		75	100		dB
Large-Signal Voltage Gain	A_{OA}	R_L = 1kΩ to V_{CC}/2		80	112		dB
Output Voltage Swing		$\lvert V_{OAIN+} - V_{OAIN-} \rvert \geq$ 10mV, R_L = 1kΩ to V_{CC}/2	V_{CC} - V_{FBH}		77	300	mV
			V_{FBL}		47	200	
Input Capacitance					11		pF
Gain-Bandwidth Product					3		MHz
Slew Rate					0.3		V/µs
Capacitive-Load Stability		No sustained oscillations			400		pF
LOGIC AND I/O							
$\overline{SHDN}$ Input High Voltage	V_{IH}			0.8			V
$\overline{SHDN}$ Input Low Voltage	V_{IL}					0.4	V
$\overline{SHDN}$ No-Fault Threshold	$V_{\overline{SHDN}}$	To enable no-fault mode		12		15	V
Three-Level Input Logic Levels		SUS, $\overline{SKIP}$	High	2.7			V
			REF	1.2		2.3	
			Low			0.8	
Logic Input Current		$\overline{SHDN}$, $\overline{SKIP}$, SUS		-1		+1	µA
D0–D5 Logic Input High Voltage				1.6			V

Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, $V_{CC} = V_{DD} = V_{\overline{SHDN}} = V_{\overline{SKIP}} = V_{S0} = V_{S1}$ = 5V, $V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN}$ = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
D0–D5 Logic Input Low Voltage						0.8	V
D0–D5 Input Current		D0–D5		-2		+2	µA
Four-Level Input Logic Levels		TON, S0 and S1	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.4	
Four-Level Input Current		TON, S0 and S1 forced to GND or V_{CC}		-3		+3	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, $V_{CC} = V_{DD} = V_{\overline{SHDN}} = V_{\overline{SKIP}} = V_{S0} = V_{S1}$ = 5V, $V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN}$ = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range		Battery voltage, V+		4	28	V
		V_{CC}, V_{DD}		4.5	5.5	
DC Output Voltage Accuracy (Note 2)		V+ = 4.5V to 28V, includes load regulation error	DAC codes ≥ 1V	-13	+13	mV
			DAC codes from 0.375V to 1V	-20	+20	
OFS Input Range				0	2	V
OFS GAIN	A_{OFS}	$\Delta V_{OUT}/\Delta V_{OFS}$; $\Delta V_{OFS} = V_{OFS}$, V_{OFS} = 0 to 1V		-0.131	-0.115	V/V
		$\Delta V_{OUT}/\Delta V_{OFS}$; $\Delta V_{OFS} = V_{OFS} - V_{REF}$, V_{OFS} = 1V to 2V		-0.131	-0.115	
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.94	1.01	V/V
TIME Frequency Accuracy	f_{TIME}	1000kHz nominal, R_{TIME} = 15kΩ		880	1120	kHz
		500kHz nominal, R_{TIME} = 30kΩ		450	550	
		250kHz nominal, R_{TIME} = 60kΩ		220	280	
On-Time (Note 3)	t_{ON}	V+ = 12V, $V_{FB} = V_{CCI}$ = 1.2V	TON = GND (550kHz)	150	210	ns
			TON = REF (300kHz)	315	395	
			TON = open (200kHz)	470	580	
			TON = V_{CC} (100kHz)	910	1150	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	TON = GND			380	ns
		TON = V_{CC}, open, or REF			490	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = $V_{\overline{SKIP}}$ = V_{S0} = V_{S1} = 5V, V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN} = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
BIAS AND REFERENCE						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point, OAIN- = FB, V_{OAIN+} = 1.3V			3.2	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point			20	µA
Quiescent Battery Supply Current (V+)	I_{V+}	Measured at V+			50	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			20	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND			20	µA
Shutdown Battery Supply Current (V+)		Measured at V+, $\overline{SHDN}$ = GND, V_{CC} = V_{DD} = 0V or 5V			20	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.985	2.015	V
FAULT PROTECTION						
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		67	73	%
VROK Threshold		Measured at FB with respect to unloaded output voltage	Lower threshold (undervoltage)	-13	-7	%
			Upper threshold (overvoltage), $\overline{SKIP}$ = V_{CC}	+7	+13	
VROK Startup Delay		Measured from the time when FB first reaches the voltage set by the DAC code after startup		3		ms
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, hysteresis = 90mV, PWM disabled below this level		3.90	4.45	V
CURRENT LIMIT AND BALANCE						
Current-Limit Threshold Voltage (Positive, Default)	V_{LIMIT}	CMP - CMN, CSP - CSN; ILIM = V_{CC}		27	33	mV
Current-Limit Threshold Voltage (Positive, Adjustable)	V_{LIMIT}	CMP - CMN, CSP - CSN	V_{ILIM} = 0.2V	7	13	mV
			V_{ILIM} = 1.5V	72	78	
Current-Limit Threshold Voltage (Negative)	$V_{LIMIT(NEG)}$	CMP - CMN, CSP - CSN; ILIM = V_{CC}, $\overline{SKIP}$ = V_{CC}		-30	-42	mV
Current-Balance Offset	$V_{OS(IBAL)}$	(V_{CMP} - V_{CMN}) - (V_{CSP} - V_{CSN}); I_{CCI} = 0, -20mV < (V_{CMP} - V_{CMN}) < 20mV, 1.0V < V_{CCI} < 2.0V		-3	+3	mV
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V			4.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, $V_{CC} = V_{DD} = V_{\overline{SHDN}} = V_{\overline{SKIP}} = V_{S0} = V_{S1}$ = 5V, $V_{FB} = V_{CMP} = V_{CMN} = V_{CSP} = V_{CSN}$ = 1.3V, OFS = SUS = GNDS = D0–D5 = GND, **T_A = -40°C to +100°C**, unless otherwise specified.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			4.5	Ω
		Low start (pulldown)			2	
VOLTAGE-POSITIONING AMPLIFIER						
Input Offset Voltage	V_{OS}			-2.0	+2.0	mV
Common-Mode Input Voltage Range	V_{CM}	Guaranteed by CMRR test		0	2.5	V
Output Voltage Swing		$\lvert V_{OAIN+} - V_{OAIN-} \rvert \geq$ 10mV, R_L = 1kΩ to V_{CC}/2	$V_{CC} - V_{FBH}$		300	mV
			V_{FBL}		200	
LOGIC AND I/O						
$\overline{SHDN}$ Input High Voltage	V_{IH}			0.8		V
$\overline{SHDN}$ Input Low Voltage	V_{IL}				0.4	V
Tri-Level Input Logic Levels		SUS, $\overline{SKIP}$	High	2.7		V
			REF	1.2	2.3	
			Low		0.8	
D0–D5 Logic Input High Voltage				1.6		V
D0–D5 Logic Input Low Voltage					0.8	V
Four-Level Input Logic Levels		TON, S0 and S1	High	V_{CC} - 0.4		V
			Open	3.15	3.85	
			REF	1.65	2.35	
			Low		0.4	

Note 2: DC output accuracy specifications refer to the trip level of the error amplifier. When pulse skipping, the output slightly rises (<0.5%) when transitioning from continuous conduction to no load.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DHM and DHS pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

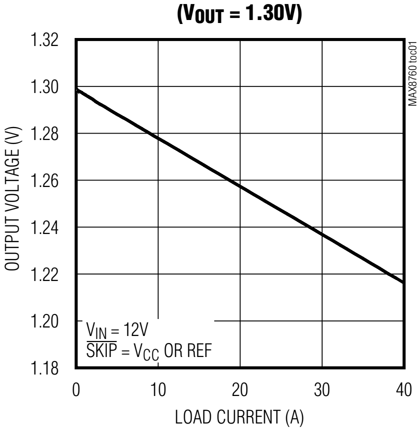
Note 4: The output fault-blanking time is measured from the time when FB reaches the regulation voltage set by the DAC code. During normal operation (SUS = GND), the regulation voltage is set by the VID DAC inputs (D0–D5). During suspend mode (SUS = REF or high), the regulation voltage is set by the suspend DAC inputs (S0 and S1).

Note 5: Specifications to T_A = -40°C and +100°C are guaranteed by design and are not production tested.

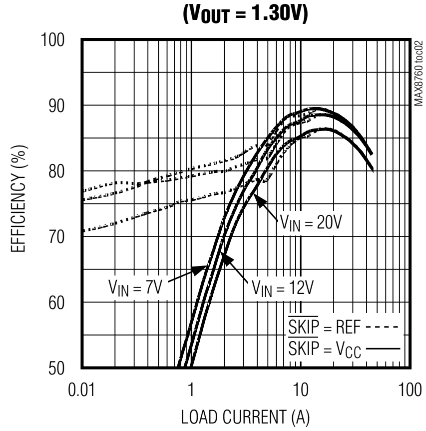
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D5 set for 1.5V (SUS = GND), S0 and S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

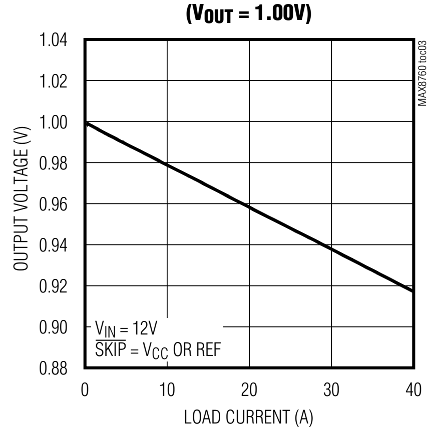
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.30V)



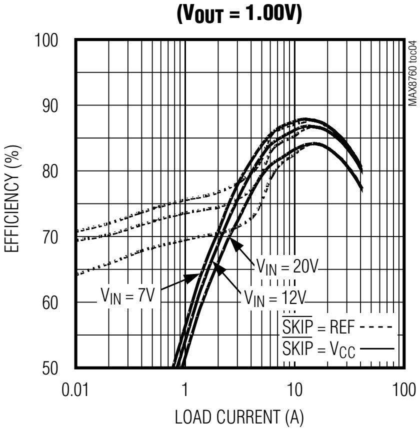
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.30V)



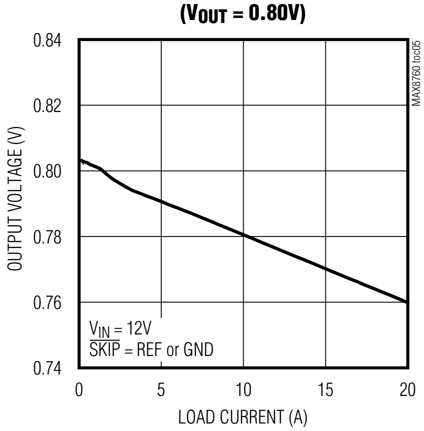
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.00V)



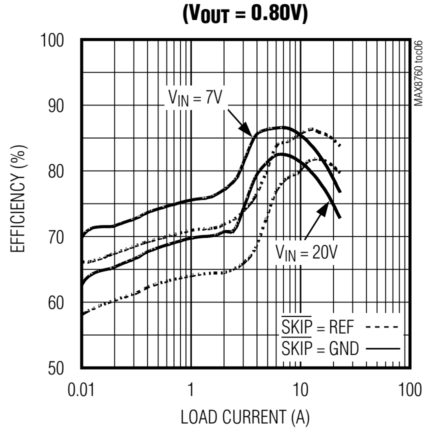
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.00V)



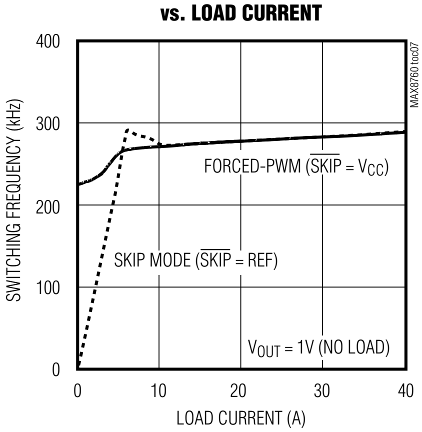
OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.80V)



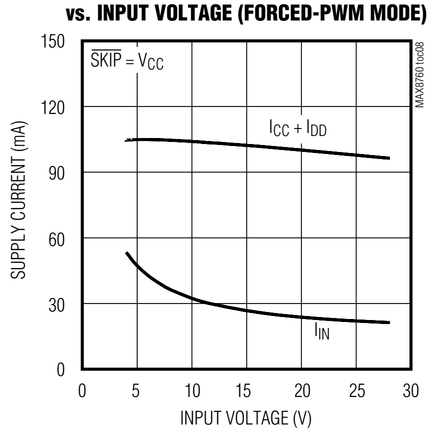
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.80V)



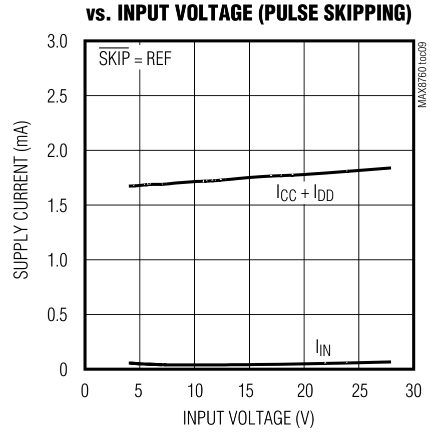
SWITCHING FREQUENCY vs. LOAD CURRENT



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (FORCED-PWM MODE)



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PULSE SKIPPING)

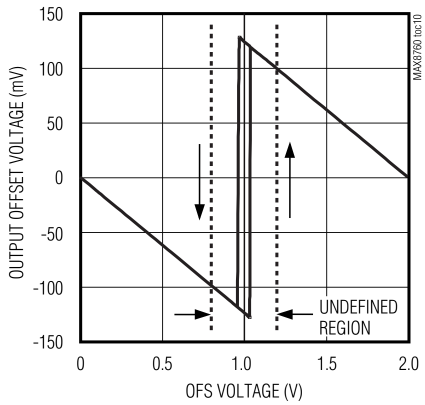


Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

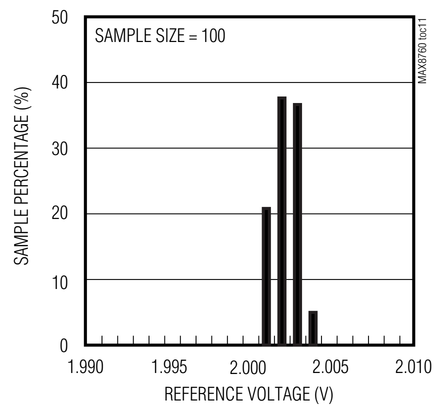
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D5 set for 1.5V (SUS = GND), S0 and S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

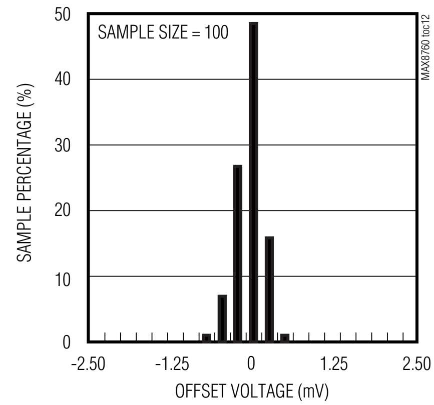
OUTPUT OFFSET VOLTAGE vs. OFS VOLTAGE



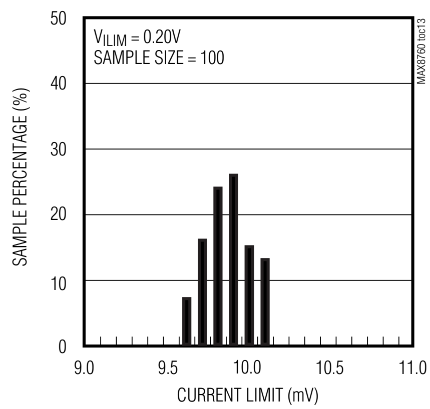
REFERENCE VOLTAGE DISTRIBUTION



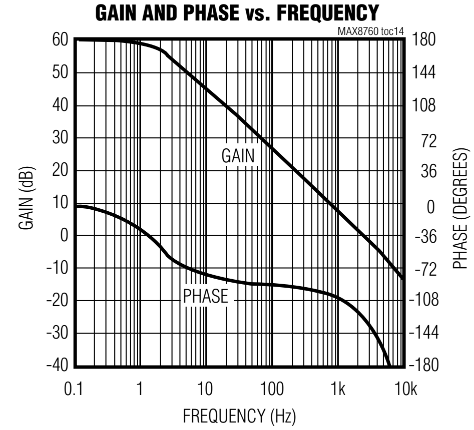
CURRENT-BALANCE OFFSET VOLTAGE DISTRIBUTION



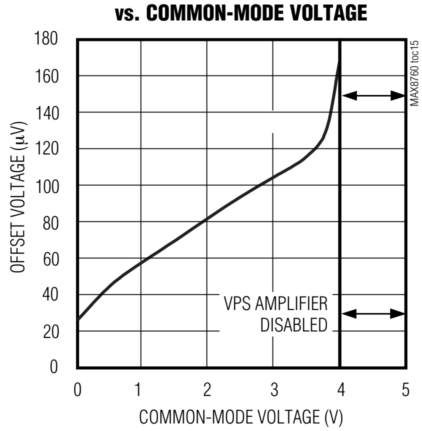
CURRENT-LIMIT THRESHOLD DISTRIBUTION



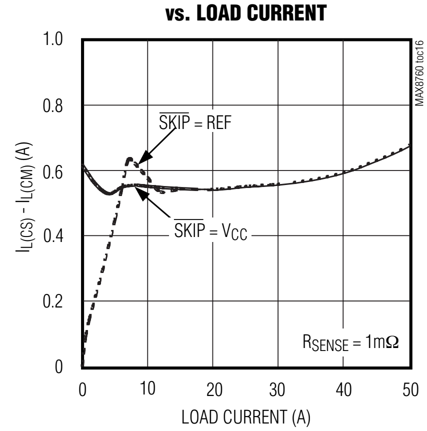
VOLTAGE-POSITIONING AMPLIFIER GAIN AND PHASE vs. FREQUENCY



VPS AMPLIFIER OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



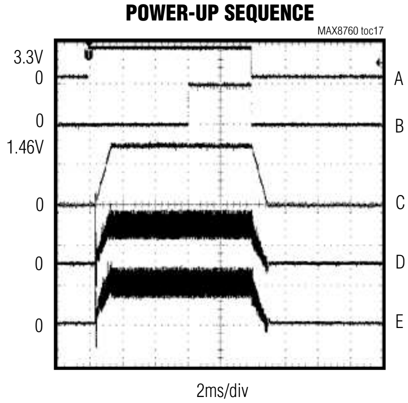
INDUCTOR CURRENT DIFFERENCE vs. LOAD CURRENT



Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D5 set for 1.5V (SUS = GND), S0 and S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

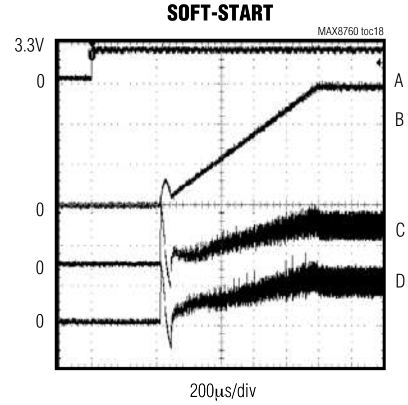
POWER-UP SEQUENCE



A. $\overline{SHDN}$, 5V/div
B. VROK, 5V/div
C. 1.5V OUTPUT, 1V/div
D. I_{L1}, 10A/div
E. I_{L2}, 10A/div

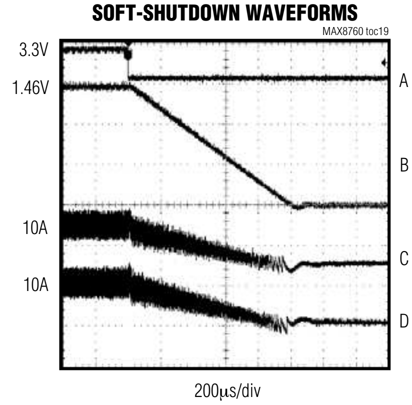
R_{LOAD} = 75mΩ

SOFT-START



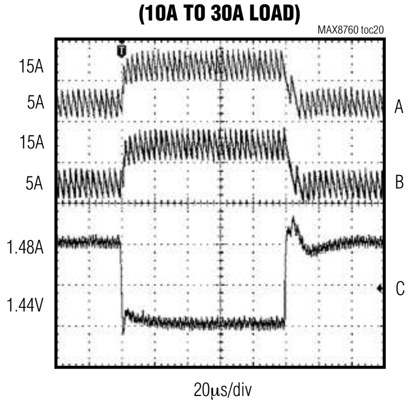
A. $\overline{SHDN}$, 5V/div
B. 1.5V OUTPUT, 500mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
R_{LOAD} = 75mΩ

SOFT-SHUTDOWN WAVEFORMS



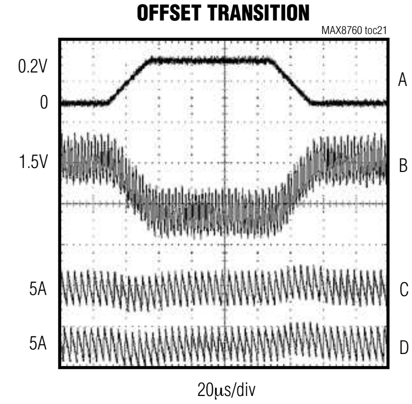
A. $\overline{SHDN}$, 5V/div
B. 1.5V OUTPUT, 500mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
R_{LOAD} = 75mΩ

1.30V LOAD TRANSIENT (10A TO 30A LOAD)



A. I_{L1}, 10A/div
B. I_{L2}, 10A/div
C. OUTPUT VOLTAGE, 20mV/div

OFFSET TRANSITION



A. V_{OFS} = 0 TO 200mV, 0.2V/div
B. V_{OUT} = 1.500V TO 1.475V, 20mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
10A LOAD

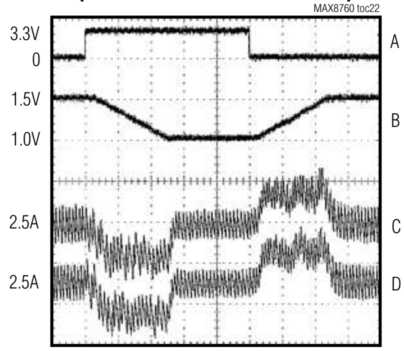
Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D5 set for 1.5V (SUS = GND), S0 and S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

SUSPEND TRANSITION (DUAL-PHASE PWM OPERATION)

MAX8760 toc22

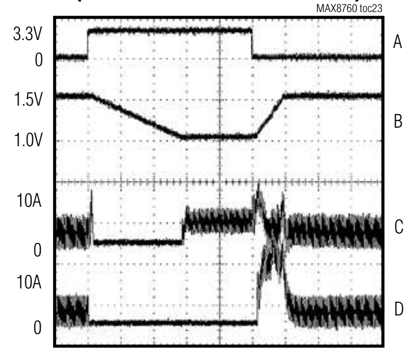


40µs/div

A. SUS, 5V/div
B. V_{OUT} = 1.5V TO 1.0V, 0.5V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
5A LOAD, $\overline{SKIP}$ = V_{CC}, R_{TIME} = 64.9kΩ

SUSPEND TRANSITION (SINGLE-PHASE SKIP OPERATION)

MAX8760 toc23

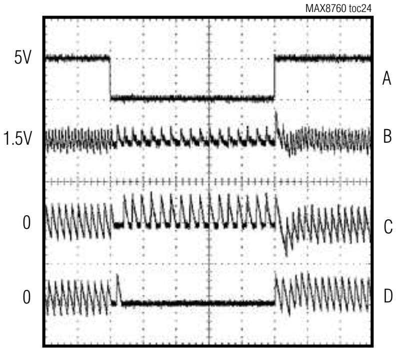


100µs/div

A. SUS, 5V/div
B. V_{OUT} = 1.5V TO 1.0V, 0.5V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
5A LOAD, C_{OUT} = (4) 680µF, $\overline{SKIP}$ = $\overline{SUS}$, R_{TIME} = 64.9kΩ

SINGLE-PHASE SKIP TO DUAL-PHASE PWM TRANSITION

MAX8760 toc24

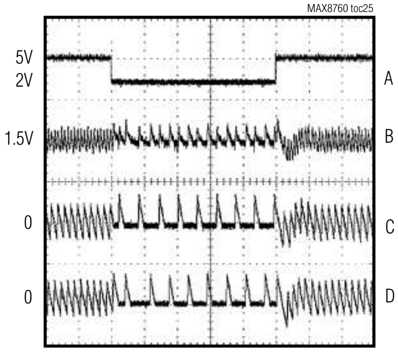


20µs/div

A. $\overline{SKIP}$ = V_{CC} TO GND, 5V/div
B. 1.5V OUTPUT, 50mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
2A LOAD

DUAL-PHASE SKIP TO DUAL-PHASE PWM TRANSITION

MAX8760 toc25



20µs/div

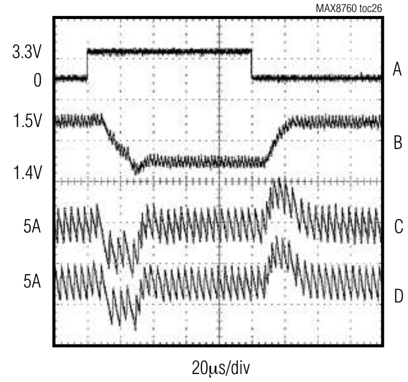
A. $\overline{SKIP}$ = V_{CC} TO REF, 5V/div
B. 1.5V OUTPUT, 50mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
2A LOAD

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = $\overline{SKIP}$ = V_{CC}, D0–D5 set for 1.5V (SUS = GND), S0 and S1 set for 1V (SUS = V_{CC}), OFS = GND, T_A = +25°C, unless otherwise specified.)

100mV DAC CODE TRANSITION

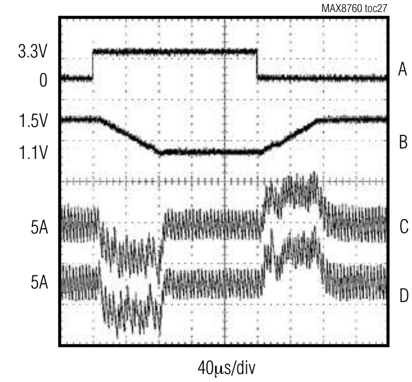
MAX8760 toc26



A. D1, 5V/div
B. V_{OUT} = 1.50V TO 1.40V, 100mV/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
10A LOAD

400mV DAC CODE TRANSITION

MAX8760 toc27



A. D3, 5V/div
B. V_{OUT} = 1.50V TO 1.10V, 0.5V/div
C. I_{L1}, 10A/div
D. I_{L2}, 10A/div
10A LOAD

Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

Pin Description

PIN	NAME	FUNCTION
1	TIME	Slew-Rate Adjustment Pin. Connect a resistor from TIME to GND to set the internal slew-rate clock. A 150kΩ to 15kΩ resistor sets the clock from 100kHz to 1MHz, f_{SLEW} = 500kHz x 30kΩ/R_{TIME}. During startup and shutdown, the internal slew-rate clock operates at 1/4 the programmed rate.
2	TON	On-Time Selection Control Input. This four-level input sets the K-factor value used to determine the DH_ on-time (see the *On-Time One-Shot (TON)* section): GND = 550kHz, REF = 300kHz, OPEN = 200kHz, V_{CC} = 100kHz
3	SUS	Suspend Input. SUS is a tri-level logic input. When the controller detects on-transition on SUS, the controller slews the output voltage to the new voltage level determined by SUS, S0, S1, and D0–D5. The controller blanks VROK during the transition and another 24 R_{TIME} clock cycles after the new DAC code is reached. Connect SUS as follows to select which multiplexer sets the nominal output voltage: 3.3V or V_{CC} (high) = Suspend mode; S0, S1 low-range suspend code (Table 5) REF = Suspend mode; S0, S1 high-range suspend code (Table 5) GND = Normal operation; D0–D5 VID DAC code (Table 4)
4, 5	S0, S1	Suspend-Mode Voltage-Select Inputs. S0, S1 are four-level digital inputs that select the suspend mode VID code (Table 5) for the suspend mode multiplexer inputs. If SUS is high, the suspend mode VID code is delivered to the DAC (see the *Internal Multiplexers* section), overriding any other voltage setting (Figure 3).
6	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA (typ) shutdown state. During the transition from normal operation to shutdown, the output voltage ramps down at 4 times the output-voltage slew rate programmed by the TIME pin. In shutdown mode, DLM and DLS are forced to V_{DD} to clamp the output to ground. Forcing $\overline{SHDN}$ to 12V ~ 15V disables both overvoltage protection and undervoltage protection circuits, disables overlap operation, and clears the fault latch. Do not connect $\overline{SHDN}$ to >15V.
7	OFS	Voltage-Divider Input for Offset Control. For 0 < V_{OFS} < 0.8V, 0.125 times the voltage at OFS is subtracted from the output. For 1.2V < V_{OFS} < 2V, 0.125 times the difference between REF and OFS is added to the output. Voltages in the 0.8V < V_{OFS} < 1.2V range are undefined. The controller disables the offset amplifier during suspend mode (SUS = REF or high).
8	REF	2V Reference Output. Bypass to GND with a 0.22µF or greater ceramic capacitor. The reference can source 100µA for external loads. Loading REF degrades output voltage accuracy according to the REF load regulation error.
9	ILIM	Current-Limit Adjustment. The current-limit threshold defaults to 30mV if ILIM is connected to V_{CC}. In adjustable mode, the current-limit threshold voltage is precisely 1/20 the voltage seen at ILIM over a 0.2V to 1.5V range. The logic threshold for switchover to the 30mV default value is approximately V_{CC} - 1V.
10	V_{CC}	Analog Supply Voltage Input for PWM Core. Connect V_{CC} to the system supply voltage (4.5V to 5.5V) with a series 10Ω resistor. Bypass to GND with a 1µF or greater ceramic capacitor, as close to the IC as possible.
11	GND	Analog Ground. Connect the MAX8760's exposed pad to analog ground.
12	CCV	Voltage Integrator Capacitor Connection. Connect a 47pF to 1000pF (150pF typ) capacitor from CCV to analog ground (GND) to set the integration time constant.
13	GNDS	Ground Remote-Sense Input. Connect GNDS directly to the CPU ground-sense pin. GNDS internally connects to an amplifier that adjusts the output voltage, compensating for voltage drops from the regulator ground to the load ground.

Pin Description (continued)

PIN	NAME	FUNCTION
14	CCI	Current Balance Compensation. Connect a 470pF capacitor between CCI and FB. See the *Current Balance Compensation* section.
15	FB	Feedback Input. FB is internally connected to both the feedback input and the output of the voltage-positioning op amp. See the *Setting Voltage Positioning* section to set the voltage-positioning gain.
16	OAIN-	Op Amp Inverting Input and Op Amp Disable Input. When using the internal op amp for additional voltage-positioning gain, connect to the negative terminal of current-sense resistor through a resistor as described in the *Setting Voltage Positioning* section. Connect OAIN- to V_{CC} to disable the op amp. The logic threshold to disable the op amp is approximately V_{CC} - 1V.
17	OAIN+	Op Amp Noninverting Input. When using the internal op amp for additional voltage-positioning gain, connect to the positive terminal of current-sense resistor through a resistor as described in the *Setting Voltage Positioning* section.
18	$\overline{\text{SKIP}}$	Pulse-Skipping Select Input. When pulse skipping, the controller blanks the VROK upper threshold: 3.3V or V_{CC} (high) = Dual-phase forced-PWM operation REF = Dual-phase pulse-skipping operation GND = Single-phase pulse-skipping operation
19–24	D5–D0	Low-Voltage VID DAC Code Inputs. The D0–D5 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. In normal mode (Table 4, SUS = GND), the output voltage is set by the VID code indicated by the logic-level voltages on D0–D5. In suspend mode (Table 5, SUS = REF or high), the decoded state of the four-level S0, S1 inputs sets the output voltage.
25	VROK	Open-Drain Power-Good Output. After output voltage transitions, except during power-up and power-down, if OUT is in regulation then VROK is high impedance. The controller blanks VROK whenever the slew-rate control is active (output voltage transitions). VROK is forced low in shutdown. A pullup resistor on VROK causes additional finite shutdown current. During power-up, VROK includes a 3ms (min) delay after the output reaches the regulation voltage.
26	BSTM	Main Boost Flying Capacitor Connection. An optional resistor in series with BSTM allows the DHM pullup current to be adjusted.
27	LXM	Main Inductor Connection. LXM is the internal lower supply rail for the DHM high-side gate driver.
28	DHM	Main High-Side Gate-Driver Output. Swings LXM to BSTM.
29	DLM	Main Low-Side Gate-Driver Output. DLM swings from PGND to V_{DD}. DLM is forced high after the MAX8760 powers down.
30	V_{DD}	Supply Voltage Input for the DLM and DLS Gate Drivers. Connect to the system supply voltage (4.5V to 5.5V). Bypass V_{DD} to PGND with a 2.2µF or greater ceramic capacitor as close to the IC as possible.
31	PGND	Power Ground. Ground connection for low-side gate drivers DLM and DLS.

Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
32	DLS	Secondary Low-Side Gate-Driver Output. DLS swings from PGND to V_{DD}. DLS is forced high after the MAX8760 powers down.
33	DHS	Secondary High-Side Gate-Driver Output. Swings LXS to BSTS.
34	LXS	Secondary Inductor Connection. LXS is the internal lower supply rail for the DHS high-side gate driver.
35	BSTS	Secondary Boost Flying Capacitor Connection. An optional resistor in series with BSTS allows the DHS pullup current to be adjusted.
36	V+	Battery Voltage-Sense Connection. Used only for PWM one-shot timing. DH_ on-time is inversely proportional to input voltage over a 4V to 28V range.
37	CMP	Main Inductor Positive Current-Sense Input
38	CMN	Main Inductor Negative Current-Sense Input
39	CSN	Secondary Inductor Positive Current-Sense Input
40	CSP	Secondary Inductor Negative Current-Sense Input

Detailed Description

Dual 180° Out-of-Phase Operation

The two phases in the MAX8760 operate 180° out-of-phase ($\overline{SKIP}$ = REF or high) to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX8760 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide transfer power using only one phase instead of dividing the power among several phases. In these applications, the input capacitors must support high-instantaneous current requirements. The high-RMS ripple current can lower efficiency due to I^2R power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input voltage ripple, to reduce ESR-related power losses, and to meet the necessary RMS ripple current rating.

With the MAX8760, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively cut in half, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). As a result, the same performance can be achieved with fewer or less-expensive input capacitors. Table 1 lists component selection for standard multiphase selections and Table 2 is a list of component suppliers.

Transient Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180 degrees out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. To provide fast transient response, the MAX8760 supports a phase-overlap mode, which allows the dual regulators to operate in-phase when heavy-load transients are detected, reducing the response time. After either high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on both high-side MOSFETs during the next on-time cycle. This maximizes the total inductor current slew rate. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires.

After the phase-overlap mode ends, the controller automatically begins with the opposite phase. For example, if the secondary phase provided the last on-time pulse before overlap operation began, the controller starts switching with the main phase when overlap operation ends.

Power-Up Sequence

The MAX8760 is enabled when $\overline{SHDN}$ is driven high (Figure 2). The reference powers up first. Once the reference exceeds its UVLO threshold, the PWM controller evaluates the DAC target and starts switching.

Table 1. Component Selection for Standard Multiphase Applications

DESIGNATION	MAX8760 AMD MOBILE COMPONENTS Circuit of Figure 1
Input Voltage Range	7V to 24V
VID Output Voltage (D5–D0)	1.3V (D5–D0 = 001010)
Suspend Voltage (SUS, S0, S1)	Not used (SUS = GND)
Maximum Load Current	30A
Number of Phases (η_{TOTAL})	Two phases
Inductor (per Phase)	0.56µH Panasonic ETQP4LR56WFC
Switching Frequency	300kHz (TON = REF)
High-Side MOSFET (N_H, per phase)	Siliconix (1) Si7886DP
Low-Side MOSFET (N_L, per phase)	Siliconix (2) Si7356DP
Total Input Capacitance (C_{IN})	(4) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Total Output Capacitance (C_{OUT})	(4) 330µF, 2.5V Sanyo 2R5TPE330M9
Current-Sense Resistor (R_{SENSE}, per Phase)	1mΩ Panasonic ERJM1WTJ1M0U

For the MAX8760, the slew-rate controller ramps up the output voltage in 12.5mV increments to the proper operating voltage (see Tables 3 and 4) set by either D0–D5 (SUS = GND) or S0, S1 (SUS = REF or high). The ramp rate is set with the R_{TIME} resistor (see the *Output Voltage Transition Timing* section).

The ramp rate is 1/4 the rate set by the R_{TIME} resistor (see the *Output Voltage Transition Timing* section). The controller pulls VROK low until at least 3ms after the MAX8760 reaches the target DAC code.

Shutdown

When $\overline{SHDN}$ goes low, the MAX8760 enters low-power shutdown mode. VROK is pulled low immediately, and the output voltage ramps down to 0V in LSB increments at 4 times the clock rate set by R_{TIME}:

$$t_{SHDN} \le \frac{4}{f_{SLEW}}\left(\frac{V_{DAC}}{V_{LSB}}\right)$$

where f_{SLEW} = 500kHz × 30kΩ/R_{TIME}, V_{DAC} is the DAC setting when the controller begins the shutdown sequence, and V_{LSB} = 12.5mV is the DAC's smallest voltage increment. Slowly discharging the output capacitors by slewing the output over a long period of time ($4/f_{SLEW}$) keeps the average negative inductor current low (damped response), thereby eliminating the negative output voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output voltage excursion. When the DAC reaches the 0V setting, DL_ goes high, DH_ goes low, the reference turns off, and the supply current drops to about 1µA. When a fault condition—output undervoltage lockout, output overvoltage lockout, or thermal shutdown—activates the shutdown sequence, the controller sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle $\overline{SHDN}$ or cycle V_{CC} power below 1V.

When $\overline{SHDN}$ goes high, the reference powers up. Once the reference voltage exceeds its UVLO threshold, the controller evaluates the DAC target and starts switching. The slew-rate controller ramps up from 0V in LSB increments to the currently selected output-voltage setting at 1/4 the slew rate set by the R_{TIME} resistor (see the *Power-Up Sequence* section). There is no traditional soft-start (variable current-limit) circuitry, so full output current is available immediately.

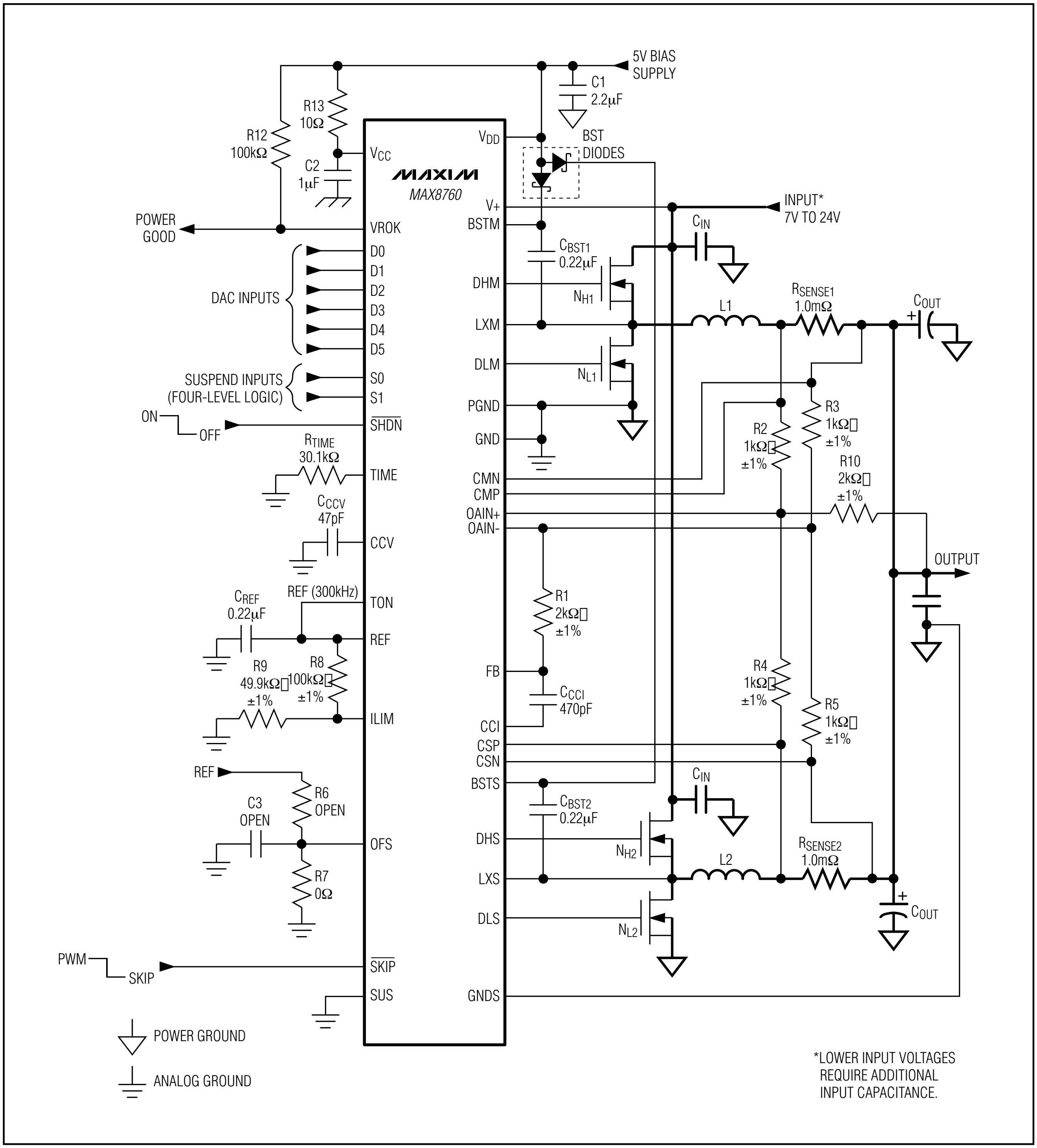


Figure 1. Standard Two-Phase AMD Mobile 30A Application Circuit

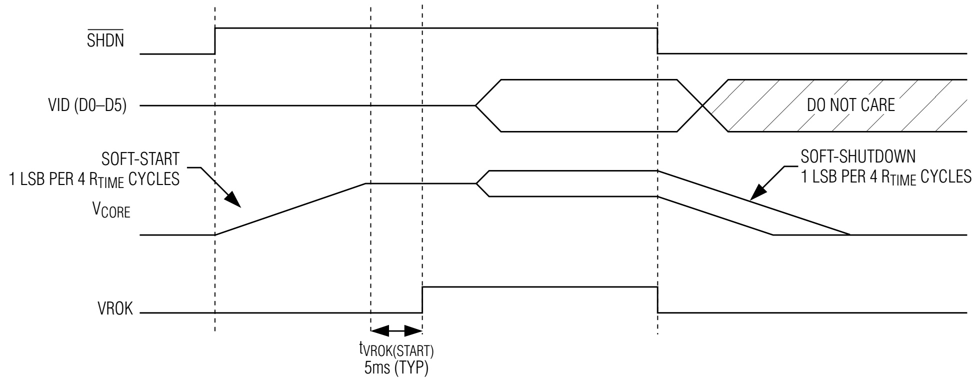


Figure 2. Power-Up and Shutdown Sequence Timing Diagram

Table 2. Component Suppliers

MANUFACTURER	PHONE	WEBSITE
BI Technologies	714-447-2345 (USA)	www.bitechnologies.com
Central Semiconductor	631-435-1110 (USA)	www.centralsemi.com
Coilcraft	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	561-752-5000 (USA)	www.coiltronics.com
Fairchild Semiconductor	888-522-5372 (USA)	www.fairchildsemi.com
International Rectifier	310-322-3331 (USA)	www.irf.com
Kemet	408-986-0424 (USA)	www.kemet.com
Panasonic	847-468-5624 (USA)	www.panasonic.com
Sanyo	65-6281-3226 (Singapore)	www.secc.co.jp
Siliconix (Vishay)	203-268-6261 (USA)	www.vishay.com
Sumida	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	03-3667-3408 (Japan) 408-573-4150 (USA)	www.t-yuden.com
TDK	847-803-6100 (USA) 81-3-5201-7241 (Japan)	www.component.tdk.com
TOKO	858-675-8013 (USA)	www.tokoam.com

Internal Multiplexers

The MAX8760 has a unique internal DAC input multiplexer (MUXes) that selects one of three different DAC code settings for different processor states (Figure 3). On startup, the MAX8760 selects the DAC code from the D0–D5 (SUS = GND) or S0, S1 (SUS = REF or high) input decoders.

DAC Inputs (D0–D5)

During normal forced-PWM operation (SUS = GND), the digital-to-analog converter (DAC) programs the output voltage using the D0–D5 inputs. Do not leave D0–D5 unconnected. D0–D5 can be changed while the MAX8760 is active, initiating a transition to a new output voltage level. Change D0–D5 together, avoiding greater than 1µs skew between bits. Otherwise, incorrect DAC readings can cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with AMD K9 voltage specifications (Table 4).

Table 3. Operating Mode Truth Table

$\overline{SHDN}$	SUS	$\overline{SKIP}$	OFS	OUTPUT VOLTAGE	OPERATING MODE
GND	x	x	x	GND	Low-Power Shutdown Mode. DL_ is forced high, DH_ is forced low, and the PWM controller is disabled. The supply current drops to 1µA (typ).
V_{CC}	GND	V_{CC}	GND or REF	D0–D5 (no offset)	Normal Operation. The no-load output voltage is determined by the selected VID DAC code (D0–D5, Table 4).
V_{CC}	x	GND or REF	GND or REF	D0–D5 (no offset)	Pulse-Skipping Operation. When $\overline{SKIP}$ is pulled low, the MAX8760 immediately enters pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The VROK upper threshold is blanked.
V_{CC}	GND	x	0 to 0.8V or 1.2V to 2V	D0–D5 (plus offset)	Deep-Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D5, Table 4) plus the offset voltage set by OFS.
V_{CC}	REF or High	x	x	SUS, S0–S1 (no offset)	Suspend Mode. The no-load output voltage is determined by the selected suspend code (SUS, S0, S1, Table 5), overriding all other active modes of operation.
V_{CC}	x	x	x	GND	Fault Mode. The fault latch has been set by either UVP, OVP, or thermal shutdown. The controller remains in FAULT mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

Four-Level Logic Inputs

TON and S0, S1 are four-level logic inputs. These inputs help expand the functionality of the controller without adding an excessive number of pins. The four-level inputs are intended to be static inputs. When left open, an internal resistive voltage-divider sets the input voltage to approximately 3.5V. Therefore, connect the four-level logic inputs directly to V_{CC}, REF, or GND when selecting one of the other logic levels. See the *Electrical Characteristics* table for exact logic level voltages.

Suspend Mode

When the processor enters low-power suspend mode, it sets the regulator to a lower output voltage to reduce power consumption. The MAX8760 includes independent suspend-mode output voltage codes set by the four-level S0, S1 inputs and the tri-level SUS input. When the CPU suspends operation (SUS = REF or high), the controller disables the offset amplifier and overrides the 5-bit VID DAC code set by either D0–D5 (normal operation). The master controller slews the output to the selected suspend-mode voltage. During the transition, the MAX8760 blanks VROK and the UVP fault protection until 24 R_{TIME} clock cycles after the slew-rate controller reaches the suspend-mode voltage.

SUS is a tri-level logic input: GND, REF, or high. This expands the functionality of the controller without adding an additional pin. This input is intended to be driven by a dedicated open-drain output with the pullup resistor connected either to REF (or a resistive divider from V_{CC}) or to a logic-level bias supply (3.3V or greater). When pulled up to REF, the MAX8760 selects the upper suspend voltage range. When pulled high (2.7V or greater), the controller selects the lower suspend voltage range. See the *Electrical Characteristics* table for exact logic-level voltages.

Output Voltage Transition Timing

The MAX8760 is designed to perform mode transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance.

At the beginning of an output voltage transition, the MAX8760 blanks the VROK output, preventing it from changing states. VROK remains blanked during the transition and is enabled 24 clock cycles after the slew-rate controller has set the final DAC code value. The slew-rate clock frequency (set by resistor R_{TIME}) must be set fast enough to ensure that the transition is completed within the maximum allotted time.

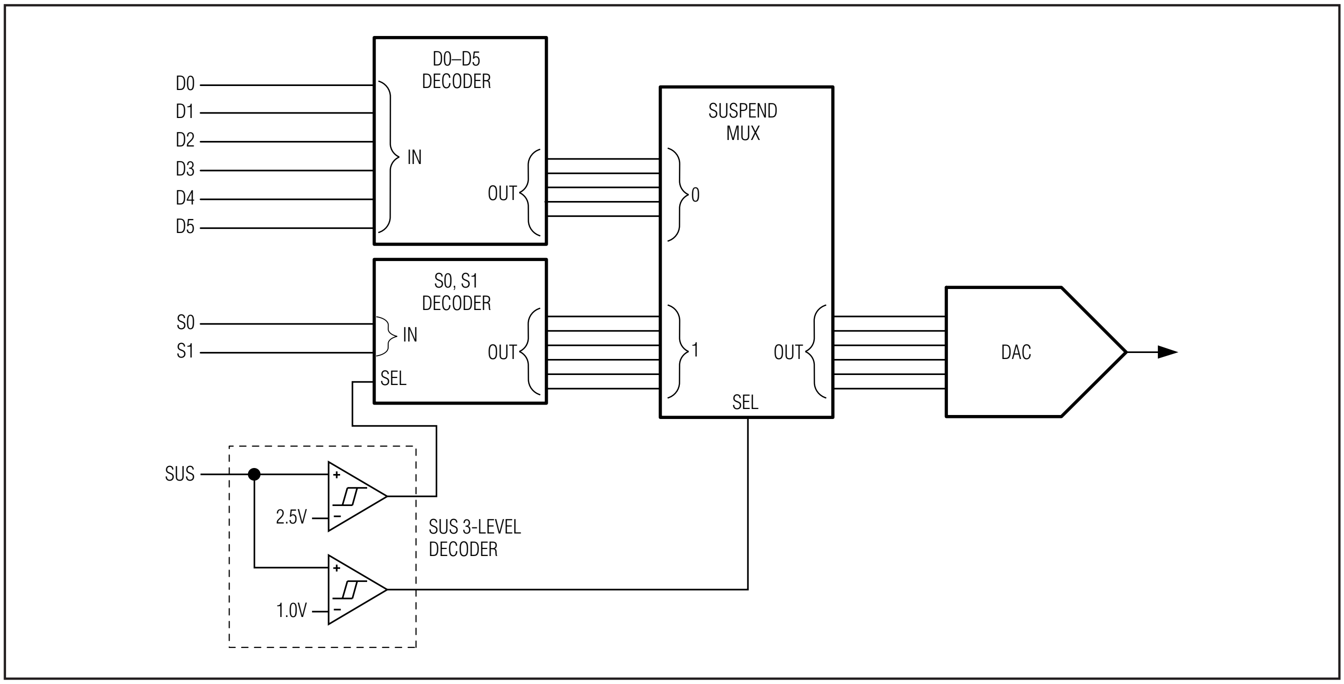


Figure 3. Internal Multiplexers Functional Diagram

The slew-rate controller transitions the output voltage in 12.5mV steps during soft-start, soft-shutdown, and suspend-mode transitions. The total time for a transition depends on R_{TIME}, the voltage difference, and the accuracy of the MAX8760's slew-rate clock, and is not dependent on the total output capacitance. The greater the output capacitance, the higher the surge current required for the transition. The MAX8760 automatically controls the current to the minimum level required to complete the transition in the calculated time, as long as the surge current is less than the current limit set by ILIM. The transition time is given by:

$$t_{SLEW} \approx \frac{1}{f_{SLEW}}\left(\frac{V_{OLD} - V_{NEW}}{V_{LSB}}\right) \text{ for } V_{OUT} \text{ rising}$$

$$t_{SLEW} \approx \frac{1}{f_{SLEW}}\left[\left(\frac{V_{OLD} - V_{NEW}}{V_{LSB}}\right) + 2\right] \text{ for } V_{OUT} \text{ falling}$$

where f_{SLEW} = 500kHz × 30kΩ / R_{TIME}, V_{OLD} is the original DAC setting, V_{NEW} is the new DAC setting, and V_{LSB} = 12.5mV is the DAC's smallest voltage increment. The additional two clock cycles on the falling edge time are due to internal synchronization delays. See TIME Frequency Accuracy in the *Electrical Characteristics* table for f_{SLEW} limits.

The practical range of R_{TIME} is 15kΩ to 150kΩ, corresponding to 1.0µs to 10µs per 12.5mV step. Although the DAC takes discrete steps, the output filter makes the transitions relatively smooth. The average inductor current required to make an output voltage transition is:

$$I_L \cong C_{OUT} \times V_{LSB} \times f_{SLEW}$$

Dual-Phase, Quick-PWM Controller for AMD Mobile Turion 64 CPU Core Power Supplies

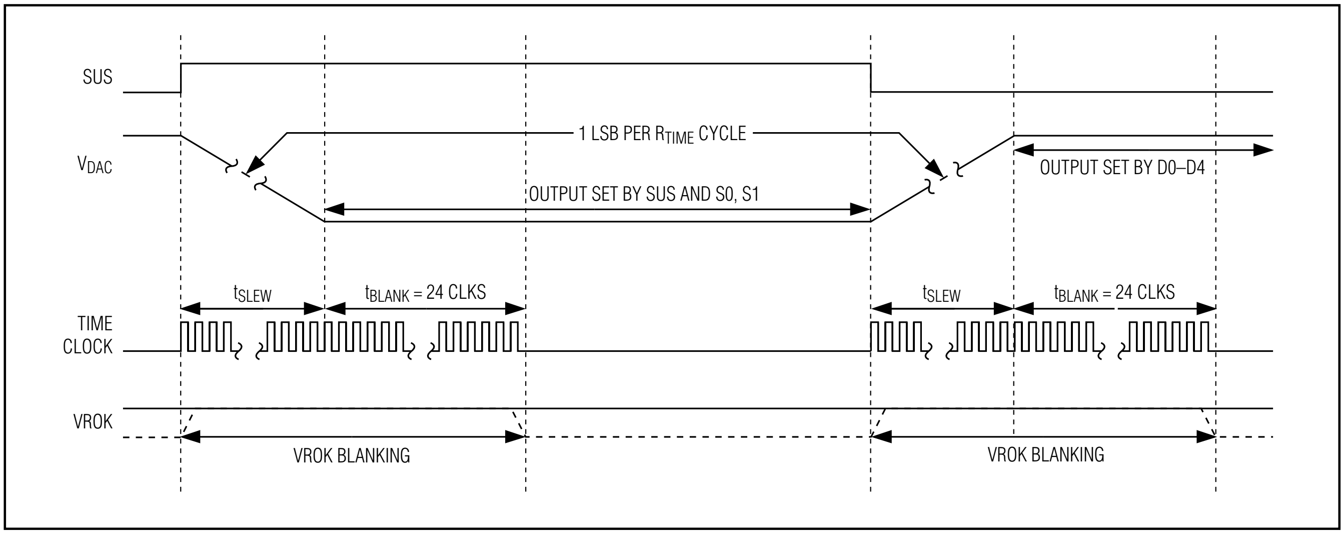


Figure 4. Suspend Transition

Fault Protection

Output Overvoltage Protection

The OVP circuit is designed to protect the CPU against a shorted high-side MOSFET by drawing high current and blowing the battery fuse. The MAX8760 continuously monitors the output for an overvoltage fault. The controller detects an OVP fault if the output voltage exceeds the fixed 2.0V (typ) threshold. When the OVP circuit detects an overvoltage fault, it immediately sets the fault latch, turns off the high-side MOSFETs, and forces DL high.

This action discharges the output filter capacitor and forces the output to ground. If the condition that caused the overvoltage (such as a shorted high-side MOSFET) persists, the battery fuse blows. The controller remains shut down until the fault latch is cleared by toggling $\overline{SHDN}$ or cycling the V_{CC} power supply below 1V.

The OVP is disabled when the controller is in the no-fault test mode (see the *No-Fault Test Mode* section).

Output Undervoltage Shutdown

The output UVP function is similar to foldback current limiting, but employs a timer rather than a variable current limit. If the MAX8760 output voltage is under 70% of the nominal value, the controller activates the shutdown sequence and sets the fault latch.

Once the controller ramps down to the 0V DAC code setting, it forces the DL_ low-side gate driver high and pulls the DH_ high-side gate driver low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller. UVP is ignored during output voltage transitions and remains blanked for an additional 24 clock cycles after the controller reaches the final DAC code value.

UVP can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

Thermal-Fault Protection

The MAX8760 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch and the soft-shutdown sequence. Once the controller ramps down to the 0V DAC code setting, it forces the DL_ low-side gate driver high, and pulls the DH_ high-side gate driver low. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 1V to clear the fault latch and reactivate the controller after the junction temperature cools by 15°C.

Thermal shutdown can be disabled through the no-fault test mode (see the *No-Fault Test Mode* section).

No-Fault Test Mode

The latched-fault protection features and overlap mode can complicate the process of debugging prototype breadboards since there are (at most) a few milliseconds in which to determine what went wrong. Therefore, a no-fault test mode is provided to disable the fault protection (overvoltage protection, undervoltage protection, and thermal shutdown) and overlap mode. Additionally, the test mode clears the fault latch if it has been set. The no-fault test mode is entered by forcing 12V to 15V on $\overline{SHDN}$.

Table 4. Output Voltage ID DAC Codes (SUS = GND)

D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750

D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Table 5. Suspend Mode DAC Codes

LOWER SUSPEND CODES			
SUS	S1	S0	OUTPUT VOLTAGE (V)
HIGH	GND	GND	0.800
HIGH	GND	REF	0.775
HIGH	GND	OPEN	0.750
HIGH	GND	V_{CC}	0.725
HIGH	REF	GND	0.700
HIGH	REF	REF	0.675
HIGH	REF	OPEN	0.650
HIGH	REF	V_{CC}	0.625
HIGH	OPEN	GND	0.600
HIGH	OPEN	REF	0.575
HIGH	OPEN	OPEN	0.550
HIGH	OPEN	V_{CC}	0.525
HIGH	V_{CC}	GND	0.500
HIGH	V_{CC}	REF	0.475
HIGH	V_{CC}	OPEN	0.450
HIGH	V_{CC}	V_{CC}	0.425

UPPER SUSPEND CODES			
SUS	S1	S0	OUTPUT VOLTAGE (V)
REF	GND	GND	1.200
REF	GND	REF	1.175
REF	GND	OPEN	1.150
REF	GND	V_{CC}	1.125
REF	REF	GND	1.100
REF	REF	REF	1.075
REF	REF	OPEN	1.050
REF	REF	V_{CC}	1.025
REF	OPEN	GND	1.000
REF	OPEN	REF	0.975
REF	OPEN	OPEN	0.950
REF	OPEN	V_{CC}	0.925
REF	V_{CC}	GND	0.900
REF	V_{CC}	REF	0.875
REF	V_{CC}	OPEN	0.850
REF	V_{CC}	V_{CC}	0.825

**Connect the tri-level SUS input to a 2.7V or greater supply (3.3V or V_{CC}) for an input logic level high.*

Multiphase Quick-PWM

5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V bias supply can be generated with an external linear regulator.

The 5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}(Q_{G(LOW)} + Q_{G(HIGH)})$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V+ and V_{DD} can be connected together if the input power source is a fixed 4.5V to 5.5V supply. If the 5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudofixed-frequency, constant-on-time, current-mode regulator with input voltage feed-forward (Figure 5). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot with a period inversely proportional to input voltage, and directly proportional to output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* (*TON*) section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 180° out-of-phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output voltage set point.

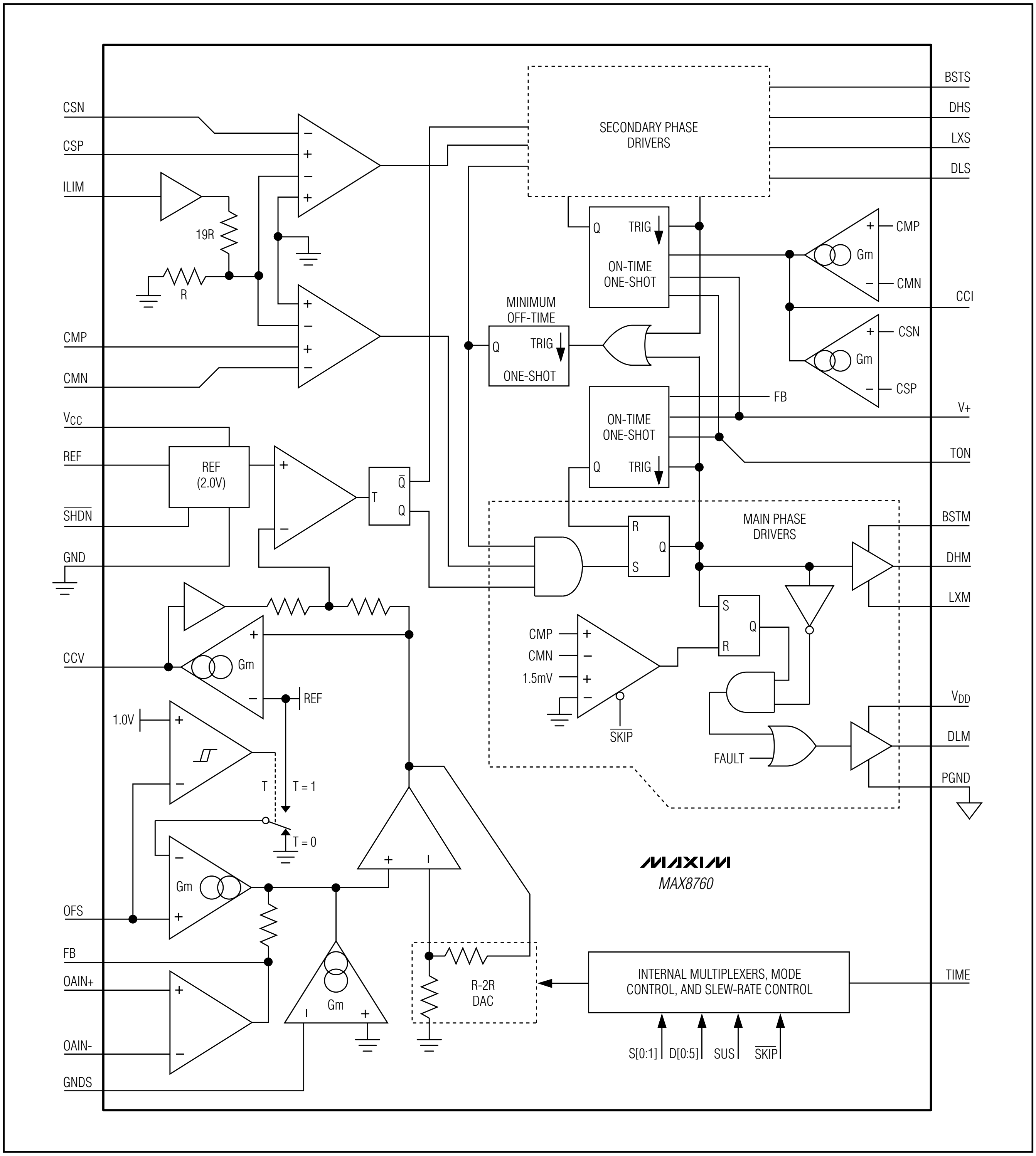


Figure 5. Dual-Phase Quick-PWM Functional Diagram