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MAXIM

MAX8770/MAX8771/MAX8772 Dual-Phase, Quick-PWM Controller for IMVP-6+ CPU Core Power Supplies

General Description

The MAX8770/MAX8771/MAX8772 are 2/1-phase interleaved Quick-PWM™ step-down VID power-supply controllers for notebook CPUs. True out-of-phase operation reduces input ripple current requirements and output voltage ripple while easing component selection and layout difficulties. The Quick-PWM control provides instantaneous response to fast load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX8770/MAX8771/MAX8772 are intended for two different notebook CPU core applications: either bucking down the battery directly to create the core voltage, or else bucking down the +5V system supply. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

A slew-rate controller allows controlled transitions between VID codes, controlled soft-start and shutdown, and controlled exit from suspend. A thermistor-based temperature sensor provides a programmable thermal-fault output ($\overline{VRHOT}$). A power-monitor output (POUT) provides an analog voltage output proportional to the power consumed by the CPU. The MAX8770/MAX8771/MAX8772 include output undervoltage protection (UVP) and thermal protection, and the MAX8770/MAX8771 also include overvoltage protection (OVP). When any of these protection features detect a fault, the controller shuts down. A voltage-regulator power-OK (PWRGD) output indicates the output is in regulation. A clock enable ($\overline{CLKEN}$) output provides proper system startup sequencing. Additionally, the MAX8771 has a phase-good (PHASEGD) output, and the MAX8770/MAX8772 includes true differential current sense.

The MAX8770/MAX8771/MAX8772 implement the Intel IMVP-6+ code set and the required IMVP-6+ control signals. The MAX8770/MAX8771/MAX8772 are available in a 40-pin TQFN package.

Applications

IMVP-6+ Core Supply
Multiphase CPU Core Supply
Voltage-Positioned, Step-Down Converters
Notebook/Desktop Computers
Blade Servers

Intel is a registered trademark of Intel, Corp.

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **Single/Dual-Phase, Quick-PWM Controller**
- **±0.4% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **7-Bit On-Board DAC: 0 to +1.5000V Output Adjust Range**
- **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
- **Transient Phase Overlap Reduces Output Capacitance**
- **Integrated Boost Switches**
- **Active Voltage Positioning with Adjustable Gain**
- **Programmable 200kHz to 600kHz Switching Frequency**
- **Accurate Current Balance and Current Limit**
- **Adjustable Slew-Rate Control**
- **Power-Good (PWRGD), Clock Enable ($\overline{CLKEN}$), Power Monitor (POUT) and Thermal Fault ($\overline{VRHOT}$) Outputs**
- **Phase Fault (PHASEGD) Output (MAX8771)**
- **Drives Large Synchronous Rectifier MOSFETs**
- **4V to 26V Battery-Input-Voltage Range**
- **Output OV Protection (MAX8770/MAX8771)**
- **UV and Thermal-Fault Protection**
- **Power Sequencing and Timing**
- **Soft-Startup and Soft-Shutdown**

Ordering Information

PART	TEMP	PIN-PACKAGE
MAX8770GTL+	-40°C to +105°C	40 Thin QFN 6mm x 6mm
MAX8771GTL+	-40°C to +105°C	40 Thin QFN 6mm x 6mm
MAX8772GTL+	-40°C to +105°C	40 Thin QFN 6mm x 6mm

+Denotes lead-free package.

Pin Configuration appears at end of data sheet.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD} to GND .....-0.3V to +6V
D0–D6, CSP_ to GND .....-0.3V to +6V
CSN12 (MAX8771) to GND .....-0.3V to +6V
CSN_ (MAX8770/MAX8772) to GND .....-0.3V to +6V
PHASEGD (MAX8771) to GND .....-0.3V to +6V
THRM, $\overline{VRHOT}$, $\overline{CLKEN}$ to GND .....-0.3V to +6V
TIME, PWRGD, POUT to GND .....-0.3V to V_{CC} + 0.3V
REF, FB, CCV, CCI to GND .....-0.3V to V_{CC} + 0.3V
$\overline{SHDN}$ to GND (Note 1) .....-0.3V to +14V
TON to GND .....-0.3V to +30V
DPRSLPVR, $\overline{DPRSTP}$, $\overline{PSI}$ to GND .....-0.3V to +6V
GNDS, PGND_ to GND .....-0.3V to +0.3V
DL_ to PGND_ .....-0.3V to V_{DD} + 0.3V
BST_ to GND .....-0.3V to +36V
LX_ to BST_ .....-6V to +0.3V
BST_ to VDD .....-0.3V to +30V
DH_ to LX_ .....-0.3V to $V_{BST\_}$ +0.3V
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation
40-Pin 6mm x 6mm Thin QFN
(derate 23.2mW/°C above +70°C) 2051mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ may be forced to 12V for the purpose of debugging prototype boards using the no-fault test mode, which disables fault protection and disables overlapping operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
DC Output-Voltage Accuracy	V_{OUT}	Includes load-regulation error (Note 2)	DAC codes from 0.8375V to 1.500V	-0.4		+0.4	%
			DAC codes from 0.500V to 0.825V	-4		+4	mV
			DAC codes below 0.4875V	-10		+10	
Boot Voltage	V_{BOOT}			1.19	1.20	1.21	V
GNDS Input Range	V_{GNDS}			-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ V_{GNDS} ≤ +200mV		0.95	1.00	1.05	V/V
GNDS Input Bias Current	I_{GNDS}			-25	-15	+2	µA
FB Input Bias Current	I_{FB}	CSP_ = CSN_ for both enabled phases		-2		+2	µA
On-Time Accuracy (Note 3)	t_{ON}	V_{IN} = 12V, V_{FB} = V_{CCI} = 1.2V	R_{TON} = 96.75kΩ	142	167	192	ns
			R_{TON} = 200kΩ	300	333	366	
			R_{TON} = 303.25kΩ	425	500	575	
TON Shutdown Input Current		$\overline{SHDN}$ = 0, V_{IN} = 26V, V_{CC} = V_{DD} = 0 or 5V			0.01	0.1	µA
Minimum FB and CCI Voltages for Pseudo-Fixed-Frequency Operation		Switching frequency is reduced if FB and/or CCI are less than this value			0.2	0.25	V
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			300	375	ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)	-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)	-15		+15	
		$\overline{DPRSTP}$ = high, DPRSLPVR = high, R_{TIME} = 35.7kΩ to 178kΩ, SR = 6.25mV/µs nominal to 1.25mV/µs nominal	-20		+20	
		Startup and shutdown, R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)	-20		+20	
BIAS AND REFERENCE						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point, DPRSLPVR = V_{CC}		5	10	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point, DPRSLPVR = V_{CC}		0.01	1	µA
Shutdown Supply Current (V_{CC})	$I_{CC(SHDN)}$	Measured at V_{CC}, $\overline{SHDN}$ = GND		0.01	1	µA
Shutdown Supply Current (V_{DD})	$I_{DD(SHDN)}$	Measured at V_{DD}, $\overline{SHDN}$ = GND		0.01	1	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0	1.986	2.000	2.014	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = 0 to 500µA	-2	-0.2		mV
		I_{REF} = -100µA to 0		0.21	6.2	
FAULT PROTECTION						
Output Overvoltage Protection Threshold (MAX8770/MAX8771 Only)	V_{OVP}	Measured at FB with respect to unloaded output voltage; rising edge; PWM mode or skip mode after output reaches the regulation voltage	250	300	350	mV
		Measured at FB; rising edge; Skip mode and output have not reached the regulation voltage	1.75	1.80	1.85	V
		Measured at FB; rising edge; Minimum OVP threshold		0.8		
Output Overvoltage-Propagation Delay (MAX8770/MAX8771 Only)	t_{OVP}	FB forced 25mV above trip threshold		10		µs
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage	-450	-400	-350	mV
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold		10		µs
$\overline{CLKEN}$ Startup Delay (Boot Time Period)	t_{BOOT}	Measured from the time when FB reaches the boot target voltage based on the slew rate set by R_{TIME}	20	60	100	µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWRGD, PHASEGD Startup Delay	t_{PWRGD}	Measured at startup from the time when $\overline{CLKEN}$ goes low		3	5	8	ms
$\overline{CLKEN}$, PWRGD Threshold		Measured at FB with respect to unloaded output voltage	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
		15mV hysteresis (typ)	Upper threshold, rising edge (overvoltage)	+150	+200	+250	
$\overline{CLKEN}$, PWRGD, PHASEGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
$\overline{CLKEN}$, PWRGD, PHASEGD Transition Blanking Time	t_{BLANK}	Measured from the time when FB reaches the target voltage based on the slew rate set by R_{TIME}			20		µs
PHASEGD Transition Blanking Time	$t_{PHASEGD}$	Number of DH2 pulses from when phase 2 is enabled			32		Cycles
PHASEGD Window Comparator Thresholds		V(CCI, FB), 0.4V ≤ V(FB) ≤ 1.5V	Lower threshold, $0.6V_{FB}$ nominal	-20		+20	mV
		15mV hysteresis (typ)	Upper threshold, $1.4V_{FB}$ nominal	-20		+20	
$\overline{CLKEN}$, PWRGD, PHASEGD Output Low Voltage		I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$, PWRGD, PHASEGD Leakage Current		High state, $\overline{CLKEN}$, PWRGD, PHASEGD forced to 5V				1	µA
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}; falling edge, 115mV hysteresis (typ)		29.5	30	30.5	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold; falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{\overline{VRHOT}}$	Low state			3.5	11	Ω
$\overline{VRHOT}$ Leakage Current		High state. $\overline{VRHOT}$ forced to 5V				1	µA
THRM Input Leakage				-100		+100	nA
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 50mV hysteresis, DL_ pulled low below this level		4.1	4.25	4.45	V
V_{CC} Power-On Reset Threshold		Falling edge, typical hysteresis = 1.1V, faults cleared and DL_ forced high when V_{CC} falls below this level			1.8		V
Thermal Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			160		°C

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DROOP AND BALANCE						
DC Droop Amplifier Offset			-1.0		+1.0	mV
DC Droop Amplifier Transconductance	$G_{m(FB)}$	$\Delta I_{FB}/(\Sigma\Delta V_{CS})$, V_{FB} = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = 0 to +60mV	590	600	610	µS
Current-Balance Preamplifier Offset		[V(CSP1, CSN_) - V(CSP2, CSN_)] at I_{CCI} = 0	-1.0		+1.0	mV
Current-Balance Amplifier Transconductance	$G_{m(CCI)}$	$\Delta I_{CCI}/\Delta$ [V(CSP1, CSN_), V(CSP2, CSN_)] CCI = FB = CSN_ = 0.45V to 1.5V, and V(CSP_, CSN_) = -10mV to +10mV		200		µS
CURRENT LIMIT						
Valley Current-Limit Threshold (Positive)	V_{LIMIT}	CSP_ - CSN_	19.5	22.5	25.5	mV
Valley Current-Limit Threshold (Negative)		CSP_, CSN_	-35	-30	-25	mV
Zero Crossing Threshold	V_{ZX}	PGND1 - LX1, DPRSLPVR = high (skip mode)		2.5		mV
Current-Sense Input Current		CSP_	-0.2		+0.2	µA
		CSN_	-0.2		+0.2	
		CSN12 (MAX8771)	-0.4		+0.4	
Common-Sense Common-Mode Input Range		CSP_ -CSN_		0	2	V
Phase 2 Disable Threshold Gate Drivers		CSP2	3	V_{CC} - 1	V_{CC} - 0.4	V
GATE DRIVERS						
DH_ Gate Driver On-Resistance	$R_{ON(DH\_)}$	BST_ -LX_ forced to 5V, High state (pullup)		0.9	2.5	Ω
		BST_ -LX_ forced to 5V, Low state (pulldown)		0.7	2.5	Ω
DL_ Gate Driver On-Resistance	$R_{ON(DL\_)}$	High state (pullup)		0.7	2.0	Ω
		Low state (pulldown)		0.25	0.5	Ω
DH_ Gate Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V		2.2		A
DL_ Gate Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V		2.7		A
DL_ Gate Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V		8		A
Driver Propagation Delay		DH_ low to DL_ high	18	25		ns
		DL_ low to DH_ high	9	20		ns
DL_ Transition Time		DL_ falling, $C_{DL\_}$ = 3nF		20		ns
		DL_ rising, $C_{DL\_}$ = 3nF		20		ns
DH_ Transition Time		DH_ falling, $C_{DH\_}$ = 3nF		20		ns
		DH_ rising, $C_{DH\_}$ = 3nF		20		ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Boost Charging Switch On-Resistance		V_{DD} to BST_		10	20	Ω
POWER MONITOR						
Power-Monitor Output Voltage for Typical HFM Conditions		V_{FB} - V_{GNDS} = 1.200V, $\Sigma\Delta V_{CS}$ = 30mV	2.08	2.16	2.24	V
Power-Monitor Gain Referred to Feedback Voltage		$\Sigma\Delta V_{CS}$ = 30mV	1.72	1.80	1.88	V/V
Power-Monitor Gain Referred to ΣV (CSP_, CSN)		V_{FB} - V_{GNDS} = 1.200V, T_A = +25°C to +85°C	70.5	72	73.5	V/V
Power-Monitor Load Regulation		Sourcing: I_{POUT} = 0 to 500µA	-6			µV/µA
		Sinking: I_{POUT} = 0 to 100µA		50		mV
LOGIC AND I/O						
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, DPRSLPVR, rising edge, hysteresis = 200mV	1.2	1.7	2.3	V
$\overline{SHDN}$ No-Fault Level		To enable no-fault mode	11		13	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	D0–D6, $\overline{PSI}$, $\overline{DRPSTP}$	0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	D0–D6, $\overline{PSI}$, $\overline{DRPSTP}$			0.33	V
Logic Input Current		$\overline{SHDN}$, $\overline{PSI}$, DPRSLPVR, D0–D6 = 0 to 5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0-D6 = 0001100). **T_A = -40°C to +105°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
DC Output Voltage Accuracy	V_{OUT}	Includes load-regulation error (Note 2)	DAC codes from 0.8375V to 1.500V	-0.6		+0.6	%
			DAC codes from 0.500V to 0.825V	-6		+6	mV
			DAC codes below 0.4875V	-15		+15	
Boot Voltage	V_{BOOT}			1.182		1.218	V
GNDS Input Range	V_{GNDS}			-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ V_{GNDS} ≤ +200mV		0.95		1.05	V/V
On-Time Accuracy (Note 3)	t_{ON}	V_{IN} = 12V, V_{FB} = V_{CCI} = 1.2V	R_{TON} = 96.75kΩ	142		192	ns
			R_{TON} = 200kΩ	300		366	
			R_{TON} = 303.25kΩ	425		575	
Minimum FB and CCI Voltages for Pseudo-Fixed-Frequency Operation		Switching frequency is reduced if FB and/or CCI are less than this value				0.25	V
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)				375	ns
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		DPRSTP = high, DPRSLPVR = high, R_{TIME} = 35.7kΩ to 178kΩ, SR = 6.25mV/µs nominal to 1.25mV/µs nominal		-20		+20	
		Startup and shutdown, R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-20		+20	
BIAS AND REFERENCE							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, FB forced above the regulation point, DPRSLPVR = V_{CC}				10	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, FB forced above the regulation point, DPRSLPVR = V_{CC}				1	µA
Shutdown Supply Current (V_{CC})	$I_{CC(SHDN)}$	Measured at V_{CC}, SHDN = GND				1	µA
Shutdown Supply Current (V_{DD})	$I_{DD(SHDN)}$	Measured at V_{DD}, SHDN = GND				1	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, I_{REF} = 0		1.98		2.02	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = 0 to 500µA		-2			mV
		I_{REF} = -100µA to 0				6.2	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0-D6 = 0001100). **T_A = -40°C to +105°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Output Overvoltage Protection Threshold (MAX8770/MAX8771 Only)	V_{OVP}	Measured at FB with respect to unloaded output voltage, rising edge, PWM mode, or skip mode after output reaches the regulation voltage		250		350	mV
		Measured at FB, rising edge	Skip mode and output have not reached the regulation voltage	1.75		1.85	V
Output Undervoltage Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		-450		-350	mV
CLKEN Startup Delay (Boot Time Period)	t_{BOOT}	Measured from the time when FB reaches the boot target voltage based on the slew rate set by R_{TIME}		20		100	µs
PWRGD, PHASEGD Startup Delay	t_{PWRGD}	Measured at startup from the time when CLKEN goes low		3		8	ms
$\overline{CLKEN}$, PWRGD Threshold		Measured at FB with respect to unloaded output voltage	Lower threshold, falling edge (undervoltage)	-350		-250	mV
		15mV hysteresis (typ)	Upper threshold, rising edge (overvoltage)	+150		+250	
PHASEGD Window Comparator Thresholds		V(CCI,FB), 0.4V ≤ V(FB) ≤ 1.5V	Lower threshold, 0.6V_{FB} nominal	-20		+20	mV
		15mV hysteresis (typ)	Upper threshold, 1.4V_{FB} nominal	-20		+20	
$\overline{CLKEN}$, PWRGD, PHASEGD Output Low Voltage		I_{SINK} = 3mA				0.4	V
$\overline{VRHOT}$ Trip Threshold	V_{HOT}	Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5		30.5	%
$\overline{VRHOT}$ Output On-Resistance	R_{VRHOT}	Low state				11	Ω
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 50mV hysteresis, DL_ pulled low below this level		4.1		4.45	V
DROOP AND BALANCE							
DC Droop Amplifier Offset				-1.5		+1.5	mV
DC Droop Amplifier Transconductance	$G_{m(FB)}$	$\Delta I_{FB}/(\Sigma\Delta V_{CS})$, V_{FB} = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = 0 to +60mV		580		620	µs
Current-Balance Preamplifier Offsets		[V(CSPI, CSN_) - V(CPS2, CSN_)] at I_{CCI} = 0		-1.5		+1.5	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{DD} = V_{CC} = $V_{\overline{SHDN}}$ = $V_{\overline{PSI}}$ = $V_{\overline{DPRSTP}}$ = 5V, DPRSLPVR = GNDS = PGND_ = GND, V_{FB} = V_{CCI} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1.200V, D0–D6 set for 1.20V (D0-D6 = 0001100). **T_A = -40°C to +105°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT LIMIT							
Valley Current-Limit Threshold (Positive)	V_{LIMIT}	CSP_ - CSN_		18.5		26.5	mV
Valley Current-Limit Threshold (Negative)		CSP_ - CSN_		-36		-24	mV
Current-Sense Common-Mode Input Range		CSP_, CSN_		0		2	V
Phase 2 Disable Threshold		CSP2		3		V_{CC} - 0.4	V
GATE DRIVERS							
DH_ Gate Driver On-Resistance	$R_{ON(DH\_)}$	BST_ – LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.5	
DL_ Gate Driver On-Resistance	$R_{ON(DL\_)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.5	
Driver Propagation Delay		DH_ Low to DL_ High		15			ns
		DL_ Low to DH_ High		9			
Internal Boost Charging Switch On-Resistance		V_{DD} to BST_				20	Ω
POWER MONITOR							
Power-Monitor Output Voltage for Typical HFM Conditions		V_{FB} - V_{GNDS} = 1.200V, $\Sigma\Delta V_{CS}$ = 30mV		2.04		2.28	V
Power-Monitor Gain Referred to Feedback Voltage		$\Sigma\Delta V_{CS}$ = 30mV		1.70		1.90	V/V
Power-Monitor Gain Referred to ΣV(CSP_,CSN)		V_{FB} - V_{GNDS} = 1.200V		70		74	V/V
Power-Monitor Load Regulation		Sourcing: I_{POUT} = 0 to 500µA		-6			µV/µA
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, DPRSLPVR, rising edge, hysteresis = 200mV		1.2		2.3	V
Low-Voltage Logic-Input High	V_{IHLV}	D0–D6, $\overline{PSI}$, DRPSTP		0.67			V
Low-Voltage Logic-Input Low	V_{ILLV}	D0–D6, $\overline{PSI}$, DRPSTP				0.33	V

Note 2: DC output accuracy specifications refer to the trip level of the error amplifier. The output voltage has a DC regulation higher than the trip level by 50% of the output ripple. When pulse skipping, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

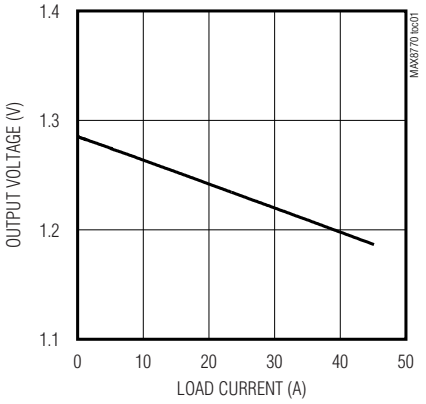
Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ and DH_ pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

Note 4: Specifications to T_A = -40°C and +105°C are guaranteed by design and are not production tested.

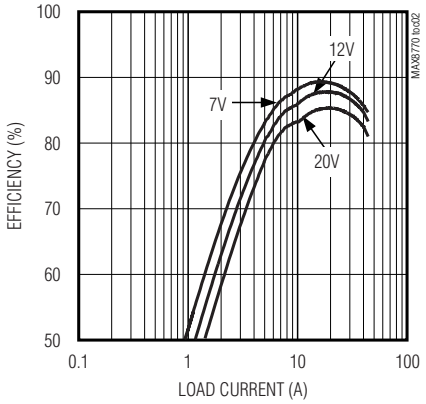
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, $\overline{SHDN}$ = $\overline{PSI}$ = 5V, DPRSLPVR = GND, D0–D6 set for 1.1500V, T_A = 25°C, unless otherwise specified.)

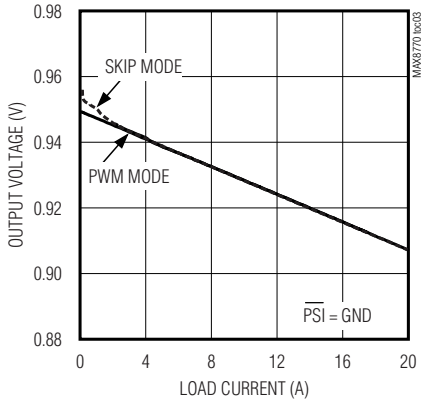
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.2875V)



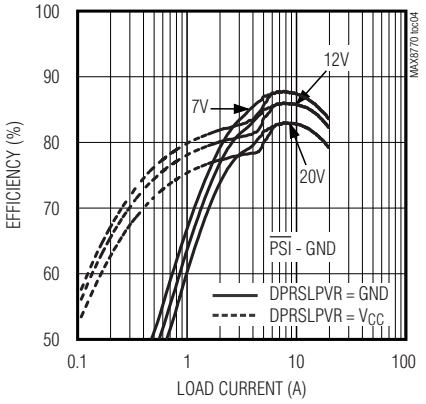
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.2875V)



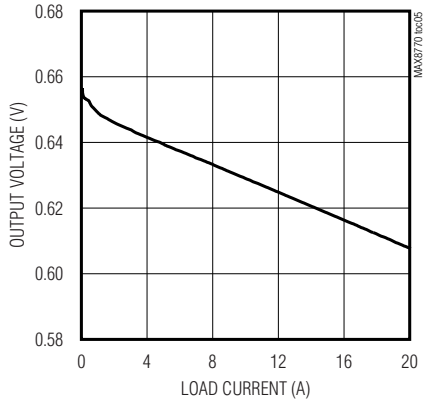
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.9500V)



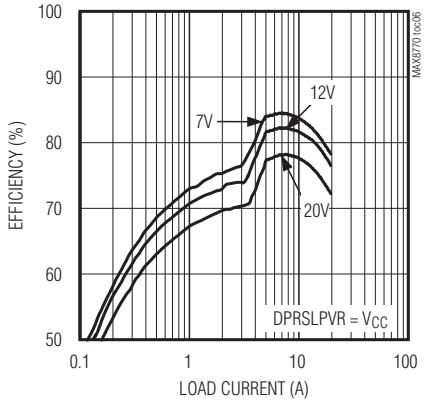
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.9500V)



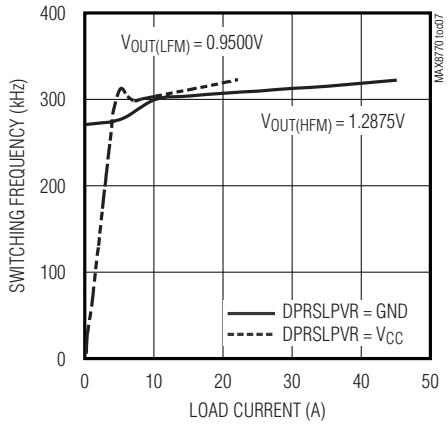
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(C4)}$ = 0.6500V)



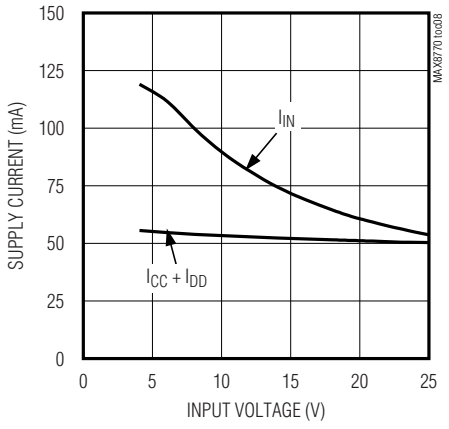
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(C4)}$ = 0.6500V)



SWITCHING FREQUENCY vs. LOAD CURRENT



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE ($V_{OUT(HFM)}$ = 1.2875V)

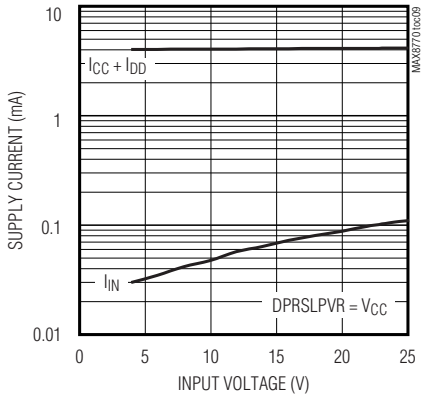


MAX8770/MAX8771/MAX8772 Dual-Phase, Quick-PWM Controller for IMVP-6+ CPU Core Power Supplies

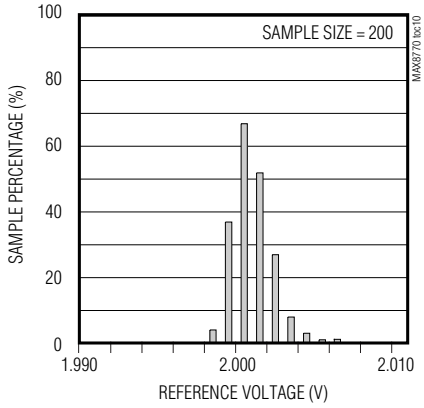
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, $\overline{SHDN}$ = $\overline{PSI}$ = 5V, DPRSLPVR = GND, D0–D6 set for 1.1500V, T_A = 25°C, unless otherwise specified.)

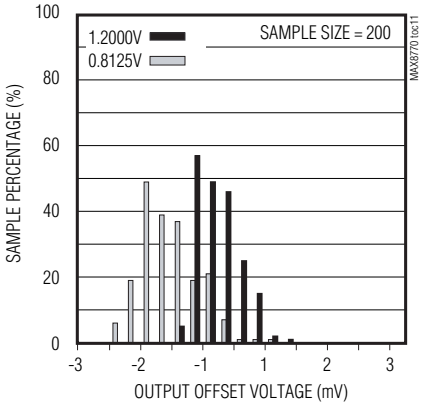
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE AT SKIP MODE



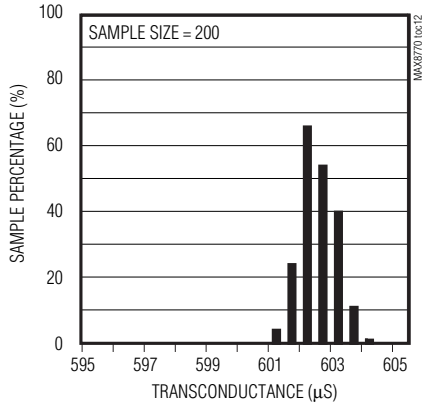
REFERENCE VOLTAGE DISTRIBUTION



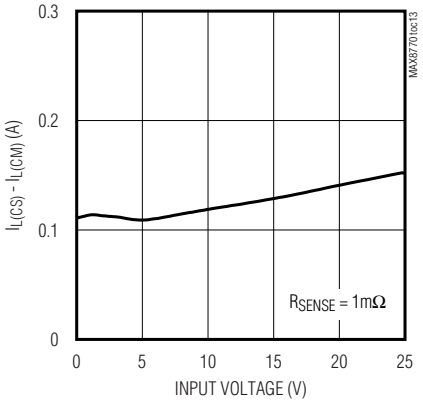
OUTPUT OFFSET VOLTAGE DISTRIBUTION



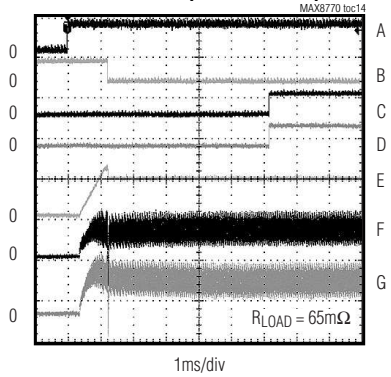
$G_{m(FB)}$ TRANSCONDUCTANCE DISTRIBUTION



INDUCTOR CURRENT DIFFERENCE vs. LOAD CURRENT

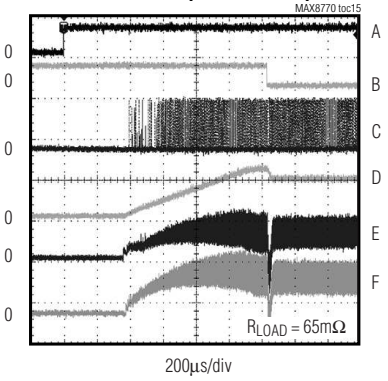


SOFT-START (UP TO PWRGD)



A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 10V/div
C. PWRGD, 10V/div
D. PHASEGD, 10V/div
E. V_{OUT}, 1V/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10V/div

SOFT-START (UP TO $\overline{CLKEN}$)

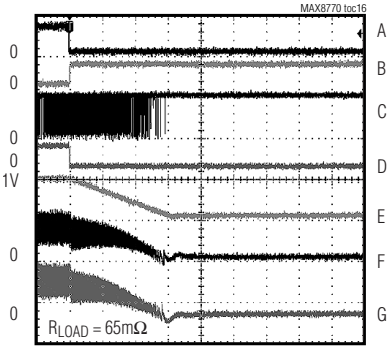


A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 10V/div
C. LX1, 10V/div
D. V_{OUT}, 1V/div
E. I_{LX1}, 10A/div
F. I_{LX2}, 10V/div

Typical Operating Characteristics (continued)

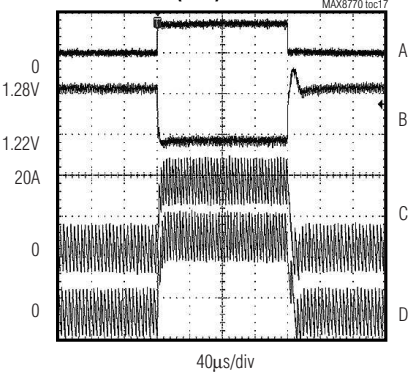
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, $\overline{SHDN}$ = $\overline{PSI}$ = 5V, DPRSLPVR = GND, D0–D6 set for 1.1500V, T_A = 25°C, unless otherwise specified.)

SHUTDOWN WAVEFORMS



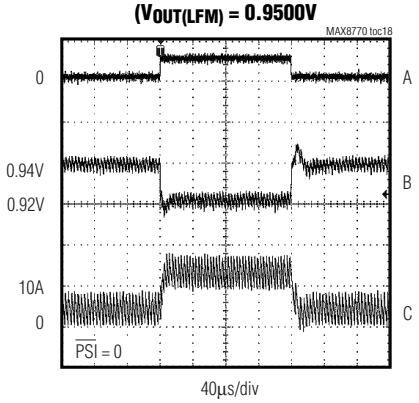
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 10V/div
C. DL1, 10V/div
D. PWRGD, 10V/div
E. V_{OUT}, 1V/div
F. I_{LXI}, 10A/div
G. I_{LX2}, 10V/div

HFM LOAD TRANSIENT ($V_{OUT(HFM)}$ = 1.2875V



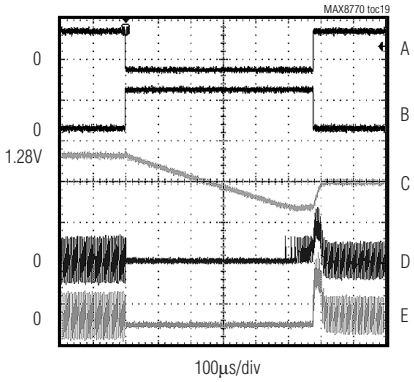
A. I_{OUT} = 5A TO 36A, 10A/div
B. V_{OUT}, 50mV/div
C. I_{LXI}, 10A/div
D. I_{LX2},10A/div

LFM LOAD TRANSIENT ($V_{OUT(LFM)}$ = 0.9500V



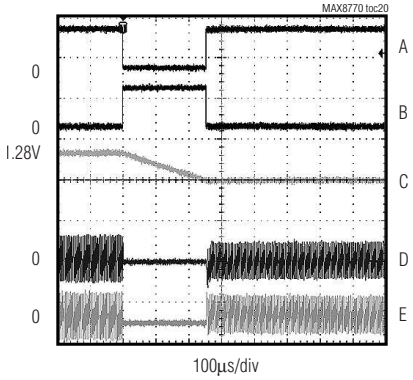
A. I_{OUT} = 5A TO 15A, 10A/div
B. V_{OUT}, 50mV/div
C. I_{LXI}, 10A/div
D. I_{LX2},10A/div

ENTERING DEEPER SLEEP EXITING TO LFM



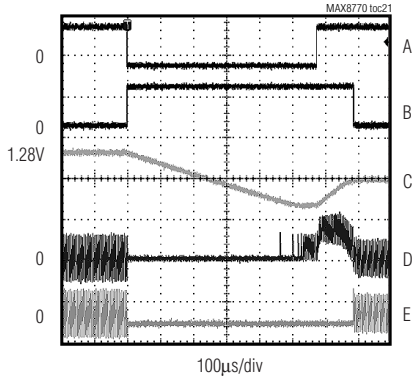
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 5V/div
C. V_{OUT}, 500mV/div
I_{OUT} = 2A
D. I_{LXI}, 10A/div
E. I_{LX2}, 10A/div

ENTERING DEEPER SLEEP EXITING TO NEAREST VID



A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 5V/div
C. V_{OUT}, 500mV/div
I_{OUT} = 2A
D. I_{LXI}, 10A/div
E. I_{LX2}, 10A/div

ENTERING DEEPER SLEEP EXITING TO LFM



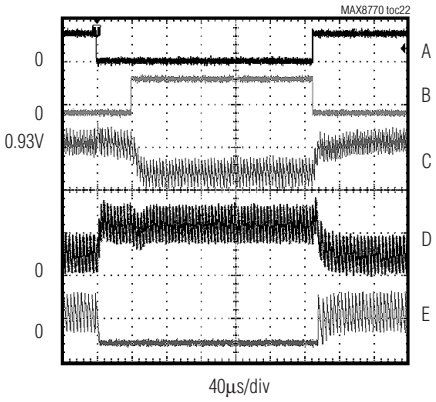
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 5V/div
C. V_{OUT}, 500mV/div
I_{OUT} = 2A
D. I_{LXI}, 10A/div
E. I_{LX2}, 10A/div

MAX8770/MAX8771/MAX8772 Dual-Phase, Quick-PWM Controller for IMVP-6+ CPU Core Power Supplies

Typical Operating Characteristics (continued)

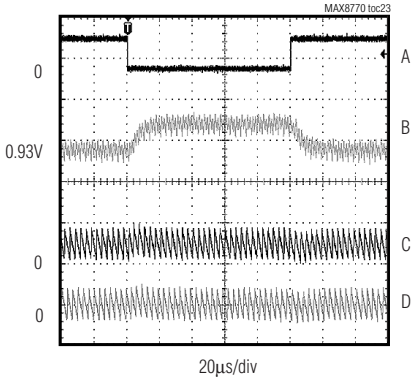
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD}, $\overline{SHDN}$ = $\overline{PSI}$ = 5V, DPRSLPVR = GND, D0–D6 set for 1.1500V, T_A = 25°C, unless otherwise specified.)

$\overline{PSI}$ + 1-LSB TRANSITION



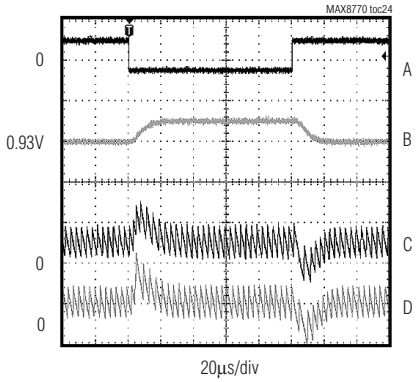
A. $\overline{PSI}$, 5V/div
B. D0, 5V/div
C. V_{OUT}, 20mV/div
I_{OUT} = 10A
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div

D0 DYNAMIC VID CODE CHANGE



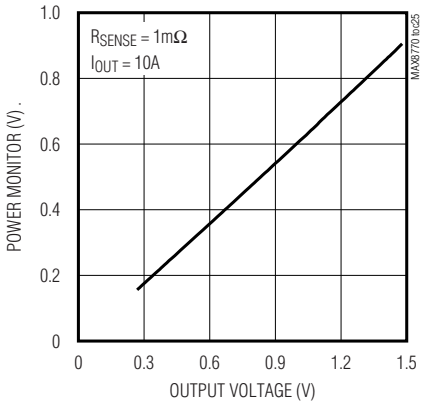
A. D0, 5V/div
B. V_{OUT}, 20mV/div
I_{OUT} = 10A
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

D3 DYNAMIC VID CODE CHANGE

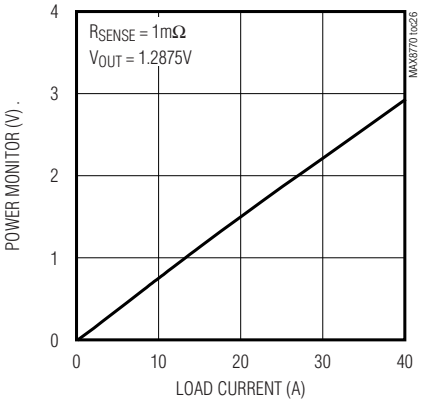


A. D3, 5V/div
B. V_{OUT}, 200mV/div
I_{OUT} = 10A
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

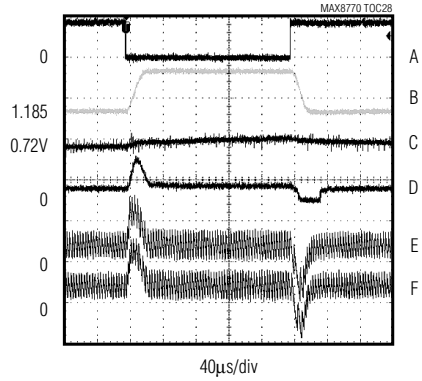
POWER MONITOR vs. OUTPUT VOLTAGE



POWER MONITOR vs. LOAD CURRENT



POWER MONITOR - VID TRANSITION RESPONSE



A. D3, 5V/div
B. V_{OUT}, 200mV/div
C. POUT WITH RC FILTER (10kΩ, 0.1µF), 200mV/div
D. POUT, 2V/div
E. I_{LX1}, 10A/div
F. I_{LX2}, 10A/div
I_{OUT} = 10A

Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{CLKEN}}$	Clock-Enable Logic Output. This inverted logic output indicates when the output voltage sensed at FB is in regulation. $\overline{\text{CLKEN}}$ is forced low during VID transitions. Except during startup, $\overline{\text{CLKEN}}$ is the inverse of PWRGD. See the *Startup Timing Diagram* (Figure 9). When in pulse-skipping mode (DPRSLPVR high), the upper $\overline{\text{CLKEN}}$ threshold is disabled.
2	PWRGD	Open-Drain, Power-Good Output. After output-voltage transitions, except during power-up and power-down, if FB is in regulation then PWRGD is high impedance. During startup, PWRGD is held low and continues to be low while the part is in boot mode and until 5ms (typ) after $\overline{\text{CLKEN}}$ goes low. PWRGD is forced low in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). When in pulse-skipping mode (DPRSLPVR high), the upper PWRGD threshold comparator is blanked. A pullup resistor on PWRGD causes additional finite shutdown current.
3	$\overline{\text{PSI}}$	Logic Input to Indicate Power Usage. $\overline{\text{PSI}}$ and DPRSLPVR together determine the operating mode as shown in the truth table below. Blank the PWRGD upper threshold when the part is in skip mode. **The part is forced into full-phase PWM mode during startup, while in boot mode, during the transition from boot mode to VID mode and during shutdown:** DPRSLPVR / $\overline{\text{PSI}}$ / Mode 1 / 0 / Very low current (1-phase skip) 1 / 1 / Low current (approximately 3A) (1-phase skip) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (2- or 1-phase PWM as configured at CSP2)
4	POUT	Power-Monitor Output: $V_{POUT} = K_{PWR} \times V(CSNpm, GNDS) \times \Sigma V(CSP\_, CSN\_)$, where K_{PWR} is the power monitor scale factor: CSNpm = CSN12 for MAX8771. CSNpm = CSN2 for MAX8770/MAX8772. POUT is zero in shutdown.
5	$\overline{\text{VRHOT}}$	Open-Drain Output of Internal Comparator. $\overline{\text{VRHOT}}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{\text{VRHOT}}$ is high impedance in shutdown.
6	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components such that the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
7	TIME	Slew-Rate Adjustment Pin. Connect a resistor R_{TIME} from TIME to GND to set the internal slew rate: $\text{Slew rate} = (12.5\text{mV}/\mu\text{s}) \times (71.5\text{k}\Omega\_/ R_{TIME})$ where R_{TIME} is between 35.7kΩ and 178kΩ. This slew rate applies to transitions into and out of the low-power pulse-skipping modes (and to the transition from boot mode to VID mode. The slew rate for startup and shutdown is 1/8 this value. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the one set by R_{TIME} as defined above.
8	TON	Switching-Frequency Setting Input. An external resistor between the input power source and TON sets the switching period ($T_{SW} = 1/f_{SW}$) per phase according to the following equation: $T_{SW} = C_{TON} (R_{TON} + 6.5\text{k}\Omega)$ where C_{TON} = 16.26pF. TON is high impedance in shutdown.
9	CCV	Integrator Capacitor Connection. Connect a 470pF x $(2/\eta_{TOTAL})$ x 300kHz/f_{SW} capacitor from CCV to GND to set the integration time constant. The integrator is internally disabled when the part is in skip mode and the output is above regulation.

Pin Description (continued)

PIN	NAME	FUNCTION
10	CCI	Current-Balance Compensation. Connect a 470pF capacitor between CCI and the positive side of the feedback remote sense (or between CCI and GND). CCI is internally forced low in shutdown.
11	REF	2.0V Reference Output. Bypass to GND with a 1µF **maximum** low-ESR (ceramic) capacitor. Can source 500µA for external loads. Loading REF degrades OUT accuracy, according to the REF load-regulation error.
12	FB	Output of the DC-Voltage Positioning Transconductance Amplifier. Connect a resistor R_{FB} between FB and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $$R_{FB} = R_{DROOP} / (R_{SENSE} \times G_{m(FB)})$$ where R_{DROOP} is the desired voltage-positioning slope and $G_{m(FB)}$ = 600µS (typ). R_{SENSE} is the value of the current-sense resistors that are used to provide the (CSP_, CSN_) current-sense voltages. If lossless sensing is used, $R_{SENSE} = R_L$. In this case, consider making R_{FB} a resistor network that includes an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope. DC droop can be disabled by shorting FB to the positive remote-sense point. FB is high impedance in shutdown.
13	GNDS	Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS internally connects to a transconductance amplifier that fine tunes the output voltage— compensating for voltage drops from the regulator ground to the load ground.
14	CSP2	Positive Input of the Output Current Sense of Phase 2. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. Tie this pin to V_{CC} for 1-phase operation.
15	CSN12 (MAX8771)	Combined Negative Current-Sense Input for Phases 1 and 2. The negative current-sense signals of the two phases (taken from the negative sides of the output current-sensing resistors or the filtering capacitors if the DC resistances of the output inductors are utilized for current sensing) are resistively averaged, and the resulting signal is connected to this pin. Pay special attention to board layout to maximize current-sensing accuracy; either place the sense elements (inductors for lossless sensing or sense resistors) close to each other, or equalize the layout paths and PC board trace resistances between the sense elements and the remote load. CSN12 is also used as the voltage input to the power monitor.
	CSN2 (MAX8770 /MAX8772)	Negative Input of the Output Current Sense of Phase 2. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. CSN2 is also used as the voltage input to the power monitor.
16	CSP1 (MAX8771)	Positive Input of the Output Current Sense of Phase 1. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
	CSN1 (MAX8770/ MAX8772)	Negative Input of the Output Current Sense of Phase 1. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.

Pin Description (continued)

PIN	NAME	FUNCTION
17	PHASEGD (MAX8771)	Open-Drain, Phase-Good Output. Used to signal the system that one of the two phases either has a fault condition or is not matched with the other. Detection is done by identifying the need for a large on-time difference between phases in order to achieve or move towards current balance. PHASEGD is low in shutdown. PHASEGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). PHASEGD is forced high impedance while in 1-phase operation (DPRSLPVR = high or $\overline{PSI}$ = low).
	CSP1 (MAX8770 MAX8772)	Positive Input of the Output Current Sense of Phase 1. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
18	GND	Analog Ground. Connect to the exposed backside pad and low-current analog ground terminations.
19	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
20	BST2	Boost Flying-Capacitor Connection for the DH2 high-side gate driver. An internal switch between V_{DD} and BST2 charges the flying capacitor during the time the low-side FET is on.
21	DH2	Phase-2, High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
22	LX2	Phase-2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to the phase 2's zero-crossing comparator.
23	PGND2	Power Ground for Phase 2. Ground connection for the DL2 driver. Also used as an input to phase 2's zero crossing comparator.
24	DL2	Phase-2, Low-Side Gate-Driver Output. DL2 swings from PGND2 to V_{DD}. DL2 is forced high in shutdown. DL2 is also forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. DL2 is forced low in skip mode (DPRSLPVR high) after an inductor current zero crossing (PGND2 - LX2) is detected. DL2 is forced low in 1-phase mode (TWO - PH = low).
25	V_{DD}	Supply Voltage Input for the DL1 and DL2 Drivers. V_{DD} is also the supply voltage used to internally recharge the BST1, BST2 flying capacitors during the off-times of the respective phases. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to PGND1 and PGND2 with a 1µF each or greater ceramic capacitors.
26	DL1	Phase 1, Low-Side Gate-Driver Output. DL1 swings from PGND1 to V_{DD}. DL1 is forced high in shutdown. DL1 is also forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. DL1 is forced low in skip mode (DPRSLPVR high) whenever an inductor current zero crossing (PGND1 - LX1) is detected.
27	PGND1	Power Ground for Phase 1. Ground connection for the DL1 driver. Also used as an input to the phase 1's zero crossing comparator.
28	LX1	Phase 1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to the phase-1's zero-crossing comparator.
29	DH1	Phase 1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
30	BST1	Boost Flying Capacitor Connection for the DH1 High-Side Gate Driver. An internal switch between V_{DD} and BST1 charges the flying capacitor during the time the low-side FET is on.

Pin Description (continued)

PIN	NAME	FUNCTION
31–37	D0–D6	Low-Voltage VID DAC Code Input. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 4).
38	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA max shutdown state. During startup, the output voltage is ramped up to the boot voltage slowly at a slew rate that is 1/8 the slew rate set by the TIME resistor. During the transition from normal operation to shutdown, the output voltage is ramped down at the same slow slew rate. Forcing $\overline{SHDN}$ to 11V~13V disables both OVP and UVP protection circuits, clears the fault latch, disables transient phase overlap, and disables the BST_ charging switches. Do not connect $\overline{SHDN}$ to > 13V.
39	DPRSLPVR	Logic Input to Indicate Power Usage. $\overline{PSI}$ and DPRSLPVR together determine the operating mode as shown in the truth table below. The PWRGD upper threshold is blanked when the part is in skip mode. **The part is forced into full-phase PWM mode during startup, while in boot mode, during the transition from boot mode to VID mode, and during shutdown.** DPRSLPVR / $\overline{PSI}$ / Mode 1 / 0 / Very low current (1-phase skip) 1 / 1 / Low current (approximately 3A) (1-phase skip) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: number of phases by CSP2)
40	$\overline{DPRSTP}$	1.0V Logic-Input Signal. This signal from the system is usually the logical complement of the DPRSLPVR signal. However, there is a special condition during C4 exit when both $\overline{DPRSTP}$ and DPRSLPVR could temporarily be simultaneously high. If this happens, the slew rate reduces to 1/4 of the normal (R_{TIME}-based) slew rate for the duration of this condition. The slew rate returns to normal when this condition is exited. Note that only DPRSLPVR and $\overline{PSI}$ (but not $\overline{DPRSTP}$) determine the mode of operation (PWM vs. skip) and the number of active phases: DPRSLPVR / $\overline{DPRSTP}$ / Functionality 0 / 0 / Normal slew rate, number of phases set by $\overline{PSI}$ and CSP2 (DPRSLPVR low → $\overline{DPRSTP}$ is ignored) 0 / 1 / Normal slew rate, number of phases set by $\overline{PSI}$ and CSP2 (DPRSLPVR low → $\overline{DPRSTP}$ is ignored) 1 / 0 / Normal slew rate, 1-phase skip mode 1 / 1 / Slew rate reduced to 1/4 of normal,1-phase skip mode
EP	EP	Exposed Backside Pad. Connect the exposed backside pad to AGND.

Table 1. Component Selection for Standard Applications

DESIGNATION	1.2875V/36A COMPONENTS (FIGURE 1)	1.1500V/44A COMPONENTS (FIGURE 1)	0.9000V/9A COMPONENTS (FIGURE 12)
Input Voltage Range	7V to 24V	7V to 24V	7V to 24V
VID Output Voltage (D6–D0)	1.2875V (D6–D0 = 0010001)	1.1500V (D6–D0 = 0011100)	0.9000V (D6–D0 = 0110000)
Load Line	-2.1mV/A	-2.1mV/A	-5.1mV/A
Maximum Load Current	36A	44A	9A
Inductor (per Phase)	0.36µH, 0.8mΩ NEC/Tokin MPC1055LR36	0.33µH, 0.82mΩ Panasonic ETQP5LR33XFC	0.56µH, 1.3mΩ NEC/Tokin MPC1040LR56
Switching Frequency	300kHz (R_{TON} = 200kΩ)	300kHz (R_{TON} = 200kΩ)	300kHz (R_{TON} = 200kΩ)
High-Side MOSFET (N_H, per Phase)	Siliconix (1) Si7892ADP	Siliconix (1) Si7892ADP	Siliconix (1) Si7892ADP
Low-Side MOSFET (N_L, per Phase)	Siliconix (2) Si7336ADP	Siliconix (2) Si7336ADP	Siliconix (1) Si7336ADP
Total Input Capacitance (C_{IN})	(4) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M	(4) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM or TDK C4532X5R1E106M
Total Output Capacitance (C_{OUT})	(4) 330µF, 2.5V, 6mΩ Panasonic EEFSX0D0D331XR	(4) 330µF, 2.5V, 6mΩ Panasonic EEFSX0D0D331XR	(2) 330µF, 2.5V, 6mΩ Panasonic EEFSX0D0D331XR
Current-Sense Resistor (R_{CS}, per Phase)	1.0mΩ Panasonic ERJM1WTJ1M0U	1.0mΩ Panasonic ERJM1WTJ1M0U	2.0mΩ Panasonic ERJM1WTJ2M0U

Table 2. Component Suppliers

MANUFACTURER	WEBSITE		MANUFACTURER	WEBSITE
AVX	www.avxcorp.com		Pulse	www.pulseeng.com
BI Technologies	www.bitechnologies.com		Renesas	www.renesas.com
Central Semiconductor	www.centralsemi.com		Sanyo	www.secc.co.jp
Fairchild Semiconductor	www.fairchildsemi.com		Siliconix (Vishay)	www.vishay.com
International Rectifier	www.irf.com		Sumida	www.sumida.com
Kemet	www.kemet.com		Taiyo Yuden	www.t-yuden.com
NEC/Tokin	www.nec-tokin.com		TDK	www.component.tdk.com
Panasonic	www.panasonic.com		TOKO	www.tokoam.com

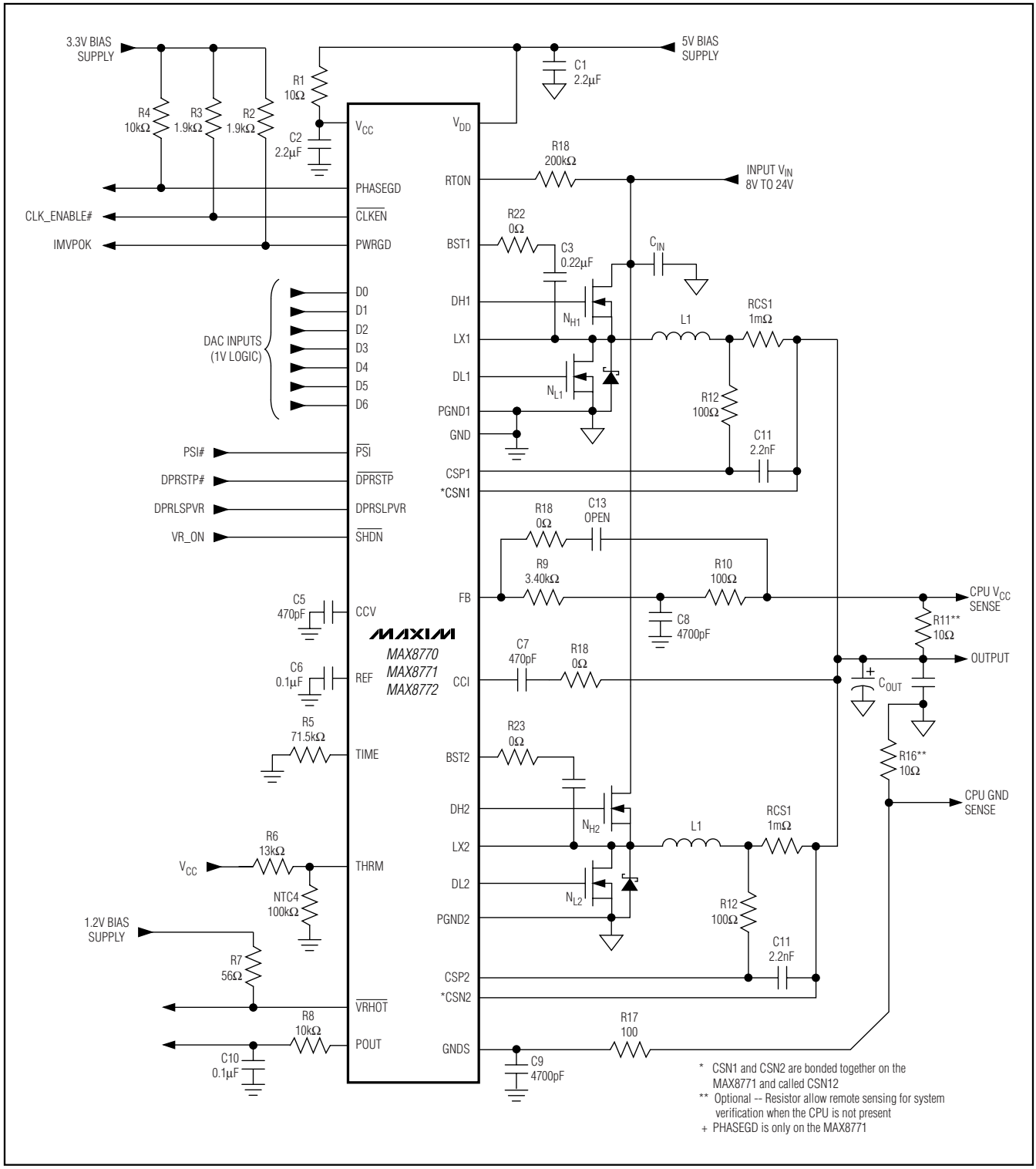


Figure 1. Standard 2-Phase IMVP-6 44A Application Circuit

MAX8770/MAX8771/MAX8772 Detailed Description

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 180° out-of-

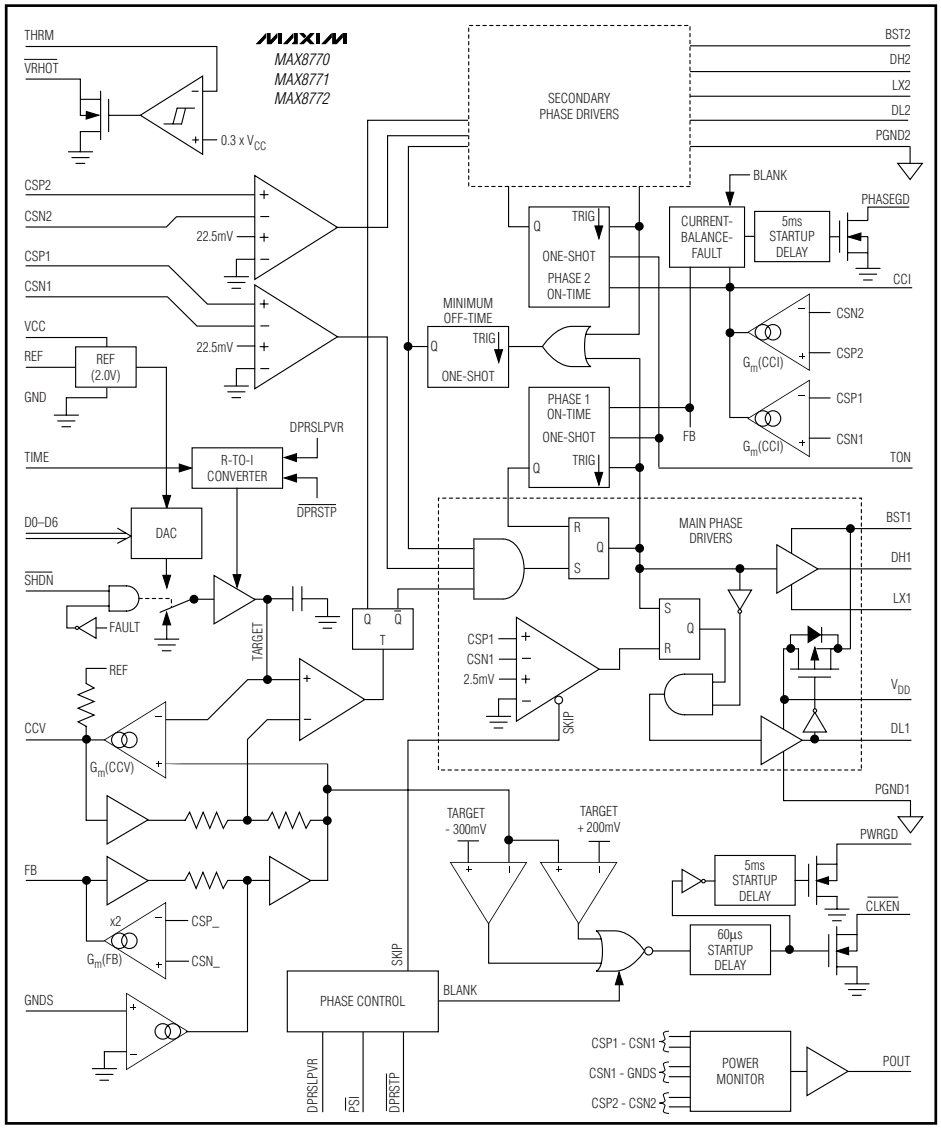


Figure 2. Functional Block Diagram

phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output voltage set point.

Dual 180° Out-of-Phase Operation

The two phases in the MAX8770/MAX8771/MAX8772 operate 180° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements— making the MAX8770/MAX8771/MAX8772 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide power using only 1 phase instead of dividing the power among several phases. In these applications, the input capacitors must support high instantaneous current requirements. The high RMS ripple current can lower efficiency due to I^2R® power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input voltage ripple, to reduce ESR-related power losses, and to meet the necessary RMS ripple current rating.

With the MAX8770/MAX8771/MAX8772, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively halved, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance may be achieved with fewer or less-expensive input capacitors.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} - f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$

where I_{CC} is provided in the *Electrical Characteristics* Table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be tied together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1/f_{SW}$, per phase:

$$T_{SW} = C_{TON} (R_{TON} + 6.5k\Omega)$$

where C_{TON} = 16.26pF.

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

On-Time One-Shot

The core of each phase contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFETs on-time. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage (V_{IN}), and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{T_{SW} (V_{FB} + 0.075V)}{V_{IN}}$$

where the switching period ($T_{SW} = 1/f_{SW}$) is set by the resistor at the TON pin, and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

The one-shot for the secondary phase varies the on-time in response to the input voltage and the difference between the main and secondary inductor currents. Two identical transconductance amplifiers integrate the difference between the master and slave current-sense signals. The summed output is internally connected to

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CCI, allowing adjustment of the integration time constant with a compensation network connected between CCI and FB. The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_M (V_{CMP} - V_{CMN}) - G_M (V_{CSP} - V_{CSN})$$

$$V_{CCI} = V_{FB} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output. The secondary on-time one-shot uses this integrated signal (V_{CCI}) to set the secondary high-side MOSFETs on-time. When the main and secondary current-sense signals ($V_{CM} = V_{CMP} - V_{CMN}$ and $V_{CS} = V_{CSP} - V_{CSM}$) become unbalanced, the transconductance amplifiers adjust the secondary on-time, which increases or decreases the secondary inductor current until the current-sense signals are properly balanced:

$$t_{ON(SEC)} = T_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$

$$= T_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + T_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$

= (Main On-Time)

+ (Secondary Current Balance Correction)

This algorithm results in a nearly constant switching frequency and balanced inductor currents, despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics* table. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range. For example, the 600kHz setting typically runs about 5% slower, with inputs much greater than +12V due to the very short on-times required.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PC board copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output-voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{\left(V_{OUT} + V_{DIS}\right)}{t_{ON}\left(V_{IN} + V_{DIS} - V_{CHG}\right)}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PC board resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PC board resistances; and t_{ON} is the on-time as determined above.

Current Sense

The output current of each phase is sensed. Low-offset amplifiers are used for current balance, voltage-positioning gain, and current limit. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 3). The resistive divider used should provide a current-sense resistance (R_{CS}) low enough to meet the current-limit requirements, and the time constant of the RC network should match the inductor's time constant (L/R_{CS}):

$$R_{CS} = \left(\frac{R2}{R1+R2}\right)R_{DCR} \text{ and}$$

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To

minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1||R2 to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and the Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step cause by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 3). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method above, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, and C_{EQ} and R_{EQ} are the time-constant matching components.

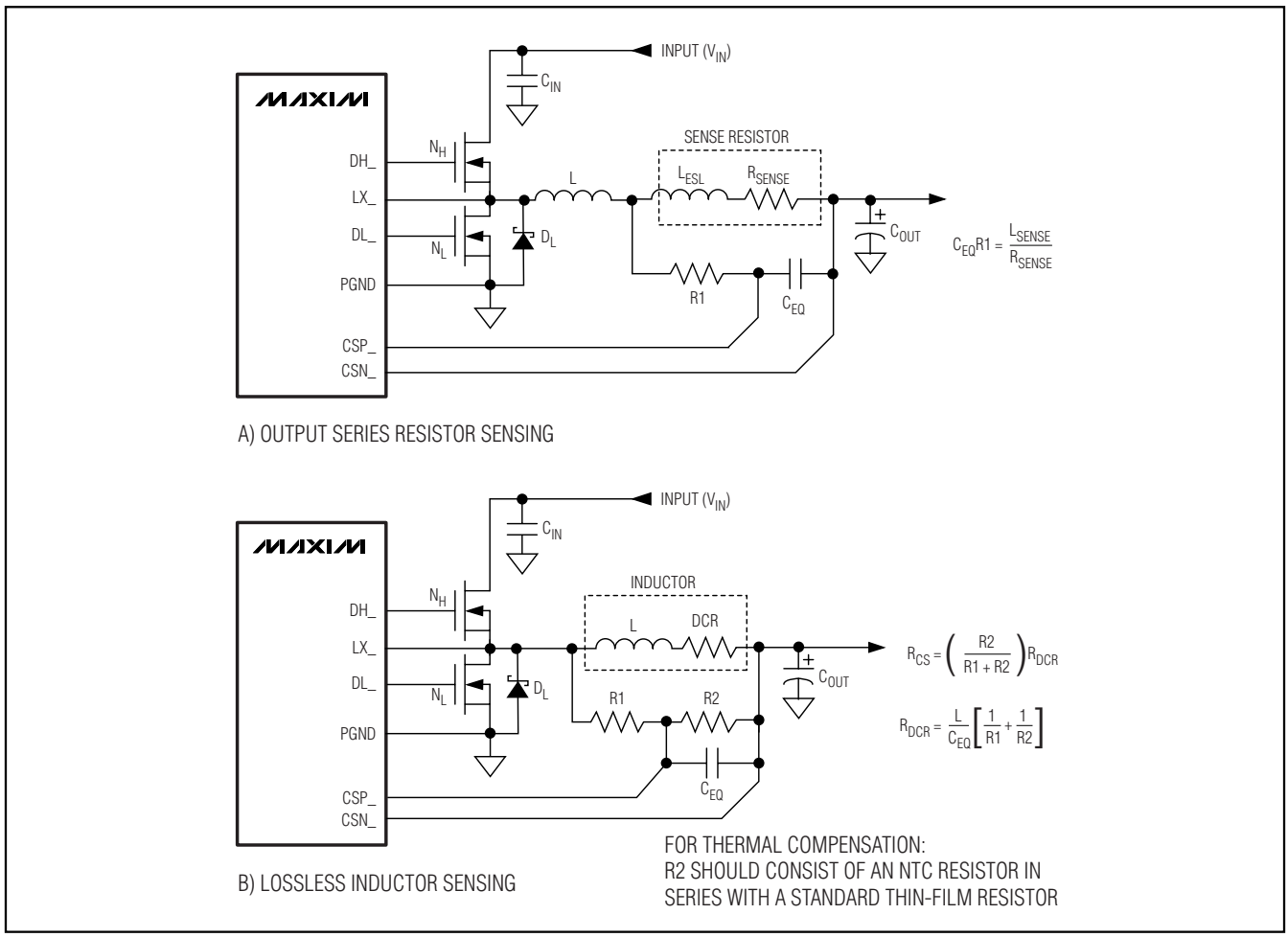

Figure 3. Current-Sense Methods

Current Balance

Without active current-balance circuitry, the current matching between phases depends on the MOSFETs' on-resistance ($R_{DS(ON)}$), thermal ballasting, on/off-time matching, and inductance matching. For example, variation in the low-side MOSFET on-resistance (ignoring thermal effects) results in a current mismatch that is proportional to the on-resistance difference:

$$I_{MAIN} - I_{SEC} = I_{MAIN}\left[1 - \left(\frac{R_{MAIN}}{R_{SEC}}\right)\right]$$

However, mismatches between on-times, off-times, and inductor values increase the worst-case current imbalance, making it impossible to passively guarantee accurate current balancing.

The MAX8770/MAX8771/MAX8772 integrate the difference between the current-sense voltages and adjust the on-time of the secondary phase to maintain current balance. The current balance now relies on the accuracy of the current-sense resistors instead of the inaccurate, thermally sensitive on-resistance of the low-side MOSFETs. With active current balancing, the current mismatch is determined by the current-sense resistor values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where $R_{SENSE} = R_{CM} = R_{CS}$ and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics* table .

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different di/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses current-sense resistors between the current-sense inputs (CSP_ to CSN12 for MAX8771, CSP_ to CSN_ for MAX8770/MAX8772) as the current-sensing elements. If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When either phase trips the current limit, both phases are effectively current limited since the interleaved controller does not initiate a cycle with either phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the UVP circuit, this current-limit method is effective in almost every circumstance.

The positive current-limit threshold is fixed internally at 22.5mV. There is also a negative current limit that prevents excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set at -30mV. When a phase drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PC board layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_). For the MAX8771, where the negative current-sense returns are to a common pin, it is recommended that the current-sense elements (sense resistor or inductor DCR) be placed close to each other to minimize any voltage differences that might arise due to trace impedance between the two common nodes.

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

The MAX8770/MAX8771/MAX8772 include a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by summing the current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)} \sum_{X=1}^{\eta_{PH}} V_{CSX}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FB)}$ is typically 600µS as defined in the *Electrical Characteristics* table.

Differential Remote Sense

The MAX8770/MAX8771/MAX8772 include differential, remote-sense inputs to eliminate the effects of voltage drops along the PC board traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}), and ground sense (GNDS) input directly to the processor's remote-sense outputs as shown in Figure 1.

Integrator Amplifier

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±60mV (typ), including DC offset and AC ripple. The integration time constant can be set easily with an external compensation capacitor at the CCV pin. Use a 470pF x ($2/\eta_{TOTAL}$) x 300kHz/f_{SW} or greater ceramic capacitor.

The MAX8770/MAX8771/MAX8772 disable the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (DPRSLPVR = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient-Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. In order to provide fast transient response, the MAX8770/MAX8771/MAX8772 support a phase-overlap mode that allows the dual regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After either high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on both high-side MOSFETs during the next on-time cycle. This maximizes the total inductor current slew rate. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires.

After the phase-overlap mode ends, the controller automatically begins with the opposite phase. For example, if the secondary phase provided the last on-time pulse before overlap operation began, the controller starts switching with the main phase when overlap operation ends.

Nominal Output-Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}), as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, the MAX8770/MAX8771/MAX8772 slew the target voltage from ground to the preset boot voltage.

DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output-voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings may cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the IMVP-6 (Table 4) specifications.