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EVALUATION KIT AVAILABLE

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

General Description

The MAX8819_ is a complete power solution for MP3 players and other handheld applications. The IC includes a battery charger, step-down converters, and WLED power. It features an input current-limit switch to power the IC from an AC-to-DC adapter or USB port, a 1-cell lithium ion (Li+) or lithium polymer (Li-Poly) charger, three step-down converters, and a step-up converter with serial step dimming for powering two to six white LEDs. All power switches for charging and switching the system load between battery and external power are included on-chip. No external MOSFETs are required. The MAX8819C offers a sequenced power-up/power-down of OUT1, OUT2, and then OUT3.

Maxim's Smart Power Selector™ makes the best use of AC-to-DC adapter power or limited USB power. Battery charge current and input current limit are independently set. Input power not used by the system charges the battery. Charge current is resistor programmable and the input current limit can be selected as 100mA, 500mA, or 1A. Automatic input selection switches the system load from battery to external power. In addition, on-chip thermal limiting reduces the battery charge rate to prevent charger overheating.

Applications

MP3 Players

Portable GPS Devices

Low-Power Handheld Products

Cellular Telephones

Digital Cameras

Handheld Instrumentation

PDAs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	SYS VOLTAGE (V)
MAX8819AETI+	-40°C to +85°C	28 TQFN-EP*	4.35
MAX8819BETI+	-40°C to +85°C	28 TQFN-EP*	5.3
MAX8819CETI+	-40°C to +85°C	28 TQFN-EP*	4.35

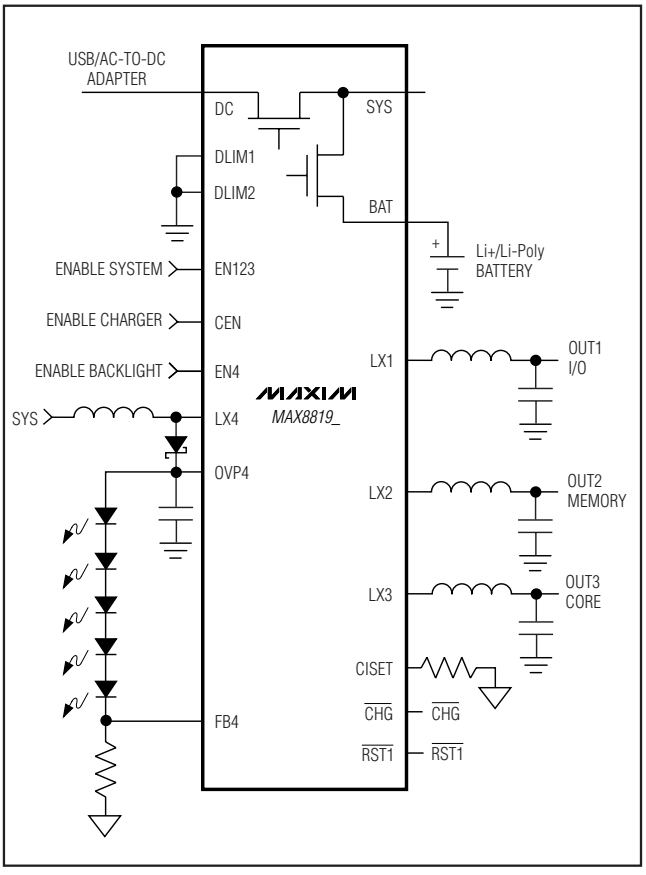
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

Features

- **Smart Power Selector**
- **Operates with No Battery Present**
- **USB/AC Adapter One-Cell Li+ Charger**
- **Three 2MHz Step-Down Converters**
  - **95% Peak Efficiency**
  - **100% Duty Cycle**
  - **±3% Output Accuracy over Load/Line/Temperature**
- **2 to 6 Series WLED Driver with Dimming Control**
- **Active-Low REG1 Reset Output**
- **Short-Circuit/Thermal-Overload/Input Undervoltage/Overvoltage Protection**
- **Power-Up/Down Sequencing (MAX8819C)**
- **Total Solution Size: Less Than 90mm²**

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

ABSOLUTE MAXIMUM RATINGS

DC, SYS, BAT, CISET, DLIM1, DLIM2, EN123
CEN, EN4, $\overline{CHG}$, $\overline{RST1}$, FB1, FB2, FB3 to GND....-0.3V to +6V
PV2 to GND.....-0.3V to (V_{SYS} + 0.3V)
PV13 to SYS.....-0.3V to +0.3V
PG1, PG2, PG3, PG4 to GND.....-0.3V to +0.3V
COMP4, FB4 to GND .....-0.3V to (V_{SYS} + 0.3V)
LX4 to PG4 .....-0.3V to +33V
OVP4 to GND .....-0.3V to +33V
LX1, LX2, LX3 Continuous Current (Note 1) 1.5A
LX4 Current .....750mA_{RMS}
Output Short-Circuit Duration.....Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN Single-Layer Board (derate 20.8mW/°C above +70°C).....1666.7mW
28-Pin Thin QFN Multilayer Board (derate 28.6mW/°C above +70°C).....2285.7mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 2)
28-Lead Thin QFN.....3°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....-40°C to +125°C
Storage Temperature.....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX1, LX2, LX3 have clamp diodes to their respective PG_ and PV_. Applications that forward bias these diodes must take care not to exceed the package power dissipation limits.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **http://www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DC, LX_ unconnected; $V_{EP} = V_{GND} = 0V$, $V_{BAT} = 4V$, DLIM[1:2] = 00, EN123 = EN4 = low, $V_{FB1} = V_{FB2} = V_{FB3} = 1.1V$, $V_{FB4} = 0.6V$, PV13 = PV2 = SYS, T_A = -40°C to +85°C, capacitors as shown in Figure 1, R_{CISET} = 3kΩ, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC POWER INPUT							
DC Voltage Range	V_{DC}			4.1		5.5	V
SYS Regulation Voltage	V_{SYS_REG}	V_{DC} = 5.75V	MAX8819A/MAX8819C	4.3	4.35	4.4	V
			MAX8819B	5.1	5.3	5.5	
DC Undervoltage Threshold	V_{UVLO_DC}	V_{DC} rising, 500mV typical hysteresis		3.95	4.00	4.05	V
DC Overvoltage Threshold	V_{OVLO_DC}	V_{DC} rising, 300mV typical hysteresis		5.811	5.9	6.000	V
DC Current Limit (Note 4)	I_{DCLIM}	V_{DC} = 5.75V, V_{SYS} = 5V for MAX8819B or V_{SYS} = 4V for MAX8819A/MAX8819C	DLIM[1:2] = 10	90	95	100	mA
			DLIM[1:2] = 01	450	475	500	
			DLIM[1:2] = 00	900	1000	1100	
DC Quiescent Current	I_{DCIQ}	DLIM[1:2] = 11 (suspend)			0.02	0.035	mA
		DLIM[1:2] ≠ 11, I_{SYS} = 0mA, I_{BAT} = 0mA, EN123 = low, EN4 = low, CEN = high, V_{DC} = 5.5V			1.33		
		DLIM[1:2] ≠ 11, I_{SYS} = 0mA, EN123 = low, EN4 = low, CEN = low, V_{DC} = 5.5V			0.95		
DC-to-SYS Dropout Resistance	R_{DS}	V_{DC} = 4V, I_{SYS} = 400mA, DLIM[1:2] = 01			0.330	0.700	Ω
DC-to-SYS Soft-Start Time	t_{SS-D-S}				1.5		ms
DC Thermal-Limit Temperature		Die temperature where current limit is reduced			100		°C
DC Thermal-Limit Gain		Amount of input current reduction above thermal-limit temperature			5		%/°C
SYSTEM							
System Operating Voltage Range	V_{SYS}			2.6		5.5	V

ELECTRICAL CHARACTERISTICS (continued)

(DC, LX_ unconnected; $V_{EP} = V_{GND} = 0V$, $V_{BAT} = 4V$, DLIM[1:2] = 00, EN123 = EN4 = low, $V_{FB1} = V_{FB2} = V_{FB3} = 1.1V$, $V_{FB4} = 0.6V$, PV13 = PV2 = SYS, T_A = -40°C to +85°C, capacitors as shown in Figure 1, $R_{CISET} = 3k\Omega$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
System Undervoltage Lockout Threshold	V_{UVLO_SYS}	V_{SYS} falling, 100mV hysteresis	2.45	2.5	2.55	V
BAT-to-SYS Reverse Regulation Voltage	V_{BSREG}	DC and BAT are delivering current to SYS; $I_{BAT} = 95mA$; $V_{DC} = 4.3V$, MAX8819A/MAX8819C (only)	50	66	90	mV
Quiescent Current	$I_{SYS} + I_{PV13} + I_{PV2}$	$V_{DC} = 0V$, EN123 = low, EN4 = low, $V_{BAT} = 4V$		10	20	µA
		$V_{DC} = 5V$, DLIM[1:2] ≠ 11, EN123 = low, EN4 = low, $V_{BAT} = 4V$		0	10	
		$V_{DC} = 0V$, EN123 = high, EN4 = low, $V_{BAT} = 4V$ (step-down converters are not in dropout)		128	290	
		$V_{DC} = 0V$, EN123 = high, EN4 = high, $V_{BAT} = 4V$ (step-down converters are not in dropout)		362	730	
BATTERY CHARGER (V_{DC} = 5.0V)						
BAT-to-SYS On-Resistance	R_{BS}	$V_{DC} = 0V$, $V_{BAT} = 4.2V$, $I_{SYS} = 0.9A$		0.073	0.165	Ω
BAT Regulation Voltage (Figure 2)	V_{BATREG}	T_A = +25°C	4.174	4.200	4.221	V
		T_A = -40°C to +85°C	4.158	4.200	4.242	
BAT Recharge Threshold		(Note 4)	-135	-100	-65	mV
BAT Prequalification Threshold	V_{BATPRQ}	V_{BAT} rising, 180mV hysteresis, Figure 2	2.9	3.0	3.1	V
R_{CISET} Resistance Range		Guaranteed by BAT fast-charge current limit	3		15	kΩ
CISET Voltage	V_{CISET}	$R_{CISET} = 7.5k\Omega$, $I_{BAT} = 267mA$	0.9	1.0	1.1	V
BAT Fast-Charge Current Limit	I_{CHGMAX}	DLIM[1:2] = 10, $R_{CISET} = 3k\Omega$	87	92	100	mA
		DLIM[1:2] = 01, $R_{CISET} = 3k\Omega$	450	472	500	
		DLIM[1:2] = 00, $R_{CISET} = 15k\Omega$	170	200	230	
		DLIM[1:2] = 00, $R_{CISET} = 7.5k\Omega$	375	400	425	
		DLIM[1:2] = 00, $R_{CISET} = 3.74k\Omega$	740	802	860	
BAT Prequalification Current	$I_{PREQUAL}$	$V_{BAT} = 2.5V$, $R_{CISET} = 3.74k\Omega$	60	82	105	mA
Top-Off Threshold (Note 5)	I_{TOPOFF}	T_A = +25°C, $R_{CISET} = 3.74k\Omega$	60	82	105	mA
BAT Leakage Current		$V_{DC} = 0V$, EN123 = low, EN4 = low, CEN = low, $V_{BAT} = 4V$		10	20	µA
		$V_{DC} = 5V$, DLIM[1:2] = 11, EN123 = low, EN4 = low, $V_{BAT} = 4V$		0		

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

ELECTRICAL CHARACTERISTICS (continued)

(DC, LX_ unconnected; V_{EP} = V_{GND} = 0V, V_{BAT} = 4V, DLIM[1:2] = 00, EN123 = EN4 = low, V_{FB1} = V_{FB2} = V_{FB3} = 1.1V, V_{FB4} = 0.6V, PV13 = PV2 = SYS, T_A = -40°C to +85°C, capacitors as shown in Figure 1, R_{CISET} = 3kΩ, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Charger Soft-Start Time	t_{SS_CHG}	Slew rate			333		mA/ms
		Time from 0 to 500mA			1.5		ms
		Time from 0 to 100mA			0.3		
		Time from 100mA to 500mA			1.2		
Timer Accuracy						+15	%
Timer Suspend Threshold		CISET voltage when the fast-charge timer suspends; 300mV translates to 20% of the maximum fast-charge current limit		250	300	350	mV
Timer Extend Threshold		CISET voltage when the fast-charge timer extends; 750mV translates to 50% of the maximum fast-charge current limit		700	750	800	mV
Prequalification Time	$t_{PREQUAL}$				33		min
Fast-Charge Time	t_{FSTCHG}				660		min
Top-Off Time	t_{TOPOFF}				33		min
POWER SEQUENCING (Figures 6 and 7)							
REG1, REG2, REG3 Soft-Start Time	t_{SS1}, t_{SS2}, t_{SS3}				2.6		ms
REG4 Soft-Start Time	t_{SS4}	C_{COMP4} = 0.022µF to GND			5		ms
REGULATOR THERMAL SHUTDOWN							
Thermal Shutdown Temperature		T_J rising			+165		°C
Thermal Shutdown Hysteresis					15		°C
REG1–SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV13 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_{LSR} = 0.13Ω (Note 6)	MAX8819A/MAX8819B	400			mA
			MAX8819C	550			
Short-Circuit Current		L = 4.7µH, R_{LSR} = 0.13Ω			600		mA
Short-Circuit Detection Threshold					230		mV
Short-Circuit Foldback Frequency					f_{OSC}/3		Hz
FB1 Voltage		(Note 7)		0.997	1.01	1.028	V
Output Voltage Range				1		V_{SYS}	V
FB1 Leakage Current		V_{FB1} = 1.01V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-10		
Load Regulation		I_{OUT1} = 100mA to 300mA			1		%
Line Regulation		(Note 9)			1		%/D
p-Channel On-Resistance		V_{PV13} = 4.0V, I_{LX1} = 180mA			190		mΩ
n-Channel On-Resistance		V_{PV13} = 4.0V, I_{LX1} = 180mA			250		mΩ
p-Channel Current-Limit Threshold		MAX8819A/MAX8819B		0.565	0.600	0.640	A
		MAX8819C		0.615	0.650	0.750	

ELECTRICAL CHARACTERISTICS (continued)

(DC, LX_ unconnected; $V_{EP} = V_{GND} = 0V$, $V_{BAT} = 4V$, DLIM[1:2] = 00, EN123 = EN4 = low, $V_{FB1} = V_{FB2} = V_{FB3} = 1.1V$, $V_{FB4} = 0.6V$, PV13 = PV2 = SYS, T_A = -40°C to +85°C, capacitors as shown in Figure 1, $R_{CISET} = 3k\Omega$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Skip-Mode Transition Current		(Note 8)			80		mA
n-Channel Zero-Crossing Threshold					10		mA
Maximum Duty Cycle				100			%
Minimum Duty Cycle					12.5		%
PWM Frequency	f_{OSC}			1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN123 = low, resistance from LX1 to PG1			1.0		kΩ
REG2–SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV2 supplied from SYS			V_{SYS}		V
Maximum Output Current		L = 4.7µH, R_{LSR} = 0.13Ω (Note 6)	MAX8819A/MAX8819B	300			mA
			MAX8819C	500			
Short-Circuit Current		L = 4.7µH, R_{LSR} = 0.13Ω			600		mA
Short-Circuit Detection Threshold					230		mV
Short-Circuit Foldback Frequency					$f_{OSC}/3$		Hz
FB2 Voltage		(Note 7)		0.997	1.012	1.028	V
Output Voltage Range				1		V_{SYS}	V
FB2 Leakage Current		V_{FB2} = 1.01V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-50		
Load Regulation		I_{OUT2} = 100mA to 300mA			1		%
Line Regulation		(Note 9)			1		%/D
p-Channel On-Resistance		V_{PV2} = 4.0V, I_{LX2} = 180mA			290		mΩ
n-Channel On-Resistance		V_{PV2} = 4.0V, I_{LX2} = 180mA			200		mΩ
p-Channel Current-Limit Threshold		MAX8819A/MAX8819B		0.512	0.550	0.595	A
		MAX8819C		0.565	0.600	0.700	
Skip-Mode Transition Current		(Note 8)			80		mA
n-Channel Zero-Crossing Threshold					10		mA
Maximum Duty Cycle				100			%
Minimum Duty Cycle					12.5		%
PWM Frequency	f_{OSC}			1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN123 = low, resistance from LX2 to PG2			1.0		kΩ
REG2 Disable	ΔI_{SYS}	V_{PV2} = 0V, REG2 disabled (Note 10)			-25		µA
REG3–SYNCHRONOUS STEP-DOWN CONVERTER							
Input Voltage		PV13 supplied from SYS			V_{SYS}		V

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

ELECTRICAL CHARACTERISTICS (continued)

(DC, LX_ unconnected; V_{EP} = V_{GND} = 0V, V_{BAT} = 4V, DLIM[1:2] = 00, EN123 = EN4 = low, V_{FB1} = V_{FB2} = V_{FB3} = 1.1V, V_{FB4} = 0.6V, PV13 = PV2 = SYS, T_A = -40°C to +85°C, capacitors as shown in Figure 1, R_{CISET} = 3kΩ, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Output Current		L = 4.7µH, R_{LSR} = 0.13Ω (Note 6)	MAX8819A/MAX8819B	300			mA
			MAX8819C	500			
Short-Circuit Current		L = 4.7µH, R_{LSR} = 0.13Ω			600		mA
Short-Circuit Detection Threshold					230		mV
Short-Circuit Foldback Frequency					f_{OSC}/3		Hz
FB3 Voltage		(Note 7)		0.997	1.01	1.028	V
Output Voltage Range				1		V_{SYS}	V
FB3 Leakage Current		V_{FB3} = 1.01V	T_A = +25°C	-50	-5	+50	nA
			T_A = +85°C		-50		
Load Regulation		I_{OUT3} = 100mA to 300mA			1.3		%
Line Regulation		(Note 9)			1		%/D
p-Channel Current-Limit Threshold		MAX8819A/MAX8819B		0.512	0.550	0.595	A
		MAX8819C		0.565	0.600	0.700	
Skip-Mode Transition Current		(Note 8)			80		mA
n-Channel Zero-Crossing Threshold					10		mA
p-Channel On-Resistance		V_{PV13} = 4.0V, I_{LX3} = 180mA			290		mΩ
n-Channel On-Resistance		V_{PV13} = 4.0V, I_{LX3} = 180mA			120		mΩ
Maximum Duty Cycle				100			%
Minimum Duty Cycle					12.5		%
PWM Frequency	f_{OSC}			1.8	2.0	2.2	MHz
Internal Discharge Resistance in Shutdown		EN123 = low, resistance from LX3 to PG3			1.0		kΩ
REG4–STEP-UP CONVERTER							
Input Voltage		Power supplied from SYS (see Figure 1)		2.4		5.5	V
Output Voltage Range	V_{OUT4}			V_{SYS}		24	V
FB4 Regulation Voltage	V_{FB4}	No dimming		475	500	525	mV
FB4 Leakage		REG4 disabled (EN4 = low)		-0.050	+0.005	+0.050	µA
Switching Frequency				0.9	1	1.1	MHz
Minimum Duty Cycle					5		%
Maximum Duty Cycle				90	94		%
OVP4 Overvoltage Detection	V_{OVP}			24	25	26	V
OVP4 Input Current		OVP4 = SYS, EN4 = high			4		µA
OVP4 Leakage Current		REG4 disabled (EN4 = low), OVP4 = SYS		-1	+0.001	+1	µA
n-Channel On-Resistance		V_{SYS} = 4.0V, I_{LX4} = 200mA			395		mΩ
n-Channel Off-Leakage Current		V_{LX4} = 28V		-1	+0.001	+1	µA
n-Channel Current Limit				555	695	950	mA

ELECTRICAL CHARACTERISTICS (continued)

(DC, LX_ unconnected; V_{EP} = V_{GND} = 0V, V_{BAT} = 4V, DLIM[1:2] = 00, EN123 = EN4 = low, V_{FB1} = V_{FB2} = V_{FB3} = 1.1V, V_{FB4} = 0.6V, PV13 = PV2 = SYS, T_A = -40°C to +85°C, capacitors as shown in Figure 1, R_{CISET} = 3kΩ, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED DIMMING CONTROL (EN4)						
EN4 Low Shutdown Delay	t_{SHDN}			2	3.2	ms
EN4 High Enable Delay (Figure 8)	t_{HI_INIT}		100			µs
EN4 Low Time	t_{LO}		0.5		500	µs
EN4 High Time	t_{HI}		0.5			µs
RESET ($\overline{RST1}$)						
Reset Trip Threshold	V_{THRST}	Voltage from FB1 to GND, V_{FB1} falling, 50mV hysteresis	0.765	0.858	0.945	V
Reset Deassert Delay Time	t_{DRST}		180	200	220	ms
Reset Glitch Filter	t_{GLRST}			50		µs
LOGIC (DLIM1, DLIM2, EN123, EN4, $\overline{CHG}$, $\overline{RST1}$)						
Logic Input-Voltage Low		V_{DC} = 4.1V to 5.5V, V_{SYS} = 2.6V to 5.5V			0.4	V
Logic Input-Voltage High		V_{DC} = 4.1V to 5.5V, V_{SYS} = 2.6V to 5.5V	1.2			V
Logic Input Pulldown Resistance		V_{LOGIC} = 0.4V to 5.5V, CEN, EN123, EN4	400	760	1200	kΩ
Logic Leakage Current		V_{LOGIC} = 0 to 5.5V, DLIM1, DLIM2	-1.0	+0.001	+1.0	µA
Logic Output Voltage Low		I_{SINK} = 1mA		7	15	mV
Logic Output-High Leakage Current		V_{LOGIC} = 5.5V	-1.0	+0.001	+1.0	µA

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 4: The charger transitions from done to fast-charge mode at this BAT recharge threshold.

Note 5: The charger transitions from fast-charge to top-off mode at this top-off threshold (Figure 2).

Note 6: The maximum output current is guaranteed by correlation to the p-channel current-limit threshold, p-channel on-resistance, n-channel on-resistance, oscillator frequency, input voltage range, and output voltage range. The parameter is stated for a 4.7µH inductor with 0.13Ω series resistance. See the *Step-Down Converter Maximum Output Current* section for more information.

Note 7: The step-down output voltages are 1% high with no load due to the load-line architecture.

Note 8: The skip-mode current threshold is the transition point between fixed-frequency PWM operation and skip-mode operation. The specification is given in terms of output load current for inductor values shown in the typical application circuit (Figure 1).

Note 9: Line regulation for the step-down converters is measured as $\Delta V_{OUT}/\Delta D$, where D is the duty cycle (approximately V_{OUT}/V_{IN}).

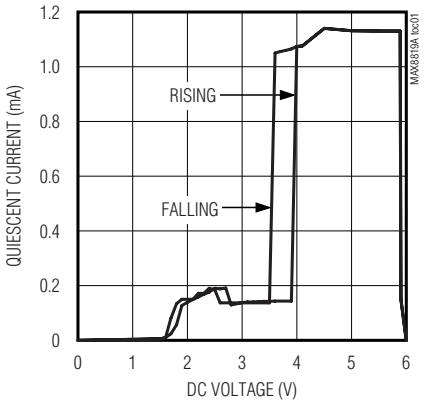
Note 10: REG2 is disabled by connecting PV2 to ground, decreasing the quiescent current.

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

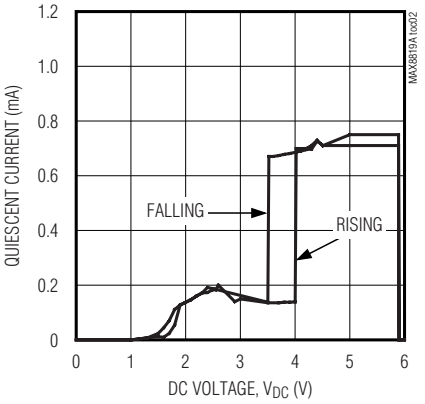
Typical Operating Characteristics

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

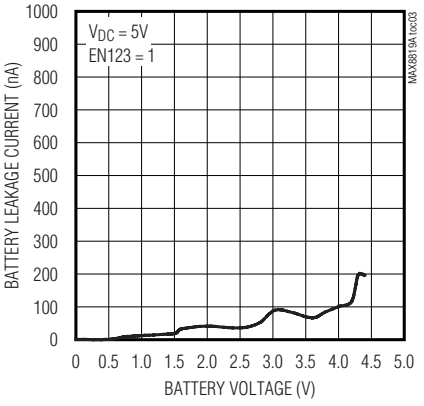
DC QUIESCENT CURRENT vs. DC VOLTAGE (CHARGER ENABLED)



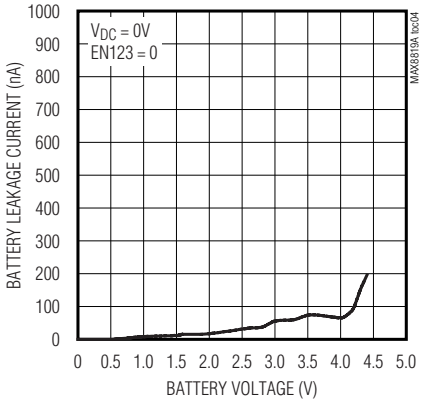
DC QUIESCENT CURRENT vs. DC VOLTAGE (CHARGER DISABLED)



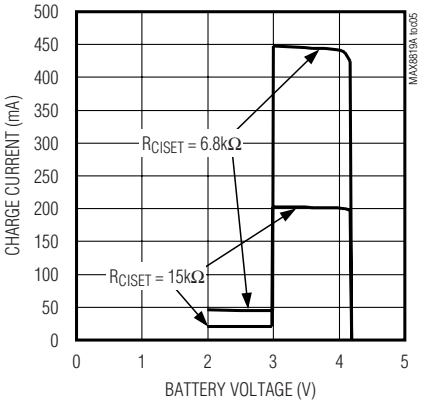
BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE



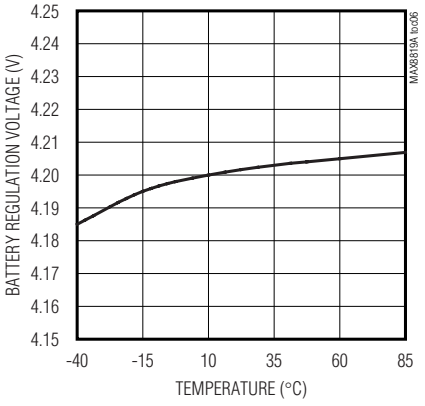
BATTERY LEAKAGE CURRENT vs. BATTERY VOLTAGE



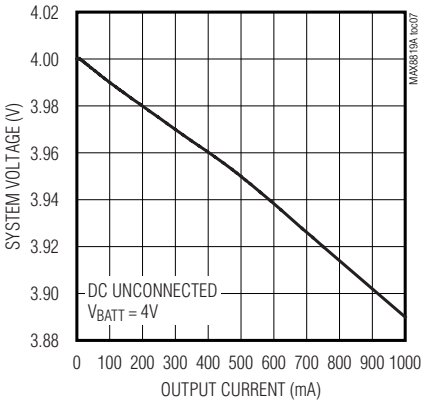
CHARGE CURRENT vs. BATTERY VOLTAGE



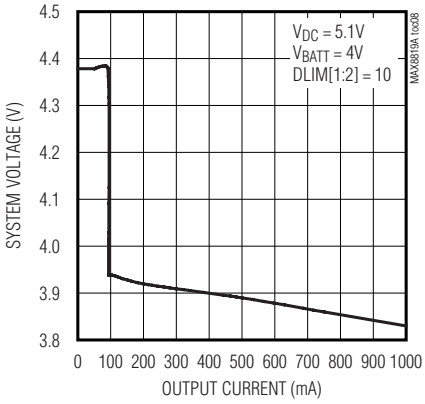
BATTERY REGULATION VOLTAGE vs. TEMPERATURE



SYSTEM VOLTAGE vs. SYSTEM CURRENT



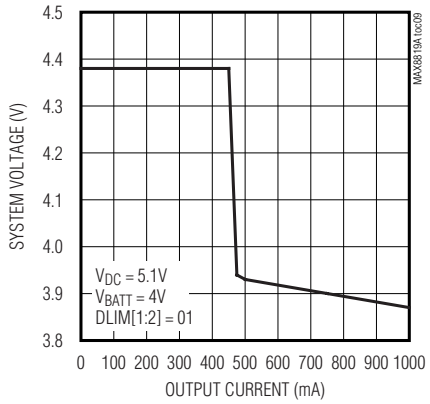
SYSTEM VOLTAGE vs. SYSTEM CURRENT



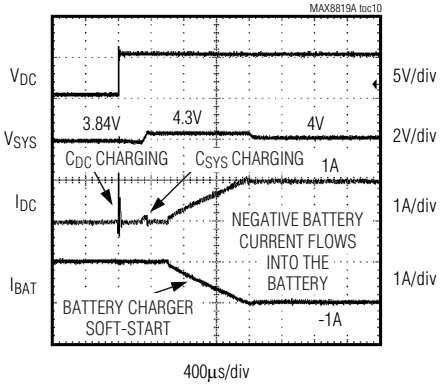
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

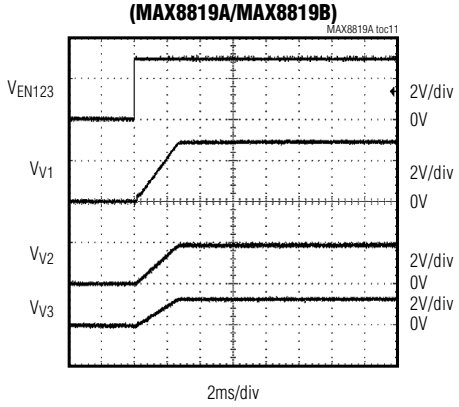
SYSTEM VOLTAGE vs. SYSTEM CURRENT



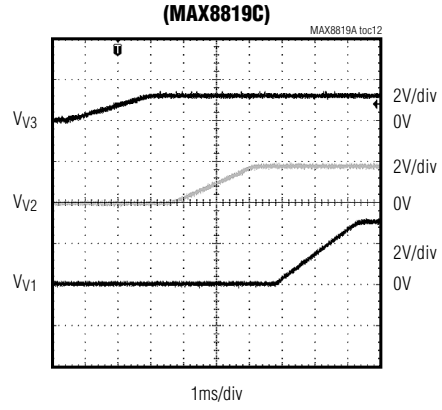
AC-TO-DC ADAPTER CONNECT



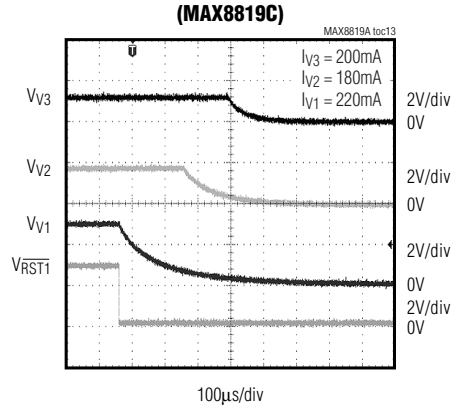
POWER-UP SEQUENCING (MAX8819A/MAX8819B)



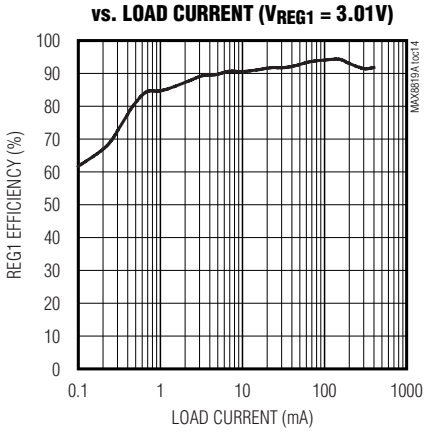
POWER-UP SEQUENCING (MAX8819C)



POWER-DOWN SEQUENCING (MAX8819C)



REG1 EFFICIENCY vs. LOAD CURRENT (V_{REG1} = 3.01V)

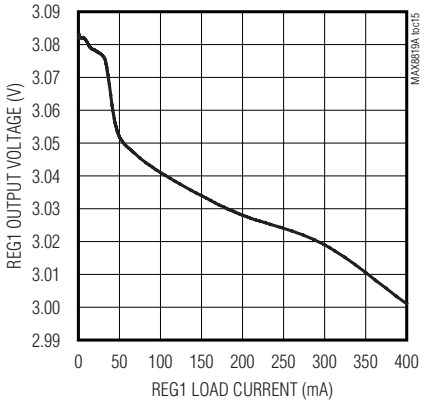


PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

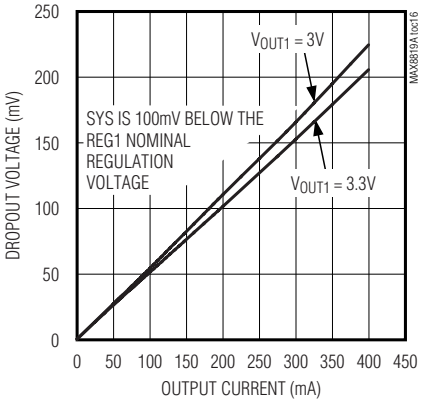
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

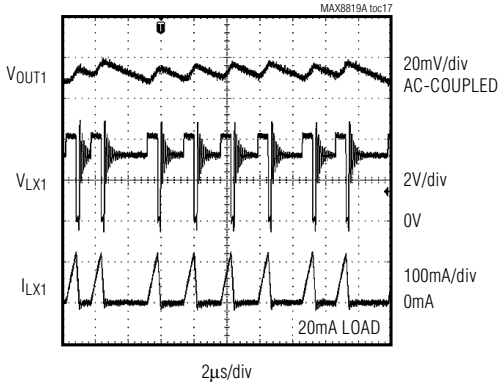
REG1 LOAD REGULATION



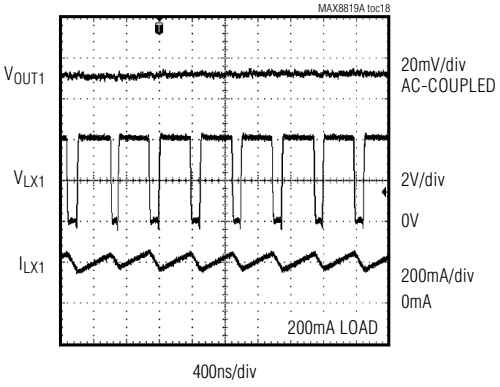
REG1 DROPOUT VOLTAGE vs. LOAD CURRENT



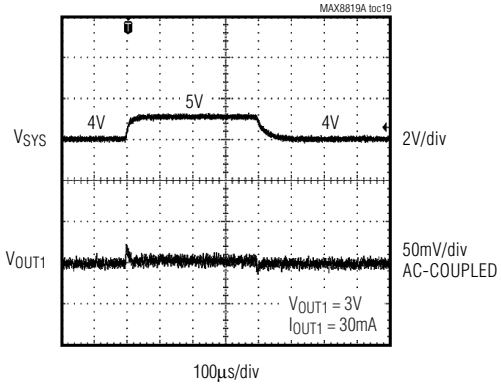
REG1 LIGHT-LOAD SWITCHING WAVEFORMS



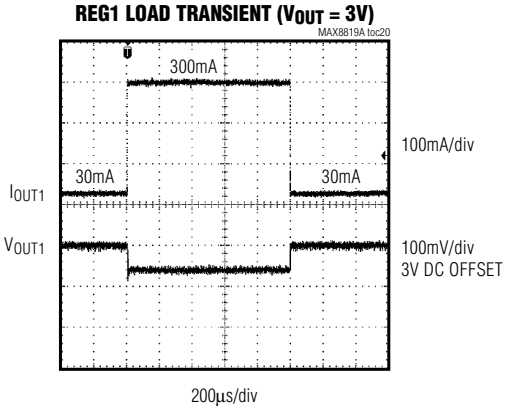
REG1 HEAVY-LOAD SWITCHING WAVEFORMS



LINE TRANSIENT



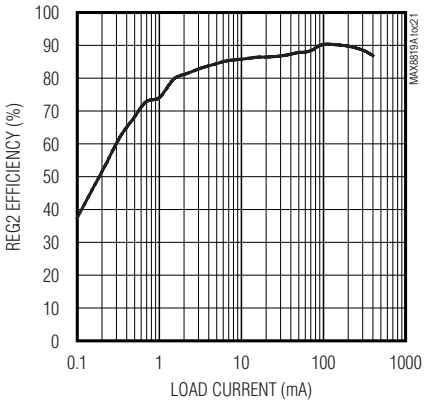
REG1 LOAD TRANSIENT (V_{OUT} = 3V)



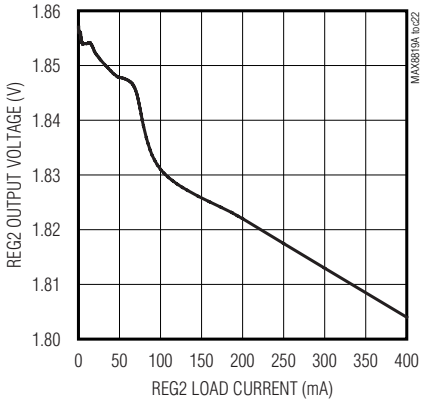
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

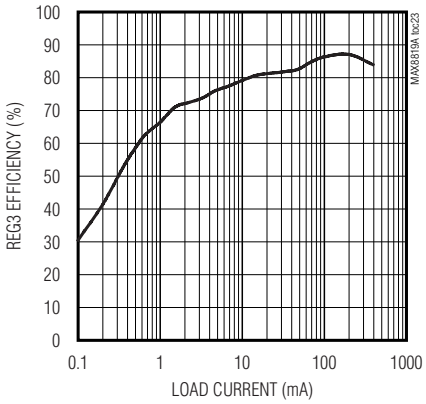
REG2 EFFICIENCY vs. LOAD CURRENT (V_{REG2} = 1.82V)



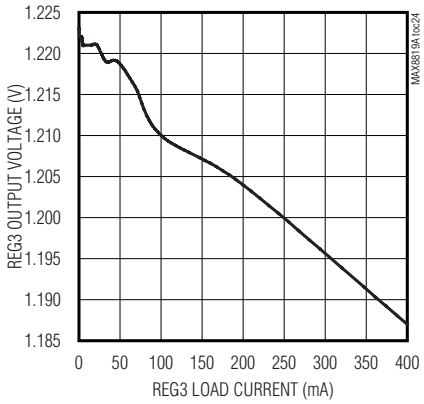
REG2 LOAD REGULATION



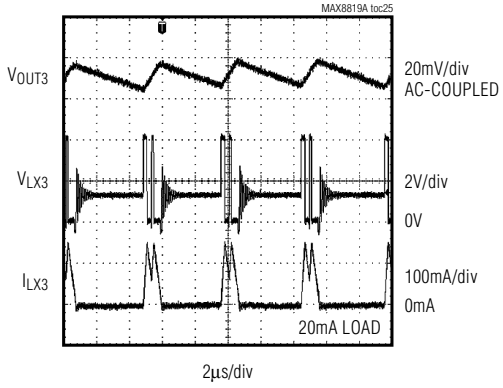
REG3 EFFICIENCY vs. LOAD CURRENT (V_{REG3} = 1.21V)



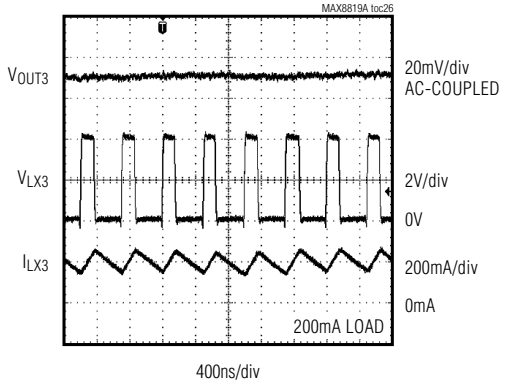
REG3 LOAD REGULATION



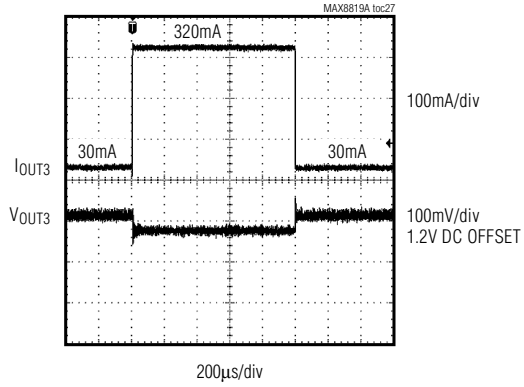
REG3 LIGHT-LOAD SWITCHING WAVEFORMS



REG3 HEAVY-LOAD SWITCHING WAVEFORMS



REG3 LOAD TRANSIENT

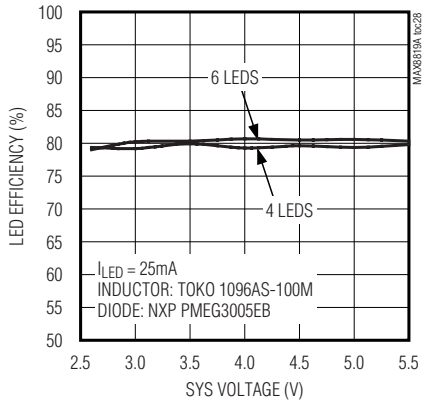


PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

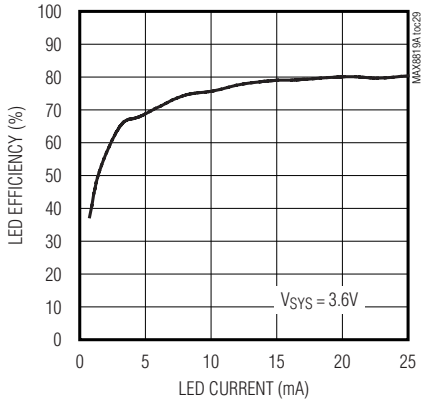
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

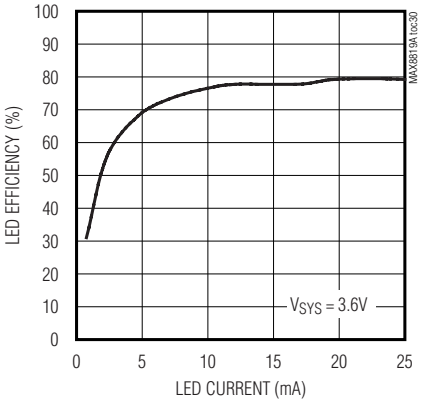
LED EFFICIENCY vs. SYS VOLTAGE



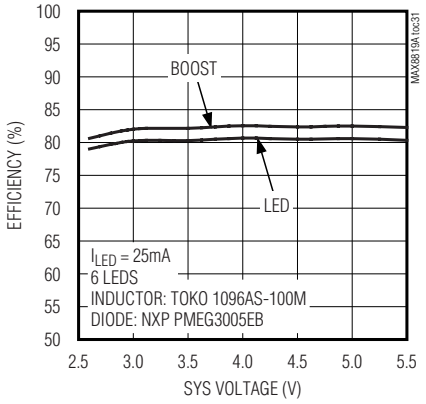
LED EFFICIENCY vs. LED CURRENT (6 LEDS)



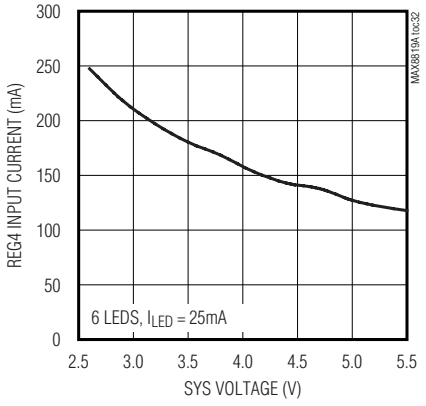
LED EFFICIENCY vs. LED CURRENT (4 LEDS)



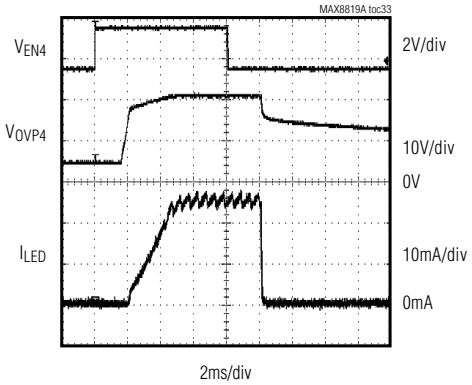
LED AND BOOST EFFICIENCY vs. SYS VOLTAGE



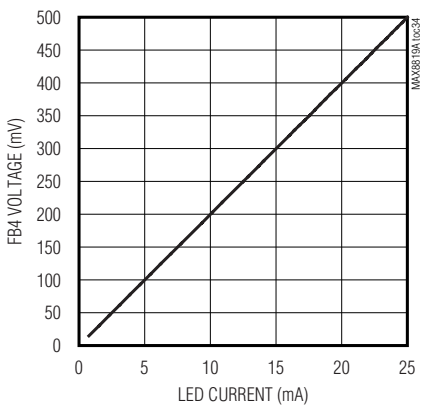
REG4 INPUT CURRENT vs. SYS VOLTAGE



REG4 STARTUP AND SHUTDOWN RESPONSE



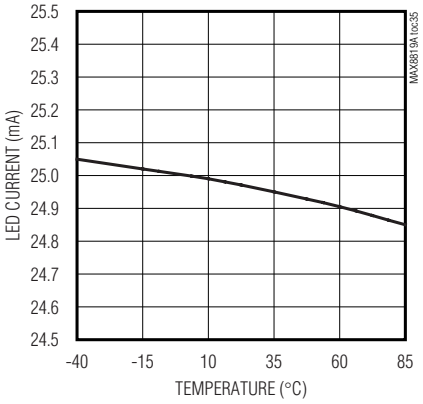
FB4 VOLTAGE vs. LED CURRENT



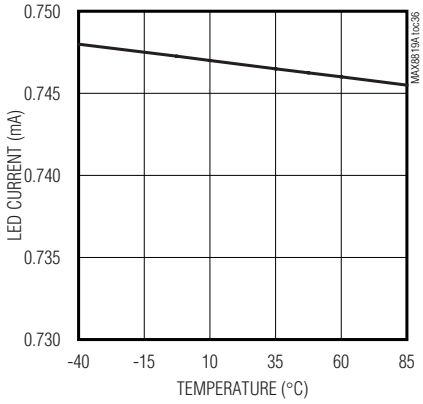
Typical Operating Characteristics (continued)

(Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

MAXIMUM LED CURRENT vs. TEMPERATURE



MINIMUM LED CURRENT vs. TEMPERATURE



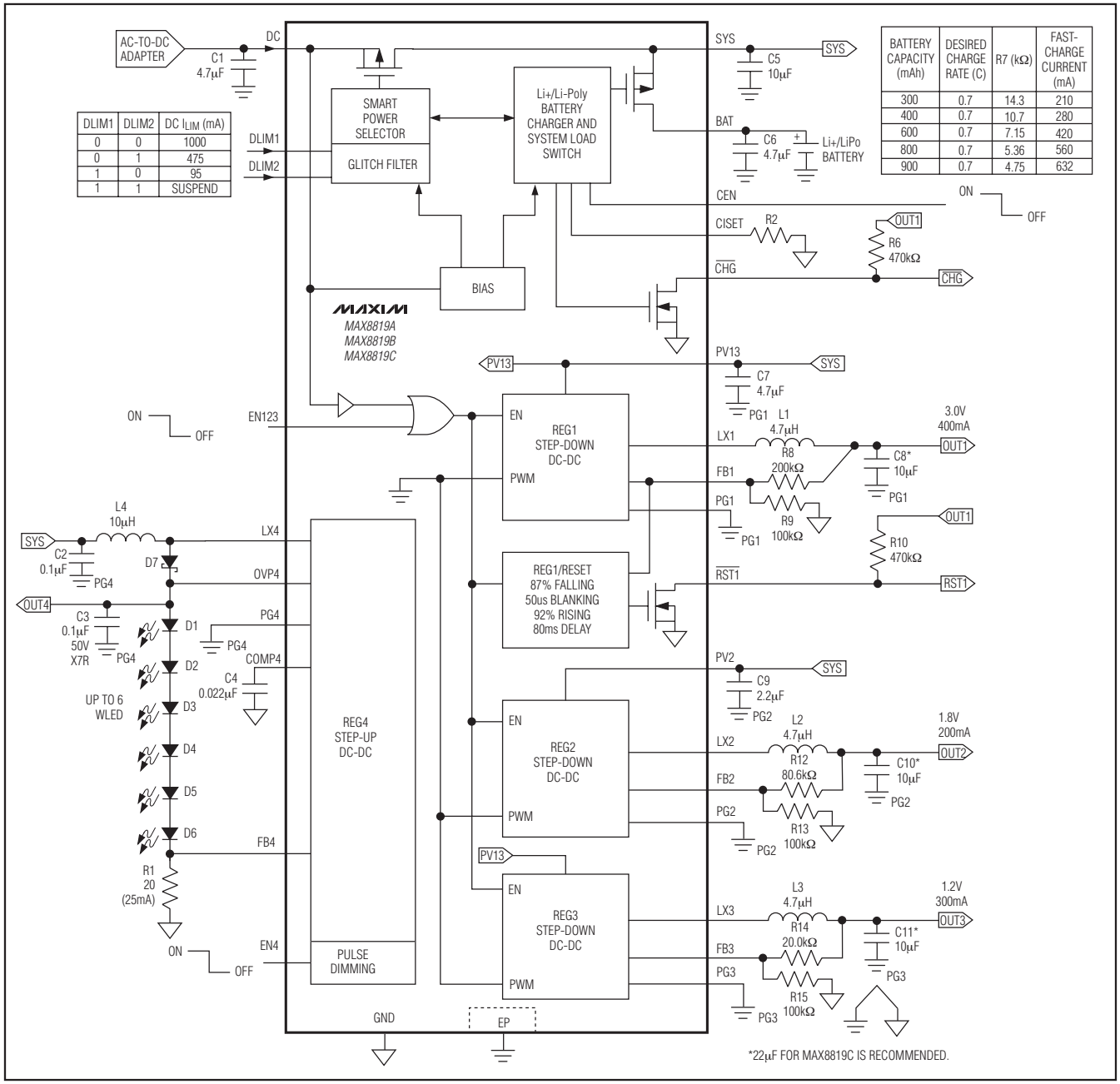
Pin Description

PIN	NAME	FUNCTION
1	COMP4	External Compensation Capacitor for REG4
2	FB4	REG4 Feedback Input
3	OVP4	Overvoltage Protection Node for REG4
4	PG4	REG4 Power Ground
5	LX4	Inductor Switching Node for REG4
6	GND	Analog Ground
7	EN4	REG4 Enable Input and Dimming Control Digital Input
8	$\overline{RST1}$	Active-Low, Open-Drain Reset Output. $\overline{RST1}$ pulls low to indicate that FB1 is below its regulation threshold. $\overline{RST1}$ goes high 200ms after FB1 reaches its regulation threshold. $\overline{RST1}$ is high-impedance when EN123 is low, and DC is unconnected.
9	BAT	Positive Battery Terminal Connection. Connect BAT to the positive terminal of a single-cell Li+/Li-Poly battery. Bypass BAT to GND with a 4.7µF ceramic capacitor.
10	SYS	System Supply Output. Bypass SYS to GND with a 10µF ceramic capacitor. When a valid voltage is present at DC and DLIM[1:2] ≠ 11, V_{SYS} is limited to 4.35V (MAX8819A/MAX8819C) or 5.3V (MAX8819B). When the system load (I_{SYS}) exceeds the input current limit, V_{SYS} drops 75mV (V_{BSREG}) below V_{BAT}, allowing both the external power source and the battery to service SYS. SYS is connected to BAT through an internal 70mΩ system load switch when a valid source is not present at DC.
11	DC	DC Power Input. DC is capable of delivering 1A to SYS. DC supports both AC adapters and USB inputs. As shown in Table 1, the DC current limit is controlled by DLIM1 and DLIM2.
12	CEN	Battery Charger Enable Input
13	FB1	Feedback Input for REG1. Connect FB1 to the center of a resistor voltage-divider from the REG1 output capacitors to GND to set the output voltage from 1V to V_{SYS}.

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

Pin Description (continued)

PIN	NAME	FUNCTION
14	CISET	Charge Rate Select Input. Connect a resistor from CISET to GND (R_{CISET}) to set the fast-charge current limit, prequalification-charge current limit, and top-off threshold.
15	$\overline{CHG}$	Active-Low, Open-Drain Charge Status Output. $\overline{CHG}$ pulls low to indicate that the battery is charging. See Figure 3 for more information.
16	PG1	REG1 Power Ground
17	LX1	Inductor Switching Node for REG1. When enabled, LX1 switches between PV13 and PG1 to regulate the FB1 voltage to 1.0V. When disabled, LX1 is pulled to PG1 by 1kΩ in shutdown.
18	PV13	Power Input for the REG1 and REG3 Converters. Connect PV13 to SYS. Bypass PV13 to PG1 with a 4.7µF ceramic capacitor.
19	LX3	Inductor Switching Node for REG3. When enabled, LX3 switches between PV13 and PG3 to regulate the FB3 voltage to 1.0V. When disabled, LX3 is pulled to PG3 by a 1kΩ internal resistor.
20	PG3	REG3 Power Ground
21	DLIM1	Input Current-Limit Selection Digital Input 1. Drive high or low according to Table 1 to set the DC input current limit.
22	FB2	Feedback Input for REG2. Connect FB2 to the center of a resistor voltage-divider from the REG2 output capacitors to GND to set the output voltage from 1V to V_{SYS}. FB2 must be connected to GND if REG2 is disabled by grounding PV2.
23	FB3	Feedback Input for REG3. Connect FB3 to the center of a resistor voltage-divider from the REG3 output capacitors to GND to set the output voltage from 1V to V_{SYS}.
24	EN123	REG1, REG2, and REG3 Enable Input. Drive EN123 high to enable REG1, REG2, and REG3. Drive EN123 low to disable REG1, REG2, and REG3. The enable/disable sequencing is shown in Figures 6 and 7.
25	PV2	Power Input for REG2. Connect PV2 to SYS for normal operation. Bypass PV2 to PG2 with a 2.2µF ceramic capacitor. For systems that do not require REG2, connect PV2, FB2, and PG2 to GND (LX2 may be unconnected or connected to GND).
26	LX2	Inductor Switching Node for REG2. When enabled, LX2 switches between PV2 and PG2 to regulate the FB2 voltage to 1.0V. When disabled, LX2 is pulled to PG2 by a 1kΩ internal resistor.
27	PG2	REG2 Power Ground
28	DLIM2	Input Current-Limit Selection Digital Input 2. Drive high or low according to Table 1 to set the DC input current limit.
—	EP	Exposed Pad



DLIM1	DLIM2	DC I_{LIM} (mA)
0	0	1000
0	1	475
1	0	95
1	1	SUSPEND

BATTERY CAPACITY (mAh)	DESIRED CHARGE RATE (C)	R7 (kΩ)	FAST-CHARGE CURRENT (mA)
300	0.7	14.3	210
400	0.7	10.7	280
600	0.7	7.15	420
800	0.7	5.36	560
900	0.7	4.75	632

Figure 1. Functional Diagram/Typical Applications Circuit

Detailed Description

The MAX8819_ is a complete power solution that includes a battery charger, step-down converters, and WLED power. As shown in Figure 1, the IC integrates a DC power input, Li+/Li-Poly battery charger, three step-down converters, and one step-up converter for powering white LEDs. All three step-down converters feature adjustable output voltages set with external resistors.

The MAX8819_ has one external power input that connects to either an AC-to-DC adapter or USB port. Logic inputs DLIM1 and DLIM2 select the desired input current limit.

PMIC with Integrated Chargers and Smart Power Selector in a 4mm x 4mm TQFN

In addition to charging the battery, the IC supplies power to the system through the SYS output. The charging current is provided from SYS so that the set input current limit controls the total SYS current, this is the sum of the system load current and the battery-charging current.

In some instances, there may not be enough DC input current to supply peak system loads. The Smart Power Selector circuitry offers flexible power distribution from an AC-to-DC adapter or USB source to the battery and system load. The battery is charged with any available power not used by the system load. If a system load peak exceeds the input current limit, supplemental current is taken from the battery. Thermal limiting prevents overheating by reducing power drawn from the input source. In the past, it might have been necessary to reduce system functionality to limit current drain when a USB source is connected. However, with the MAX8819_, this is no longer the case. When the DC or USB source hits its limit, the battery supplies supplemental current to maintain the load.

The IC features overvoltage protection. Part of this protection is a 4.35V (MAX8819A/MAX8819C) or 5.3V (MAX8819B) voltage limiter at SYS. If DC exceeds the overvoltage threshold of 5.88V (V_{OVLO_DC}), the input limiter disconnects SYS from DC, but battery-powered operation of all regulators is still allowed.

Input Limiter

The Smart Power Selector seamlessly distributes power between the current-limited external input (DC), the battery (BAT), and the system load (SYS). The basic functions performed are:

With both an external power supply (DC) and battery (BAT) connected:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load through the internal system load switch.
- When the battery is connected and there is no external power input, the system (SYS) is powered from the battery.
- When an external power input is connected and there is no battery, the system (SYS) is powered from the external power input.

A thermal-limiting circuit reduces the battery charge rate and external power source current to prevent the MAX8819_ from overheating.

System Load Switch

An internal 70mΩ MOSFET connects SYS to BAT when no voltage source is available at DC. When an external source is detected at DC, this switch opens and SYS is powered from the valid input source through the Smart Power Selector.

When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load through the internal system load switch. If the system load continuously exceeds the input current limit, the battery does not charge, even though external power is connected. This is not expected to occur in most cases because high loads usually occur only in short peaks. During these peaks, battery energy is used, but at all other times the battery charges.

DC Power Input (DC, DLIM1, DLIM2)

DC is a current-limited power input that supplies the system (SYS) up to 1A. The DC to SYS switch is a linear regulator designed to operate in dropout. This linear regulator prevents the SYS voltage from exceeding 5.3V for the MAX8819B or 4.35V for the MAX8819A/MAX8819C. As shown in Table 1, DC supports four different current limits that are set with the DLIM1 and DLIM2 digital inputs. These current limits are ideally suited for use with AC-to-DC wall adapters and USB power. The operating voltage range for DC is 4.1V to 5.5V, but it can tolerate up to 6V without damage. When the DC input voltage is below the undervoltage threshold (4V), it is considered invalid. When the DC voltage is below the battery voltage it is considered invalid. The DC power input is disconnected when the DC voltage is invalid. Bypass DC to ground with at least a 4.7µF capacitor.

Four current settings are provided based upon the settings of DLIM1 and DLIM2, see Table 1. DLIM1 and DLIM2 are deglitched. This deglitching prevents the problem of major carry transitions momentarily entering the suspend state.

Table 1. DC Current-Limit Settings

DLIM1	DLIM2	DC I_{LIM} (mA)
0	0	1000
0	1	475
1	0	95
1	1	Suspend

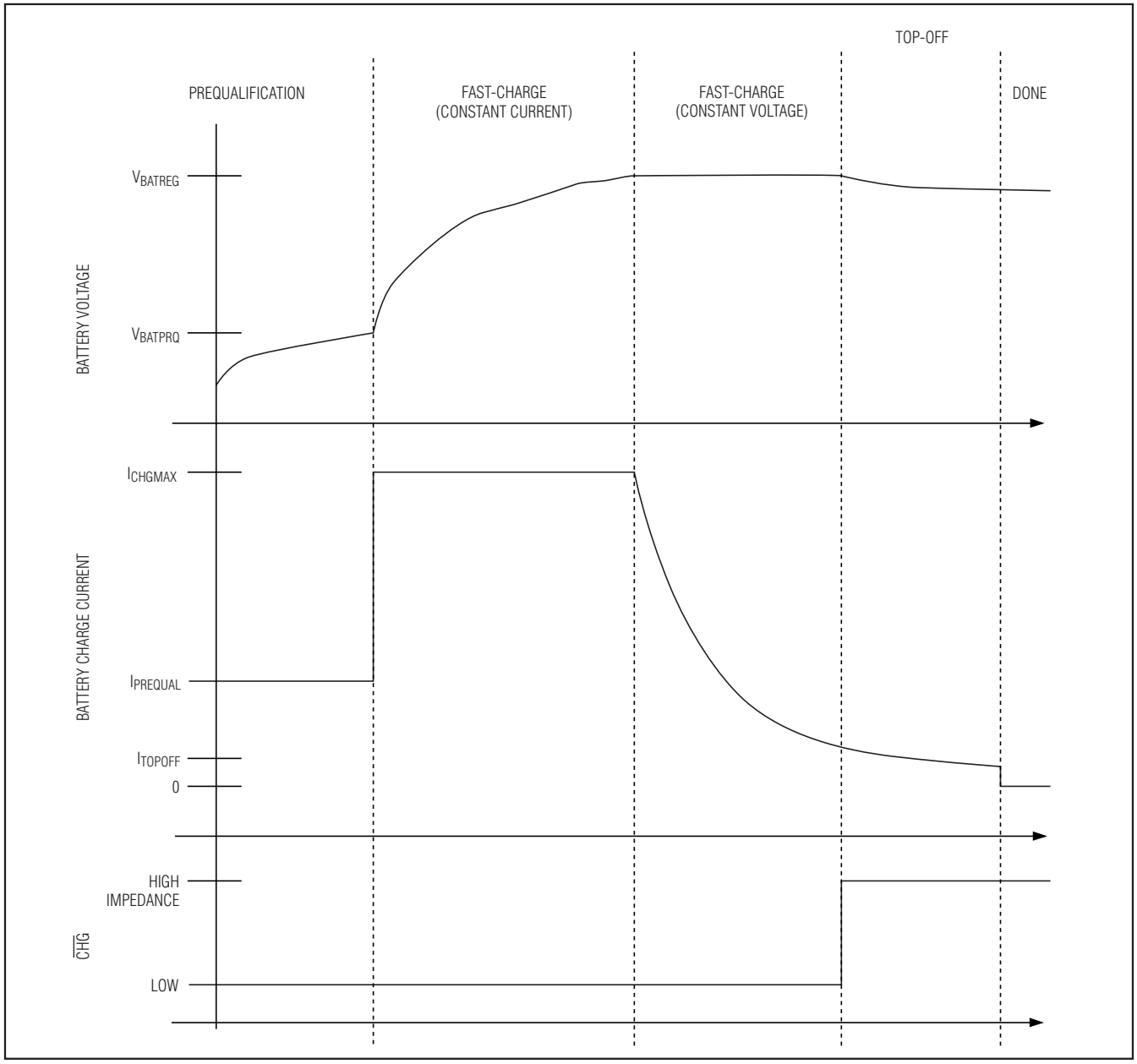


Figure 2. Li+/Li-Poly Charge Profile

Battery Charger

Figure 2 shows the typical Li+/Li-Poly charge profile for the MAX8819_, and Figure 3 shows the battery charger state diagram.

With a valid DC input that is not suspended, the battery charger initiates a charge cycle once CEN is driven high. It first detects the battery voltage. If the battery voltage is less than the prequalification threshold (3.0V), the charger enters prequalification mode and charges the battery at 10% of the maximum fast-charge current while deeply discharged. Once the battery voltage rises to 3.0V, the charger transitions to fast-charge mode and applies the maximum charge current. As charging continues, the battery voltage rises until it approaches the battery regulation voltage (4.2V typ)

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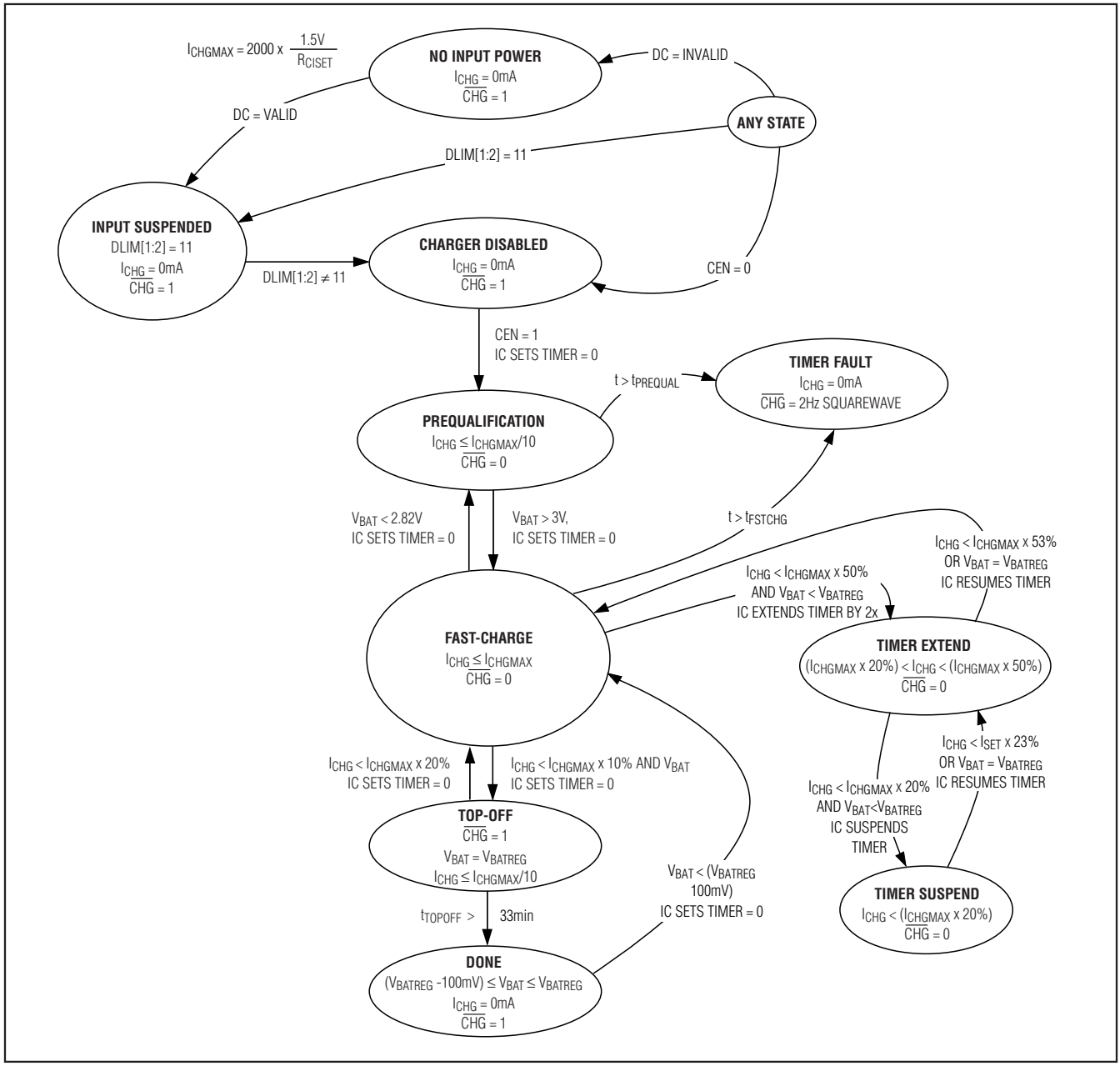

Figure 3. Li+/Li-Poly Charger State Diagram

where charge current starts tapering down. When charge current decreases to 10% of the maximum fast-charge current, the charger enters a 33min top-off state and then charging stops. If the battery voltage subsequently drops 100mV below the battery regulation voltage, charging restarts and the timers reset.

The battery charge rate is set by several factors:

- Battery voltage
- DC input current limit
- The charge-setting resistor, R_{CISET}
- The system load (I_{SYS})
- The die temperature

- The battery charger is enabled by the processor driving the CEN input high. A valid input must be available at DC. The battery charger is disabled without a valid input at DC or by driving CEN low.
- The system current has priority over the battery charger; the battery charger automatically reduces its charge current to maintain the input current limit while still providing the system current (I_{SYS}).
- The input current limit is tapered down from full current to zero current when the die temperature transitions from +100°C to +120°C. Since I_{SYS} has priority over the battery charge current, the battery charge current tapers down before I_{SYS}. The overall result is self-regulation of die temperature (see the *Thermal Limiting and Overload Protection* section for more information).
- The battery charger stops charging in done mode as shown in Figures 2 and 3.

Charge Status Output ($\overline{CHG}$)

$\overline{CHG}$ is an open-drain, active-low output that indicates charger status. As shown in Figures 2 and 3, $\overline{CHG}$ is low when the charger is in its prequalification or fast-charge states. When a timer count is exceeded in either state, $\overline{CHG}$ indicates the fault by blinking at a 2Hz rate and remains in that state until the charger is reset by CEN going low, removal of DC or setting DLIM[1:2] = 11.

When the MAX8819_ is used with a microprocessor (µP), connect a pullup resistor between $\overline{CHG}$ and the system logic voltage to indicate charge status to the µP. Alternatively, $\overline{CHG}$ sinks up to 20mA for an LED charge indicator.

If the charge status output feature is not required, connect $\overline{CHG}$ to ground or leave unconnected.

Charge Timer

As shown in Figure 3, a fault timer prevents the battery from charging indefinitely. In prequalification mode, the charge time is internally fixed to 33min.

$$t_{PREQUAL} = 33min$$

In fast-charge mode, the charge timer is internally fixed to 660min.

$$t_{FSTCHG} = 660min$$

When the charger exits fast-charge mode, a fixed 33min top-off mode is entered:

$$t_{TOPOFF} = 33min$$

While in the constant-current fast-charge mode (Figure 2), if the MAX8819_ reduces the battery charge current due to its internal die temperature or large system loads, it slows down the charge timer. This feature eliminates nuisance charge timer faults. When the battery charge current is between 100% and 50% of its programmed fast-charge level, the fast-charge timer runs at full speed. When the battery charge current is between 50% and 20% programmed fast-charge level, the fast-charge timer is slowed by 2x. Similarly, when the battery charge current is below 20% of the programmed fast-charge level, the fast-charge timer is paused. The fast-charge timer is not slowed or paused when the charger is in the constant voltage portion of its fast-charge mode (Figure 2) where the charge current reduces normally.

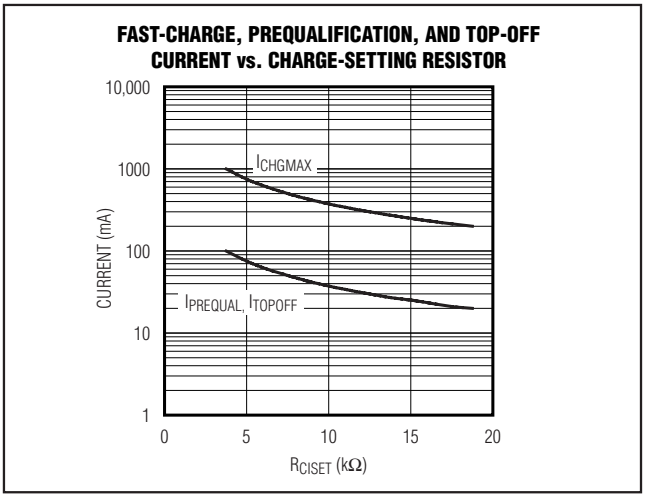

Figure 4. Calculated Charge Currents vs. R_{CISET}

Table 2. Calculated Charge Currents vs. R_{CISET}

R_{CISET} (kΩ)	I_{CHGMAX} (mA)	$I_{PREQUAL}$ (mA)	I_{TOPOFF} (mA)
3.01	1000	100	100
4.02	746	75	75
4.99	601	60	60
6.04	497	50	50
6.98	430	43	43
8.06	372	37	37
9.09	330	33	33
10	300	30	30
11	273	27	27
12.1	248	25	25
13	231	23	23
14	214	21	21
15	200	20	20

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Charge Current (CISET)

As shown in Table 2 and Figure 4, a resistor from CISET to ground (R_{CISET}) sets the maximum fast-charge current (I_{CHGMAX}), the charge current in prequalification mode ($I_{PREQUAL}$), and the top-off threshold (I_{TOPOFF}). The MAX8819_ supports values of I_{CHGMAX} from 200mA to 1000mA. Select the R_{CISET} as follows:

$$R_{CISET} = 2000 \times \frac{1.5V}{I_{CHGMAX}}$$

Determine I_{CHGMAX} by considering the characteristics of the battery. It is not necessary to limit the charge current based on the capabilities of the expected AC-to-DC adapter or USB/DC input current limit, the system load, or thermal limitations of the PCB. The IC automatically lowers the charging current as necessary to accommodate for these factors.

For the selected value of R_{CISET}, calculate I_{CHGMAX}, $I_{PREQUAL}$, and I_{TOPOFF} as follows:

$$I_{CHGMAX} = 2000 \times \frac{1.5V}{R_{CISET}}$$

$$I_{PREQUAL} = I_{TOPOFF} = 10\% \times I_{CHGMAX}$$

Step-Down Converters (REG1, REG2, REG3)

REG1, REG2, and REG3 are high-efficiency, 2MHz current-mode step-down converters with adjustable outputs. REG1 is designed to deliver 400mA for the MAX8819A/MAX8819B and 550mA for the MAX8819C. REG2 and REG3 are designed to deliver 300mA for the MAX8819A/MAX8819B and 500mA for the MAX8819C.

The PV13 step-down regulator power input must be connected to SYS. PV2 must also be connected to SYS for normal operation of REG2, but REG2 can be disabled by connecting PV2, FB2, and PG2 to GND. When REG2 is disabled, LX2 can be unconencted or connected to GND. The step-down regulators operate with V_{SYS} from 2.6V to 5.5V. Undervoltage lockout ensures that the step-down regulators do not operate with SYS below 2.55V (max).

See the *Step-Down Converter Enable/Disable (EN123) and Sequencing* section for how to enable and disable the step-down converters. When enabled, the MAX8819_ gradually ramps each output up during a 2.6ms soft-start time. When enabled, the MAX8819C sequentially ramps up each output. Soft-start eliminates input current surges when regulators are enabled.

See the *Step-Down Control Scheme* section for information about the step-down converters control scheme.

The IC uses external resistor-dividers to set the step-down output voltages between 1V and V_{SYS}. Use at least 10µA of bias current in these dividers to ensure no change in the stability of the closed-loop system. To set the output voltage, select a value for the resistor connected between FB_ and GND (R_{FBL}). The recommended value is 100kΩ. Next, calculate the value of the resistor connected from FB_ to the output (R_{FBH}):

$$R_{FBH} = R_{FBL} \times \left(\frac{V_{OUT}}{1.0V} - 1 \right)$$

REG1, REG2, and REG3 are optimized for high, medium, and low output voltages, respectively. The highest overall efficiency occurs with V1 set to the highest output voltage and V3 set to the lowest output voltage.

Step-Down Control Scheme

At light load, the step-down converter switches only as needed to supply the load. This improves light-load efficiency. At higher load currents (~80mA), the step-down converter transitions to fixed 2MHz switching.

Step-Down Dropout and Minimum Duty Cycle

All of the step-down regulators are capable of operating in 100% duty-cycle dropout, however, REG1 has been optimized for this mode of operation. During 100% duty-cycle operation, the high-side p-channel MOSFET turns on constantly, connecting the input to the output through the inductor. The dropout voltage (V_{DO}) is calculated as follows:

$$V_{DO} = I_{LOAD}(R_P + R_{LSR})$$

where:

R_P = p-channel power switch $R_{DS(ON)}$
R_{LSR} = external inductor ESR

The minimum duty cycle for all step-down regulators is 12.5% (typ), allowing a regulation voltage as low as 1V over the full SYS operating range. REG3 is optimized for low duty-cycle operation.

Step-Down Input Capacitor

The input capacitor in a step-down converter reduces current peaks drawn from the power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency must be less than that of the source impedance of the supply so that high-frequency switching currents do not pass through the input source.

The step-down regulator power inputs are critical discontinuous current paths that require careful bypassing. In the PCB layout, place the step-down converter input bypass capacitors as close as possible to each pair of switching converter power input pins (PV_ to PG_) to minimize parasitic inductance. If making connections to these capacitors through vias, be sure to use multiple vias to ensure that the layout does not insert excess inductance or resistance between the bypass capacitor and the power pins.

The input capacitor must meet the input ripple current requirement imposed by the step-down converter. Ceramic capacitors are preferred due to their low ESR and resilience to power-up surge currents. Choose the input capacitor so that its temperature rise due to input ripple-current does not exceed approximately +10°C. For a step-down DC-DC converter, the maximum input ripple current is half of the output current. This maximum input ripple current occurs when the step-down converter operates at 50% duty factor (V_{IN} = 2 x V_{OUT}).

Bypass PV13 to PG1 and PG3 with a 4.7µF ceramic capacitor. If REG2 is required, bypass PV2 to PG2 with a 2.2µF capacitor. Use capacitors that maintain their capacitance over temperature and DC bias. Ceramic capacitors with an X7R or X5R temperature characteristic generally perform well. The capacitor voltage rating should be 6.3V or greater.

Step-Down Output Capacitors

The output capacitance keeps output ripple small and ensures control-loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable with ceramic exhibiting the lowest ESR and lowest high-frequency impedance. The MAX8819A/MAX8819B require at least 10µF of output capacitance. The MAX8819C requires ar least 22µF of output capacitance.

As the case sizes of ceramic surface-mount capacitors decreases, their capacitance vs. DC bias voltage characteristic becomes poor. Due to this characteristic, it is possible for 0805 capacitors to perform well while 0603 capacitors of the same value may not. The MAX8819A/MAX8819B require a nominal output capacitance of 10µF, however, after their DC bias voltage derating, the output capacitance must be at least 7.5µF.

Step-Down Inductor

Choose the step-down converter inductance to be 4.7µH. The minimum recommended saturation current requirement is 700mA. In PWM mode, the peak inductor currents are equal to the load current plus one half of the inductor ripple current. See Table 3 for suggested inductors.

Table 3. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (mΩ)	CURRENT RATING (mA)	DIMENSIONS (mm)
Sumida	CDRH2D11HP	4.7	190	750	3.0 x 3.0 x 1.2 = $(10.8mm)^3$
	CDH2D09	4.7	218	700	3.0 x 3.0 x 1.0= $(9.0mm)^3$
Taiyo Yuden	NR3012	4.7	130	770	3.0 x 3.0 x 1.2 = $(10.8mm)^3$
	NR3010	4.7	190	750	3.0 x 3.0 x 1.0 = $(9.0mm)^3$
TDK	VLF3012	4.7	160	740	2.8 x 2.6 x 1.2 = $(8.7mm)^3$
	VLF3010	4.7	240	700	2.8 x 2.6 x 1.0 = $(7.3mm)^3$
TOKO	DE2812C	4.7	130	880	3.0 x 2.8 x 1.2 = $(10.8mm)^3$
FDK	MIPF2520	4.7	110	1100	2.5 x 2.0 x 1.0 = $(5mm)^3$
	MIPF2016	4.7	160	900	2.0 x 1.6 x 1.0 = $(3.2mm)^3$

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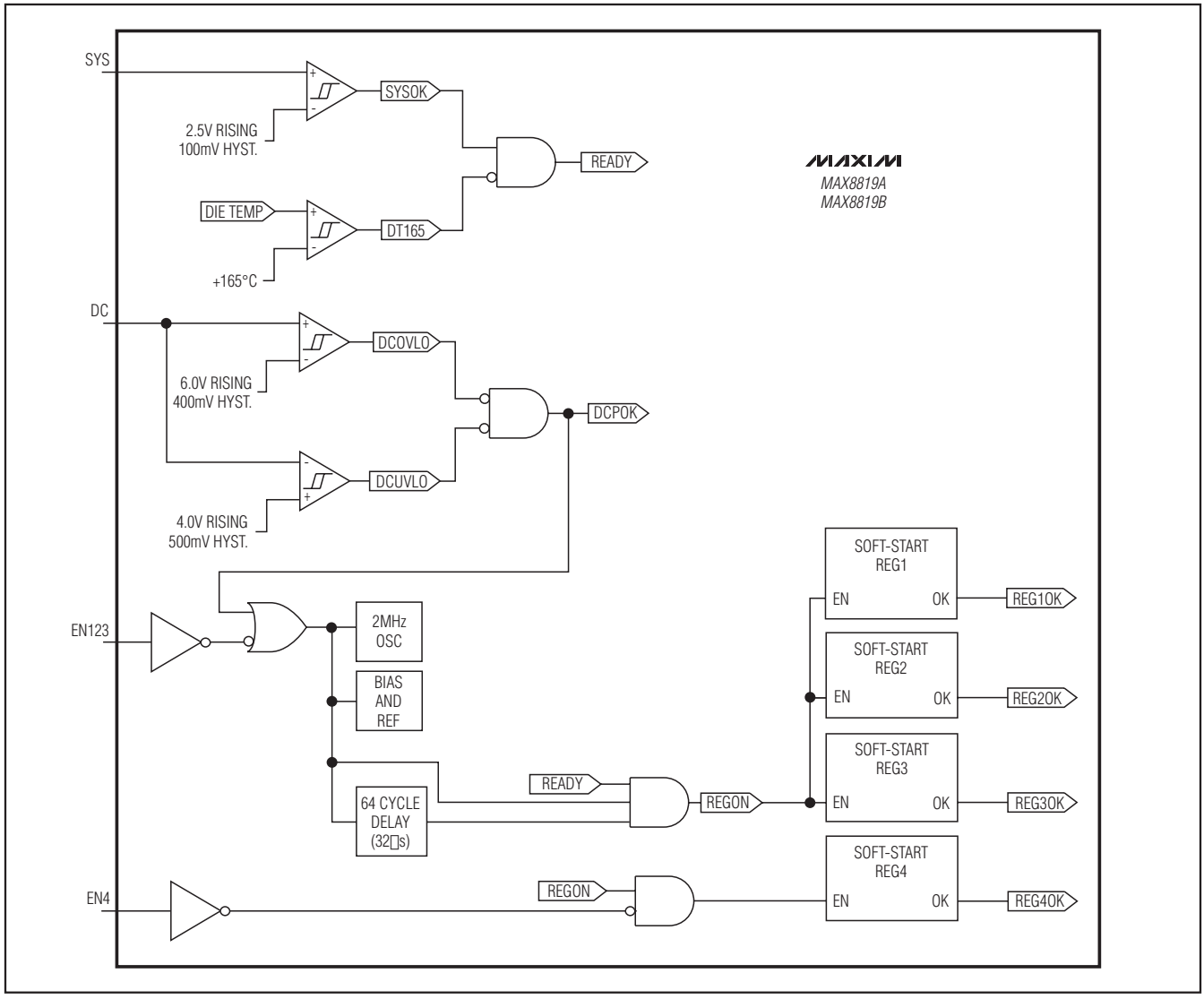

Figure 5a. MAX8819A/MAX8819B Enable/Disable Logic

The peak-to-peak inductor ripple current during PWM operation is calculated as follows:

$$I_{P-P} = \frac{V_{OUT}(V_{SYS} - V_{OUT})}{V_{SYS} \times f_S \times L}$$

where f_S is the 2MHz switching frequency.

The peak inductor current during PWM operation is calculated as follows:

$$I_{L\_PEAK} = I_{LOAD} + \frac{I_{P-P}}{2}$$

Step-Down Converter Maximum Output Current

The maximum regulated output current from a step-down converter is ultimately determined by the p-channel peak current limit (I_{PK}). The calculation follows:

$$I_{OUT\_MAX} = I_{PK} - (I_{P-P}/2)$$

For example, if V_{SYS} = 5.3V, V_{OUT} = 3V, f_S = 2MHz, L = 4.7µH, and I_{PK} = 0.6A:

I_{P-P} = 3V x (5.3V - 3V)/(5.3V x 2MHz x 4.7µH) = 0.138A

then I_{OUT_MAX} = 0.6A - (0.138A/2) = 0.531A.

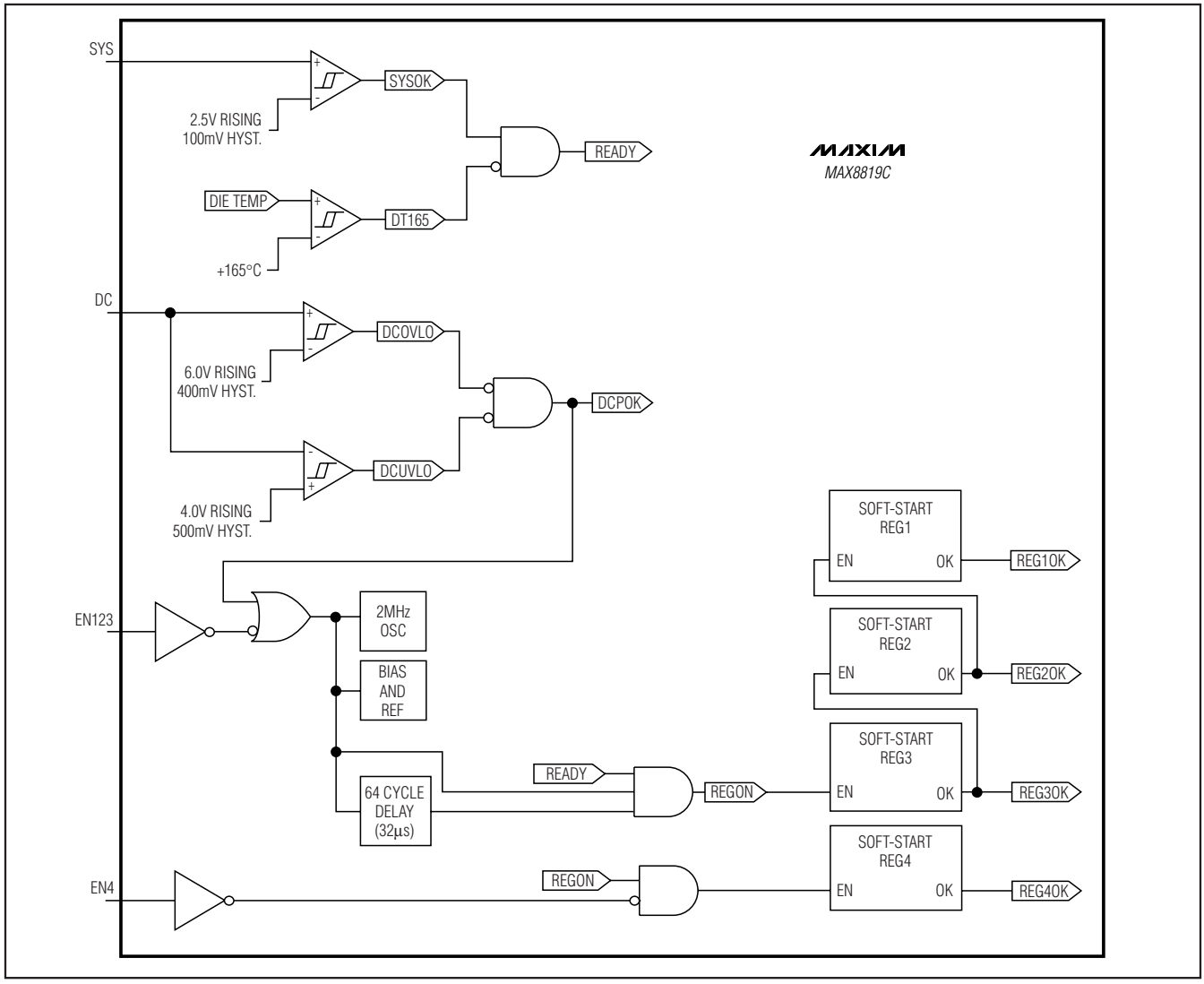

Figure 5b. MAX8819C Enable Logic

As the load current is increased beyond this point, the output voltage sags and the converter goes out of regulation because the inductor current cannot increase above the p-channel peak current limit.

Step-Down Converter Short-Circuit Protection

The step-down converter implements short-circuit protection by monitoring the feedback voltage, $V_{FB\_}$. After soft-start, if $V_{FB\_}$ drops below 0.23V, the converter reduces its switching frequency to $f_S/3$. The inductor current still reaches the p-channel peak current limit, however, at one-third the frequency. Therefore, the output and input currents are reduced to approximately one-third of the maximum value in response to an output short circuit to ground. When the short is removed, the inductor current raises the voltage on the output capacitor and the step-down converter resumes normal operation.

REG1 Reset ($\overline{RST1}$)

$\overline{RST1}$ is an active-low, open-drain output that pulls low to indicate that FB1 is below its regulation threshold. $\overline{RST1}$ goes high 200ms after FB1 reaches its regulation threshold. $\overline{RST1}$ is high-impedance when EN123 is high. See Figures 6 and 7.

A 50µs blanking delay is provided when FB1 is falling, so that $\overline{RST1}$ does not glitch if the REG1 output voltage is dynamically adjusted by altering the resistors in its feedback network.

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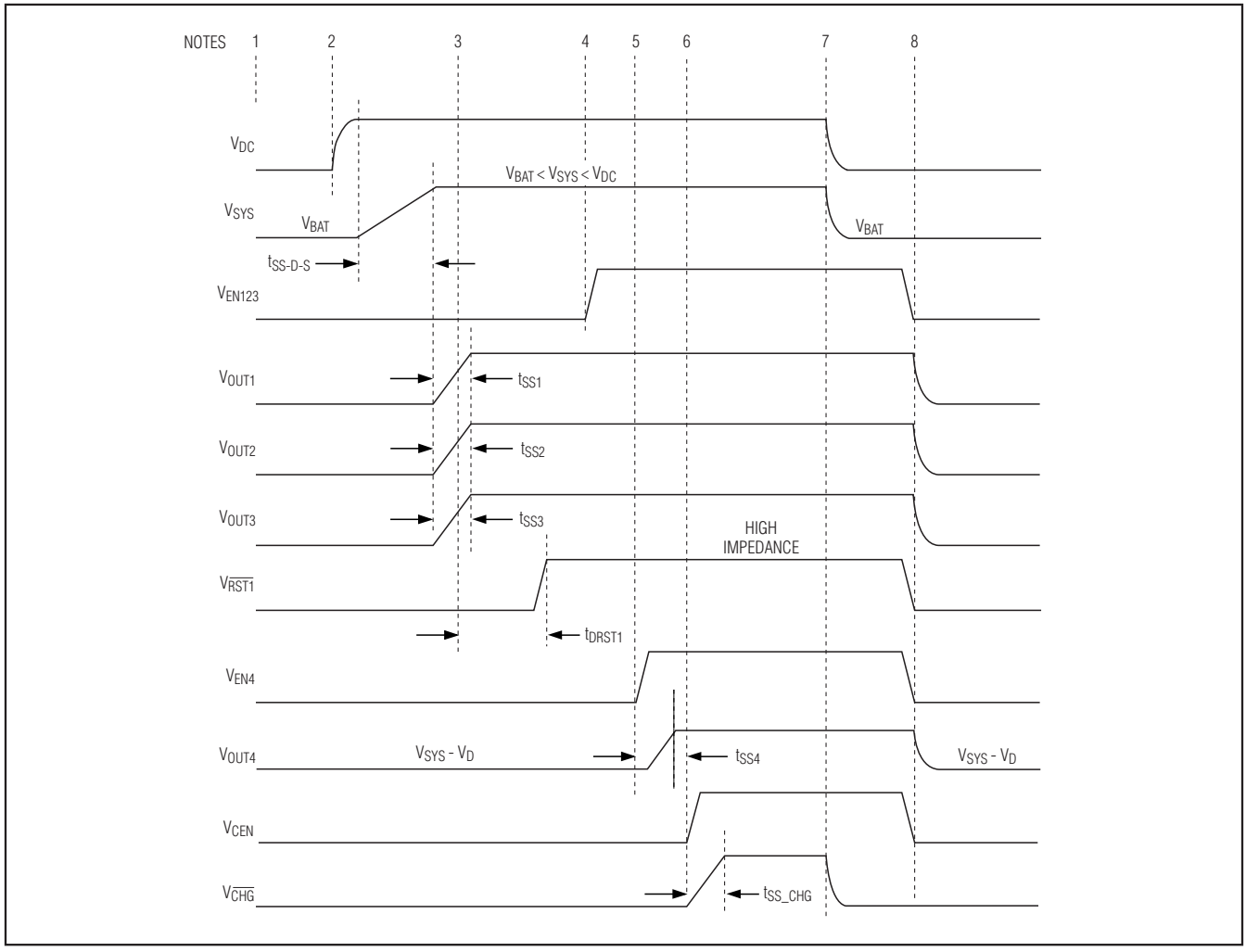

Figure 6. MAX8819A/MAX8819B Enable/Disable Waveforms Example

Step-Down Converter Active Discharge in Shutdown

Each MAX8819_ step-down converter (REG1, REG2, REG3) has an internal 1kΩ resistor that discharges the output capacitor when the converter is off. The discharge resistors ensure that the load circuitry powers down completely. The internal discharge resistors are connected when a converter is disabled and when the device is in UVLO with an input voltage greater than 1.0V. With an input voltage less than 1.0V the internal discharge resistors are not activated.

Step-Down Converter Enable/ Disable (EN123) and Sequencing

Figure 5a shows the MAX8819A/MAX8819B enable and disable logic. Figure 5b shows the MAX8819C enable/disable logic. Figure 6 shows an example of enable and disable waveforms for the MAX8819A/ MAX8819B.

Figure 6 notes:

1) The device is off with no external power applied to DC. The system voltage (V_{SYS}) is equal to the battery voltage (V_{BAT}).
2) An external supply is applied to DC that causes the step-down converter to power up after the DC-to-SYS soft-start time (t_{SS-D-S}). When the DC input is valid and DLIM[1:2] ≠ 11, V_{SYS} increases.
3) When V1 reaches the reset trip threshold (V_{THRST}), the reset deassert delay timer starts. When the reset deassert delay timer expires (t_{DRST1}), $\overline{RST1}$ goes high-impedance. If $\overline{RST1}$ is connected to the $\overline{RESET}$

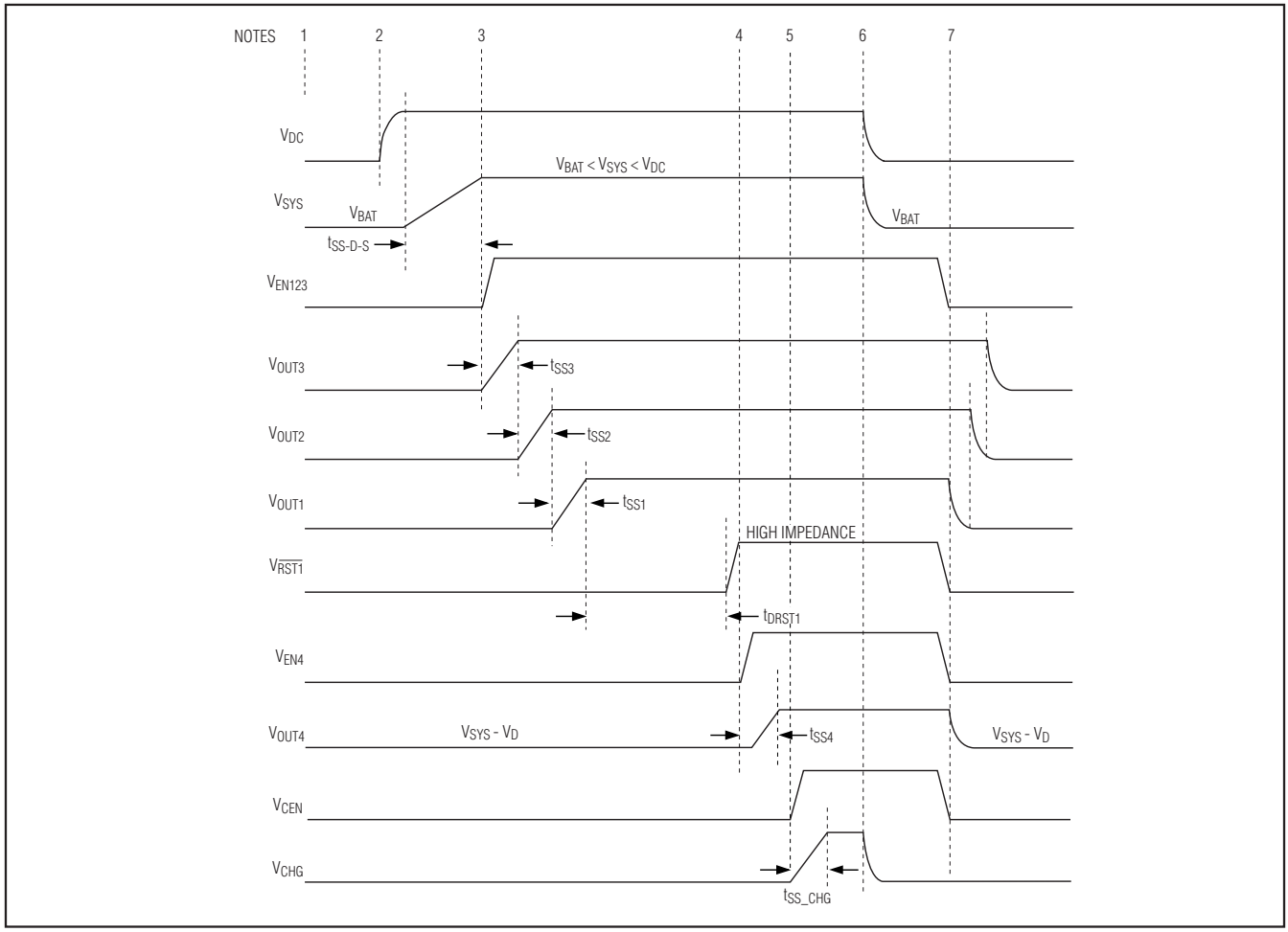

Figure 7. MAX8819C Enable/Disable Waveforms Example

input of the system µP, the processor can begin its boot-up sequence up at this time.

4) During the µP's boot-up sequence, it asserts EN123 to keep the step-down converters enabled, even if DC is removed.
5) After the µP has booted, it asserts EN4 to turn on the display's backlight.
6) CEN is asserted by the µP to start a charge cycle.
7) The external supply is removed from DC and V_{SYS} falls. The converters remain enabled because the µP has asserted EN123 and EN4, but the battery charging current drops to zero even though CEN is still asserted. $\overline{CHG}$ goes high impedance.
8) System is turned off by deasserting EN123, EN4, and CEN; $\overline{RST1}$ goes low to reset the µP.

Figure 7 notes:

1) The MAX8819C is off with no external power applied to DC. The system voltage (V_{SYS}) is equal to the battery voltage (V_{BAT}).
2) An external supply is applied to DC that causes the step-down regulator to power up after the DC-to-SYS soft-start time (t_{SS-D-S}). When the DC input is valid and DC is not suspended, V_{SYS} rises.
3) EN123 is pulled high to start the OUT3, OUT2, and OUT1 power-up sequence. When OUT1 reaches the reset trip threshold (V_{THRST}), the reset deassert delay timer starts. When the reset deassert delay timer expires (t_{DRST1} 200ms typ.), $\overline{RST1}$ goes high-impedance. If $\overline{RST1}$ is connected to the $\overline{RESET}$ input of the system µP, the processor can begin its boot-up sequence at this time.