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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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EVALUATION KIT AVAILABLE

MAX8939/MAX8939A/MAX8939B

System Power Management for Mobile Handset

General Description

The MAX8939/MAX8939A/MAX8939B power management ICs contain the necessary supplies and features for supporting cell phone designs based on the Intel Mobile Communications (IMC) 61XX 3G platform. Designed to power all peripheral components in the platform, the ICs also provide the necessary signals to control the 61XX baseband processor.

The integrated lithium-ion (Li+) charger is protected up to 28V input and features a protected output voltage for supply of a USB transceiver. Proprietary thermal-regulation circuitry limits the die temperature during fast-charging or when the ICs are exposed to high ambient temperatures, allowing maximum charging current without damaging the ICs. A dedicated current regulator is included for driving a charge indicator LED.

Four programmable low-noise, low-dropout linear regulators (LDOs) provide the supply for noise sensitive peripherals. A high power vibrator driver is I²C programmable in 70 PWM levels and 4 output voltages. The ICs also offer two step-up converters; one high power, low voltage (5V) to supply an external audio amplifier or camera flash, and a high voltage (28V) supply for the display and keyboard backlight. Two integrated 25mA current regulators provide independent ramp-up and ramp-down control, programmable through I²C.

The MAX8939/MAX8939A/MAX8939B are highly integrated ICs that require very few external components and are available in a compact 2.5mm x 3.0mm, 0.65mm max height wafer level package (WLP).

Applications

Companion Chip for Cell Phones/Smartphones

Features

- **Step-Up Converter**
  - **700mA Guaranteed Output Current**
  - **I²C Programmable Output 3.5V to 5.0V in 16 Steps**
  - **Over 90% Efficiency**
  - **On-Chip FET and Synchronous Rectifier**
  - **Fixed 2MHz PWM Switching**
  - **Small 2.2µH to 10µH Inductor**
- **WLED Boost Converter**
  - **28V Max Step-Up Output Voltage**
  - **60mA Output Current**
  - **Integrated nMOS Power Switch**
  - **Over 90% Efficiency**
  - **Fixed 2MHz Switching**
  - **Small 4.7µH to 10µH Inductor**
  - **Two 25mA Individually Programmable Current Regulators**
  - **I²C Programmable Output Current (50µA to 25.25mA) with 128-Step Pseudo Log Dimming**
  - **Individually Programmable Ramp (Up/Down) Timers**
  - **Low Dropout (150mV max)**
- **Linear One-Cell Li+ Battery Charger**
  - **No External MOSFET, Reverse Blocking Diode, or Current-Sense Resistor**
  - **Programmable Fast-Charge Current (1.5A$_{RMS}$ max for the MAX8939 or 850mA$_{RMS}$ max for the MAX8939A/MAX8939B)**
  - **Programmable Top-Off Current Threshold**
  - **Proprietary Die Temperature Regulation Control**
  - **4.1V to 10V Input Voltage Range (MAX8939)**
  - **4.1V to 6.25V Input Voltage Range (MAX8939A/MAX8939B) with Input Overvoltage Protection**
  - **Up to 28V Low-Dropout Voltage (300mV at 500mA) Input Power-Source Detection Output**
  - **Input Overvoltage Protected 4.75V Output (SAFE_OUT) from IN**
  - **Charge Current Monitor Output**
  - **Indicator LED**
  - **Hardware Input Enable**
  - **5s Watchdog Feature During Charge**
- **Four Low-Noise LDOs**
  - **1x 400mA, 2 x 200mA and 1x 100mA Output Current**
  - **High 65dB (typ) PSRR**
  - **Low Noise (45µV$_{RMS}$ typ)**
  - **1.7V to 3.2V Programmable Output Voltage**
  - **Low Quiescent Current (25µA typ)**
  - **400mA LDO with Hardware Enable Input**
- **Vibrator Driver**
  - **Guaranteed 200mA Output Current**
  - **Programmable Output Voltage 1.3V to V$_{INVIB}$**
  - **Repetition Frequency 23.8kHz**
  - **PWM Speed Control in 70 steps**
  - **Active Stop Brake**
- **Control Interface for 61XX Baseband**
  - **MAX8939/MAX8939A/MAX8939B Control Through I²C RESET_IN Reset Input**
  - **Charger Detect PWR_ON_CMP Output**
  - **IRQ Interrupt Output**
- **2.9V to 5.5V Supply Voltage Range**
- **Thermal Shutdown**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8939EWV+T	-40°C to +85°C	30 WLP (0.5mm pitch)
MAX8939AEWV+T	-40°C to +85°C	30 WLP (0.5mm pitch)
MAX8939BEWV+T	-40°C to +85°C	30 WLP (0.5mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Typical Operating Circuit appears at end of data sheet.

System Power Management for Mobile Handset

ABSOLUTE MAXIMUM RATINGS

BATT, OUT1, SAFE_OUT, and INVIB to AGND ....-0.3V to +6.0V
CHG_IN, OUT2, LED1, and LED2 to AGND ....-0.3V to +30V
LED3 and CHG_MON to AGND.... -0.3V to (V_{SAFE_OUT} + 0.3V)
COMP2, $\overline{IRQ}$, $\overline{RESET\_IN}$, COMP1, SCL, SDA, $\overline{CHG}$, PWR_ON_CMP, REF, LDO1, LDO2, LDO3, LDO4, and LDO1_EN to AGND .... -0.3V to (V_{BATT} + 0.3V)
OUTVIB to AGND ....-0.3V to (V_{INVIB} + 0.3V)
PGND1 and PGND2 to AGND ....-0.3V to +0.3V

LX1, LX2 Current (Note 1)..1.7A_{RMS}
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 24.4mW/°C above +70°C)..........................1.9W
Operating Temperature.................................... -40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Soldering Temperature (reflow) ....+260°C

Note 1: LX1 has internal clamp diodes to PGND1 and OUT1. LX2 has internal clamp diodes to PGND2 and OUT2. Applications that forward bias these diodes should take care not to exceed the IC package power dissipation limit.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....41°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS (Note 3)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATT						
BATT Operating Voltage			2.9		5.5	V
BATT Shutdown Supply Current	All outputs off, I^2C disabled, V_{SCL} = V_{SDA}= $V_{\overline{RESET\_IN}}$ = 0V	T_A = +25°C		0.4	1	µA
		T_A = +85°C		0.4	1	
BATT Standby Supply Current	All outputs off, V_{SCL} = V_{SDA} = $V_{\overline{RESET\_IN}}$ = 1.8V, I^2C ready	T_A = +25°C		5	10	µA
		T_A = +85°C		5		
BATT Biasing Supply Current	I^2C ready, one or more outputs on			60		µA
Undervoltage Lockout (UVLO) Threshold	BATT rising		2.6	2.75	2.9	V
Undervoltage Lockout Hysteresis				100		mV
THERMAL SHUTDOWN						
Threshold				+160		°C
Hysteresis				20		°C
REFERENCE						
Reference Output Voltage				1.200		V
Reference Supply Rejection				0.2		mV
LOGIC AND CONTROL INPUTS						
Input Low Level	SDA, SCL, LDO1_EN, $\overline{CHG}$, and $\overline{RESET\_IN}$				0.4	V
Input High Level	SDA, SCL, LDO1_EN, $\overline{CHG}$, and $\overline{RESET\_IN}$		1.40			V
Logic-Input Current	SDA, SCL, LDO1_EN, $\overline{CHG}$, and $\overline{RESET\_IN}$, 0 < V_{IN} < 5.5V	T_A = +25°C	-1		+1	µA
		T_A = +85°C		0.1		

ELECTRICAL CHARACTERISTICS (Note 3) (continued)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC AND CONTROL OUTPUTS					
$\overline{IRQ}$ (Open-Drain Output) Output Low Voltage	$I_{\overline{IRQ}}$ = 2mA			0.4	V
PWR_ON_CMP (Open-Drain Output) Output Low Voltage	$I_{PWR\_ON\_CMP}$ = 2mA			0.4	V
SDA Output Low Level	I_{SDA} = 6mA			0.4	V
I²C SERIAL INTERFACE (V_{SCL} = V_{SDA} = 3V) (Figure 15)					
Clock Frequency				400	kHz
Bus-Free Time Between START and STOP	t_{BUF}	1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}	0.6			µs
SCL Low Period	t_{LOW}	1.3			µs
SCL High Period	t_{HIGH}	0.6			µs
Setup Time Repeated START Condition	t_{SU_STA}	0.6			µs
SDA Hold Time	t_{HD_DAT}	0			µs
SDA Setup time	t_{SU_DAT}	100			ns
Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA and CLK Signals			50		ns
Setup Time for STOP Condition	t_{SU_STO}	0.6			µs
CHG_IN					
Input Operating Range		4.1		10	V
CHG_IN Current	V_{CHG_IN} = 28V, V_{BATT} = 4V, MAX8939A/MAX8939B	400	600	1000	µA
CHG_IN Leakage Current from CHG_IN to BATT	V_{CHG_IN} = 28V, V_{BATT} = 0V, MAX8939A/MAX8939B		21	80	µA
Reverse Leakage Current from BATT to CHG_IN	V_{CHG_IN} = 0V, V_{BATT} = 0 to 4.2V, MAX8939A/MAX8939B			10	µA
CHG_IN Trip Point	V_{CHG_IN} - V_{BATT}, rising	200	300	400	mV
	V_{CHG_IN} - V_{BATT}, falling		100		
	V_{CHG_IN} - V_{BATT}, hysteresis		200		
Input Undervoltage Threshold (UV)	MAX8939, V_{CHG_IN} rising, 500mV hysteresis (typ)	3.9	4.0	4.1	V
	MAX8939A/MAX8939B, V_{CHG_IN} rising, 900mV hysteresis (typ)	3.9	4.0	4.1	
Input Overvoltage Threshold (OVP)	MAX8939, V_{CHG_IN} rising, 200mV hysteresis (typ)	10.2	10.6	11	V
	MAX8939A/MAX8939B, V_{CHG_IN} rising, 200mV hysteresis (typ)	6.25	6.5	6.75	
Input Supply Current	I_{CHG_IN} - I_{BATT} = 90mA		750	1500	µA
Shutdown Input Current	Charger disabled			500	µA

ELECTRICAL CHARACTERISTICS (Note 3) (continued)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CHG_IN to BATT Dropout On-Resistance	V_{CHG_IN} = 3.7V, V_{BATT} = 3.6V			0.4	0.8	Ω
SAFE_OUT						
SAFE_OUT Regulated Output	I_{SAFE_OUT} = 15mA, V_{CHG_IN} = 5V, T_A = 0°C to +85°C		4.75	4.90	5.00	V
	I_{SAFE_OUT} = 15mA, V_{CHG_IN} = 10V, T_A = 0°C to +85°C				5.2	
SAFE_OUT Current Limit				100		mA
CHG_MON						
I/V Conversion Factor	Monitoring voltage to charge current - fast-charge current = 450mA (Note 4)			2.666		mV/mA
I/V Accuracy	Overall range		-10		+10	%
Output Voltage	450mA charge current - fast-charge current = 450mA (Note 4)			1200		mV
Charge Monitoring Range			0		1.2	V
Output Impedance			10	20	40	kΩ
INDICATOR LED						
LED3 Current Sink	V_{CHG_IN} = 5V, T_A = 0°C to +85°C		1.5	3	5	mA
BATT						
BATT Regulation Voltage (MAX8939)	I_{BATT} = 90mA, V_{BATT} programmed to 4.2V	T_A = +25°C	4.179	4.2	4.221	V
		T_A = -40°C to +85°C	4.158	4.2	4.242	
BATT Regulation Voltage (MAX8939A)	I_{BATT} = 90mA, T_A = +25°C	VSET = 11b	4.129	4.150	4.171	V
	I_{BATT} = 90mA, T_A = -40°C to +85°C	VSET = 00b	3.465	3.500	3.535	
		VSET = 01b	3.811	3.850	3.889	
		VSET = 10b	4.009	4.050	4.091	
		VSET = 11b	4.108	4.150	4.192	
BATT Regulation Voltage (MAX8939B)	I_{BATT} = 90mA, T_A = +25°C	VSET = 11b	4.149	4.170	4.191	V
	I_{BATT} = 90mA, T_A = -40°C to +85°C	VSET = 00b	3.465	3.500	3.535	
		VSET = 01b	3.811	3.850	3.889	
		VSET = 10b	4.009	4.050	4.091	
		VSET = 11b	4.129	4.170	4.192	
Programmable Restart Fast-Charge Threshold	From BATT regulation voltage, default = disable			-200 -300 -400 Disable		mV

ELECTRICAL CHARACTERISTICS (Note 3) (continued)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
CHG_IN Fast-Charge Current (MAX8939) (Note 5)	V_{BATT} = 3.5V	CHG_CONTROL_A.FAST_CHARGE = 000b		80	90	100	mA
		001b		240	270	300	
		010b		400	450	500	
		011b		560	630	700	
		100b		630	765	900	
		101b		700	850	1000	
		110b		940	1020	1200	
		111b		1050	1275	1500	
CHG_IN Fast-Charge Current (MAX8939A/MAX8939B) (Note 5)	V_{BATT} = 3.5V	CHG_CONTROL_A.FAST_CHARGE = 000b		82	90	98	mA
		001b		250	270	290	
		010b		420	450	480	
		011b		575	630	685	
		100b		695	765	835	
		101b		775	850	925	
		110b		100	120	140	
		111b		160	180	200	
CHG_IN Precharge Current	V_{BATT} = 2V				90	100	mA
BATT Prequalification Threshold Voltage	V_{BATT} rising hysteresis 140mV (typ)			2.5	2.55	2.6	V
Soft-Start Time	Ramp time to fast-charge current				2.5		ms
TOP-OFF							
Top-Off Threshold (% of Fast-Charge Current)	I_{BATT} falling	TOP_OFF = 00b			10		%
		TOP_OFF = 01b			20		
		TOP_OFF = 10b			30		
		TOP_OFF = 11b (default)			0		
TIMER							
Timer Accuracy				-20		+20	%
Fast-Charge Time Limit	From entering fast-charge to V_{BATT} < 4.2V	MAX8939	CCTR = 00b (default)		60		min
			CCTR = 01b		120		
			CCTR = 10b		240		
		MAX8939A/ MAX8939B	CCTR = 00b (default)		24		
			CCTR = 01b		120		
			CCTR = 10b		240		
Precharge Timer	MAX8939				30		min
	MAX8939A/MAX8939B				12		

ELECTRICAL CHARACTERISTICS (Note 3) (continued)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Top-Off Timer	TOPOFF_TIME = 00b			30		min
	TOPOFF_TIME = 01b			60		
	TOPOFF_TIME = 10b			120		
	TOPOFF_TIME = 11b			Disable		
Watchdog Timer	MAX8939		2.5	5	10	s
	MAX8939A/MAX8939B		15	30	45	
THERMAL LOOP						
Thermal Limit Temperature	Junction temperature when the charge current is reduced, T_J rising, default value	+70°C [00]		+100		°C
		+85°C [01]				
		+100°C [10]				
		+115°C [11]				
OUT1 STEP-UP DC-DC CONVERTER						
Input Voltage (V_{BATT})			2.9		5.5	V
Input Supply Current	2MHz switching, V_{OUT} = 5V, no load			11		mA
OUT1 Voltage Accuracy	500mA load	T_A = +25°C	-3		+3	%
		T_A = +85°C	-4		+4	
Maximum Output Current	V_{BATT} ≥ 3.2V, V_{OUT1} = 5.0V		550	700		mA
nFET Current Limit			2.0			A
Line Regulation	V_{BATT} = 2.9V to 4.2V			0.1		%/V
Load Regulation	0 to 500mA load			0.5		%/A
LX1 nFET On-Resistance	LX1 to PGND1, I_{LX1} = 200mA			0.1	0.2	Ω
LX1 pFET On-Resistance	LX1 to OUT1, I_{LX1} = -200mA			0.15	0.3	Ω
LX1 Leakage	V_{LX1} = 5.5V	T_A = +25°C		0.01	5	µA
		T_A = +85°C		0.1		
Switching Frequency			1.8	2	2.2	MHz
Maximum Duty Cycle			65	75		%
Minimum Duty Cycle				8		%
COMP Discharge Resistance	During shutdown or UVLO			220		Ω
VIBRATOR						
Programmable Output Voltage OUTVIB	1mA at V_{BATT} = V_{INVIB} = 5.5V, 150mA at V_{BATT} = V_{INVIB} = 3.4V, default value			3		V
Output Current					200	mA
Current Limit	V_{OUTVIB} = 0V			400	600	mA
Dropout Voltage	I_{LOAD} = 135mA, T_A = +25°C			150	300	mV
Line Regulation	3.4V ≤ V_{BATT} = V_{INVIB} < 5.5V, I_{LOAD} = 100mA			2.2		mV
Load Regulation	1mA < I_{LOAD} < 200mA			25		mV
Power-Supply Rejection $\Delta V_{INVIB}/\Delta V_{OUTVIB}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA			40		dB
Output Noise	100Hz to 100kHz, I_{LOAD} = 30mA			65		μV_{RMS}
Discharge Time Constant	T_{OFF} 90% to 5%, C = 1µF			0.1		ms

ELECTRICAL CHARACTERISTICS (Note 3) (continued)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Active Stop	nFET on-resistance		1		Ω
Active Brake on Shutdown	nFET on duration		85		ms
LDO1					
Output Accuracy	I_{LOAD} = 1mA	-3		+3	%
Maximum Output Current		400			mA
Current Limit	V_{LDO1} = 0V		600		mA
Dropout Voltage	I_{LOAD} = 200mA		200	400	mV
Line Regulation	3.4V ≤ V_{BATT} ≤ 5.5V, I_{LOAD} = 100mA		2.4		mV
Load Regulation	50µA < I_{LOAD} < 200mA		25		mV
Power-Supply Rejection $\Delta V_{LDO1}/\Delta V_{BATT}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, I_{LOAD} = 30mA		50		$µV_{RMS}$
Ground Current	I_{LOAD} = 500µA		21		µA
Shutdown Discharge Time	T_{OFF} 90% to 10%, C = 4.7µF			1	ms
Shutdown Output Impedance			50	80	Ω
LDO2, LDO3					
Output Accuracy	I_{LOAD} = 1mA	-3		+3	%
Maximum Output Current		200			mA
Current Limit	Output = 0V		400	700	mA
Dropout Voltage	I_{LOAD} = 135mA		200	400	mV
Line Regulation	3.4V ≤ V_{BATT} ≤ 5.5V, I_{LOAD} = 100mA		2.4		mV
Load Regulation	50µA < I_{LOAD} < 200mA		25		mV
Power-Supply Rejection $\Delta V_{LDO\_}/\Delta V_{BATT}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise Voltage (RMS)	100Hz to 100kHz, I_{LOAD} = 30mA		50		$µV_{RMS}$
Ground Current	I_{LOAD} = 500µA		21		µA
Shutdown Discharge Time	T_{OFF} 90% to 10%, C = 1µF			1	ms
Shutdown Output Impedance			100	150	Ω
LDO4					
Output Accuracy	I_{LOAD} = 1mA	-3		+3	%
Maximum Output Current		100			mA
Current Limit	V_{LDO4} = 0V		200	400	mA
Dropout Voltage	I_{LOAD} = 70mA		200	400	mV
Line Regulation	3.4V ≤ V_{BATT} ≤ 5.5V, I_{LOAD} = 50mA		2.4		mV
Load Regulation	50µA < I_{LOAD} < 100mA		25		mV
Power-Supply Rejection $\Delta V_{LDO4}/\Delta V_{BATT}$	f = 10Hz to 10kHz, I_{LOAD} = 30mA		60		dB
Output Noise	100Hz to 100kHz, I_{LOAD} = 30mA		50		$µV_{RMS}$
Ground Current	I_{LOAD} = 500µA		25		µA
Shutdown Discharge Time	T_{OFF} 90% to 10%, C = 1µF			1	ms
Shutdown Output Impedance			100	150	Ω

ELECTRICAL CHARACTERISTICS (Note 3) (continued)

(V_{BATT} = 3.7V, V_{CHG_IN} = 5.0V, circuit of Figure 1, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUT2 WLED STEP-UP CONVERTER					
Input Supply Voltage		2.9		5.5	V
Input Supply Current	2MHz, no load		2	2.5	mA
OUT2 Leakage Current	T_A = +25°C, V_{OUT2} = 5.5V, shutdown		0.01	1	µA
	T_A = +85°C, V_{OUT2} = 5.5V, shutdown		0.1	5	
LED1, LED2					
Current Regulator Dropout Voltage (Note 6)	25.25mA setting			200	mV
LED_ Regulation Voltage			350		mV
LED_ Current Accuracy	T_A = +25°C, $I_{LED\_}$= 25.25mA	-3		+3	%
	T_A = -40°C to +85°C, $I_{LED\_}$= 25.25mA	-5		+5	
Leakage Current	T_A = +25°C, in shutdown		0.01	1	µA
	T_A = +85°C, in shutdown		0.1	5	
LX2					
nFET Current Limit		710	860		mA
nFET On-Resistance	I_{LX2} = 200mA		0.3	0.7	Ω
LX2 Leakage Current	T_A = +25°C, 5.5V, shutdown		0.01	1	µA
	T_A = +85°C, 5.5V, shutdown		0.1	5	
Operating Frequency		1.8	2	2.2	MHz
Maximum Duty Cycle	V_{LED1} or V_{LED2} = 0.2V		90		%
COMP2					
Transconductance			20		µs
Soft-Start Charge Current			60		µA
Discharge Pulldown			20		kΩ
PROTECTION					
Overvoltage Threshold	V_{OUT2} rising	28		30	V
Overvoltage Hysteresis			4		V
Open LED Detection			100	120	mV
Shorted LED Detection		V_{OUT2} - 2.2V	V_{OUT2} - 0.7V		V

Note 3: Limits are 100% production tested at T_A = +25°C, unless otherwise noted. Min/max limits over the operating temperatures range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 4: The monitoring voltage is proportional to the charging current with a ratio depending on the programmed fast-charge current. For the current equal to the fast-charge current, the monitoring voltage is typically 1.2V.

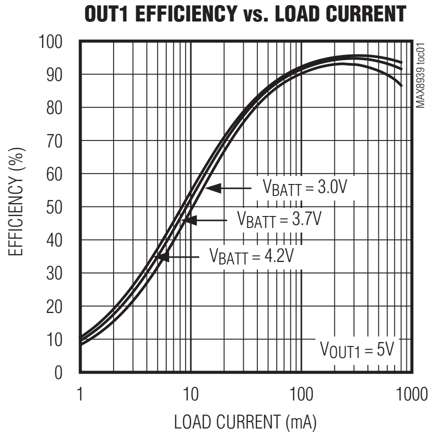
Note 5: The maximum CHG_IN current is the typical value plus 10% for currents up 700mA and the typical value plus 15% for higher currents.

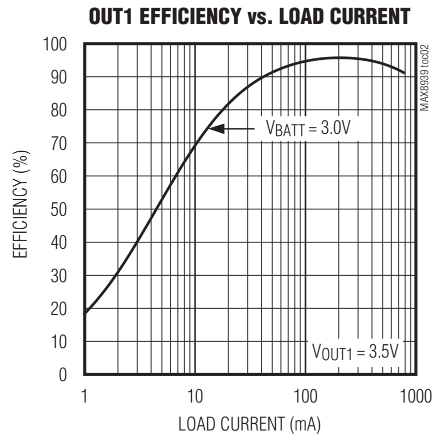
Note 6: LED dropout voltage is defined as the LED_ to ground voltage when current into LED_ drops 10% from the value at $V_{LED\_}$= 0.5V.

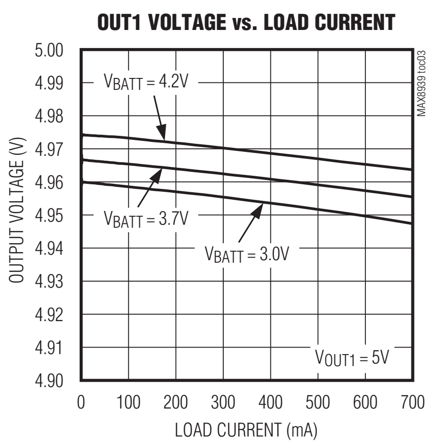
Typical Operating Characteristics

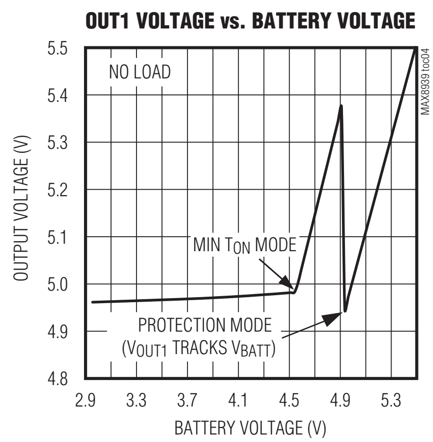
(V_{BATT} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

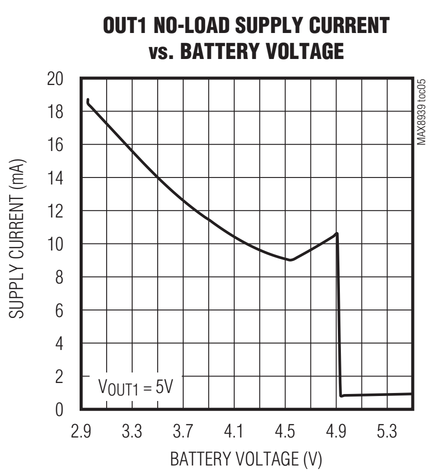
OUT1 STEP-UP CONVERTER

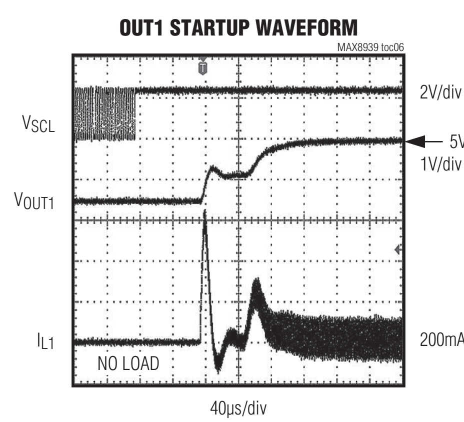








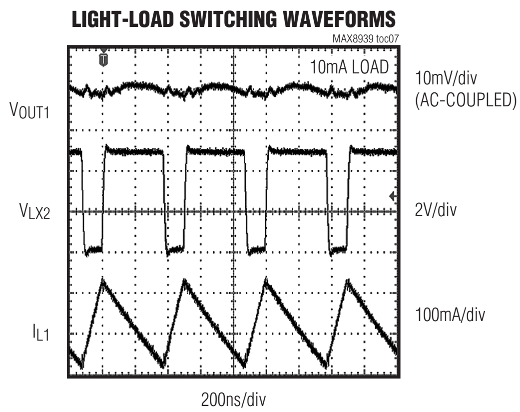


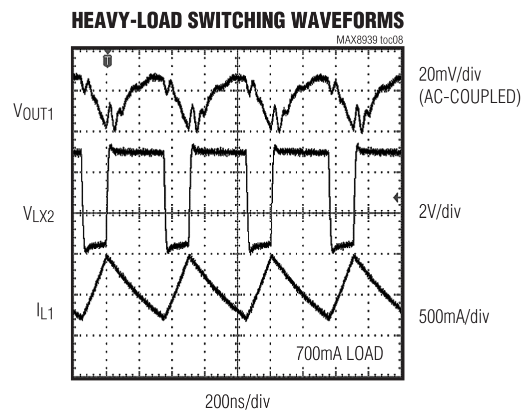


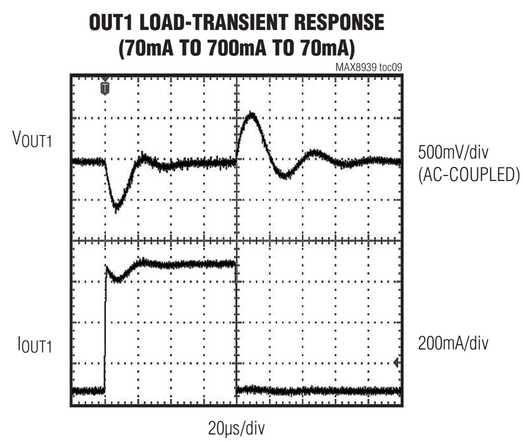
Typical Operating Characteristics (continued)

(V_{BATT} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

OUT1 STEP-UP CONVERTER (CONTINUED)



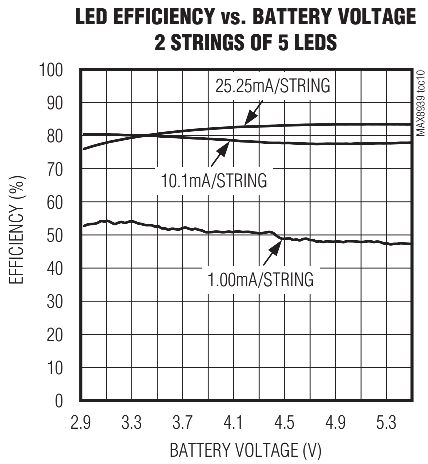


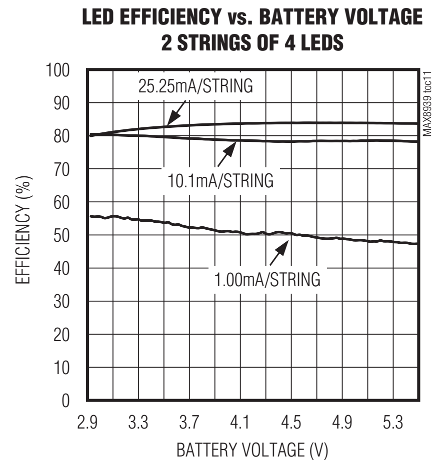


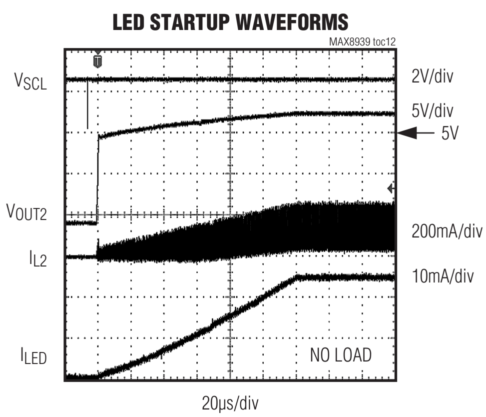
Typical Operating Characteristics (continued)

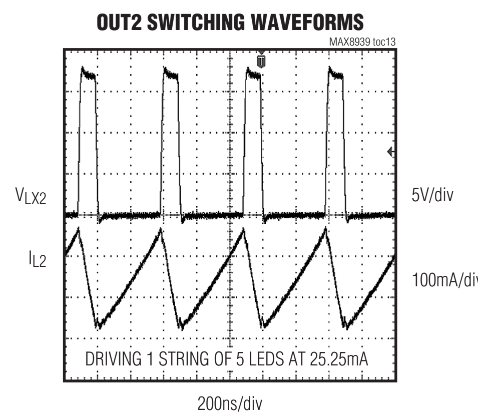
(V_{BATT} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

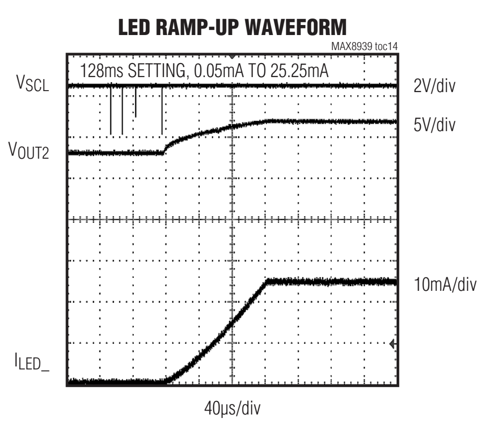
OUT2 WHITE LED DRIVER







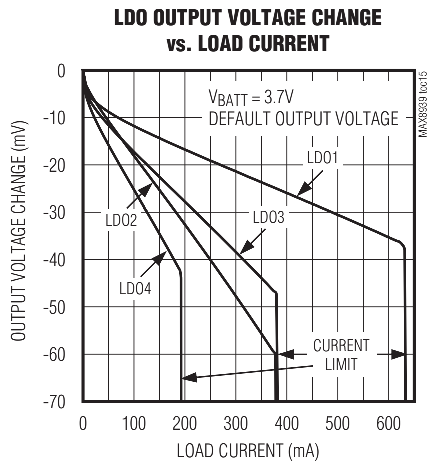


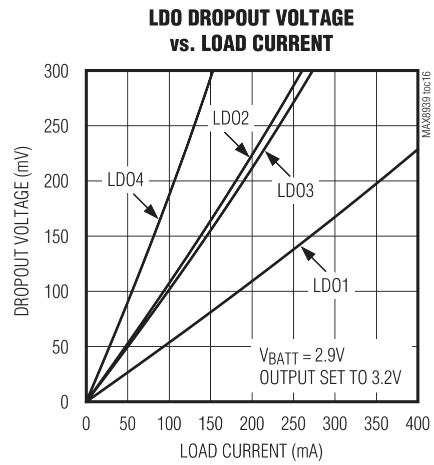


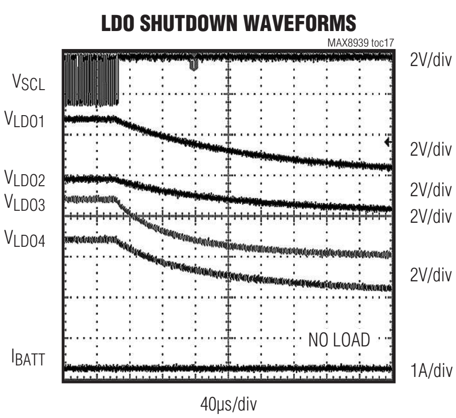
Typical Operating Characteristics (continued)

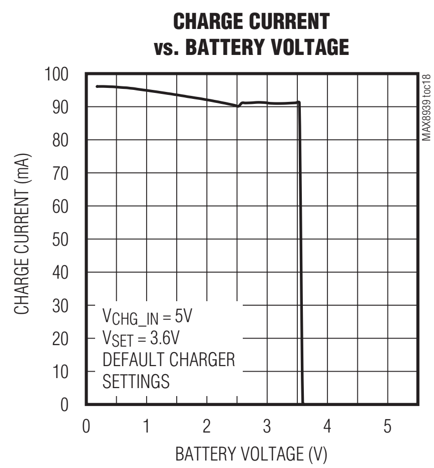
(V_{BATT} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

LDOs







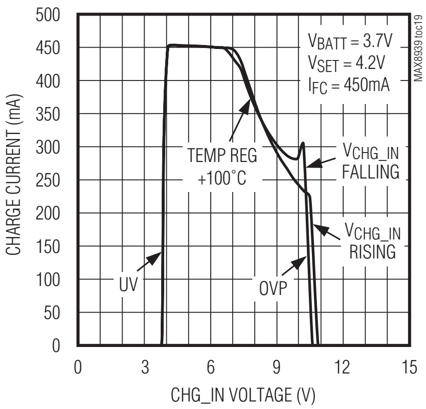


Typical Operating Characteristics (continued)

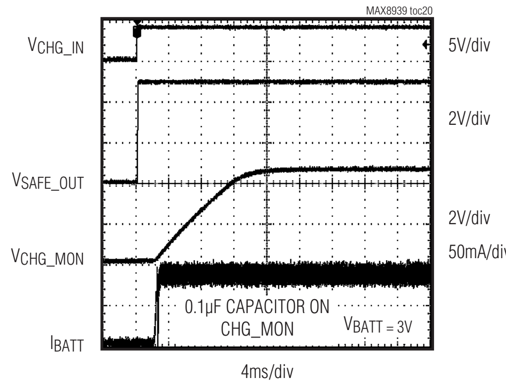
(V_{BATT} = 3.7V, circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

BATTERY CHARGER

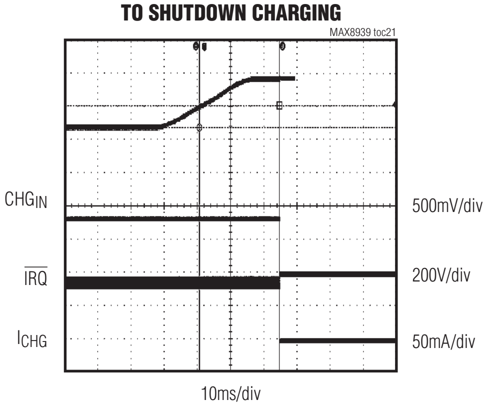
CHARGE CURRENT vs. CHG_IN VOLTAGE



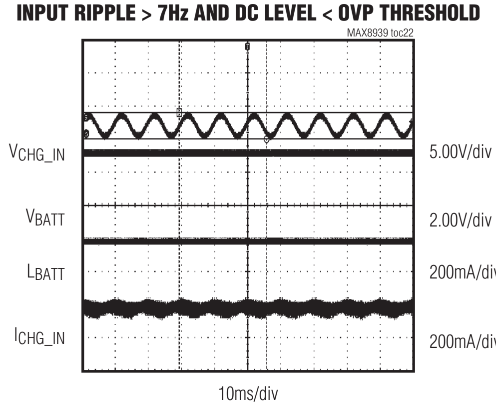
CHARGER CONNECT WAVEFORM



DEBOUNCE TIME FROM OVP DETECT TO SHUTDOWN CHARGING

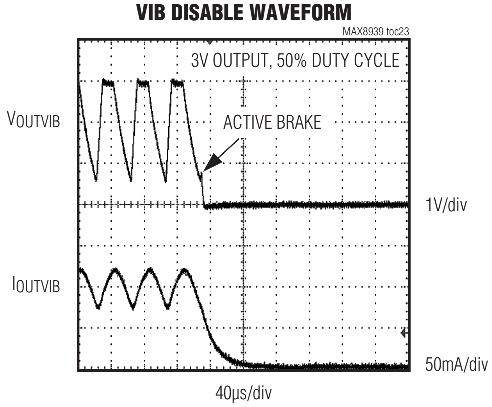


CHARGER CONTINUES CHARGING AT HIGH INPUT RIPPLE > 7Hz AND DC LEVEL < OVP THRESHOLD

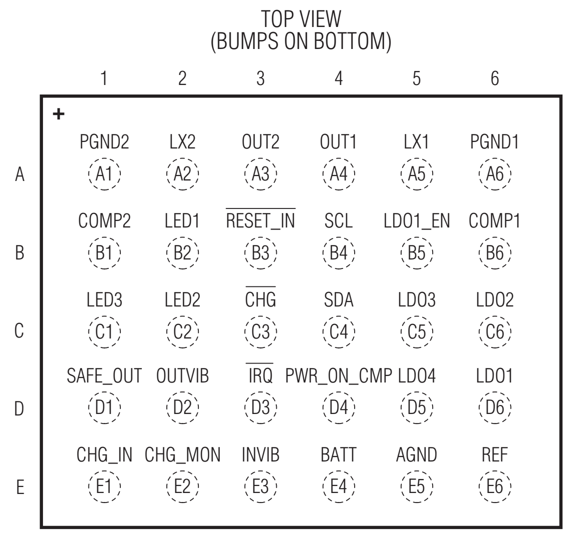


VIBRATOR DRIVER

VIB DISABLE WAVEFORM



Bump Configuration



WLP 0.5mm PITCH

Bump Description

PIN	NAME	FUNCTION
A1	PGND2	Power Ground for WLED Boost Converter. Connect PGND1, PGND2, and AGND to the PCB ground plane.
A2	LX2	Inductor Connection and Switching Node for WLED Boost Converter
A3	OUT2	WLED Step-Up Converter Output. Connect a 1µF capacitor from OUT2 to PGND2.
A4	OUT1	Step-Up Converter Output. Connect a 2.2µF capacitor from OUT1 to ground.
A5	LX1	Inductor Connection and Switching Node for OUT1 Step-Up Converter
A6	PGND1	Power Ground for OUT1 Step-Up Converter. Connect PGND1, PGND2, and AGND to the PCB ground plane.
B1	COMP2	Step-Up Compensation Node for OUT2 Step-Up Converter. Connect a 0.22µF ceramic capacitor from COMP to ground. The applied COMP capacitance stabilizes the converter and sets the soft-start time. COMP discharges to ground through a 20kΩ resistance when in shutdown.
B2	LED1	25mA LED Current Regulator. Connect LED1 to the cathode of the first LED string.
B3	$\overline{\text{RESET\_IN}}$	Active-Low Reset Input. Pulse $\overline{\text{RESET\_IN}}$ low to reset all registers (except STATUS and EVENT) to their default state.
B4	SCL	Clock Input for I^2C Serial Interface. High impedance when the I^2C interface is off.
B5	LDO1_EN	Enable Input for LDO1. Drive LDO1_EN high to enable LDO1, or low to disable LDO1. Once LDO1 is enabled or disabled through I^2C, the state of LDO1_EN is ignored until reset.
B6	COMP1	Compensation for OUT1 Step-Up Converter. Connect a 2200pF capacitor from COMP1 to ground. See the *Soft-Start OUT1* section for more details.

Bump Description (continued)

PIN	NAME	FUNCTION
C1	LED3	Indicator LED Connection. Connect LED3 to the cathode of the precharge indicator LED. If a precharge indicator LED is not used, leave LED3 unconnected.
C2	LED2	25mA LED Current Regulator. Connect LED2 to the cathode of the second LED string.
C3	$\overline{CHG}$	Charger Disable Input. Connect $\overline{CHG}$ high to disable the charger, or low to enable the charger. Once the charger is enabled or disabled through I^2C, the state of $\overline{CHG}$ is ignored until reset.
C4	SDA	Data Input for Serial Interface. High impedance when the I^2C interface is off.
C5	LDO3	200mA LDO Output. Connect a 2.2µF capacitor from LDO3 to ground. In shutdown, LDO3 is pulled to ground through an internal 100Ω.
C6	LDO2	200mA LDO Output. Connect a 2.2µF capacitor from LDO2 to ground. In shutdown, LDO2 is pulled to ground through an internal 100Ω.
D1	SAFE_OUT	4.9V Regulated LDO Output with Input Overvoltage Protection. Connect a 1µF ceramic capacitor from SAFE_OUT to ground. SAFE_OUT can be used to supply low-voltage-rated USB systems and the precharge indicator.
D2	OUTVIB	Vibrator Driver Output. Connect OUTVIB to the vibrator motor. Connect a 1µF ceramic capacitor from OUTVIB to ground.
D3	$\overline{IRQ}$	Interrupt Request Open-Drain Output
D4	PWR_ON _CMP	Open-Drain Output to Wake Sleeping Baseband. PWR_ON_CMP pulses low while the charger is connected. See the *PWR_ON_CMP* section for details.
D5	LDO4	100mA LDO Output. Connect a 1µF capacitor from LDO4 to ground. In shutdown, LDO4 is pulled to ground through an internal 100Ω.
D6	LDO1	400mA LDO Output. Connect a 4.7µF capacitor from LDO1 to ground. In shutdown, LDO1 is pulled to ground through an internal 50Ω.
E1	CHG_IN	Charger Input Supply Voltage. CHG_IN is the power-supply input for the SAFE_OUT linear regulator and the battery charger. The operating range for the charger input is 4.1V to 10V (MAX8939) or 6.25V (MAX8939A/MAX8939B). CHG_IN is protected up to 28V. When V_{CHG_IN} exceeds 10.6V (MAX8939) or 6.75 (MAX8939A/MAX8939B), SAFE_OUT and the charger are disabled. Connect a 1µF or larger ceramic capacitor from CHG_IN to ground.
E2	CHG_MON	Charge Current Monitoring Analog Output. CHG_MON outputs a voltage proportional to the charge current with 1.2V corresponding to the programmed fast-charge current. The CHG_MON output includes ripple from loads on the battery. If this is not desired, connect a small 0.01µF to 0.1µF capacitor at the input of the ADC to filter the ripple.
E3	INVIB	Input Supply for the Vibrator Driver. Connect INVIB to BATT. Connect a 1µF ceramic capacitor from INVIB to PGND.
E4	BATT	Battery Connection and IC Supply Voltage. Connect a 10µF ceramic capacitor from BATT to ground.
E5	AGND	Analog Ground. Connect PGND1, PGND2, and AGND to the PCB ground plane.
E6	REF	Reference Noise Bypass. Connect a 0.1µF ceramic capacitor from REF to AGND. Do not load. REF is high impedance when shut down.

Table 1. Output Summary

SUPPLY	OUTPUT RANGE	DEFAULT STATE AT POWER-UP	DEFAULT VALUE (V)	VOLTAGE TOLERANCE (%)	OUTPUT CURRENT (mA)	DESCRIPTION
LDO1	1.7V to 3.2V in 100mV step	Off	2.9	±3.0	400	Low-noise LDO to supply power either to the RF or analog section. LDO1 is controlled from the I²C bus or the LDO1_EN input.
LDO2	1.7V to 3.2V in 100mV step	Off	1.8	±3.0	200	Low-noise LDO to supply power either to the RF or analog section. LDO2 is controlled from the I²C bus.
LDO3	1.7V to 3.2V in 100mV step	Off	2.8	±3.0	200	Low-noise LDO to supply power either to the RF or analog section. LDO3 is controlled from the I²C bus.
LDO4	1.7V to 3.2V in 100mV step	Off	2.8	±3.0	100	Low-noise LDO to supply power either to the RF or analog section. LDO4 is controlled from the I²C bus.
OUT1 (STEP-UP)	3.5V to 5.0V in 100mV step	Off	5	±3.0	700	The OUT1 step-up converter provides a 5V power supply for an audio amplifier. The output voltage is programmable through I²C.
OUT2 (LED)	V_{BATT} to 28V	Off	N/A	N/A	60	The OUT2 step-up converter operates at 2MHz and provides a high-voltage source for the keypad and backlight display drivers.
OUTVIB (Vibrator)	1.3V, 2.5V, 3V, or INVIB bypass	Off	3	±3.0	200	High-power vibrator driver with programmable output voltage and speed control in 70 steps through I²C. The vibrator driver has active brake with stop.
Battery Charger	One-cell Li+ MAX8939: 3.6V, 4.15V, 4.20V, or 4.25V MAX8939A/ MAX8939B: 3.50V, 3.85V, 4.05V, or 4.17V	N/A*	MAX8939: 3.6 MAX8939A/ MAX8939B: 3.5	±0.6	90 default MAX8939: 1.3A (max) MAX8939A/ MAX8939B: 850mA (max)	A stand-alone constant-current, constant voltage (CC/CV), thermally regulated linear charger designed for charging a single-cell lithium-ion (Li+) battery. The charger current and protection timer is programmable through I²C.
SAFE_OUT	4.9V	N/A*	4.9	±3.0	100 (max)	Protected output SAFE_OUT can be used to supply low-voltage-rated USB systems and the precharge indicator. The output voltage is a fixed 4.9V.

**Subject to valid voltage present at CHG_IN.*

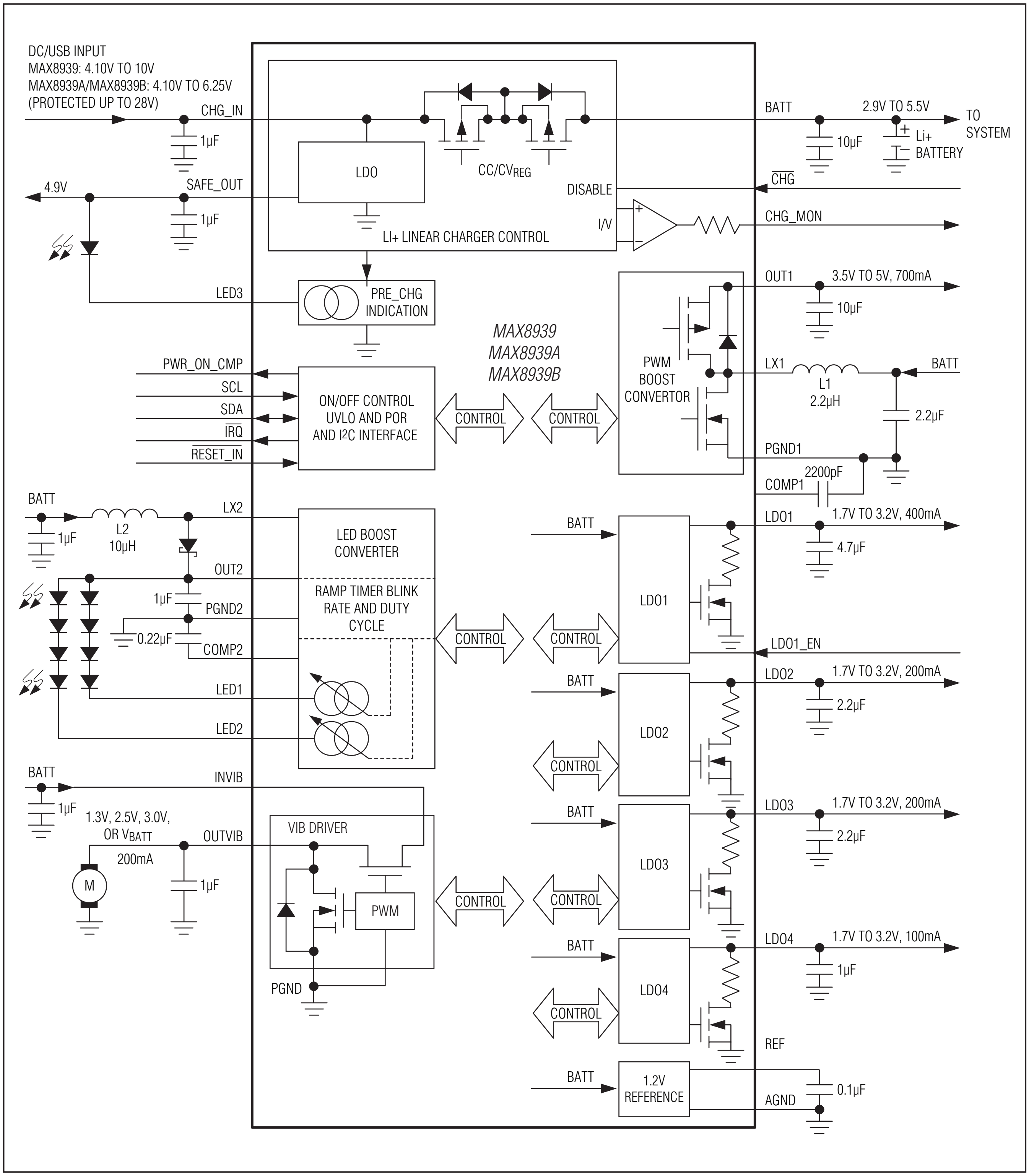


Figure 1. Typical Application Circuit and Block Diagram

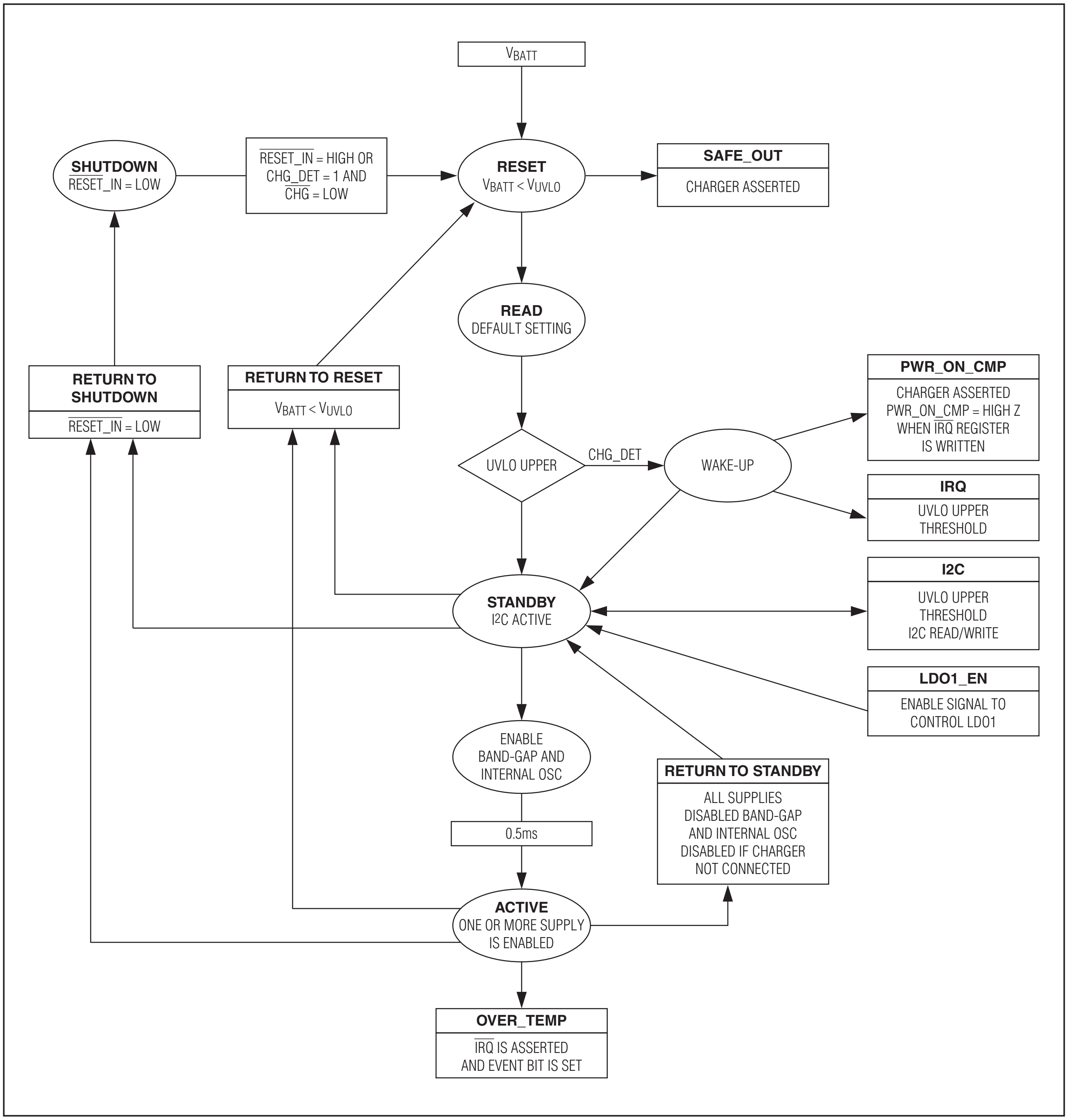


Figure 2. MAX8939/MAX8939A/MAX8939B State Diagram

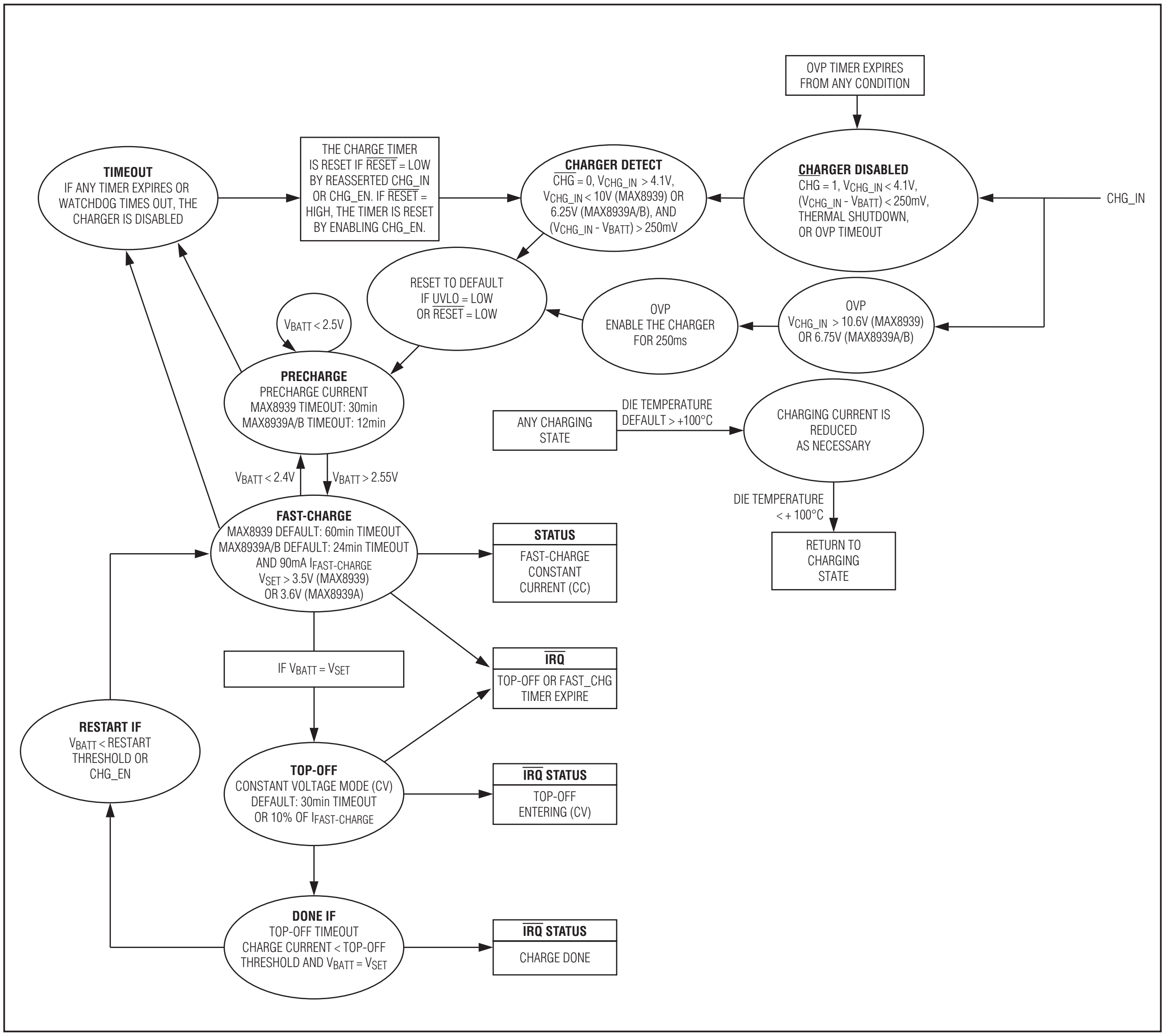


Figure 3. Battery Charger State Diagram

Detailed Description

Startup and Power States

To guarantee the correct startup of the MAX8939/MAX8939A/MAX8939B, an internal power-on reset is generated after the first connection of the battery. This resets the I^2C registers to the default values. The ICs are then in reset state. The reset state is a low power level, where the I^2C interface is disabled and it is not possible to read or write to any register. The ICs stay in reset state as long as V_{BATT} is below the UVLO upper threshold. When the battery voltage exceeds the UVLO upper threshold, the ICs enter the standby state and the I^2C bus can be written to. The typical response time of the UVLO detection is 50µs.

The UVLO upper threshold can be reached three ways:

- Fully charge battery is inserted and $\overline{\text{RESET}}$ is logic-high.
- $\overline{\text{RESET}}$ changes from logic-low to logic-high and $V_{BATT} > V_{UVLO\_UPPER}$.
- Charger is detected and $\overline{\text{CHG}}$ is logic-low.

Standby

Standby is a low-power state where the I^2C is ready for read/write operations and enables the different power units (Table 1). If a unit is enabled through I^2C or CHG_IN is powered, the bandgap and internal oscillator are started and the ICs move to the active state. The ICs stay in the active state until the last unit (including the charger) is disabled.

Reset

The ICs enter the reset state when the battery voltage drops below the UVLO lower threshold. In reset, all registers are reset except the STATUS and EVENT registers that retain their values as long as the battery is connected. In reset, all power units are disabled and only the UVLO and CHG_IN detection circuitry is active. If a fully charged battery is inserted or a charger is detected, the ICs enter standby. If a valid charger is connected, the state machine enables the PWR_ON_CMP generator and an interrupt is sent to the host when above the UVLO upper threshold. When a valid charger is detected while in the reset state, the SAFE_OUT LDO is enabled and the charger begins precharging the battery.

Shutdown

The shutdown state is an extremely low-power state. To enter shutdown, hold $\overline{\text{RESET}}$ logic-low.

In shutdown, all the internal blocks are disabled except the CHG_IN detection. If CHG_IN is asserted, the ICs move to the reset state and starts charging with the default settings. When entering from shutdown, the charger is reset and the PWR_ON_CMP generator is enabled. If the charger is removed, the ICs move back to the shudown state if $\overline{\text{RESET}}$ is still logic-low.

Charger

The ICs' charger uses voltage, current, and thermal-control loops to charge a single Li+ cell and to protect the battery. A complete charge cycle covers four states: prequalification (precharge), constant current fast-charge (CC), constant voltage top-off (CV), and charge complete (done). If the battery voltage is below 2.55V, the charger is pre-charging with 90mA until prequalification upper threshold is reach or the maximum precharge time (30min for the MAX8939 or 12min for the MAX8939A and MAX8939B) reached. The precharge timer is reset when CHG_IN is reasserted, and the charger starts charging if the battery voltage is below the precharge threshold. When the charger is in precharge mode, an LED indicator (LED3) and the SAFE_OUT LDO are turned on; all other functions are disabled.

Once the battery voltage has passed the prequalification upper threshold, the charger enters the fast-charge stage. An analog soft-start is used when entering fast charge to reduce inrush current on the input supply. When fast-charge is in progress, a safety timer is enabled and STATUS can be read out of register 0x02 bit 4. For the MAX8939/MAX8939A, the CHG_EN is cleared and starts charging if CHG_IN is asserted. The MAX8939B clears CHG_EN only if $\overline{\text{RESET}}$ is logic-low. By pulling $\overline{\text{RESET}}$ logic-high, the charger is disabled or enabled depending on the state of the CHG_EN bit. When CHG_IN is asserted, an interrupt occurs, and the host can control the state of the CHG_IN bit. The fast-charge current and safety timer are programmable through the I^2C interface. The safety timers are reset if the charger is disabled and start a new cycle when the charger is enabled. The default battery regulation voltage (V_{SET}) is 3.6V (MAX8939) or 3.5V (MAX8939A/MAX8939B), but can be programmed to 4.15V, 4.2V, or 4.25V for the MAX8939, or 3.85V, 4.05V, or 4.17V for the MAX8939A/MAX8939B.

When the battery voltage reaches V_{SET}, the charger changes to top-off mode (CV). When entering top-off, an $\overline{\text{IRQ}}$ is flagged to indicate that the charger is in constant voltage mode. Top-off mode keeps the voltage constant and the current falls slowly until the top-off current threshold is reached. An $\overline{\text{IRQ}}$ is flagged to indicate charge is done. The top-off current threshold is a percentage of the fast-charge current, the threshold is programmable. When the top-off current threshold is set to 0% and restart is disabled, the top-off mode continues until the top-off timer expires. The top-off timer is programmable and can also be disabled. With the op-off threshold set to 0% and top-off timer disabled, the charger continuously charges the battery with a constant voltage and decreasing charge current. This makes it possible to control the charge algorithm through software, without influence of automatic maintaining charge.

To qualify charge as done, the current has to be below top-off current threshold or a timeout has occurred. To maintain the battery voltage, the charger can be programmed to restart once the battery voltage drops below a programmable threshold. When restart is enabled and the battery voltage drops below the restart threshold, the charger starts a new charging cycle by entering fast-charge.

If restart is disabled, the charger stops charging when done and does not maintain the battery voltage. When charge done occurs, an $\overline{\text{IRQ}}$ is sent to the host and a flag is set in register 0x03. Reading the register disables the charger. The charger can be enabled by writing to register 0x09 bit 0 (CHG_EN). If one of the safety timers (fast-charge or top-off) expires, an interrupt is sent to the host and a flag is set in register 0x03. The charger is disabled 5s after the safety times out.

If, at any point while charging the battery, the die temperature approaches the thermal regulation threshold (+100°C default), the ICs reduce the charging current so that the die temperature does not increase. This feature not only protects the ICs from overheating, but also allows the higher charge current without risking damage to the system.

Note all charger registers are reset to their default settings by power-on reset (POR) or $\overline{\text{RESET}}$.

Charge On/Off Control

$\overline{\text{CHG}}$ is a logic hardware control input. Logic-high disables the charger and logic-low enables the charger.

1. $\overline{\text{CHG}}$ = logic-high, the charger is disabled when power pluck is asserted on CHG_IN and register 0x09 has not been affected. When $\overline{\text{CHG}}$ changes logic state, a flag is set in the event register 0x03, and an interrupt occurs.
2. $\overline{\text{CHG}}$ = Logic-low, the charger is enabled and starts charging if charging conditions are within operating limits.

Once the CHG_CONTROL_A register 0x09 is accessed either by reading or writing, the $\overline{\text{CHG}}$ is ignored. When $\overline{\text{CHG}}$ changes status after register 0x09 has been accessed, only STATUS and EVENT_A register is updated and an interrupt occurs. The CHG_EN bit in CHG_CONTROL_A register 0x09 is always [1] by default. The CHG_EN does not follow the status of $\overline{\text{CHG}}$, and the charger is enabled just by reading the CHG_CONTROL_A register 0x09 and $\overline{\text{CHG}}$ is ignored. To avoid the charger enabling just by accessing the CHG_CONTROL_A register 0x09, write [0] in the CHG_EN bit.

For the MAX8939 and MAX8939A, if the CHG_IN is reconnected, the $\overline{\text{CHG}}$ is reset and the status of the charger is following the logic level on $\overline{\text{CHG}}$, as long CHG_CONTROL_A register 0x09 is not affected. For the MAX8939B, the $\overline{\text{CHG}}$ is reset only by reasserting CHG_IN if $\overline{\text{RESET}}$ or UVLO is low.

SAFE_OUT

SAFE_OUT is an LDO powered from the CHG_IN input. SAFE_OUT is enabled when a charger is detected (4.1V < V_{CHG_IN} < 10V (MAX8939) or 6.25V (MAX8939A/MAX8939B)) and provides a protected output regulated to 4.9V (5V max). Typically, SAFE_OUT is used to power low-voltage USB systems and the precharge indicator.

Indicator LED

The LED3 output sinks 3mA (typ) to drive an indicator LED. LED3 is on by default and can be controlled by the host by I2C (bit 7 of the REG_CONTROL register). Typically, this LED indicates charge status and SAFE_OUT powers the LED as shown in Figure 1.

Charge Current Monitor (CHG_MON)

CHG_MON is an analog output used to monitor the charge current. CHG_MON outputs a voltage proportional to the charge current with 1.2V corresponding to the programmed fast-charge current.

The CHG_MON output includes ripple from loads on the battery. If this is not desired, connect a small 0.01μF to 0.1μF capacitor at the input of the ADC to filter the ripple.

Charger Watchdog Timer

During battery fast-charge, a watchdog monitoring function can be activated to ensure that the host processor has control of the charge algorithm. The watchdog timer is enabled through register REG_CONTROL bit WD_EN. When the charger is enabled by CHG_EN or CHG_IN, the watchdog timer starts counting. Within 5s of enabling the charger, the host must read or write register 0x09 or 0x0A to indicate it is alive. This resets the watchdog timer and the host must continue to read or write register 0x09 or 0x0A in intervals of under 5s. If the host takes more than 5s for reading or writing these registers, the watchdog timer expires, generates an interrupt, flags the watchdog timeout in register 0x03, and disables the charger (Figure 4).

Charge in Overvoltage Protection

To detect that a valid charger is asserted at CHG_IN, an upper and lower threshold is defined. This threshold is different for the MAX8939, MAX8939A, and MAX8939B. See the *Electrical Characteristics* table for upper/lower threshold.

If an overvoltage condition occurs on CHG_IN, a debounce timer is enabled and powers the charger down after a max delay of 324ms. When the charger is powered down, an interrupt occurs and a flag is set in event register A.

This OVP timer enables the possibility of using a low cost wall-plug adapter with poor voltage regulation. The charger continue charging and no interrupt occurs as long the OVP is not violating the max 324ms.

Fast thermal regulation ensures that the temperature does not exceed the programmed value (default is programmed at +100°C at high voltage < 30V and maximum charge current). If the junction temperature rises until the programmed value, the charge current is not switched off, but regulated down to a level to maintain the temperature around the programmed threshold.

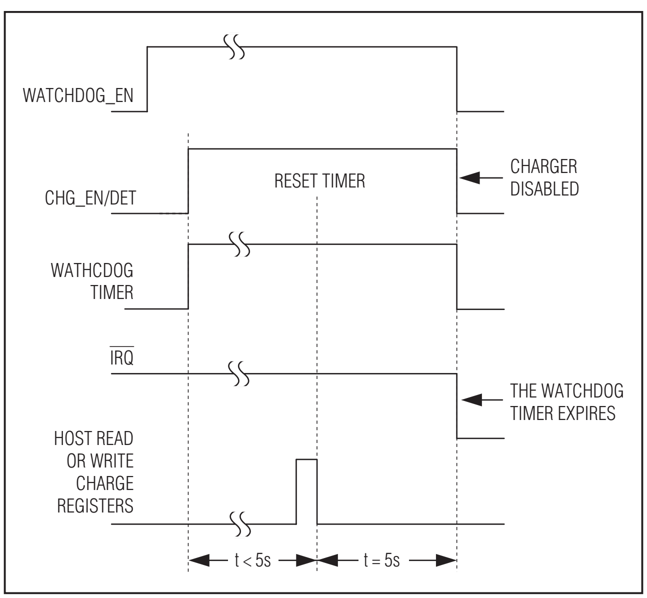


Figure 4. Watchdog Timing Diagram

Interrupt Request ($\overline{IRQ}$)

$\overline{IRQ}$ is an active-low, open-drain output signal (requires an external pullup resistor) that indicates that an interrupt event has occurred and that the event and status information are available in the event/status registers. Such information includes temperature and voltages inside the ICs fault conditions, etc. The event registers hold information about events that have occurred in the ICs. Events are triggered by a status change in the monitored signals. When an event bit is set in the event register, the $\overline{IRQ}$ signal is asserted (unless $\overline{IRQ}$ is masked by a bit in the IRQ mask register). The $\overline{IRQ}$ is also masked during power-up and is not released until the event registers have been read. Each event register is reset to its initial condition after being read. The $\overline{IRQ}$ is not released until all the event registers have been read. New events that occur during read-out of the event registers are held until all the event registers have been read to, ensuring that the host processor does not miss them.

PWR_ON_CMP is an open-drain output used to wake-up a sleeping baseband. PWR_ON_CMP is activated when a charger is detected (V_{CHG_IN} is between 4.1V and 10V (MAX8939) or 6.25V (MAX8939A/MAX8939B)) and the battery voltage is above the UVLO threshold. If the battery has already reached the UVLO upper threshold, the charger is detected by a rising edge. When such an

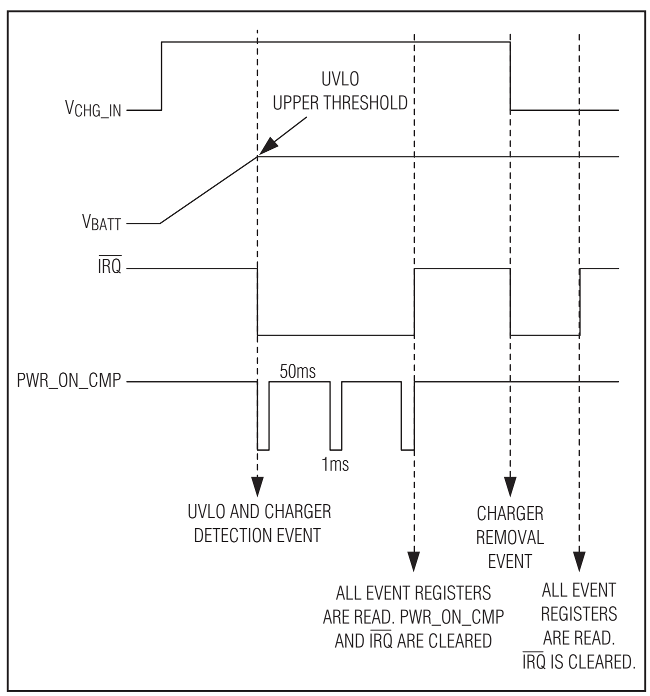


Figure 5. PWR_ON_CMP Sequence

event is detected, the ICs start pulsing the PWR_ON_CMP output every 50ms, with a duty cycle of 98%. See Figure 5.

The event is also signaled by $\overline{IRQ}$, which is asserted when the UVLO upper threshold is reached and the CHG_DET bit is set in register 0x04 (bit 6). The ICs continue pulsing PWR_ON_CMP until the EVENT registers 0x04 or 0x03 are read/written to or the charger safety timer expires. By reading/writing to the EVENT register, the register is cleared and PWR_ON_CMP and $\overline{IRQ}$ returns to high impedance.

The events causing the PWR_ON_CMP activation are triggered by a rising edge signal that must remain valid for the duration of a 10ms debounce filter.

$\overline{RESET\_IN}$

$\overline{RESET\_IN}$ is an active-low input signal to the ICs and is used to provide a full system reset inside the ICs. As long as $\overline{RESET\_IN}$ is logic-low, the ICs are not able to do anything (except the charger), until $\overline{RESET\_IN}$ is released. All registers are cleared except the STATUS and EVENT registers. When $\overline{RESET\_IN}$ is asserted, the EVENT_B bit $\overline{RESET}$ is set. If the CHG_IN voltage is valid and $\overline{RESET\_IN}$ is logic-low, the charger operates in its default state.

Linear Regulators

The ICs include four low-dropout linear regulators (LDOs). All LDOs are designed for low dropout, low noise, high PSRR, and low quiescent current to maximize battery life. When the battery voltage is above the UVLO upper threshold, the ICs' LDOs are ready to be turned on through the I²C interface. The guaranteed current drive capabilities for the LDOs are 400mA for LDO1, 200mA for LDO2 and LDO3, and 100mA for LDO4. The output voltage for each LDO is programmable through the I²C interface from 1.7V to 3.2V in 0.1V steps.

LDO1 can be enabled through a hardware pin LDO1_EN. By connecting this pin to a logic-high level, the LDO enables automatically when the UVLO upper threshold is reached. The LDO can also be controlled by the LDO1_EN bit of the REG_CONTROL. When the LDO1_EN bit is written to, the LDO1 enable state reflects the value written, overriding the state of the LDO1_EN pin. When the state of the LDO1_EN pin changes, the LDO1 enable state is determined by the new state of the LDO1_EN pin, overriding the LDO1_EN bit value. This allows the system software to reduce quiescent power consumption by turning off LDO1 without impacting other logic that may utilize the same hardware control used for the LDO1_EN pin.

OUT1 Step-Up DC-DC Converter

OUT1 is a fixed-frequency PWM step-up converter. The converter switches an internal power MOSFET and synchronous rectifier at a constant 2MHz frequency with varying duty cycle up to 75% to maintain constant output voltage as the input voltage and load current vary. Internal circuitry prevents any unwanted subharmonic switching in the critical step-down/step-up region by forcing a minimum 8% duty cycle.

OUT1 delivers up to 700mA to the load at a voltage programmable through I²C from 3.5V to 5V in 100mV steps.

Soft-Start OUT1

OUT1 soft-starts by charging C_{COMP1} with a 100μA current source. During this time, the internal MOSFET is switching at the minimum duty cycle. Once V_{COMP1} rises above 1V, the duty cycle increases until the output voltage reaches the desired regulation level. COMP1 is pulled to ground with a 30Ω internal resistor during UVLO or shutdown.

OUT2 White LED Driver

OUT2 is the output from the step-up DC-DC converter for driving white LEDs. The converter is able to drive up to 60mA at up to 28V. The step-up converter is adaptive connected to the two low-dropout LED current regulators. The step-up converter operates at a fixed 2MHz switching frequency, enabling the use of very small external components to achieve a compact circuit area. For improved efficiency, the step-up converter automatically operates in pulse-skipping mode at light loads.

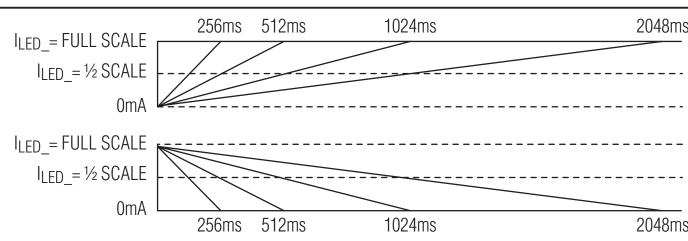


Figure 6. Ramp-Up/Ramp-Down

Soft-Start OUT2

From shutdown, once LED1 or LED2 is enabled through the I2C interface, the step-up converter prepares for soft-start. C_{COMP2} is quickly pulled to 1V by an internal pullup clamp. Since the LED_ feedback node voltage is less than the regulation threshold (0.35V typ), 40µA current is sourced from the error amplifier and further charges C_{COMP2}. Once V_{COMP2} reaches 1.25V, the step-up converter starts switching at a reduced duty cycle. As V_{COMP2} rises, the step-up converter duty cycle increases.

When V_{LED1} or V_{LED2} reaches 0.35V (typ), the error amplifier stops sourcing current to C_{COMP2}, soft-start ends, and the control loop achieves regulation as $V_{LED\_}$ settles. The V_{COMP2} where the step-up converter exits soft-start depends on the load. A 2.5V upper limit to V_{COMP2} is imposed to aid in transient recovery and to allow maximum output for low input voltages. C_{COMP2} is discharged to ground through a 20kΩ internal resistor whenever the step-up converter is turned off, allowing the device to reinitiate soft-start when it is enabled.

LED1 and LED2 Current Regulators

Each current regulator drives a series string of LEDs. The maximum number of LEDs depends of maximum forward voltage of the LEDs at the maximum desired current. The total forward voltage of the LED string must be below 27.65V. The LED current is independently programmed using the I2C interface from 50µA to 25.25mA with a 128-step logarithmic dimming scheme.

Ramp-Up/-Down

The ICs' LED current regulators provide ramp- up and ramp-down functionality for smooth transitions between different brightness settings. A controlled ramp is used when the LED current level is changed, and when the LEDs are enabled or disabled. LED1 and LED2 have individual ramp control, making it possible to ramp different groups at different rates. The ramp-up and ramp-down times are controlled by the LED__RU and LED__RD control bits, and the ramps are enabled/disabled by the LED__RAMP_EN bits. The ICs increase or decrease the current one step every t_{RAMP}/32 until the target LED current is reached.

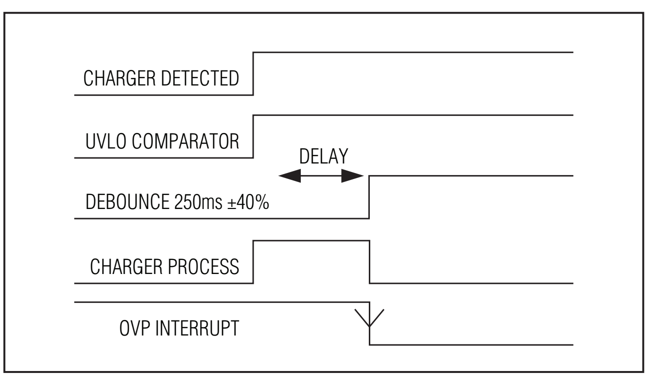


Figure 7. Timing of OVP Detection

Open/Short Detection

The ICs include comparators to detect open or shorted LEDs on LED1 and LED2. One comparator on each LED_ output detects when the voltage falls below 100mV, indicating an open LED fault. Another comparator on each LED_ output detects when the voltage rises above V_{OUT2} - 1V, indicating a shorted LED fault. The fault-detection comparators are enabled only when the corresponding LED_ current regulator is enabled and provides a continuous monitor of the current regulator conditions.

Once a fault is detected, it is flagged in the EVENT_B register and the $\overline{IRQ}$ signal is asserted (unless masked in the IRQ_MASK_B register).

Overvoltage Protection

If the voltage on the OUT2 rises above 28V (typ), the LED driver is put into the shutdown state. This protects the ICs from excessive voltage in the event of an open-circuit LED.

Vibrator Driver

The vibrator driver is an LDO with PWM control (see Figure 8). The LDO output voltage is programmable through I2C to 1.3V, 2.5V, 3.0V, and V_{BATT}.

The vibrator driver is driven with a PWM signal of duty cycle from 0% to 83% or 100%, with a repetition frequency of 23.8kHz divided into 84 steps. A PWM ratio set to greater than 83 results in the vibrator output being permanently enabled (100%). Figure 9 shows the output waveform at different output voltage and PWM settings. The duty cycle is set by the I2C interface, with a value greater than 0 enabling the PWM mode of operation. By using the enable/disable, an active stop is activated.

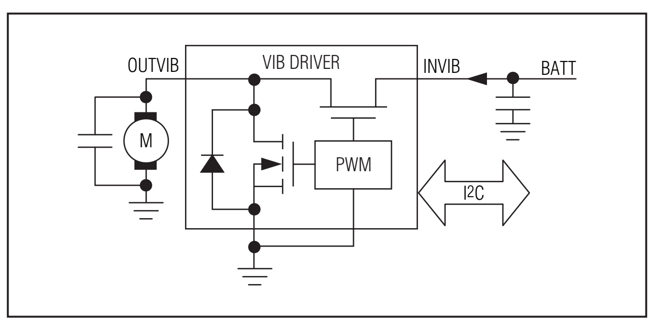


Figure 8. Vibrator Driver

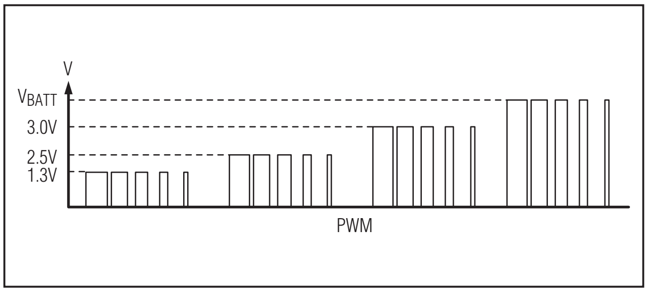


Figure 9. Vibrator Driver PWM Output

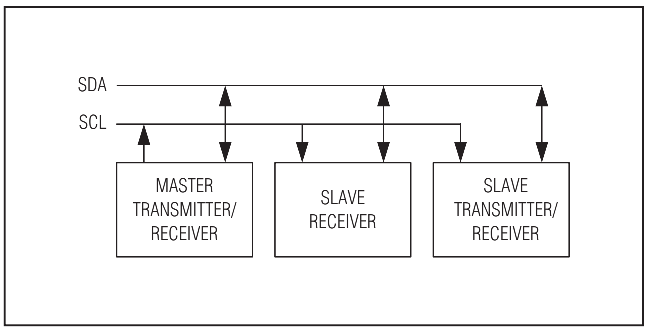


Figure 10. I²C Master/Slave Configuration

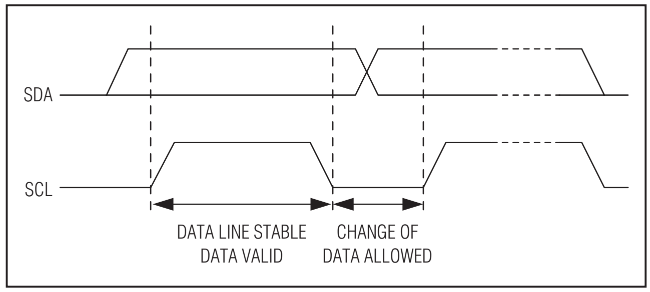


Figure 11. I²C Bit Transfer

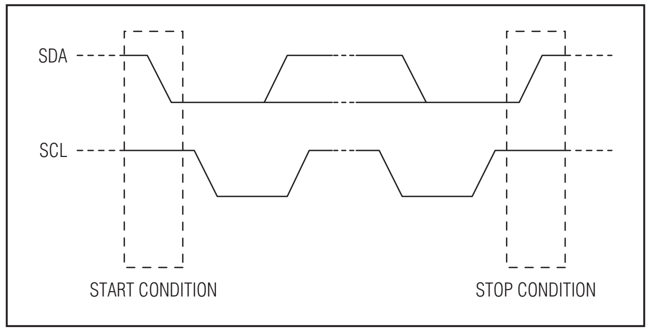


Figure 12. I²C START and STOP Conditions

When the vibrator is disabled, an nFET switch turns on and shorts the vibrator to ground. At the same time the nFET switch works as a recovery diode to protect against reverse voltage from the vibrator.

The ICs include current protection that limits the current in case the vibrator motor locks up.

Thermal Shutdown

The ICs monitor the die temperature at the charger and each LDO and DC-DC regulator. When the temperature exceeds +160°C, the individual regulator is shutdown is shutdown. Once the die cools by 20°C, the regulator may be reenabled through the I²C interface.

The charger has independent thermal control circuitry that lowers the charge current to regulate the die temperature during the charge. The charger cannot exceed a temperature higher than the programmed level (default +100°C, +115°C max).

I²C Serial Interface

The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). See Figure 10. The ICs are slave-only devices, relying upon a master to generate the clock signal. The master initiates data transfer on the bus and generates SCL to permit data transfer. The I²C slave address is 0x62 for write operations and 0x63 for read operations.

I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional (24Ω) resistors in series with SDA and SCL protect the IC inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus signals.

Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse (see Figure 11). Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section for more information).

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long; 8 bits of data followed by the acknowledge bit. The ICs support data transfer rates with SCL frequencies up to 400kHz.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low tran-