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19-1908; Rev 0; 5/01

EVALUATION KIT AVAILABLE

Quad LVDS Line Receivers with Integrated Termination

General Description

The MAX9125/MAX9126 quad low-voltage differential signaling (LVDS) line receivers are ideal for applications requiring high data rates, low power, and reduced noise. The MAX9125/MAX9126 are guaranteed to receive data at speeds up to 500Mbps (250MHz) over controlled-impedance media of approximately 100Ω. The transmission media may be printed circuit (PC) board traces or cables.

The MAX9125/MAX9126 accept four LVDS differential inputs and translate them to 3.3V CMOS outputs. The MAX9126 features integrated parallel termination resistors (nominally 115Ω), which eliminate the requirement for four discrete termination resistors and reduce stub length. The MAX9125 inputs are high impedance and require an external termination resistor when used in a point-to-point connection.

The devices support a wide common-mode input range of 0.05V to 2.35V, allowing for ground potential differences and common-mode noise between the driver and the receiver. A fail-safe feature sets the output high when the inputs are open, or when the inputs are undriven and shorted or parallel terminated. The EN and $\overline{EN}$ inputs control the high-impedance output and are common to all four receivers. Inputs conform to the ANSI TIA/EIA-644 LVDS standard. The MAX9125/MAX9126 operate from a single +3.3V supply, are specified for operation from -40°C to +85°C, and are available in 16-pin TSSOP and SO packages. Refer to the MAX9124 data sheet for a quad LVDS line driver.

Applications

Digital Copiers

Laser Printers

Cellular Phone Base Stations

Add/Drop Muxes

Digital Cross-Connects

DSLAMs

Network Switches/Routers

Backplane Interconnect

Clock Distribution

Pin Configuration appears at end of data sheet.

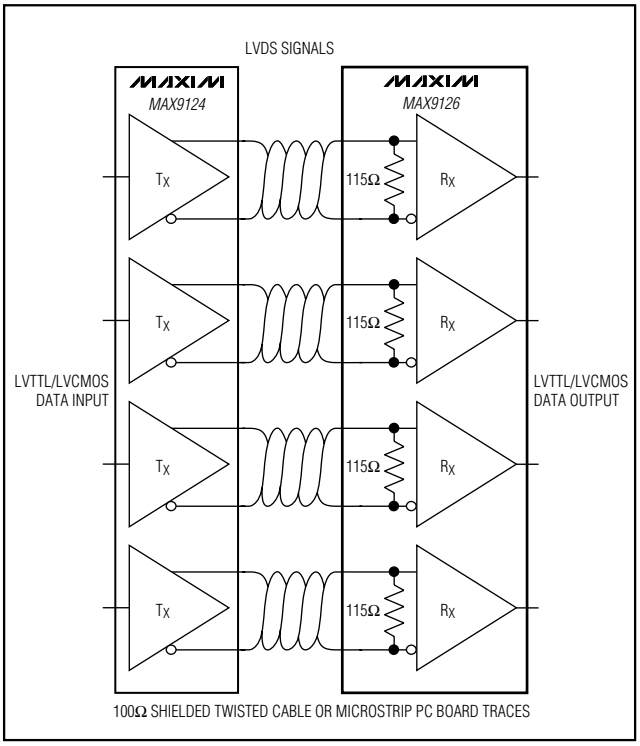
Features

- **Integrated Termination Eliminates Four External Resistors (MAX9126)**
- **Pin Compatible with DS90LV032A**
- **Guaranteed 500Mbps Data Rate**
- **300ps Pulse Skew (max)**
- **Conform to ANSI TIA/EIA-644 LVDS Standard**
- **Single +3.3V Supply**
- **Low 70µA Shutdown Supply Current**
- **Fail-Safe Circuit**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9125EUE	-40°C to +85°C	16 TSSOP
MAX9125ESE	-40°C to +85°C	16 SO
MAX9126EUE	-40°C to +85°C	16 TSSOP
MAX9126ESE	-40°C to +85°C	16 SO

Typical Application Circuit



Quad LVDS Line Receivers with Integrated Termination

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN_+, IN_- to GND .....-0.3V to +4.0V
EN, $\overline{EN}$ to GND .....-0.3V to (V_{CC} + 0.3V)
OUT_ to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
16-Pin SO (derate 8.7mW/°C above +70°C).....696mW
Storage Temperature Range .....-65°C to +150°C
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300°C
ESD Protection (Human Body Model) IN_+, IN_-, OUT_.....±7.5kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.0V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS INPUTS (IN_+, IN_-)							
Differential Input High Threshold	V_{TH}					100	mV
Differential Input Low Threshold	V_{TL}			-100			mV
Input Current (MAX9125)	I_{IN_+}, I_{IN_-}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V,		-20		20	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.0V		-25		25	
Power-Off Input Current (MAX9125)	I_{IN_+}, I_{IN_-}	0.1V ≤ $\|V_{ID}\|$ ≤ 0.6V, V_{CC} = 0		-20		20	µA
		0.6V < $\|V_{ID}\|$ ≤ 1.0V, V_{CC} = 0		-25		25	
Input Resistor 1	R_{IN1}	V_{CC} = +3.6V or 0, Figure 1		35			kΩ
Input Resistor 2	R_{IN2}	V_{CC} = +3.6V or 0, Figure 1		132			kΩ
Differential Input Resistance (MAX9126)	R_{DIFF}	V_{CC} = +3.6V or 0, Figure 1		90	115	132	Ω
LVCMOS/LVTTL OUTPUTS (OUT_)							
Output High Voltage	V_{OH}	I_{OH} = -4.0mA (MAX9125)	Open, undriven short, or undriven 100Ω parallel termination	2.7	3.2		V
			V_{ID} = +100mV	2.7	3.2		
		I_{OH} = -4.0mA (MAX9126)	Open or undriven short	2.7	3.2		
			V_{ID} = +100mV	2.7	3.2		
Output Low Voltage	V_{OL}	I_{OL} = +4.0mA, V_{ID} = -100mV			0.1	0.25	V
Output Short-Circuit Current	I_{OS}	Enabled, V_{ID} = +100mV, $V_{OUT\_}$ = 0 (Note 2)		-15		-120	mA
Output High-Impedance Current	I_{OZ}	Disabled, $V_{OUT\_}$ = 0 or V_{CC}		-10		+10	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.0V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS (EN, $\overline{EN}$)						
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		0		0.8	V
Input Current	I_{IN}	V_{IN} = V_{CC} or 0	-15		15	µA
SUPPLY						
Supply Current	I_{CC}	Enabled, inputs open		9	15	mA
Disabled Supply Current	I_{CCZ}	Disabled, inputs open		70	500	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C_L = 10pF, differential input voltage $|V_{ID}|$ = 0.2V to 1.0V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, V_{CM} = 1.2V, $|V_{ID}|$ = 0.2V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Propagation Delay High to Low	t_{PHLD}	Figures 2 and 3	1.8	2.4	3.3	ns
Differential Propagation Delay Low to High	t_{PLHD}	Figures 2 and 3	1.8	2.3	3.3	ns
Differential Pulse Skew [t_{PHLD} - t_{PLHD}] (Note 5)	t_{SKD1}	Figures 2 and 3		100	300	ps
Differential Channel-to-Channel Skew (Note 6)	t_{SKD2}	Figures 2 and 3			400	ps
Differential Part-to-Part Skew (Note 7)	t_{SKD3}	Figures 2 and 3			0.8	ns
Differential Part-to-Part Skew (Note 8)	t_{SKD4}	Figures 2 and 3			1.5	ns
Rise Time	t_{TLH}	Figures 2 and 3		0.34	1.2	ns
Fall Time	t_{THL}	Figures 2 and 3		0.32	1.2	ns
Disable Time High to Z	t_{PHZ}	R_L = 2kΩ, Figures 4 and 5			12	ns
Disable Time Low to Z	t_{PLZ}	R_L = 2kΩ, Figures 4 and 5			12	ns
Enable Time Z to High	t_{PZH}	R_L = 2kΩ, Figures 4 and 5			17	ns
Enable Time Z to Low	t_{PZL}	R_L = 2kΩ, Figures 4 and 5			17	ns
Maximum Operating Frequency (Note 9)	f_{MAX}	All channels switching	250	300		MHz

Quad LVDS Line Receivers with Integrated Termination

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, CL = 10pF, differential input voltage $|V_{ID}|$ = 0.2V to 1.0V, common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$, input rise and fall time = 1ns (20% to 80%), input frequency = 100MHz, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, V_{CM} = 1.2V, $|V_{ID}|$ = 0.2V, T_A = +25°C, unless otherwise noted.) (Notes 3, 4)

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} , V_{TL}, and V_{ID}.

Note 2: Short only one output at a time. Do not exceed the absolute maximum junction temperature specification.

Note 3: AC parameters are guaranteed by design and characterization.

Note 4: C_L includes scope probe and test jig capacitance.

Note 5: t_{SKD1} is the magnitude difference of differential propagation delays in a channel; $t_{SKD1} = |t_{PHLD} - t_{PLHD}|$.

Note 6: t_{SKD2} is the magnitude difference of the t_{PLHD} or t_{PHLD} of one channel and the t_{PLHD} or t_{PHLD} of any other channel on the same part.

Note 7: t_{SKD3} is the magnitude difference of any differential propagation delays between parts operating over rated conditions at the same V_{CC} and within 5°C of each other.

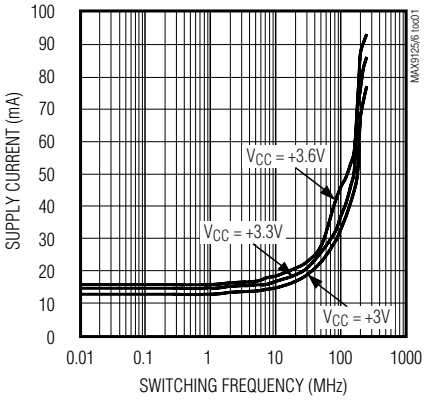
Note 8: t_{SKD4} is the magnitude difference of any differential propagation delays between parts operating over rated conditions.

Note 9: f_{MAX} generator output conditions: $t_R = t_F$ < 1ns (0% to 100%), 50% duty cycle, V_{OL} = 1.1V, V_{OH} = 1.3V. Receiver output criteria: 60% to 40% duty cycle, V_{OL} = 0.4V (max), V_{OH} = 2.7V (min), load = 10pF.

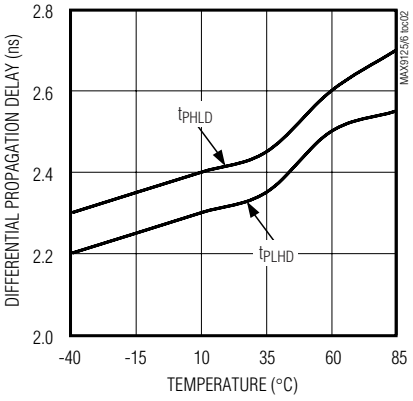
Typical Operating Characteristics

(V_{CC} = +3.3V, $|V_{ID}|$ = 200mV, V_{CM} = +1.2V, C_L = 10pF, frequency = 10MHz, T_A = +25°C, unless otherwise noted.) (Figures 2 and 3)

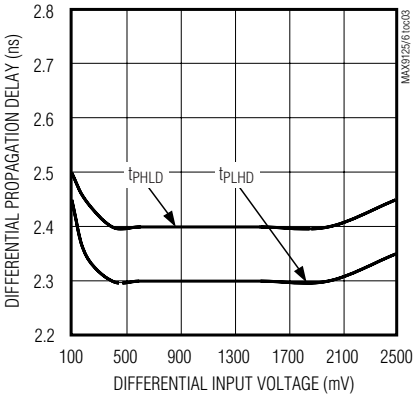
SUPPLY CURRENT vs. SWITCHING FREQUENCY, FOUR CHANNELS SWITCHING



DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



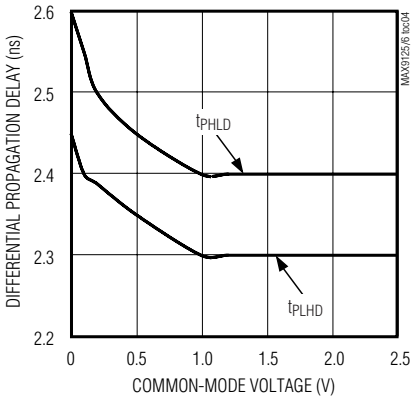
DIFFERENTIAL PROPAGATION DELAY vs. DIFFERENTIAL INPUT VOLTAGE



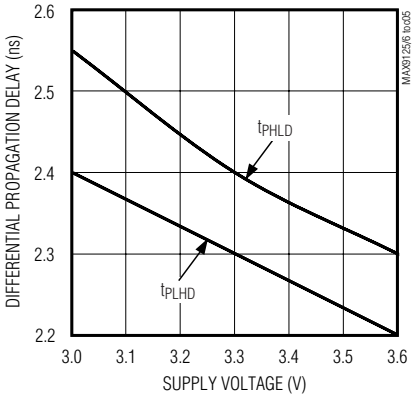
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, $|V_{ID}|$ = 200mV, V_{CM} = +1.2V, C_L = 10pF, frequency = 10MHz, T_A = +25°C, unless otherwise noted (Figures 2 and 3).)

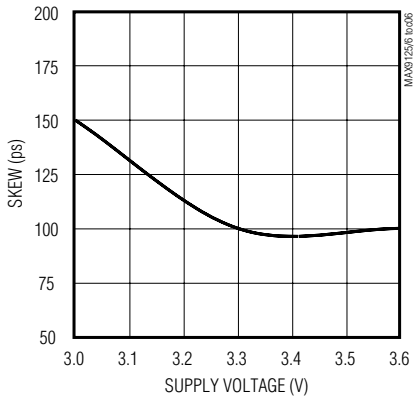
DIFFERENTIAL PROPAGATION DELAY vs. COMMON-MODE VOLTAGE



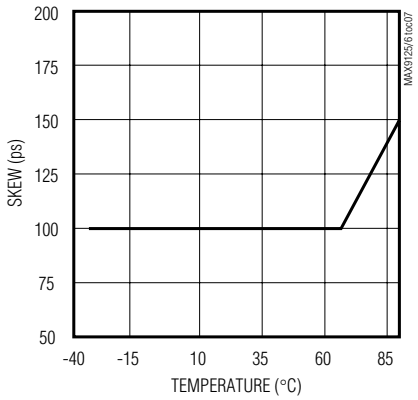
DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



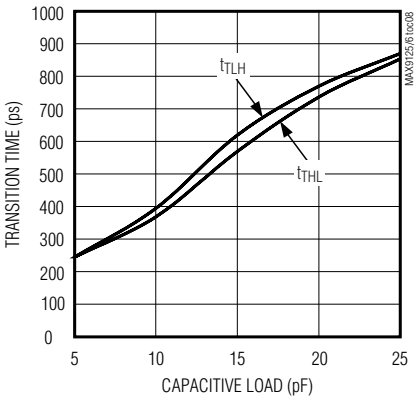
PULSE SKEW vs. SUPPLY VOLTAGE



PULSE SKEW vs. TEMPERATURE



TRANSITION TIME vs. CAPACITIVE LOAD



Pin Description

PIN	NAME	FUNCTION
1, 7, 9, 15	IN_-	Inverting Differential Receiver Inputs
2, 6, 10, 14	IN_+	Noninverting Differential Receiver Inputs
3, 5, 11, 13	OUT_	LVCMOS/LVTTL Receiver Outputs
4, 12	EN, $\overline{EN}$	Receiver Enable Inputs. When EN = low and $\overline{EN}$ = high, the outputs are disabled and in high impedance. For other combinations of EN and $\overline{EN}$, the outputs are active.
8	GND	Ground
16	V_{CC}	Power Supply Input. Bypass V_{CC} to GND with 0.1µF and 0.001µF ceramic capacitors.

Quad LVDS Line Receivers with Integrated Termination

Table 1. Input/Output Function Table

ENABLES		INPUTS		OUTPUT
EN	$\overline{EN}$	(IN_+) - (IN_-)		OUT_
L	H	X		Z
All other combinations of ENABLE inputs		V_{ID} ≥ +100mV		H
		V_{ID} ≤ -100mV		L
		MAX9125	Open, undriven short, or undriven 100Ω parallel termination	H
		MAX9126	Open or undriven short	

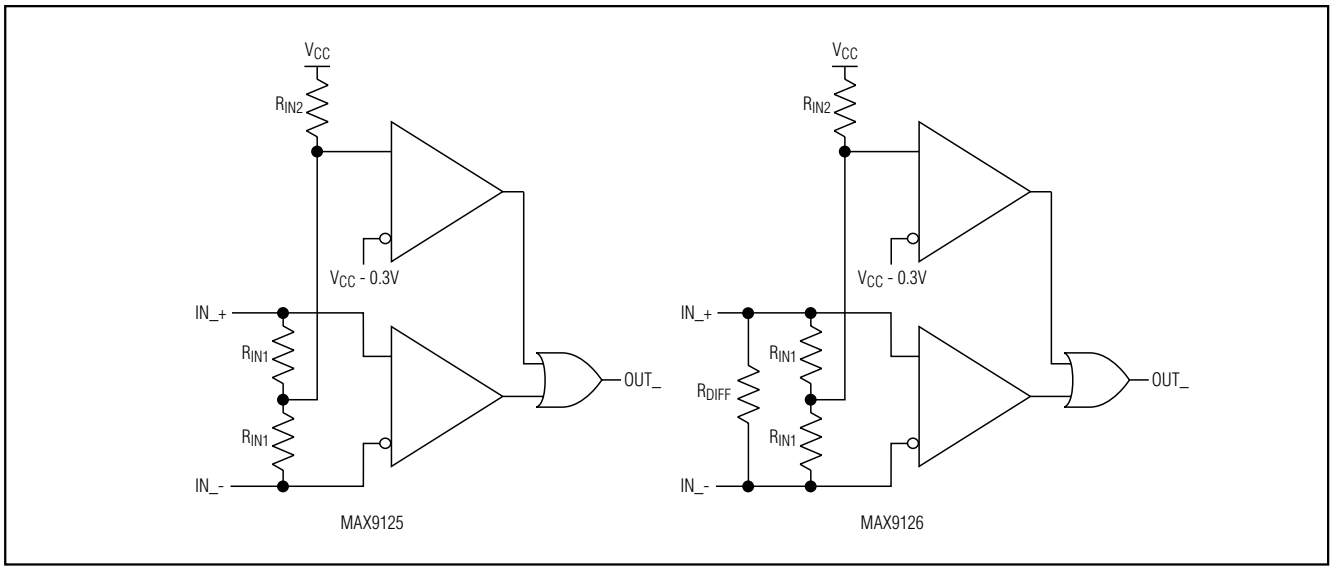


Figure 1. Inputs with Internal Fail-Safe Circuitry

Detailed Description

The LVDS interface standard is a signaling method intended for point-to-point communication over a controlled-impedance medium as defined by the ANSI TIA/EIA-644 and IEEE 1596.3 standards. The LVDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise.

The MAX9125/MAX9126 are 500Mbps, four-channel LVDS receivers intended for high-speed, point-to-point, low-power applications. Each channel accepts an LVDS input and translates it to an LVTTL/LVCMOS output. The receiver is capable of detecting differential signals as low as 100mV and as high as 1V within an input voltage range of 0 to 2.4V. The 250mV to 400mV differential output of an LVDS driver is nominally centered around a +1.2V offset. This offset, coupled with the receiver's 0 to 2.4V input voltage range, allows an approximate ±1V shift in the signal (as seen by the receiver). This allows for a difference in ground references of the transmitter and the receiver, the common-mode effects of coupled noise, or both. The LVDS standards specify an input voltage range of 0 to 2.4V referenced to receiver ground.

The MAX9126 has an integrated termination resistor internally connected across each receiver input. The internal termination saves board space, eases layout, and reduces "stub length" compared to an external termination resistor. In other words, the transmission line is terminated on the IC.

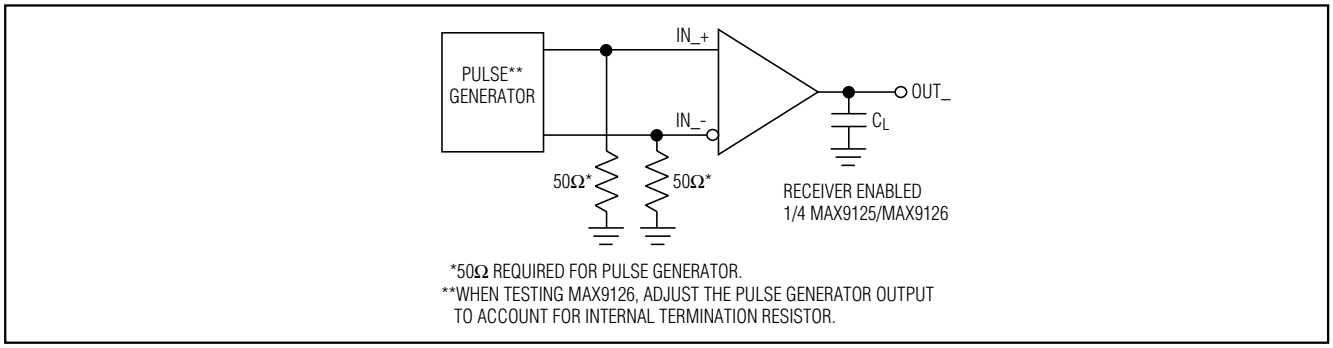


Figure 2. Transition Time and Propagation Delay Test Circuit

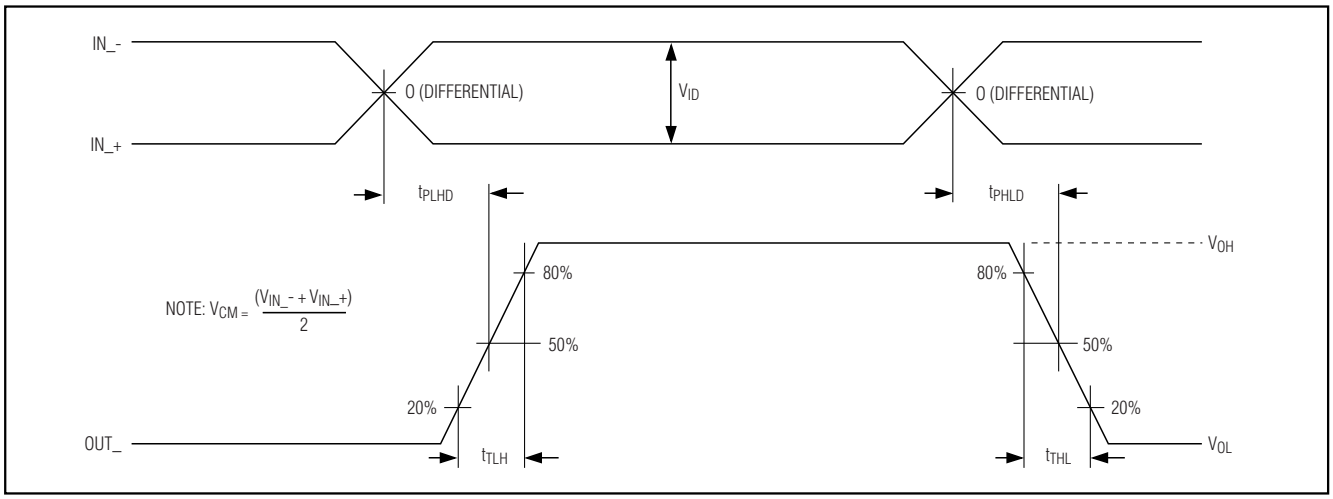


Figure 3. Transition Time and Propagation Delay Timing Diagram

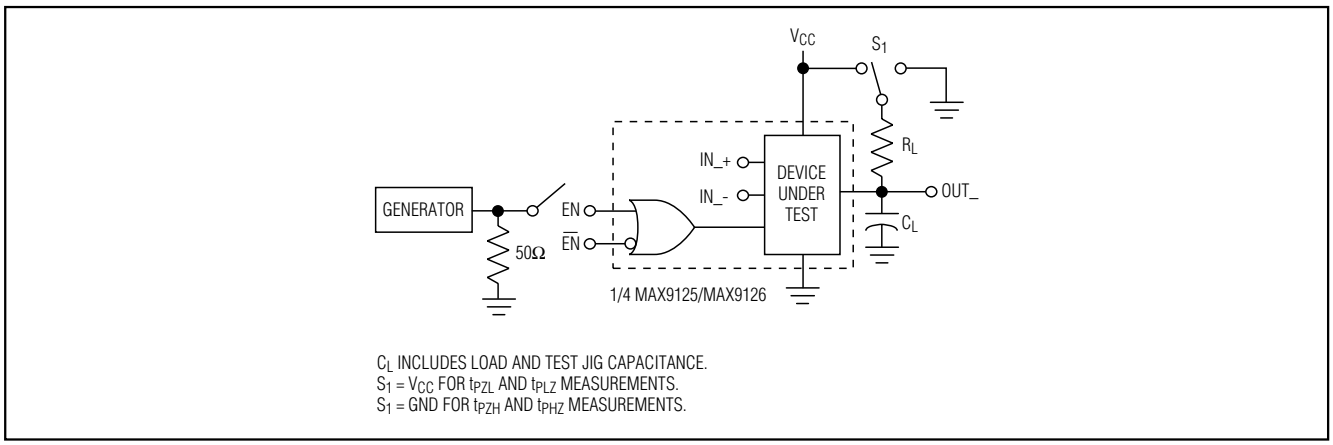


Figure 4. High-Z Delay Test Circuit

Quad LVDS Line Receivers with Integrated Termination

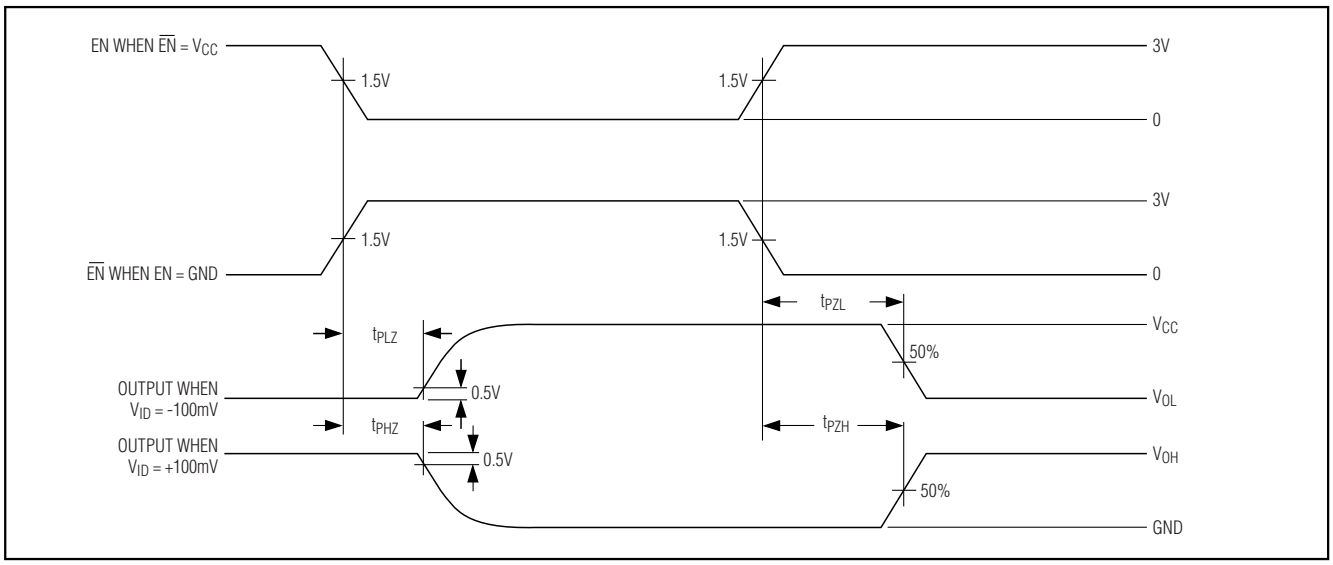


Figure 5. High-Z Delay Waveforms

Fail-Safe

The fail-safe feature of the MAX9125/MAX9126 sets the output high when:

- Inputs are open.
- Inputs are undriven and shorted.
- Inputs are undriven and terminated.

A fail-safe circuit is important because under these conditions, noise at the inputs may switch the receiver and it may appear to the system that data is being received. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when the LVDS driver outputs are high impedance. A short condition can occur because of a cable failure.

The fail-safe input network (Figure 1) samples the input common-mode voltage and compares it to V_{CC} - 0.3V (nominal). When the input is driven to levels specified in the LVDS standards, the input common-mode voltage is less than V_{CC} - 0.3V and the fail-safe circuit is not activated. If the inputs are open or if the inputs are undriven and shorted or undriven and parallel terminated, there is no input current. In this case, a pullup resistor in the fail-safe circuit pulls both inputs above V_{CC} - 0.3V, activating the fail-safe circuit and forcing the output high.

Applications Information

Power-Supply Bypassing

Bypass the V_{CC} pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel, as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Differential Traces

Input trace characteristics affect the performance of the MAX9125/MAX9126. Use controlled-impedance PC board traces to match the cable characteristic impedance. The termination resistor is also matched to this characteristic impedance.

Eliminate reflections and ensure that noise couples as common mode by running the differential traces close together. Reduce skew by matching the electrical length of the traces. Excessive skew can result in a degradation of magnetic field cancellation.

Each channel's differential signals should be routed close to each other to cancel their external magnetic field. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Avoid 90° turns and vias to further prevent impedance discontinuities.

Cables and Connectors

Transmission media typically have a controlled differential impedance of 100Ω. Use cables and connectors

that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9126 has an integrated termination resistor connected across the inputs of each receiver. The value of the integrated resistor is specified in the DC characteristics.

The MAX9125 requires an external termination resistor. The termination resistor should match the differential impedance of the transmission line. Termination resistance values range between 90Ω and 132Ω, depending on the characteristic impedance of the transmission medium.

When using the MAX9125, minimize the distance between the input termination resistors and the MAX9125 receiver inputs. Use 1% surface-mount resistors.

Board Layout

Keep the LVDS and any other digital signals separated from each other to reduce crosstalk.

For LVDS applications, use a four-layer PC board that provides separate power, ground, LVDS signals, and output signals. Isolate the input LVDS signals from the output LVCMOS/LVTTL signals to prevent coupling. Separate the input LVDS signal plane from the LVCMOS/LVTTL output signal plane with the power and ground planes for best results.

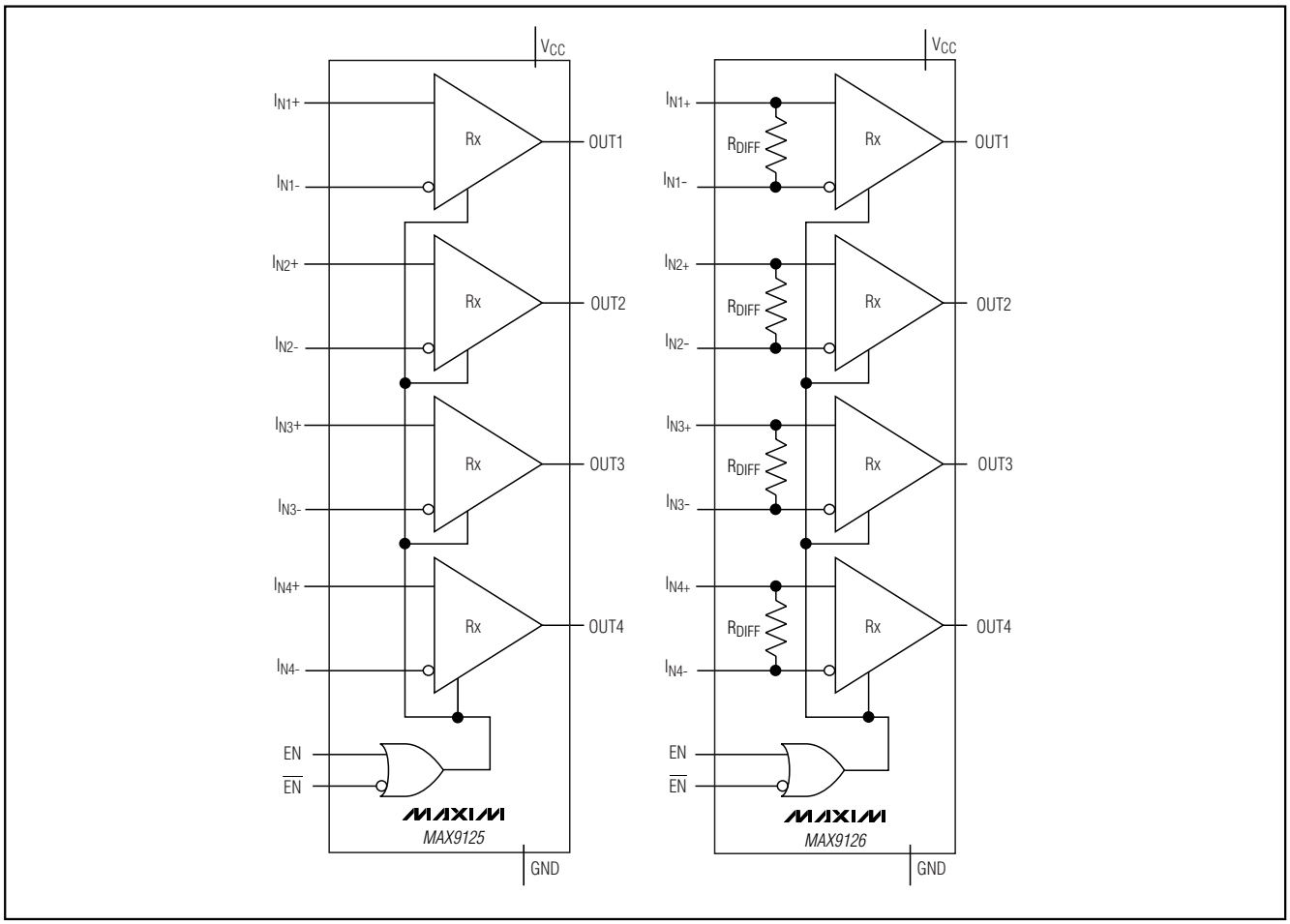
Chip Information

TRANSISTOR COUNT: 940

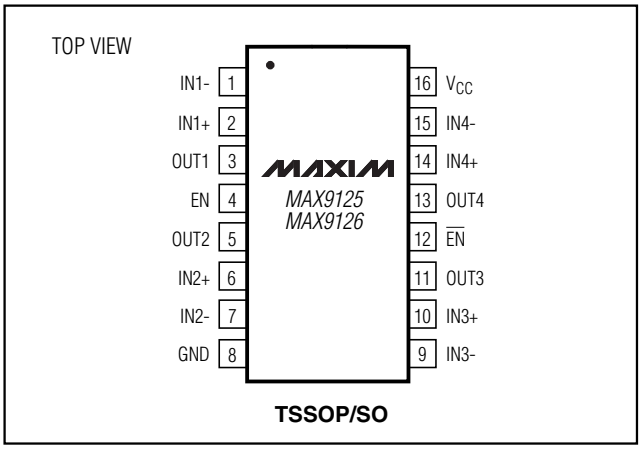
PROCESS: CMOS

Quad LVDS Line Receivers with Integrated Termination

Functional Diagram

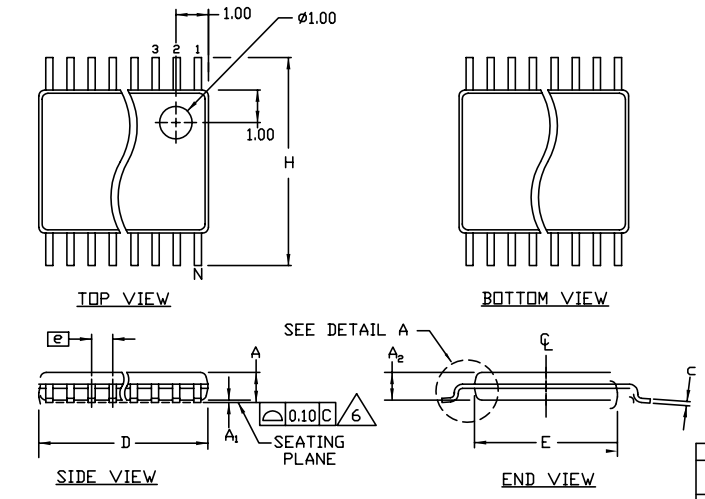


Pin Configuration



Package Information

TSSOP,NO PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM

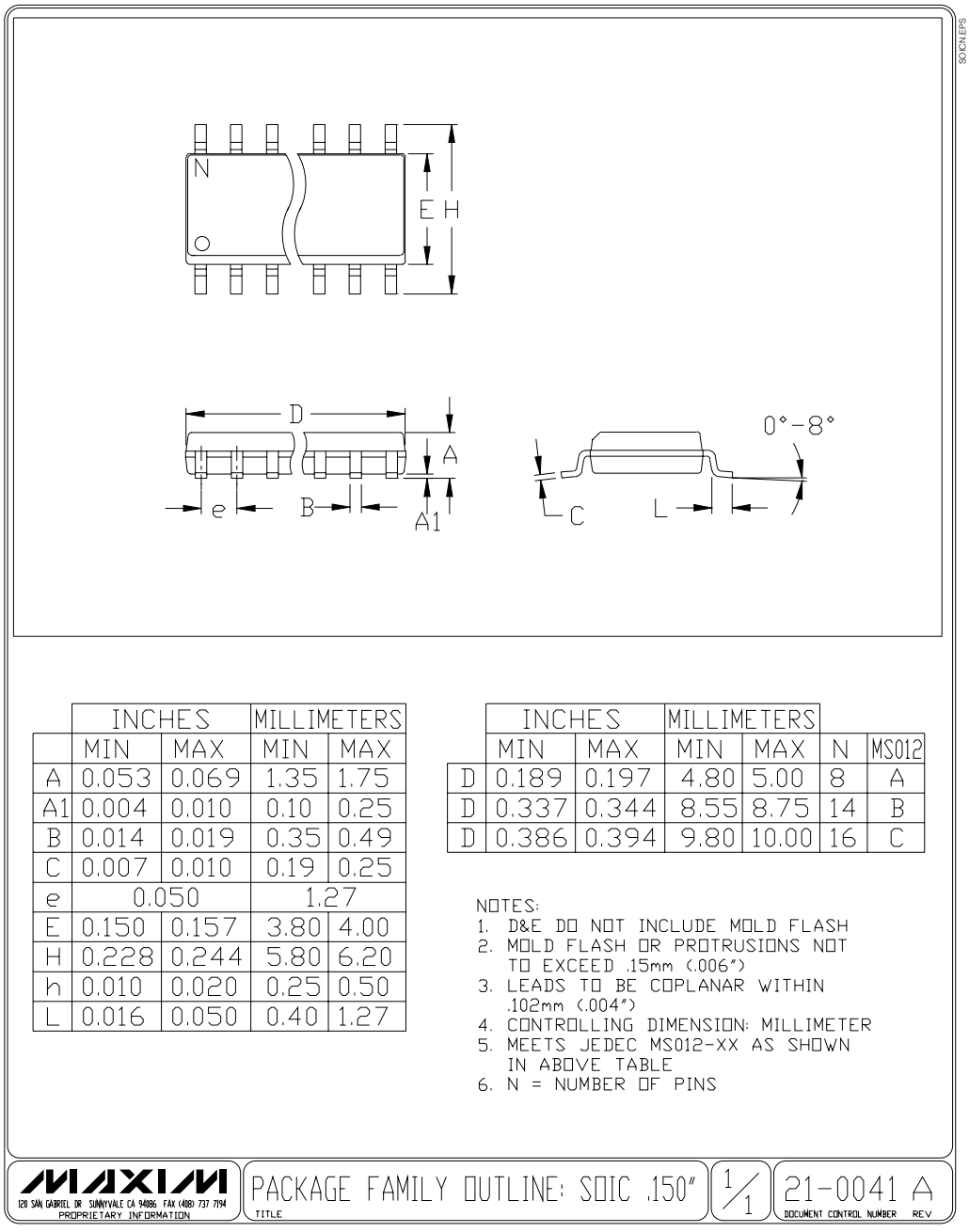
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	E	1/1

Quad LVDS Line Receivers with Integrated Termination

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" (TITLE) | 1/1 | 21-0041 A (DOCUMENT CONTROL NUMBER REV)