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19-2827; Rev 1; 4/04

MAXIM

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

General Description

The MAX9174/MAX9175 are 670MHz, low-jitter, low-skew 1:2 splitters ideal for protection switching, loopback, and clock and signal distribution. The devices feature ultra-low 1.0ps(RMS) random jitter (max) that ensures reliable operation in high-speed links that are highly sensitive to timing errors.

The MAX9174 has a fail-safe LVDS input and LVDS outputs. The MAX9175 has an anything differential input (CML/LVDS/LVPECL) and LVDS outputs. The outputs can be put into high impedance using the power-down inputs. The MAX9174 features a fail-safe circuit that drives the outputs high when the input is open, undriven and shorted, or undriven and terminated. The MAX9175 has a bias circuit that forces the outputs high when the input is open. The power-down inputs are compatible with standard LVTTL/LVCMOS logic. The power-down inputs tolerate undershoot of -1V and overshoot of V_{CC} + 1V. The MAX9174/MAX9175 are available in 10-pin µMAX and 10-lead thin QFN with exposed pad packages, and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

Applications

Protection Switching

Loopback

Clock Distribution

Functional Diagram and Pin Configurations appear at end of data sheet.

Features

- **1.0ps(RMS) Jitter (max) at 670MHz**
- **80ps(P-P) Jitter (max) at 800Mbps Data Rate**
- **+3.3V Supply**
- **LVDS Fail-Safe Inputs (MAX9174)**
- **Anything Input (MAX9175) Accepts Differential CML/LVDS/LVPECL**
- **Power-Down Inputs Tolerate -1.0V and V_{CC} + 1.0V**
- **Low-Power CMOS Design**
- **10-Lead µMAX and Thin QFN Packages**
- **-40°C to +85°C Operating Temperature Range**
- **Conform to ANSI TIA/EIA-644 LVDS Standard**
- **IEC 61000-4-2 Level 4 ESD Rating**

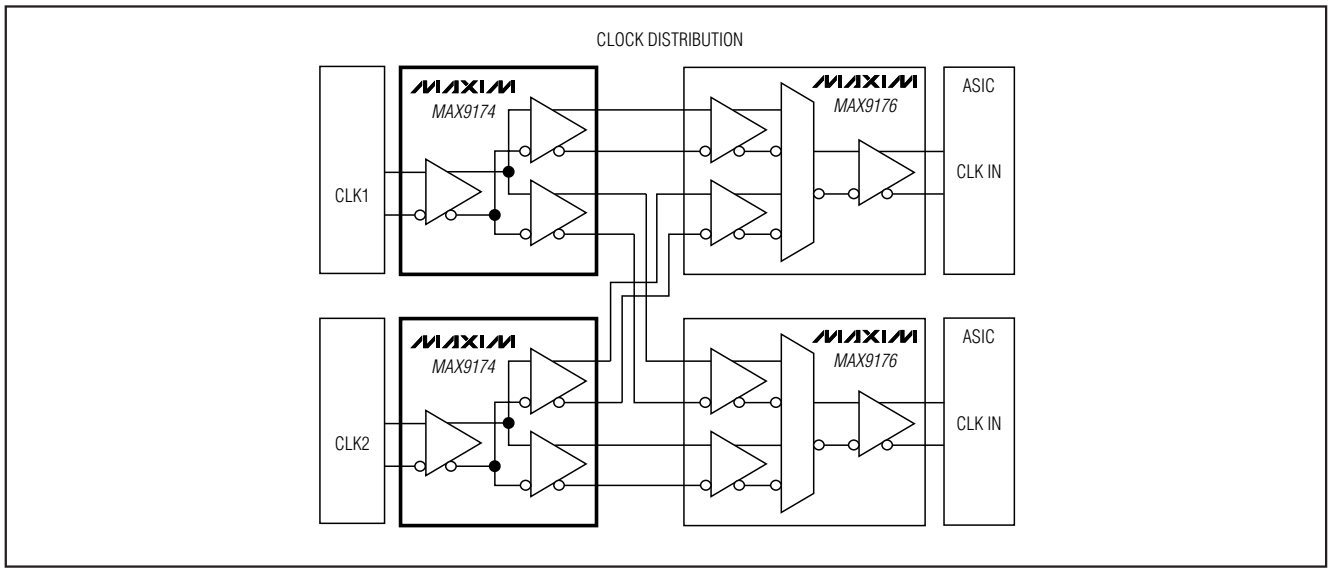
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9174EUB	-40°C to +85°C	10 µMAX
MAX9174ETB*	-40°C to +85°C	10 Thin QFN-EP**
MAX9175EUB	-40°C to +85°C	10 µMAX
MAX9175ETB*	-40°C to +85°C	10 Thin QFN-EP**

**Future product—contact factory for availability.*

***EP = Exposed paddle.*

Typical Application Circuit



670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.0V
IN+, IN- to GND .....-0.3V to +4.0V
OUT_+, OUT_- to GND .....-0.3V to +4.0V
$\overline{PD0}$, $\overline{PD1}$ to GND .....-1.4V to (V_{CC} + 1.4V)
Single-Ended and Differential Output
Short-Circuit Duration (OUT_+, OUT_-) .....Continuous
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
10-Lead QFN (derate 24.4mW/°C above +70°C) 1951mW
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
IN+, IN-, OUT_+, OUT_- .....±2kV
Other Pins (V_{CC}, $\overline{PD0}$, $\overline{PD1}$) 2kV
IEC 61000-4-2 Level 4 (R_D = 330Ω, C_S = 150pF)
Contact Discharge IN+, IN-, OUT_+, OUT_- .....±8kV
Air-Gap Discharge IN+, IN-, OUT_+, OUT_- .....±15kV
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PD\_}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, MAX9174 input common-mode voltage V_{CM} = $|V_{ID}$ /2| to (2.4V - $|V_{ID}$ /2|), MAX9175 input common-mode voltage V_{CM} = $|V_{ID}$ /2| to (V_{CC} - | V_{ID} /2|), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.25V, T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUT (IN+, IN-)							
Differential Input High Threshold	V_{TH}					+50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Current	I_{IN+}, I_{IN-}	Figure 1		-20		+20	µA
Power-Off Input Current	I_{IN+}, I_{IN-}	MAX9174	V_{CC} = 0V or open, Figure 1	-20		+20	µA
		MAX9175	V_{IN+} = 3.6V or 0V, V_{IN-} = 3.6V or 0V, V_{CC} = 0V or open, Figure 1				
Fail-Safe Input Resistors (MAX9174)	R_{IN1}	V_{CC} = 3.6V, 0V or open, Figure 1		60		108	kΩ
	R_{IN2}			200		394	
Input Resistors (MAX9175)	R_{IN3}	V_{CC} = 3.6V, 0V or open, Figure 1		212		450	kΩ
Input Capacitance	C_{IN}	IN+ or IN- to GND (Note 4)				4.5	pF
LVTTL/LVCMOS INPUTS ($\overline{PD0}$, $\overline{PD1}$)							
Input High Voltage	V_{IH}			2.0		V_{CC} + 1	V
Input Low Voltage	V_{IL}			-1.0		+0.8	V
Input Current	I_{IN}	-1.0V ≤ $\overline{PD\_}$ ≤ 0V		-1.5			mA
		0V ≤ $\overline{PD\_}$ ≤ V_{CC}		-20		+20	µA
		V_{CC} ≤ $\overline{PD\_}$ ≤ V_{CC} + 1.0V				+1.5	mA
LVDS OUTPUTS (OUT_+, OUT_-)							
Differential Output Voltage	V_{OD}	Figure 2		250	393	475	mV
Change in Differential Output Voltage Between Logic States	ΔV_{OD}	Figure 2			1.0	15	mV
Offset Voltage	V_{OS}	Figure 3		1.125	1.29	1.375	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω ±1%, $\overline{PD\_}$ = high, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, MAX9174 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to (2.4V - $|V_{ID}/2|$), MAX9175 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to (V_{CC} - $|V_{ID}/2|$), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.25V, T_A = +25°C.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Change in Offset Voltage Between Logic States	ΔV_{OS}	Figure 3			1.0	15	mV
Fail-Safe Differential Output Voltage (MAX9174)	V_{OD}	Figure 2		250	393	475	mV
Differential Output Resistance	R_{DIFF}	V_{CC} = 3.6V or 0V		86	119	160	Ω
Power-Down Single-Ended Output Current	I_{PD}	$\overline{PD\_}$ = low	V_{OUT_+} = open, V_{OUT_-} = 3.6V or 0V	-1.0	±0.03	+1.0	µA
			V_{OUT_-} = open, V_{OUT_+} = 3.6V or 0V				
Power-Off Single-Ended Output Current	I_{OFF}	$\overline{PD0}$, $\overline{PD1}$ = low, V_{CC} = 0V or open	V_{OUT_+} = open, V_{OUT_-} = 3.6V or 0V	-1.0	±0.03	+1.0	µA
			V_{OUT_-} = open, V_{OUT_+} = 3.6V or 0V				
Output Short-Circuit Current	I_{OS}	V_{ID} = +50mV or -50mV, V_{OUT_+} = 0V or V_{CC}		-15		+15	mA
		V_{ID} = +50mV or -50mV, V_{OUT_-} = 0V or V_{CC}					
Differential Output Short-Circuit Current Magnitude	$\lvert I_{OSD} \rvert$	V_{ID} = +50mV or -50mV, V_{OD} = 0V (Note 4)				15	mA
Supply Current	I_{CC}	$\overline{PD0}$ = V_{CC}, $\overline{PD1}$ = 0V or $\overline{PD0}$ = 0V, $\overline{PD1}$ = V_{CC}			17	26	mA
		$\overline{PD0}$ = Vcc, $\overline{PD1}$ = Vcc			25	35	
Power-Down Supply Current	I_{CCPD}	$\overline{PD1}$, $\overline{PD0}$ = 0V			0.5	20	µA
Output Capacitance	C_O	OUT_+ or OUT_- to GND (Note 4)				5.2	pF

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, R_L = 100Ω±1%, C_L = 5pF, differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, MAX9174 input common-mode voltage, V_{CM} = $|V_{ID}/2|$ to (2.4V - $|V_{ID}/2|$), MAX9175 input common-mode voltage V_{CM} = $|V_{ID}/2|$ to (V_{CC} - $|V_{ID}/2|$), $\overline{PD\_}$ = high, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = +1.25V, T_A = +25°C.) (Notes 5, 6, 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-to-Low Propagation Delay	t_{PHL}	Figures 4, 5	1.33	2.38	3.23	ns
Low-to-High Propagation Delay	t_{PLH}	Figures 4, 5	1.33	2.39	3.23	ns
Added Deterministic Jitter	t_{DJ}	Figures 4, 5 (Note 8)			80	$ps_{(P-P)}$
Added Random Jitter	t_{RJ}	Figures 4, 5			1.0	$ps_{(RMS)}$
Pulse Skew $\lvert t_{PLH} - t_{PHL} \rvert$	t_{SKP}	Figures 4, 5		10	141	ps
Output-to-Output Skew	t_{SKOO}	Figure 6		14	45	ps
Part-to-Part Skew	t_{SKPP1}	Figures 4, 5 (Note 9)		0.4	1.3	ns
	t_{SKPP2}	Figures 4, 5 (Note 10)			1.9	
Rise Time	t_R	Figures 4, 5	110	257	365	ps
Fall Time	t_F	Figures 4, 5	110	252	365	ps
Power-Down Time	t_{PD}	Figures 7, 8		10	13	ns
Power-Up Time	t_{PU}	$\overline{PD0}$, $\overline{PD1}$ = L → H, Figures 7, 8		18	35	µs
		$\overline{PD0}$ = H, $\overline{PD1}$ = L → H, Figures 7, 8		92	103	ns
		$\overline{PD1}$ = H, $\overline{PD0}$ L → H, Figures 7, 8		92	103	
Maximum Data Rate	D_{RMAX}	Figures 4, 5, $\lvert V_{OD} \rvert \geq$ 250mV (Note 11)	800			Mbps
Maximum Switching Frequency	f_{MAX}	Figures 4, 5, $\lvert V_{OD} \rvert \geq$ 250mV (Note 11)	670			MHz
Switching Supply Current	I_{CCSW}	f_{IN} = 670MHz		55	65	mA
		f_{IN} = 155MHz		35	44	
PRBS Supply Current	I_{CCPR}	D_R = 800Mbps, 2^{23} - 1 PRBS input		37	46	mA

Note 1: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH}, V_{TL}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 2: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are 100% tested at T_A = +25°C.

Note 3: Tolerance on all external resistors (including figures) is ±1%.

Note 4: Guaranteed by design.

Note 5: AC parameters are guaranteed by design and characterization and are not production tested. Limits are set at ±6 sigma.

Note 6: C_L includes scope probe and test jig capacitance.

Note 7: Pulse-generator output for differential inputs IN+, IN- (unless otherwise noted): f = 670MHz, 50% duty cycle, R_O = 50Ω, t_R = 700ps, and t_F = 700ps (0% to 100%). Pulse-generator output for single-ended inputs $\overline{PD0}$, $\overline{PD1}$: t_R = t_F = 1.5ns (0.2V_{CC} to 0.8V_{CC}), 50% duty cycle, V_{OH} = V_{CC} + 1.0V settling to V_{CC}, V_{OL} = -1.0V settling to zero, f = 10kHz.

Note 8: Pulse-generator output for t_{DJ}: $|V_{OD}|$ = 0.15V, V_{OS} = 1.25V, data rate 800Mbps, 2^{23} - 1 PRBS, R_O = 50Ω, t_R = 700ps, and t_F = 700ps (0% to 100%).

Note 9: t_{SKPP1} is the magnitude of the difference of any differential propagation delays between devices operating under identical conditions.

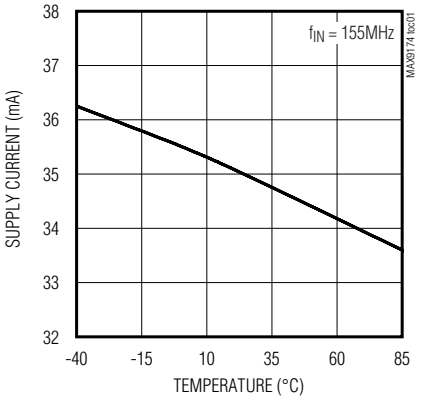
Note 10: t_{SKPP2} is the magnitude of the difference of any differential propagation delays between devices operating over rated conditions.

Note 11: Meets all AC specifications.

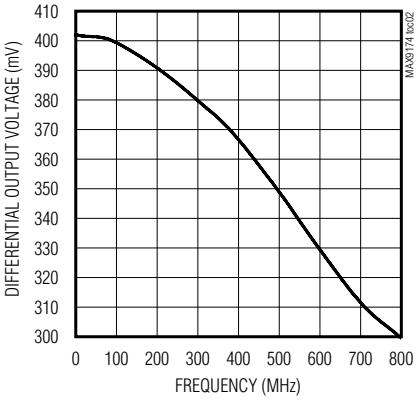
Typical Operating Characteristics

((MAX9174) V_{CC} = +3.3V, $|V_{ID}|$ = 0.15V, V_{CM} = 1.25V, T_A = +25°C, R_L = 100Ω ±1%, C_L = 5pf, $\overline{PD\_}$ = V_{CC}, unless otherwise noted.)

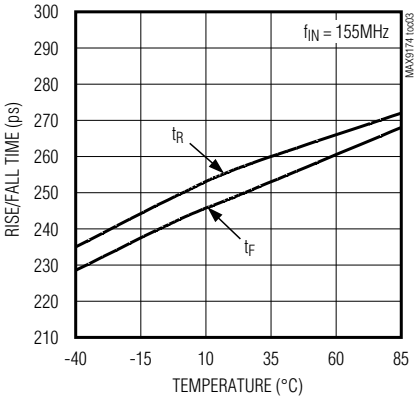
SUPPLY CURRENT vs. TEMPERATURE



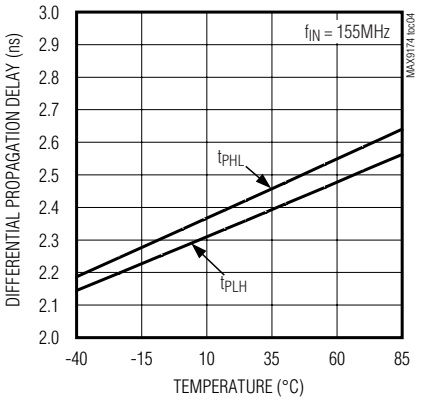
DIFFERENTIAL OUTPUT VOLTAGE vs. FREQUENCY



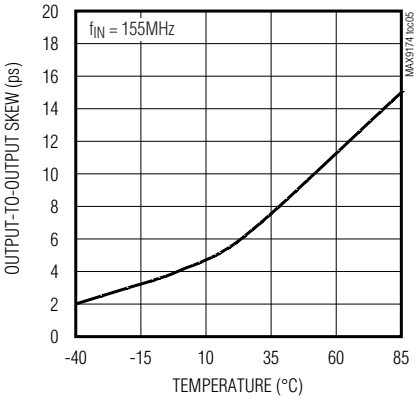
OUTPUT RISE/FALL TIME vs. TEMPERATURE



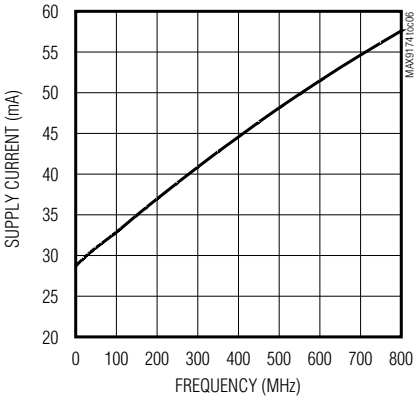
DIFFERENTIAL PROPAGATION DELAY vs. TEMPERATURE



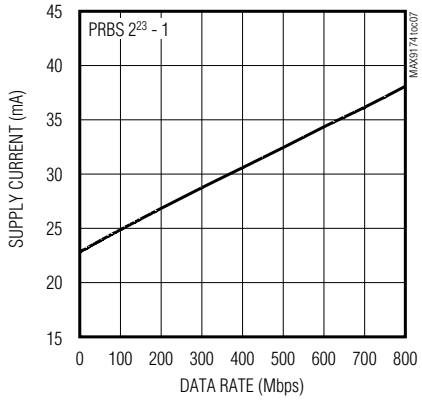
OUTPUT-TO-OUTPUT SKEW vs. TEMPERATURE



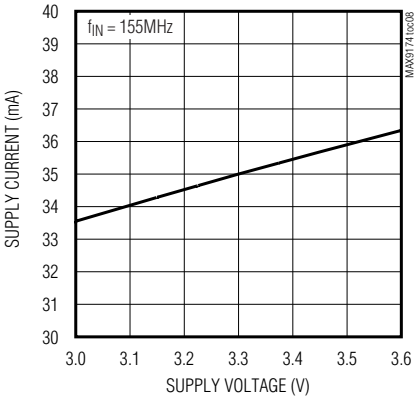
SUPPLY CURRENT vs. FREQUENCY



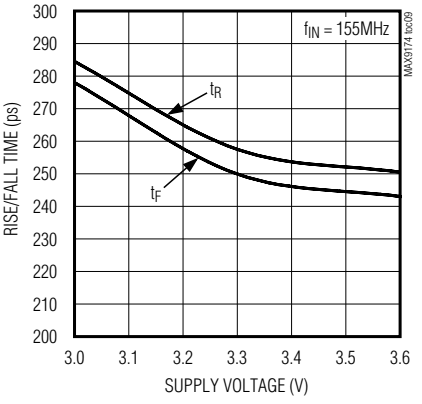
SUPPLY CURRENT vs. DATA RATE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT RISE/FALL TIME vs. SUPPLY VOLTAGE

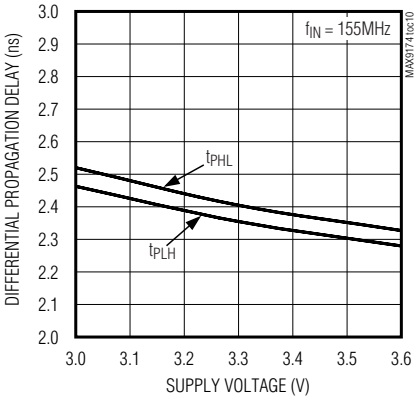


670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

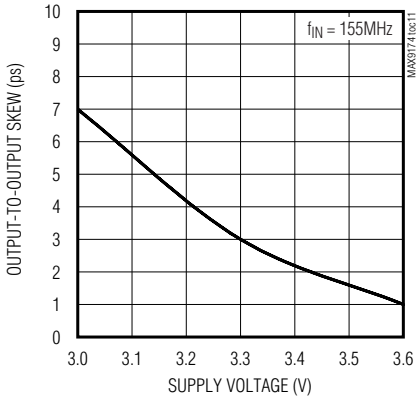
Typical Operating Characteristics (continued)

((MAX9174) V_{CC} = +3.3V, $|V_{ID}|$ = 0.15V, V_{CM} = 1.25V, T_A = +25°C, R_L = 100Ω ±1%, C_L = 5pf, $\overline{PD\_}$ = V_{CC}, unless otherwise noted.)

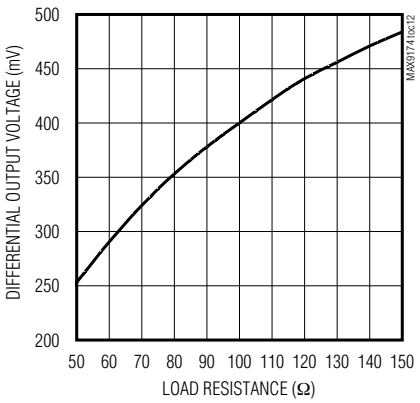
DIFFERENTIAL PROPAGATION DELAY vs. SUPPLY VOLTAGE



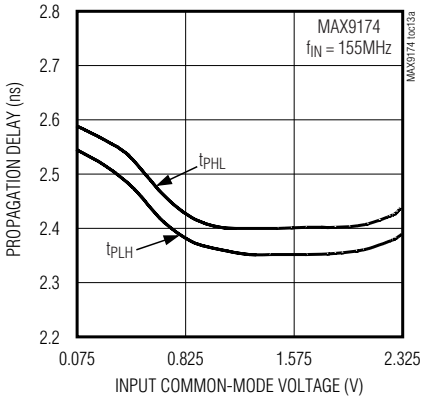
OUTPUT-TO-OUTPUT SKEW vs. SUPPLY VOLTAGE



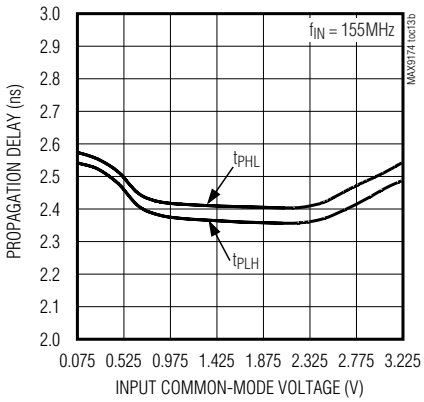
DIFFERENTIAL OUTPUT VOLTAGE vs. LOAD RESISTANCE



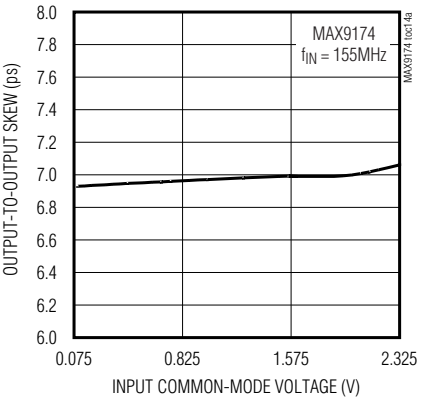
PROPAGATION DELAY vs. INPUT COMMON-MODE VOLTAGE



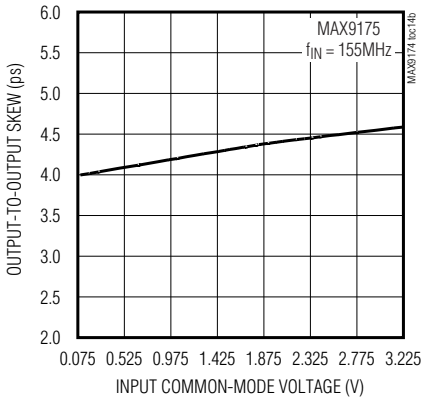
PROPAGATION DELAY vs. INPUT COMMON-MODE VOLTAGE



OUTPUT-TO-OUTPUT SKEW vs. INPUT COMMON-MODE VOLTAGE



OUTPUT-TO-OUTPUT SKEW vs. INPUT COMMON-MODE VOLTAGE



670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

Pin Description

PIN		NAME	FUNCTION
µMAX	QFN		
1	1	IN+	Noninverting Differential Input
2	2	IN-	Inverting Differential Input
3	3	GND	Ground
4	4	$\overline{PD1}$	LVTTL/LVCMOS Input. OUT1+, OUT1- are high impedance to ground when $\overline{PD1}$ is low. Internal pulldown resistor to GND.
5	5	$\overline{PD0}$	LVTTL/LVCMOS Input. OUT0+, OUT0- are high impedance to ground when $\overline{PD0}$ is low. Internal pulldown resistor to GND.
6	6	OUT0-	Inverting LVDS Output 0
7	7	OUT0+	Noninverting LVDS Output 0
8	8	V_{CC}	Power Supply
9	9	OUT1-	Inverting LVDS Output 1
10	10	OUT1+	Noninverting LVDS Output 1
—	EP	Exposed Pad	Exposed Pad. Solder to ground.

Detailed Description

The MAX9174/MAX9175 are 670MHz, low-jitter, low-skew 1:2 splitters ideal for protection switching, loopback, and clock and signal distribution. The devices feature ultra-low 80ps$_{P-P}$ deterministic jitter (max) that ensures reliable operation in high-speed links that are highly sensitive to timing error.

The MAX9174 has a fail-safe LVDS input and LVDS outputs. The MAX9175 has an anything differential input (CML/LVDS/LVPECL) and LVDS outputs. The outputs can be put into high impedance using the power-down inputs. The MAX9174 features a fail-safe circuit that drives the outputs high when the input is open, undriven and shorted, or undriven and terminated. The MAX9175 has a bias circuit that forces the outputs high when the input is open. The power-down inputs are compatible with standard LVTTL/LVCMOS logic.

The power-down inputs tolerate undershoot of -1V and overshoot of VCC + 1V. The MAX9174/MAX9175 are available in 10-pin µMAX and 10-lead thin QFN packages, and operate from a single +3.3V supply over the -40°C to +85°C temperature range.

Current-Mode LVDS Outputs

The LVDS outputs use a current-steering configuration. This approach results in less ground bounce and less output ringing, enhancing noise margin and system speed performance.

A differential output voltage is produced by steering current through the parallel combination of the integrated differential output resistor and transmission line impedance/termination resistor. When driving a 100Ω termination resistor, a differential voltage of 250mV to 475mV is produced. For loads greater than 100Ω, the output voltage is larger, and for loads less than 100Ω, the output voltage is smaller. See the Differential Output Voltage vs. Load Resistance curve in *Typical Operating Characteristics* for more information. The outputs are short-circuit current limited for single-ended and differential shorts.

MAX9174 Input Fail-Safe

The fail-safe feature of the MAX9174 sets the outputs high when the differential input is:

- Open
- Undriven and shorted
- Undriven and terminated

Without a fail-safe circuit, when the input is undriven, noise at the input may switch the outputs and it may appear to the system that data is being sent. Open or undriven terminated input conditions can occur when a cable is disconnected or cut, or when a driver output is in high impedance. A shorted input can occur because of a cable failure.

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

When the input is driven with a differential signal of $|V_{ID}|$ = 50mV to 1.2V within a voltage range of 0 to 2.4V, the fail-safe circuit is not activated. If the input is open, undriven and shorted, or undriven and terminated, an internal resistor in the fail-safe circuit pulls the input above VCC - 0.3V, activating the fail-safe circuit and forcing the outputs high (Figure 1).

Overshoot and Undershoot Voltage Protection

The MAX9174/MAX9175 are designed to protect the power-down inputs ($\overline{PD0}$ and $\overline{PD1}$) against latchup due to transient overshoot and undershoot voltage. If the input voltage goes above VCC or below GND by up to 1V, an internal circuit limits input current to 1.5mA.

Applications Information

Power-Supply Bypassing

Bypass the V_{CC} pin with high-frequency surface-mount ceramic 0.1µF and 0.001µF capacitors in parallel as close to the device as possible, with the smaller valued capacitor closest to V_{CC}.

Differential Traces

Input and output trace characteristics affect the performance of the MAX9174/MAX9175. Use controlled-impedance differential traces (100Ω typ). To reduce radiated noise and ensure that noise couples as common mode, route the differential input and output signals within a pair close together. Reduce skew by matching the electrical length of the two signal paths that make up the differential pair. Excessive skew can result in a degradation of magnetic field cancellation. Maintain a constant distance between the differential traces to avoid discontinuities in differential impedance. Minimize the number of vias to further prevent impedance discontinuities.

Cables and Connectors

Interconnect for LVDS typically has a controlled differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Avoid the use of unbalanced cables such as ribbon or simple coaxial cable. Balanced cables such as twisted pair offer superior signal quality and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

Termination

The MAX9174/MAX9175 require external input and output termination resistors. For LVDS, connect an input termination resistor across the differential input and at the far end of the interconnect driven by the LVDS outputs. Place the input termination resistor as close to the receiver input as possible. Termination resistors should match the differential impedance of the transmission line. Use 1% surface-mount resistors.

Table 1. Input Function Table

INPUT		OUTPUTS
(IN+) - (IN-)		(OUT_+) - (OUT_-)
≥ +50mV		H
≤ -50mV		L
-50mV < VID < +50mV		Indeterminate
MAX9175	Open	H
MAX9174	Open, undriven short, or undriven parallel termination	H

Table 2. Power-Down Function Table

$\overline{PD1}$	$\overline{PD0}$	OUT_+, OUT_-
H	H	Both outputs enabled
L or open	L or open	Shutdown to minimum power, outputs high impedance to ground
L or open	High	OUT0 enabled, OUT1 high impedance to ground
High	L or open	OUT1 enabled, OUT0 high impedance to ground

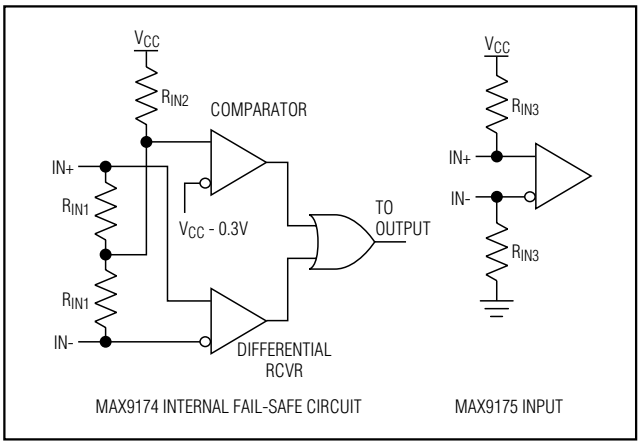


Figure 1. Input Structure

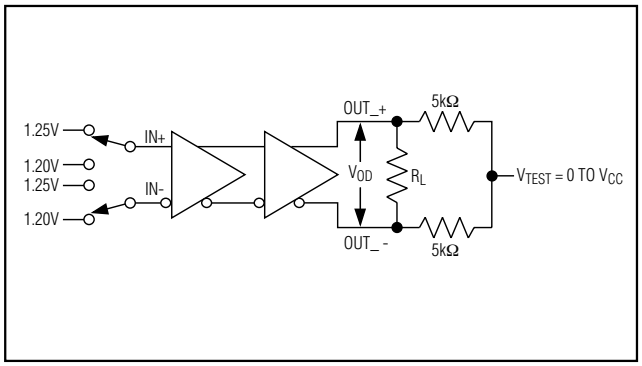


Figure 2. V_{OD} Test Circuit

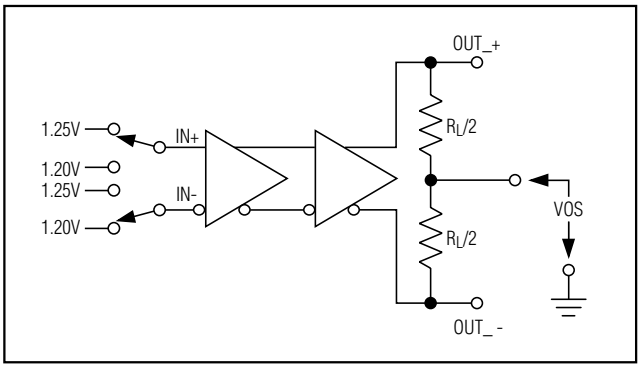


Figure 3. V_{OS} Test Circuit

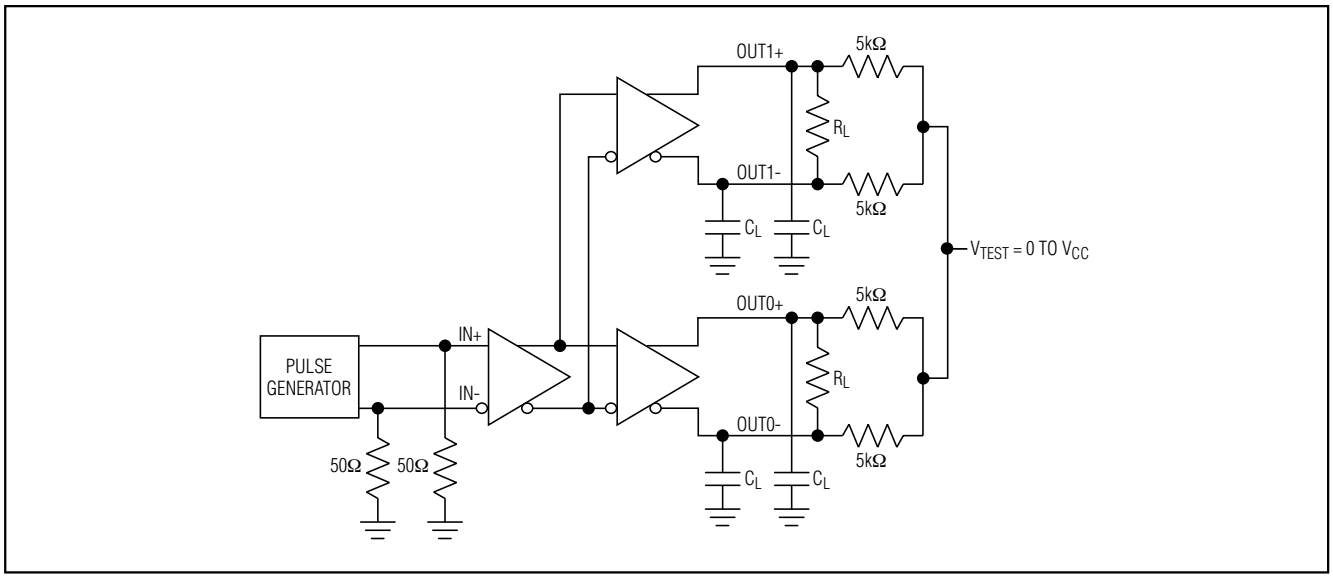


Figure 4. Transition Time, Propagation Delay, and Output-to-Output Skew Test Circuit

The MAX9174/MAX9175 feature an integrated differential output resistor. This resistor reduces jitter by damping reflections produced by a mismatch between the transmission line and termination resistor at the far end of the interconnect.

Board Layout

Separate the differential and single-ended signals to reduce crosstalk. A four-layer printed circuit board with separate layers for power, ground, differential signals, and single-ended logic signals is recommended. Separate the differential signals from the logic signals with power and ground planes for best results.

IEC 61000-4-2 Level 4 ESD Protection

The IEC 61000-4-2 standard (Figure 9) specifies ESD tolerance for electronic systems. The IEC 61000-4-2 model specifies a 150pF capacitor that is discharged into the device through a 330Ω resistor. The MAX9174/MAX9175 differential inputs and outputs are rated for IEC 61000-4-2 level 4 (±8kV Contact Discharge and ±15kV Air-Gap Discharge). The Human Body Model (HBM, Figure 10) specifies a 100pF capacitor that is discharged into the device through a 1.5kΩ resistor. IEC 61000-4-2 level 4 discharges higher peak current and more energy than the HBM due to the lower series resistance and larger capacitor.

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

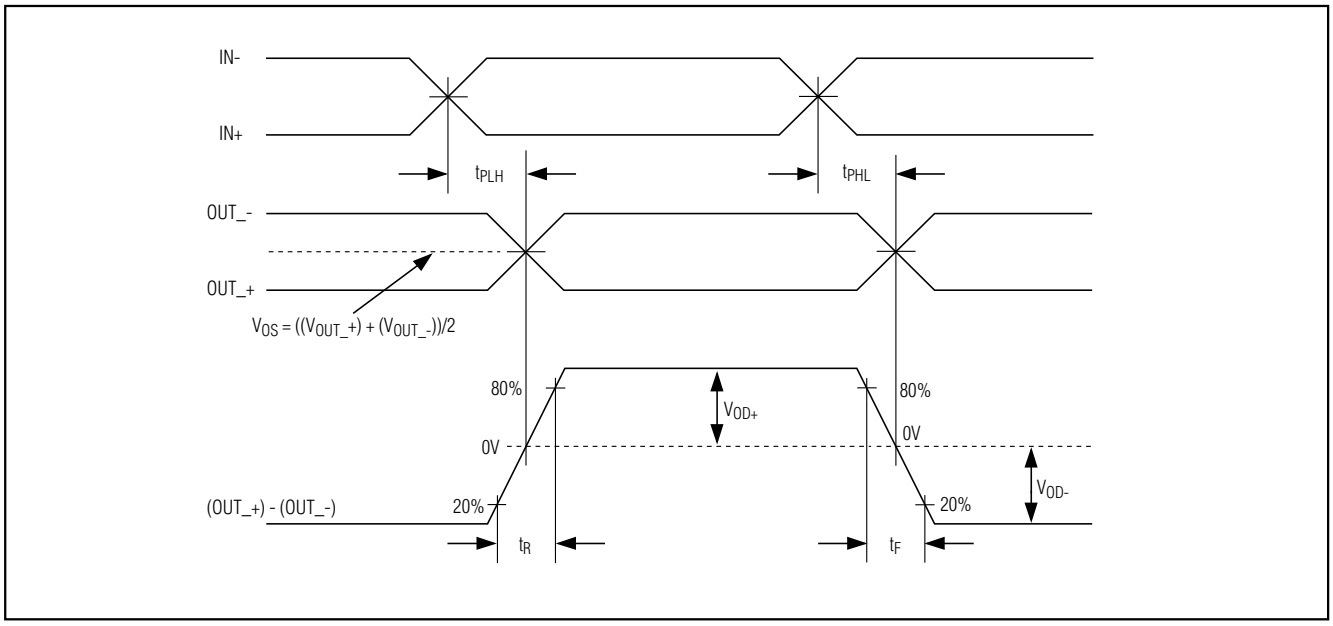


Figure 5. Transition Time and Propagation Delay Timing

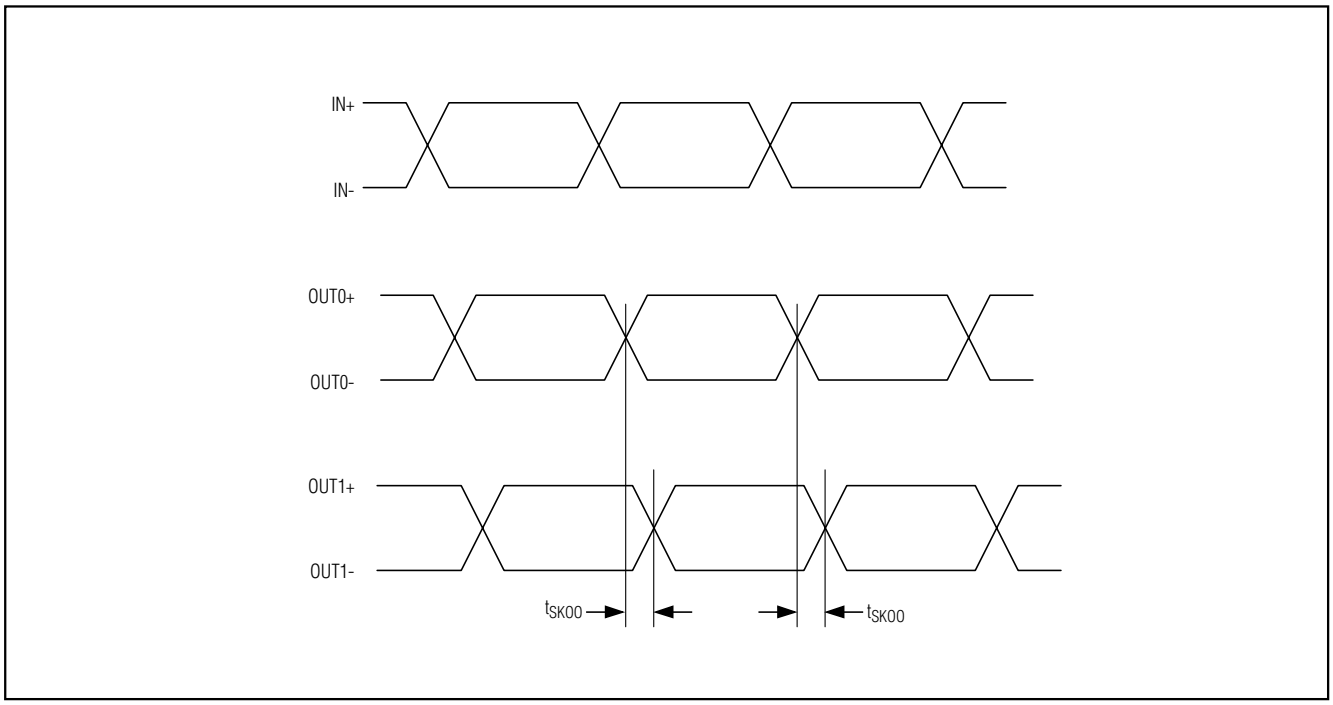


Figure 6. Output-to-Output Skew

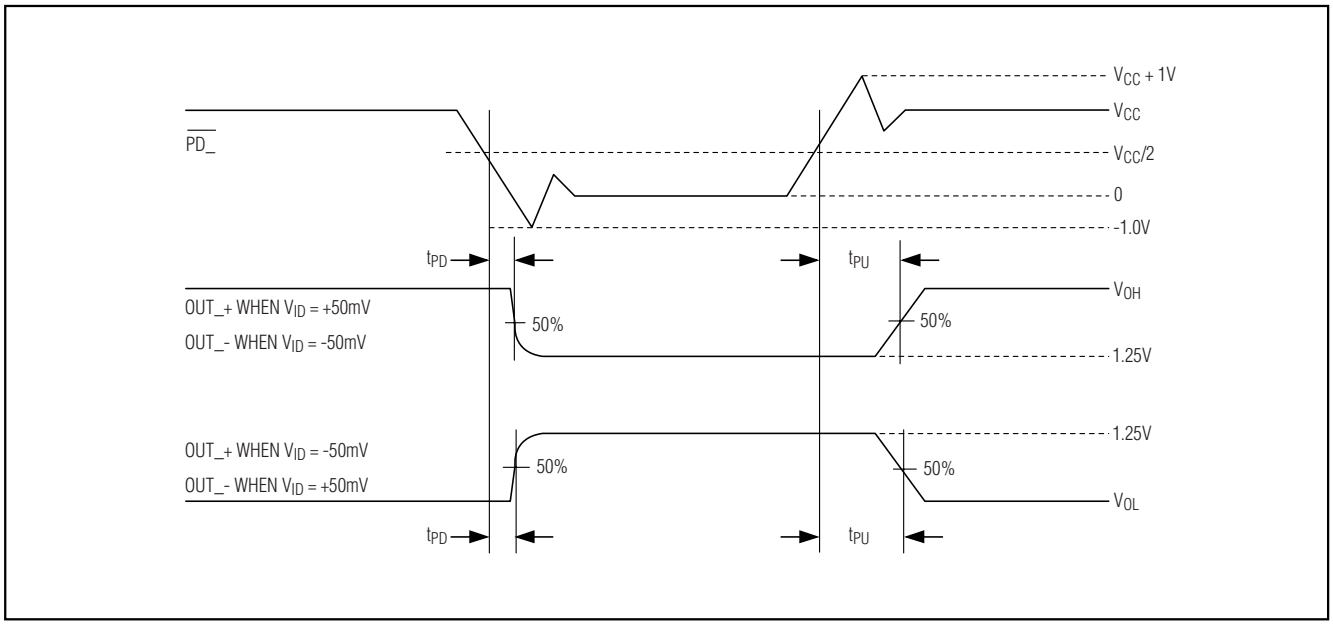


Figure 7. Power-Up/Down Delay Waveform

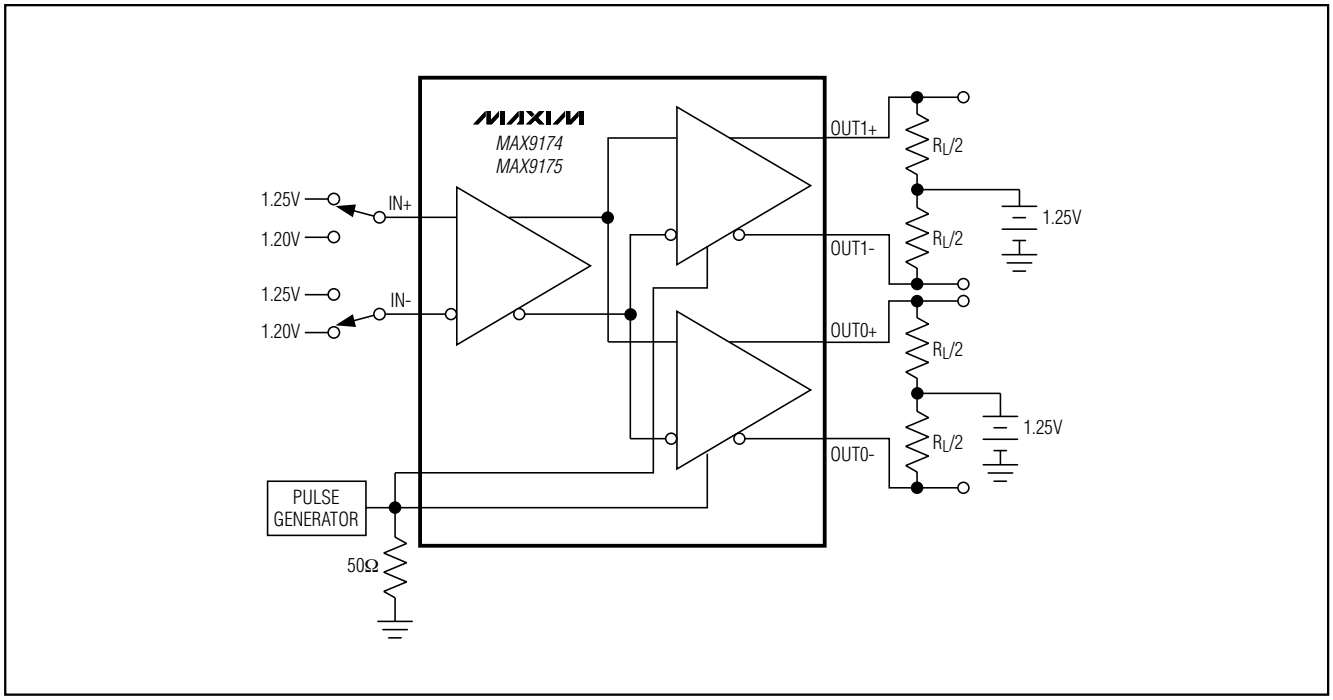


Figure 8. Power-Up/Down Delay Test Circuit

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

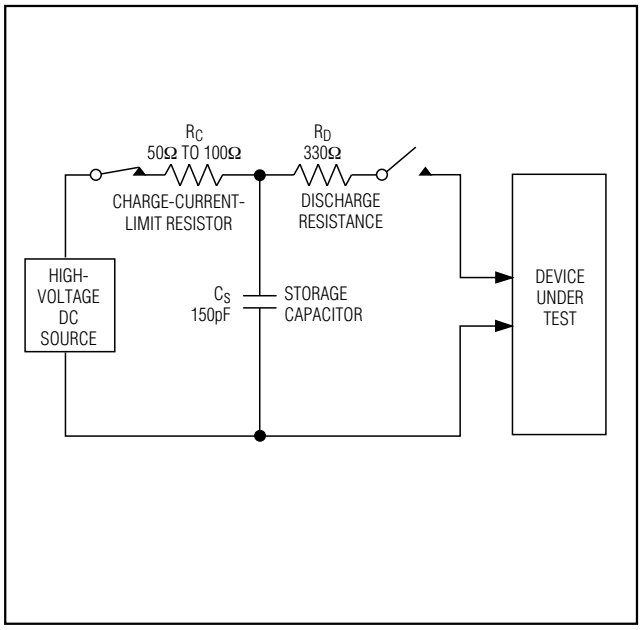


Figure 9. IEC 61000-4-2 Contact Discharge ESD Test Model

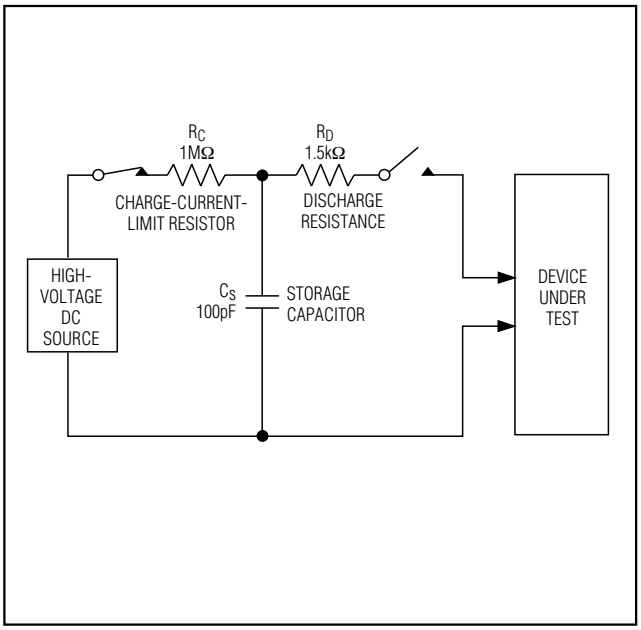
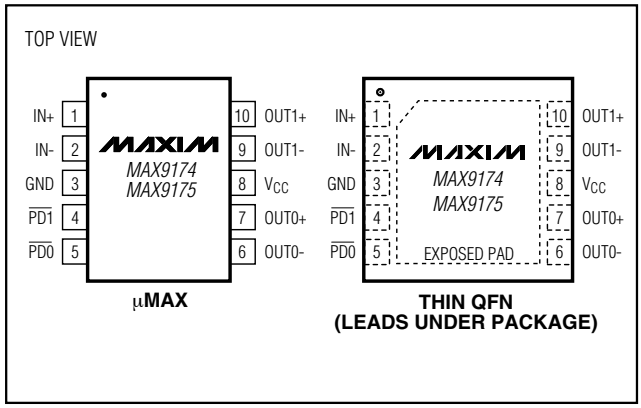
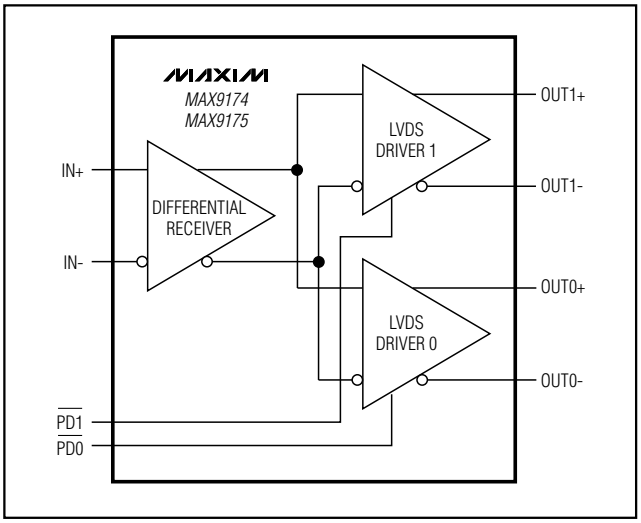


Figure 10. Human Body ESD Test Model

Pin Configurations



Functional Diagram



Chip Information

TRANSISTOR COUNT: 693

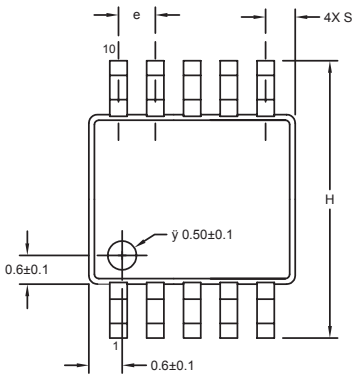
PROCESS: CMOS

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

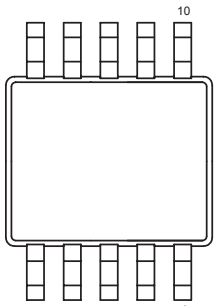
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

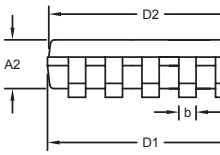


TOP VIEW

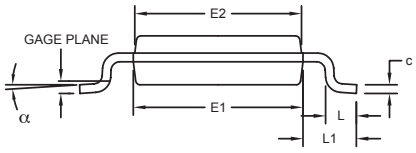


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

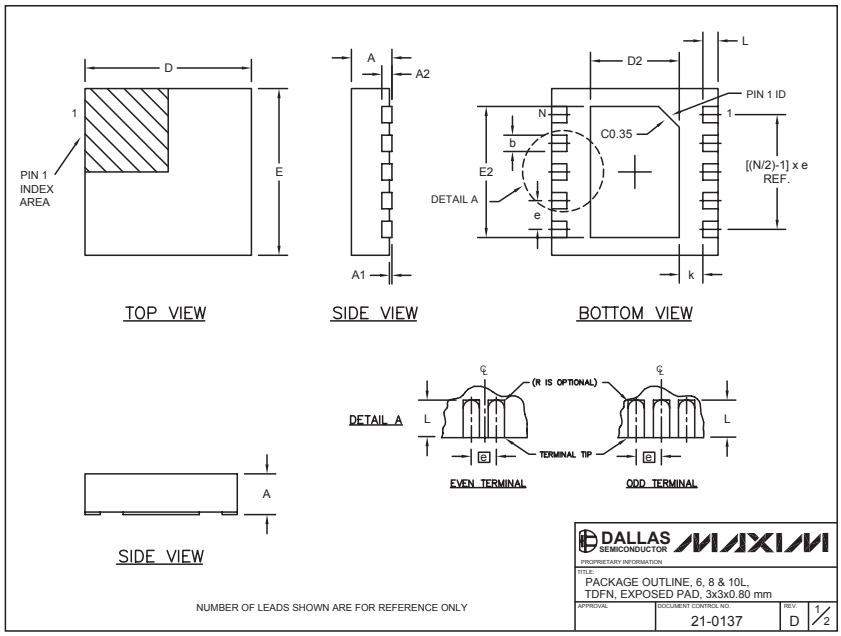
TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

670MHz LVDS-to-LVDS and Anything-to-LVDS 1:2 Splitters

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 6, 8 & 10L,
TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
D
2/2