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EVALUATION KIT AVAILABLE

Gigabit Multimedia Serial Link Serializer with LVDS System Interface

General Description

The MAX9249 serializer with LVDS system interface utilizes Maxim's Gigabit multimedia serial link (GMSL) technology. The MAX9249 serializer pairs with any GMSL deserializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data.

The MAX9249 allows a maximum serial payload data rate of 2.5Gbps for a 15m shielded twisted-pair (STP) cable. The serializer operates up to a maximum clock rate of 104MHz (3-channel LVDS) or 78MHz (4-channel LVDS). This serial link supports display panels from QVGA (320 x 240) to WXGA (1280 x 800) and higher with 24-bit color.

The 3-channel mode handles three lanes of LVDS data (21 bits), UART control signals, and three audio signals. The 4-channel mode handles four lanes of LVDS data (28 bits), UART control signals, three audio signals, and/or up to three auxiliary parallel inputs. The three audio inputs form a standard I²S interface, supporting sample rates from 8kHz to 192kHz and audio word lengths of 4 to 32 bits. The embedded control channel forms a full-duplex, differential, 100kbps to 1Mbps UART link between the serializer and deserializer. The electronic control unit (ECU), or microcontroller (µC), can be located on the MAX9249 side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. In addition, the control channel enables ECU/µC control of peripherals on the remote side, such as backlight control, grayscale Gamma correction, camera module, and touch screen. Base-mode communication with peripherals uses either I²C or the GMSL UART format. A bypass mode enables full-duplex communication using custom UART formats.

The MAX9249 serializer driver preemphasis, along with the channel equalizer on the GMSL deserializer, extends the link length and enhances the link reliability. Spread spectrum is available on the MAX9249 to reduce EMI on the serial link and the parallel output of the GMSL deserializer. The serial output complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

The core supply for the MAX9249 is 1.8V. The I/O supply ranges from 1.8V to 3.3V. The MAX9249 is available in a 48-pin TQFP package (7mm x 7mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +105°C automotive temperature range.

Features

- ♦ **Pairs with Any GMSL Deserializer**
- ♦ **2.5Gbps Payload Rate AC-Coupled Serial Link with 8B/10B Line Coding**
- ♦ **Supports Up to WXGA (1280 x 800) with 24-Bit Color**
- ♦ **8.33MHz to 104MHz (3-Channel LVDS) or 6.25MHz to 78MHz (4-Channel LVDS) Input Clock**
- ♦ **4-Bit to 32-Bit Word Length, 8kHz to 192kHz I²S Audio Channel Supports High-Definition Audio**
- ♦ **Embedded Half-/Full-Duplex Bidirectional Control Channel (100kbps to 1Mbps)**
- ♦ **Interrupt Supports Touch-Screen Functions for Display Panels**
- ♦ **Remote-End I²C Master for Peripherals**
- ♦ **Preemphasis Line Driver**
- ♦ **Programmable Spread Spectrum on the Serial Outputs for Reduced EMI**
- ♦ **Automatic Data-Rate Detection Allows "On-the-Fly" Data-Rate Change**
- ♦ **Input Clock PLL Jitter Attenuator**
- ♦ **Built-In PRBS Generator for BER Testing of the Serial Link**
- ♦ **Line-Fault Detector Detects Serial Link Shorts to Ground, Battery, or Open Link**
- ♦ **ISO 10605 and IEC 61000-4-2 ESD Protection**
- ♦ **-40°C to +105°C Operating Temperature Range**
- ♦ **1.8V to 3.3V I/O, 1.8V Core, and 3.3V LVDS Supplies**
- ♦ **Patent Pending**

Applications

High-Resolution Automotive Navigation

Rear-Seat Infotainment

Megapixel Camera Systems

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9249GCM/V+	-40°C to +105°C	48 TQFP-EP*
MAX9249GCM/V+T	-40°C to +105°C	48 TQFP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND ....-0.5V to +1.9V
LVDSVDD to AGND...-0.5V to +3.9V
DVDD to GND ....-0.5V to +1.9V
IOVDD to GND ....-0.5V to +3.9V
Any Ground to Any Ground ....-0.5V to +0.5V
RXIN_ _, RXCLKIN_ to AGND ....-0.5V to +3.9V
OUT+, OUT- to AGND ....-0.5V to +1.9V
LMN_ to AGND (15mA current limit)....................-0.5V to +3.9V
All Other Pins to Any Ground.............. -0.5V to (V_{IOVDD} + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply ....Continuous
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFP (derate 36.2mW/°C above +70°C)....2898.6mW
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
(RXIN_ _, RXCLKIN_, OUT+, OUT-) to AGND ....±8kV
All Other Pins to GND...±3kV

IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge
(RXIN_ _, RXCLKIN_) to AGND......................................±4kV
(OUT+, OUT-) to AGND ....±10kV
Air Discharge
(RXIN_ _, RXCLKIN_) to AGND......................................±8kV
(OUT+, OUT-) to AGND ....±12kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge
(RXIN_ _, RXCLKIN_) to AGND......................................±6kV
(OUT+, OUT-) to AGND ....±10kV
Air Discharge
(RXIN_ _, RXCLKIN_) to AGND....................................±20kV
(OUT+, OUT-) to AGND ....±30kV
Operating Temperature Range........................ -40°C to +105°C
Junction Temperature ....+150°C
Storage Temperature Range........................... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

48 TQFP-EP
Junction-to-Ambient Thermal Resistance (θ_{JA}).......27.6°C/W
Junction-to-Case Thermal Resistance (θ_{JC})................2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS ($\overline{PWDN}$, SSEN, BWS, DRS, MS, CDS, $\overline{AUTOS}$, SD/CNTL0, SCK, WS, CNTL_)							
High-Level Input Voltage	V_{IH1}	$\overline{PWDN}$, SSEN, BWS, DRS, MS, CDS, $\overline{AUTOS}$		0.65 x V_{IOVDD}			V
		SD/CNTL0, SCK, WS, CNTL_		0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUT (INT)							
High-Level Output Voltage	V_{OH1}	I_{OH} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C AND UART I/O, OPEN-DRAIN OUTPUT (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)		-110		+5	µA
Low-Level Open-Drain Output Voltage	V_{OL2}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV
		3.3dB preemphasis setting, $V_{OD(P)}$ (Figure 2)		350		610	
		3.3dB deemphasis setting, $V_{OD(D)}$ (Figure 2)		240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}					15	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}					15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}					27	mV
Low Switching Threshold	V_{CLR}			-27			mV
LINE-FAULT DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 3				0.3	V
Normal Thresholds	V_{TN}	Figure 3		0.57		1.07	V
Open Thresholds	V_{TO}	Figure 3		1.45		V_{IO} + 60mV	V
Open Input Voltage	V_{IO}	Figure 3		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 3		2.47			
LVDS INPUTS (RXIN_ _, RXCLKIN_)							
Differential Input High Threshold	V_{TH}					50	mV
Differential Input Low Threshold	V_{TL}			-50			mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, $V_{LVDSVDD}$ = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Differential Termination Resistance	R_{TERM}			85	110	135	Ω
Input Current	I_{IN+}, I_{IN-}	$\overline{PWDN}$ = high or low, IN+ and IN- are shorted		-25		+25	µA
Power-Off Input Current	I_{IN0+}, I_{IN0-}	V_{AVDD} = V_{DVDD} = V_{IOVDD} = 0V		-40		+40	µA
POWER SUPPLY							
Worst-Case Supply Current (Figure 4)	I_{WCS}	BWS = GND	$f_{RXCLKIN\_}$ = 16.6MHz		125	165	mA
			$f_{RXCLKIN\_}$ = 33.3MHz		135	175	
			$f_{RXCLKIN\_}$ = 66.6MHz		150	190	
			$f_{RXCLKIN\_}$ = 104MHz		175	220	
Sleep-Mode Supply Current	I_{CCS}	LVDS inputs are not driven			45	125	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND, LVDS inputs are not driven			5	80	µA

AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (RXCLKIN_)						
Clock Frequency	$f_{RXCLKIN\_}$	BWS = GND, V_{DRS} = V_{IOVDD}	8.33		16.66	MHz
		BWS = GND, DRS = GND	16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}	6.25		12.5	
		V_{BWS} = V_{IOVDD}, DRS = GND	12.5		78	
I²C/UART PORT TIMING (Note 3)						
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 5)	100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 5)	0			ns
SWITCHING CHARACTERISTICS (Note 3)						
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial-bit rate = 3.125Gbps (Note 3)		90	150	ps
Total Serial Output Jitter	t_{TSOJ1}	3.125Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 6)		0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.125Gbps PRBS signal		0.15		UI
CNTL_ Input Setup Time	t_{SET}	CNTL_ (Figure 7)	3			ns
CNTL_ Input Hold Time	t_{HOLD}	CNTL_ (Figure 7)	1.5			ns
RXIN_ _ Skew Margin	t_{RSKM}	Figure 8	0.3			UI

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.15V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Serializer Delay (Note 4)	t_{SD}	Figure 9	Spread spectrum enabled			2950	Bits
			Spread spectrum disabled			390	
Link Start Time	t_{LOCK}	Figure 10				3.5	ms
Power-Up Time	t_{PU}	Figure 11				3.5	ms
I²S INPUT TIMING							
WS Frequency	f_{WS}	Table 3		8		192	kHz
Sample Word Length	n_{WS}	Table 3		4		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times 2$		(8 x 4) x 2		(192 x 32) x 2	kHz
SCK Clock High Time (Note 3)	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SCK Clock Low Time (Note 3)	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SD/CNTL0, WS Setup Time	t_{SET}	Figure 12 (Note 3)		2			ns
SD/CNTL0, WS Hold Time	t_{HOLD}	Figure 12 (Note 3)		2			ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.

Note 3: Not production tested.

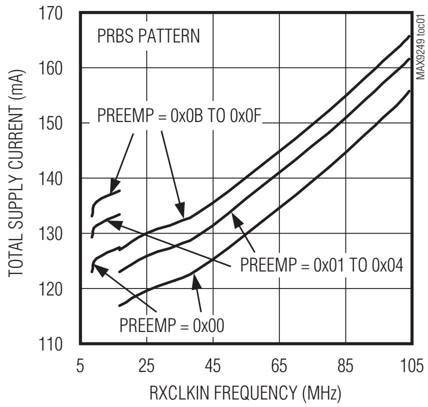
Note 4: Bit time $= \frac{1}{30 \times f_{RXCLKIN\_}}$ (BWS = 0), $= \frac{1}{40 \times f_{RXCLKIN\_}}$ (BWS = V_{IOVDD})

Gigabit Multimedia Serial Link Serializer with LVDS System Interface

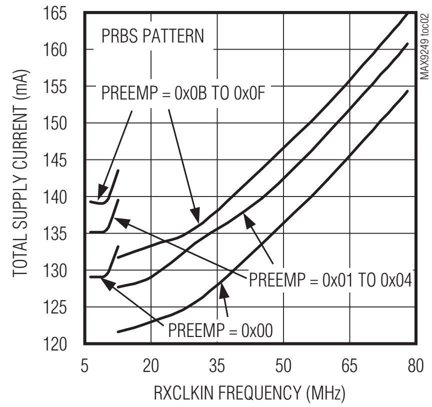
Typical Operating Characteristics

($V_{DVDD} = V_{AVDD} = V_{IOVDD}$ = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

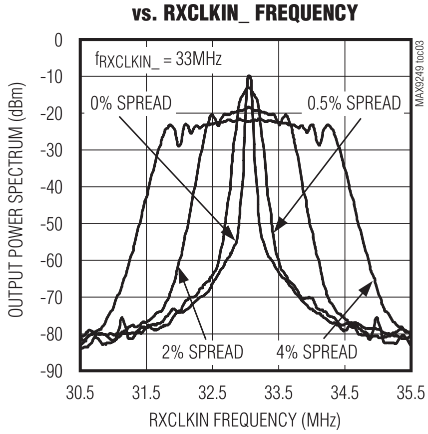
TOTAL SUPPLY CURRENT vs. RXCLKIN_ FREQUENCY (3-CHANNEL MODE)



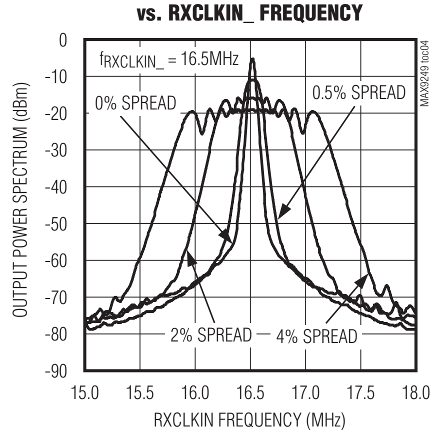
TOTAL SUPPLY CURRENT vs. RXCLKIN_ FREQUENCY (4-CHANNEL MODE)



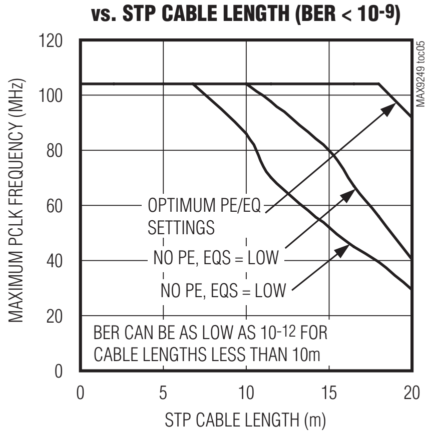
OUTPUT POWER SPECTRUM vs. RXCLKIN_ FREQUENCY



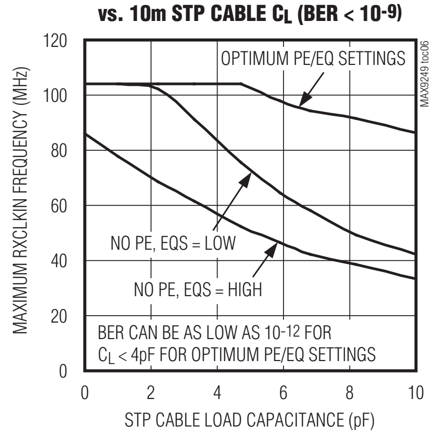
OUTPUT POWER SPECTRUM vs. RXCLKIN_ FREQUENCY



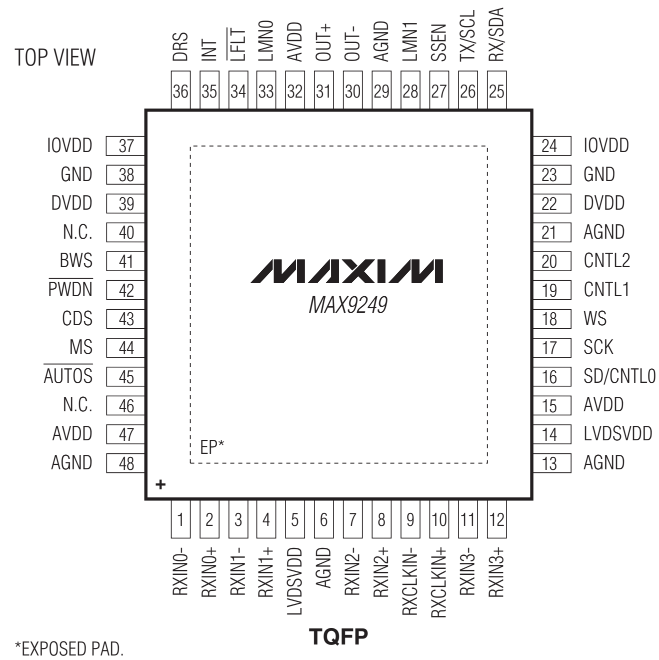
MAXIMUM PCLK FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-9})



MAXIMUM RXCLKIN_ FREQUENCY vs. 10m STP CABLE C_L (BER < 10^{-9})



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1–4, 7, 8, 11, 12	RXIN_-, RXIN_+	Differential LVDS Data Inputs. Set BWS = low (3-channel mode) to use RXIN0_ to RXIN2_. Set BWS = high (4-channel mode) to use RXIN0_ to RXIN3_.
5, 14	LVDSVDD	3.3V LVDS Power Supply. Bypass LVDSVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to LVDSVDD.
6, 13, 21, 29, 48	AGND	Analog Ground
9, 10	RXCLKIN-, RXCLKIN+	LVDS Input for the LVDS Clock
15, 32, 47	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to AVDD.
16	SD/CNTL0	I^2S Serial-Data Input with Internal Pulldown to GND. Disable I^2S to use SD/CNTL0 as an additional input.
17	SCK	I^2S Serial-Clock Input with Internal Pulldown to GND
18	WS	I^2S Word-Select Input with Internal Pulldown to GND
19	CNTL1	Control Input 1 with Internal Pulldown to GND. Data is latched every RXCLKIN_ cycle (Figure 7). CNTL1 is not available in 3-channel mode. Drive BWS high (4-channel mode) to use this input. CNTL1 or RES (RES from VESA Standard Panel Specification) is mapped to DIN27 (see the *Reserved Bit (RES)* section).

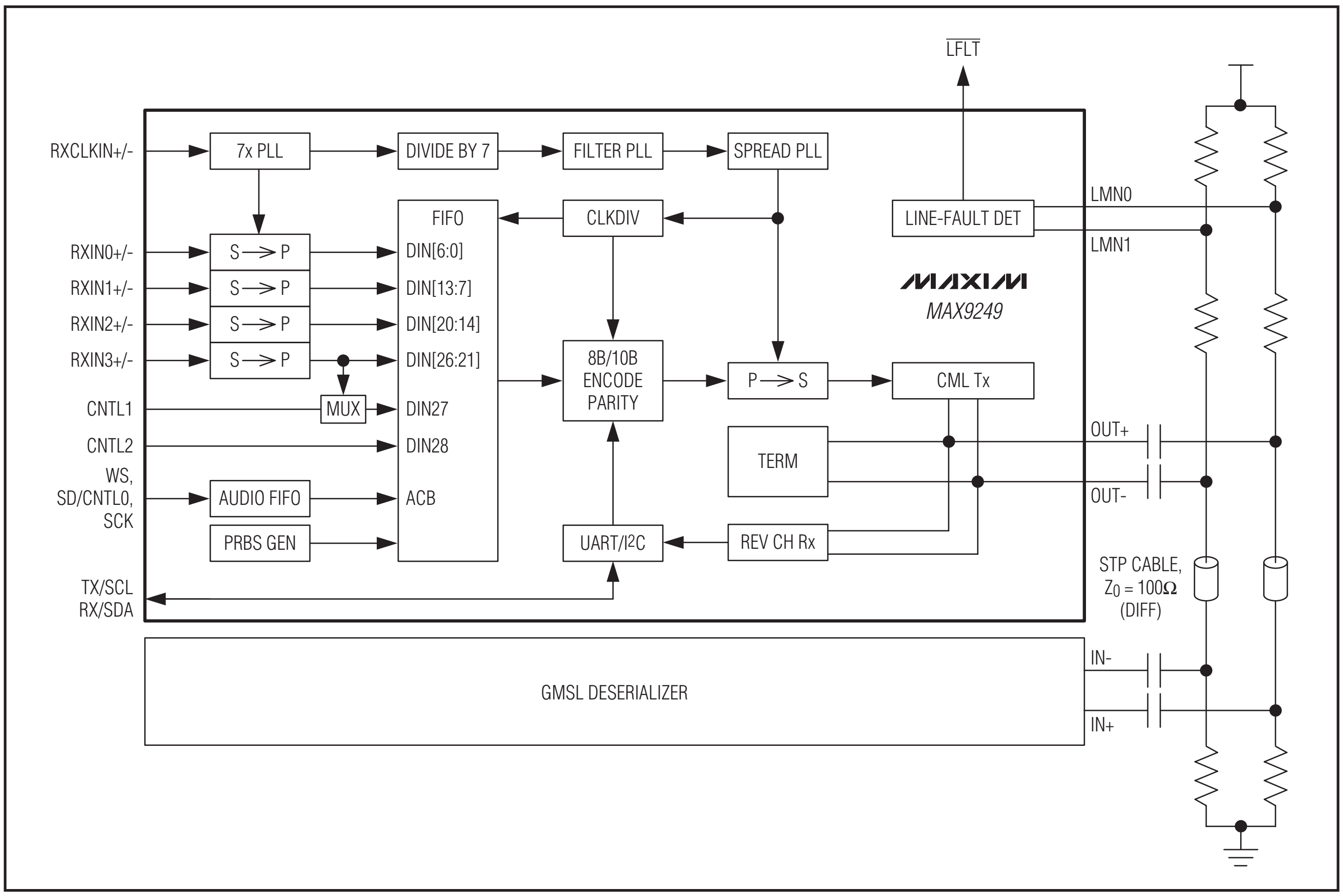
Pin Description (continued)

PIN	NAME	FUNCTION
20	CNTL2	Control Input 2 with Internal Pulldown to GND. Data is latched every RXCLKIN_ cycle (Figure 7). CNTL2 is not available in 3-channel mode. Drive BWS high (4-channel mode) to use this input. CNTL2 is mapped to DIN28.
22, 39	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
23, 38	GND	Digital and I/O Ground
24, 37	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
25	RX/SDA	Receive/Serial Data. UART receive or I²C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9249's UART. In I²C mode, RX/SDA is the SDA input/output of the MAX9249's I²C master.
26	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9249's UART. In I²C mode, TX/SCL is the SCL output of the MAX9249's I²C master.
27	SSEN	Spread-Spectrum Enable. Serial link spread-spectrum enable input requires external pulldown or pullup resistors. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
28	LMN1	Line-Fault Monitor Input 1 (see Figure 3 for details)
30, 31	OUT-, OUT+	Differential CML Output+/-. Differential outputs of the serial link.
33	LMN0	Line-Fault Monitor Input 0 (see Figure 3 for details)
34	$\overline{\text{LFLT}}$	Line Fault. Active-low, open-drain line-fault output with a 60kΩ internal pullup resistor. $\overline{\text{LFLT}}$ = low indicates a line fault. $\overline{\text{LFLT}}$ is high impedance when $\overline{\text{PWDN}}$ = low.
35	INT	Interrupt Output to Indicate Remote Side Requests. INT = low upon power-up and when $\overline{\text{PWDN}}$ = low. A transition on the INT input of the GMSL deserializer toggles the MAX9249's INT output.
36	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistors. Set DRS = high for RXCLKIN_ frequencies of 8.33MHz to 16.66MHz (3-channel mode) or 6.25MHz to 12.5MHz (4-channel mode). Set DRS = low for RXCLKIN_ frequencies of 16.66MHz to 104MHz (3-channel mode) or 12.5MHz to 78MHz (4-channel mode).
40, 46	N.C.	Internally Not Connected. Connect to GND or leave unconnected.
41	BWS	Bus-Width Select. Input width selection requires external pulldown or pullup resistors. Set BWS = low for 3-channel mode. Set BWS = high for 4-channel mode.
42	$\overline{\text{PWDN}}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistors.
43	CDS	Control Direction Selection. Control link direction selection input requires external pulldown or pullup resistors. Set CDS = low for µC use on the MAX9249 side of the serial link. Set CDS = high for µC use on the GMSL deserializer side of the serial link.
44	MS	Mode Select. Control link mode-selection input requires external pulldown or pullup resistors. Set MS = low to select base mode. Set MS = high to select the bypass mode.

Pin Description (continued)

PIN	NAME	FUNCTION
45	$\overline{\text{AUTOS}}$	Autostart Setting. Active-low power-up mode-selection input requires external pulldown or pullup resistors. Set $\overline{\text{AUTOS}}$ = high to power up the device with no link active. Set $\overline{\text{AUTOS}}$ = low to have the MAX9249 power up the serial link with autorange detection (see Tables 8 and 9).
—	EP	Exposed Pad. EP internally connected to AGND. **MUST** externally connect EP to the AGND plane for proper thermal and electrical performance.

Functional Diagram



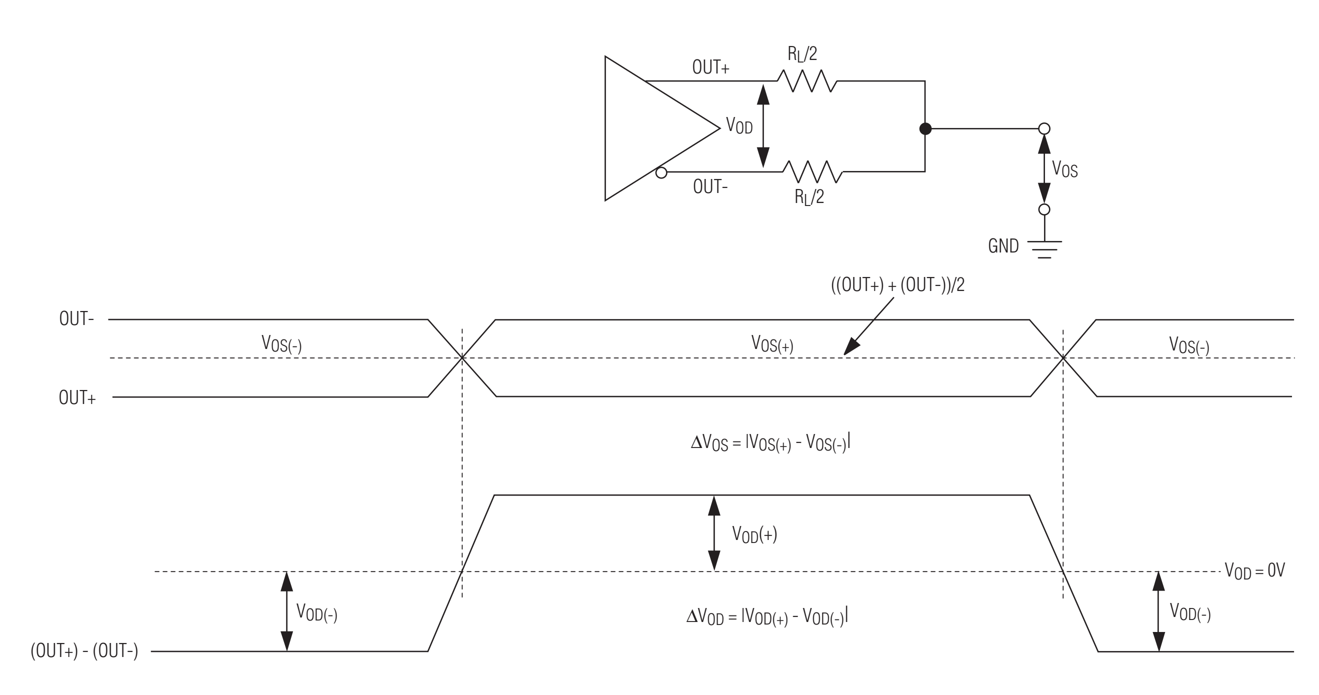


Figure 1. Serial-Output Parameters

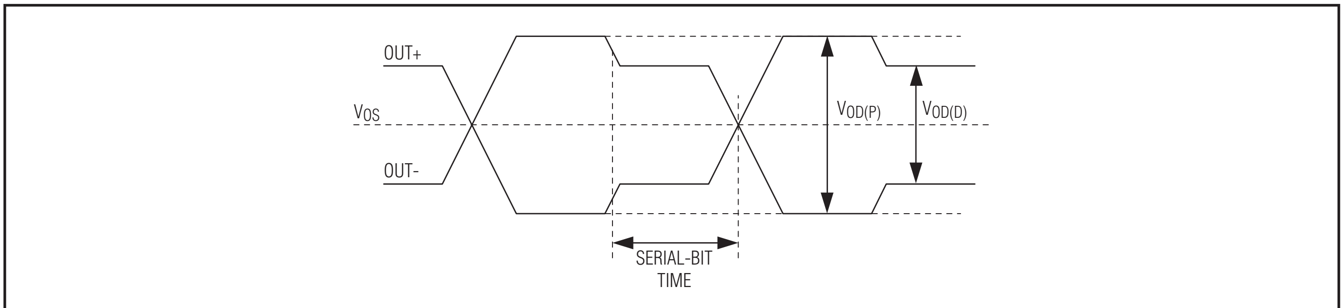


Figure 2. Output Waveforms at OUT+ and OUT-

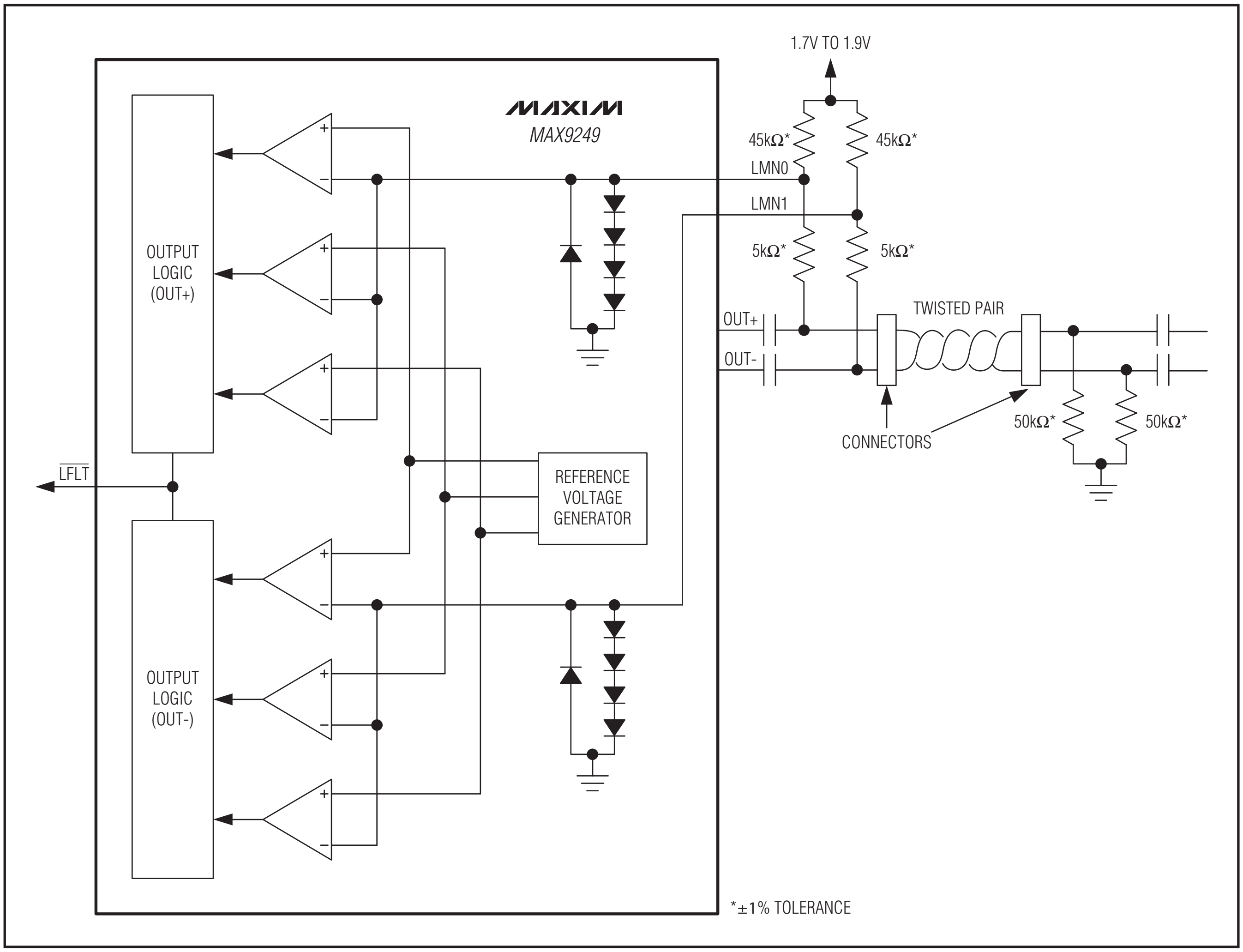


Figure 3. Line-Fault Detector Circuit

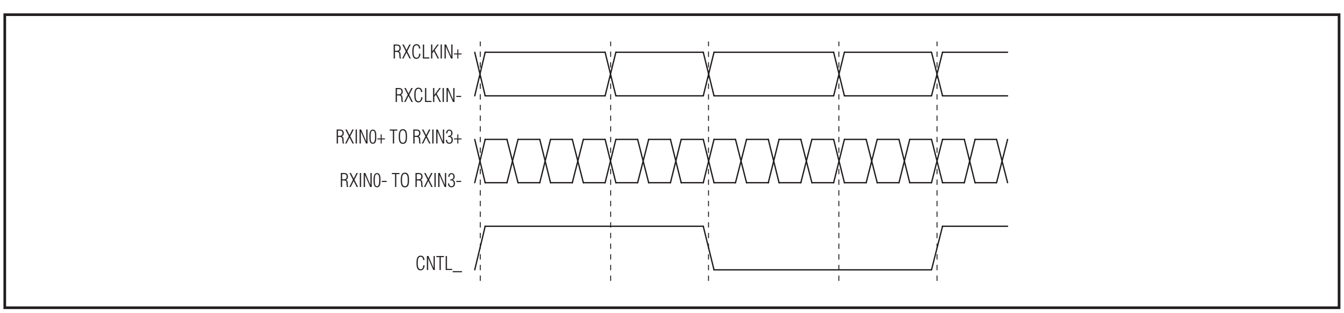


Figure 4. Worst-Case Pattern Input

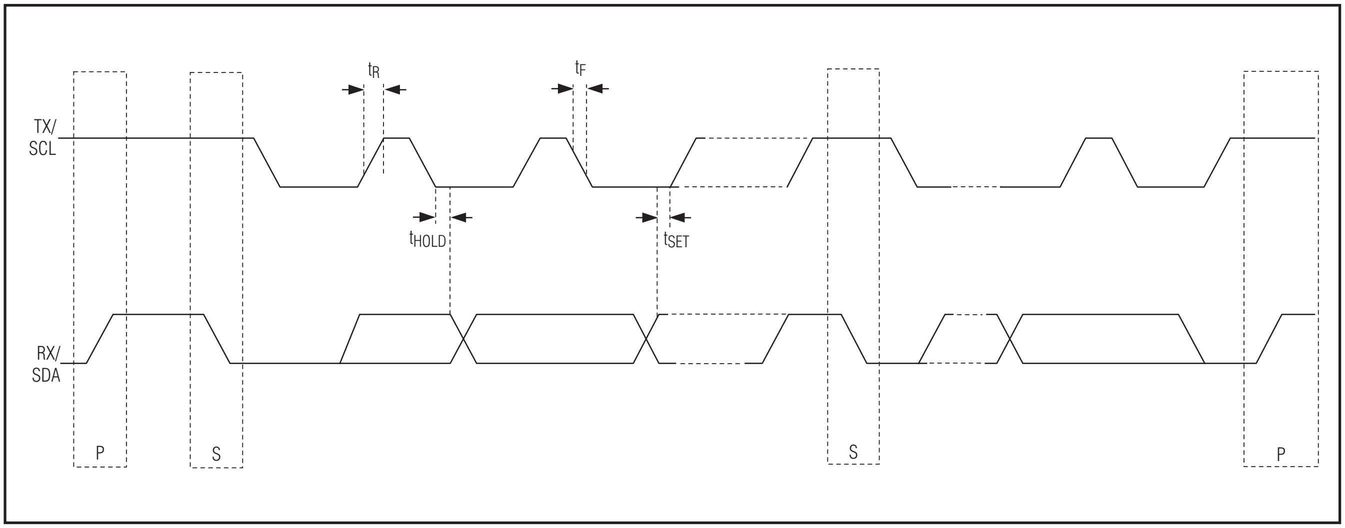


Figure 5. I2C Timing Parameters

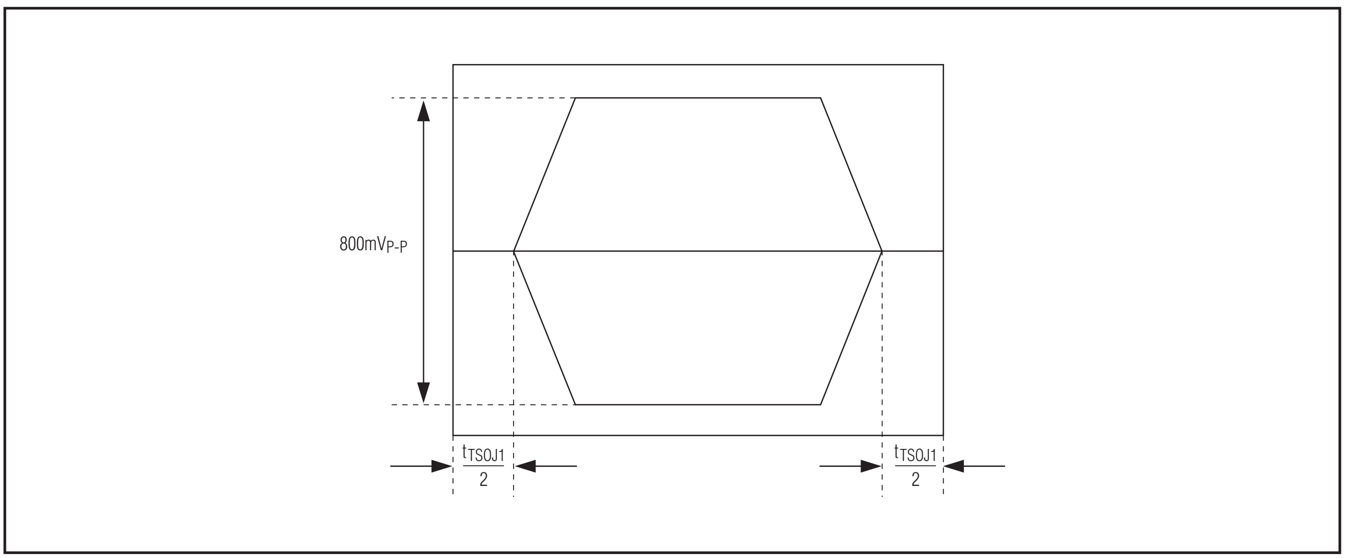


Figure 6. Differential Output Template

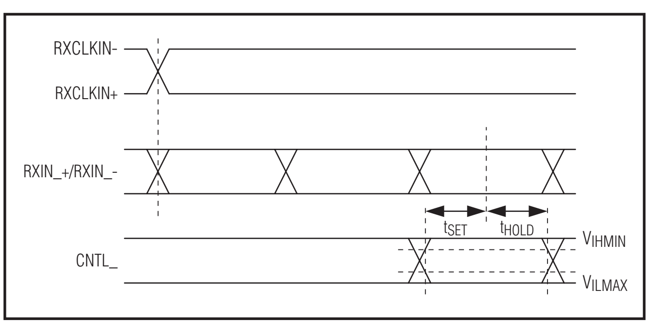


Figure 7. Input Setup-and-Hold Times

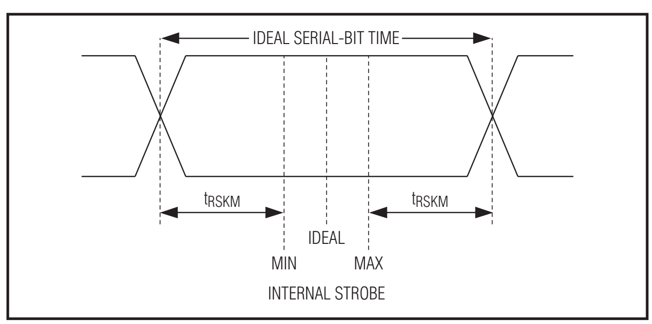


Figure 8. LVDS Receiver Input Skew Margin

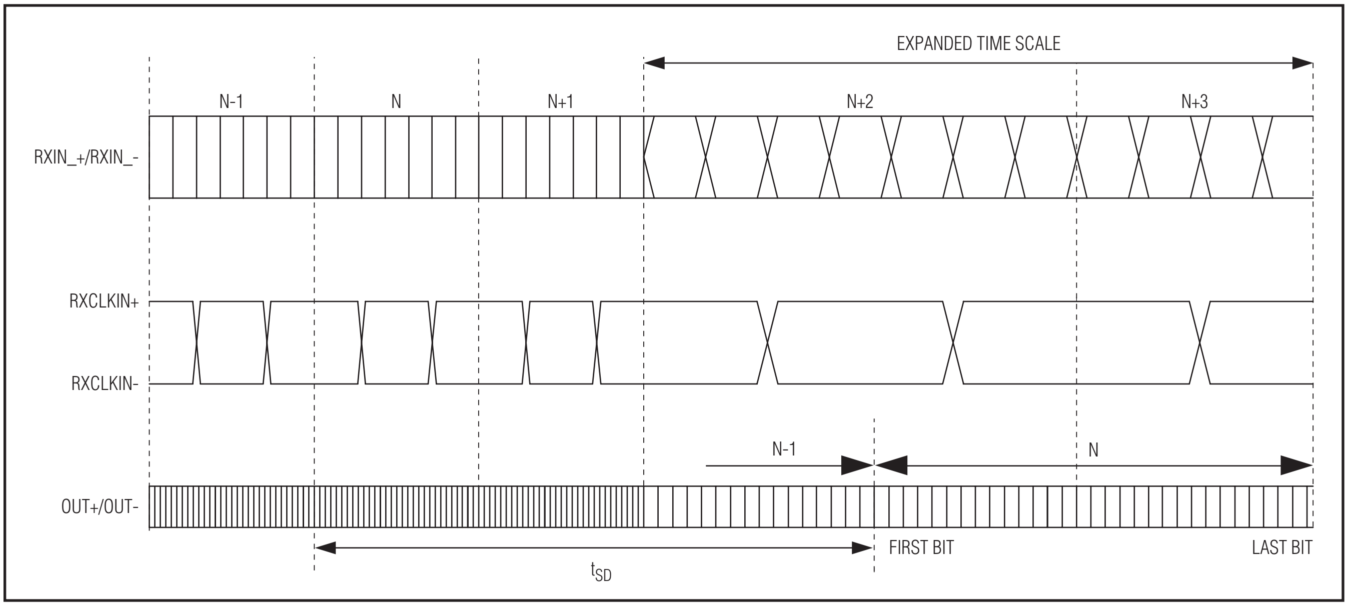


Figure 9. Serializer Delay

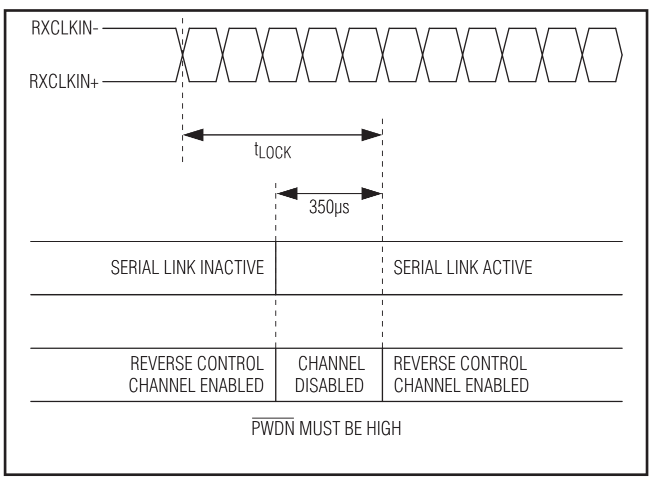


Figure 10. Link Startup Time

Gigabit Multimedia Serial Link Serializer with LVDS System Interface

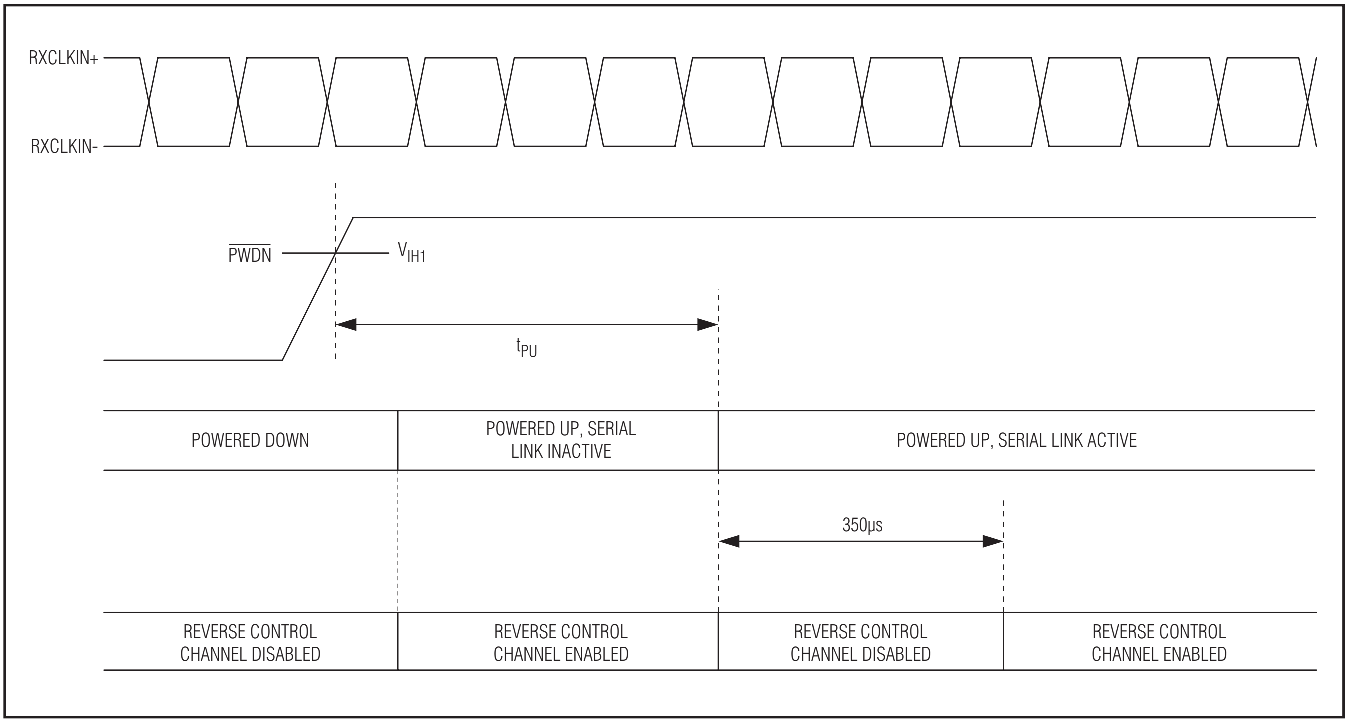


Figure 11. Power-Up Delay

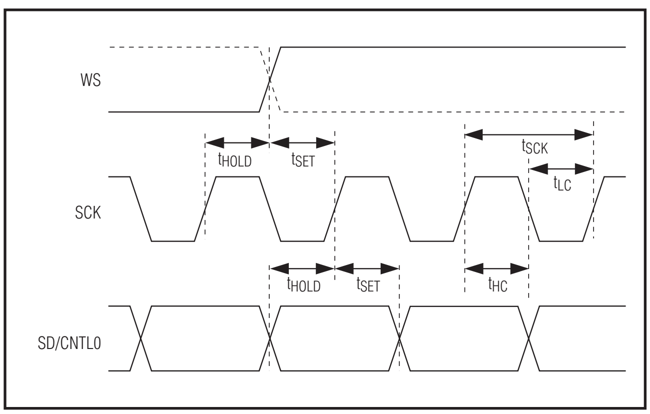


Figure 12. Input I²S Timing Parameters

Detailed Description

The MAX9249 serializer with LVDS system interface utilizes Maxim's GMSL technology. The MAX9249 serializer pairs with any GMSL deserializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data.

The MAX9249 allows a maximum serial payload data rate of 2.5Gbps for a greater than 15m STP cable. The serializer operates up to a maximum clock of 104MHz for a 3-channel LVDS input or 78MHz for a 4-channel LVDS input. This serial link supports display panels from QVGA (320 x 240) up to WXGA (1280 x 800) with 24-bit color.

The 3-channel mode handles three lanes of LVDS data (21 bits), UART control signals, and three audio signals. The 4-channel mode handles four lanes of LVDS data (28 bits), UART control signals, three audio signals, and/or up to three auxiliary parallel inputs. The three audio inputs form a standard I^2S interface, supporting sample rates from 8kHz to 192kHz and audio word lengths of 4 to 32 bits. The embedded control channel forms a full-duplex, differential, 100kbps to 1Mbps UART link between the serializer and deserializer. The ECU, or µC, can be located on the MAX9249 side of the link (typical for video display), on the deserializer side of the link (typical for image sensing), or on both sides. In addition, the control channel enables ECU/µC control of peripherals in the remote side, such as backlight control, grayscale Gamma correction, camera module, and touch screen. Base-mode communication with peripherals uses either I^2C or the GMSL UART format. A bypass mode enables full-duplex communication using custom UART formats.

The MAX9249 serializer driver preemphasis, along with the channel equalizer on the GMSL deserializer, extends the link length and enhances the link reliability. Spread spectrum is available on the MAX9249 to reduce EMI on the serial link and the parallel output of the GMSL deserializer. The serial output complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

The µC configures various operating conditions of the MAX9249 and GMSL deserializer through internal registers. The default device addresses stored in the R0 and R1 registers of both the MAX9249 and GSML deserializer are 0x80 and 0x90, respectively. Write to the R0/R1 registers in both devices to change the device address of the MAX9249 or GMSL deserializer.

Table 1. Power-Up Default Register Map (see Table 12)

REGISTER ADDRESS (HEX)	POWER-UP DEFAULT (HEX)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID =1000000, serializer device address is 1000 000 RESERVED = 0
0x01	0x90	DESID =1001000, deserializer device address is 1001 000 RESERVED = 0
0x02	0x1F, 0x3F	SS = 000 (SSEN = low), SS = 001 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up AUDIOEN = 1, I^2S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking SDIV = 000000, autocalibrate sawtooth divider

Table 1. Power-Up Default Register Map (see Table 12) (continued)

REGISTER ADDRESS (HEX)	POWER-UP DEFAULT (HEX)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x04	0x03, 0x13, 0x83 or 0x93	SEREN = 0 ($\overline{\text{AUTOS}}$ = high), SEREN = 1 ($\overline{\text{AUTOS}}$ = low), serial link enable default depends on $\overline{\text{AUTOS}}$ pin state at power-up CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, sleep-mode state depends on CDS and $\overline{\text{AUTOS}}$ pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I^{2}C REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)
0x05	0x70	I2CMETHOD = 0, I^{2}C packets include register address DISFPLL = 1, filter PLL disabled CMLLVL = 11, 400mV CML signal level PREEMP = 0000, preemphasis off
0x06	0x40	RESERVED = 01000000
0x07	0x22	RESERVED = 00100010
0x08	0x0A (read only)	RESERVED = 0000 LFNEG = 10, no faults detected LFPOS = 10, no faults detected
0x0C	0x70	RESERVED = 01110000
0x0D	0x0F	SETINT = 0, interrupt output set to low RESERVED = 00 DISRES = 0, RES mapped to DIN27 SKEWADJ = 1111, no X7PLL clock skew adjustment
0x1E	0x03 (read only)	ID = 00000011, device ID is 0x03
0x1F	0x0X (read only)	RESERVED = 0000 REVISION = XXXX, revision number

VESA Standard Panel Bitmapping and Bus-Width Selection

The LVDS input has two selectable widths, 3-channel and 4-channel. The MAX9249 accepts the VESA standard panel 3- or 4-channel LVDS (Table 2). Inputs on the MAX9249 are mapped internally, according to Figures 13 and 14. In 3-channel mode, RXIN3_ and CNTL1/CNTL2 are not available. For both modes, the SD/CNTL0, SCK, and WS pins are for I^{2}S audio. The MAX9249 accepts clock rates from 8.33MHz to 104MHz for 3-channel mode and 6.25MHz to 78MHz for 4-channel mode.

Serial Link Signaling and Data Format

The MAX9249 high-speed data serial output uses CML signaling with programmable preemphasis and AC-coupling. The GMSL deserializer uses AC-coupling and programmable channel equalization. When using both the preemphasis and equalization, the MAX9249/GMSL deserializer can operate up to 3.125Gbps over STP cable lengths to 15m or more.

The MAX9249 serializer scrambles and encodes the LVDS input data and sends the 8B/10B coded signal through the serial link. The GMSL deserializer recovers

Table 2. Bus-Width Selection Using BWS

INPUT BITS	3-CHANNEL MODE (BWS = LOW)		4-CHANNEL MODE (BWS = HIGH)	
	VESA STANDARD PANEL MAPPING	AUXILIARY SIGNALS MAPPING	VESA STANDARD PANEL MAPPING	AUXILIARY SIGNALS MAPPING
DIN[0:5]	R[0:5]	—	R[0:5]	—
DIN[6:11]	G[0:5]	—	G[0:5]	—
DIN[12:17]	B[0:5]	—	B[0:5]	—
DIN[18:20]	HS, VS, DE	—	HS, VS, DE	—
DIN[21:22]	Not used	Not used	R6, R7	—
DIN[23:24]	Not used	Not used	G6, G7	—
DIN[25:26]	Not used	Not used	B6, B7	—
DIN27	Not used	Not used	RES*	CNTL1
DIN28	Not used	Not used	—	CNTL2
SD/CNTL0	—	SD/CNTL0	—	SD/CNTL0

RES = Reserved (see the Reserved Bit (RES) section for details).

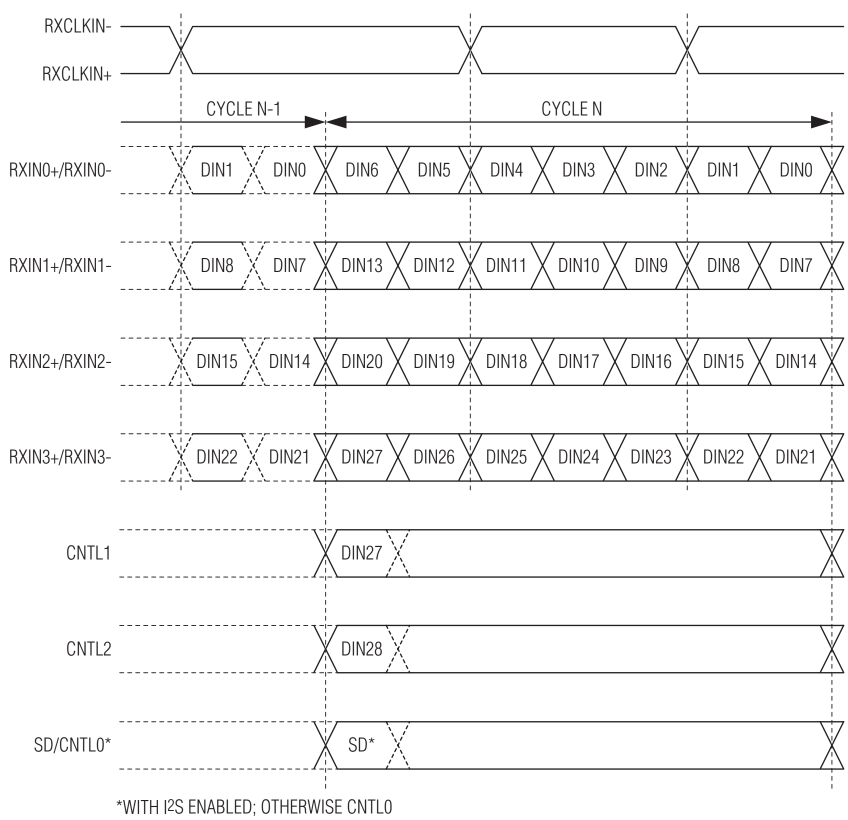


Figure 13. LVDS Input Timing

Gigabit Multimedia Serial Link Serializer with LVDS System Interface

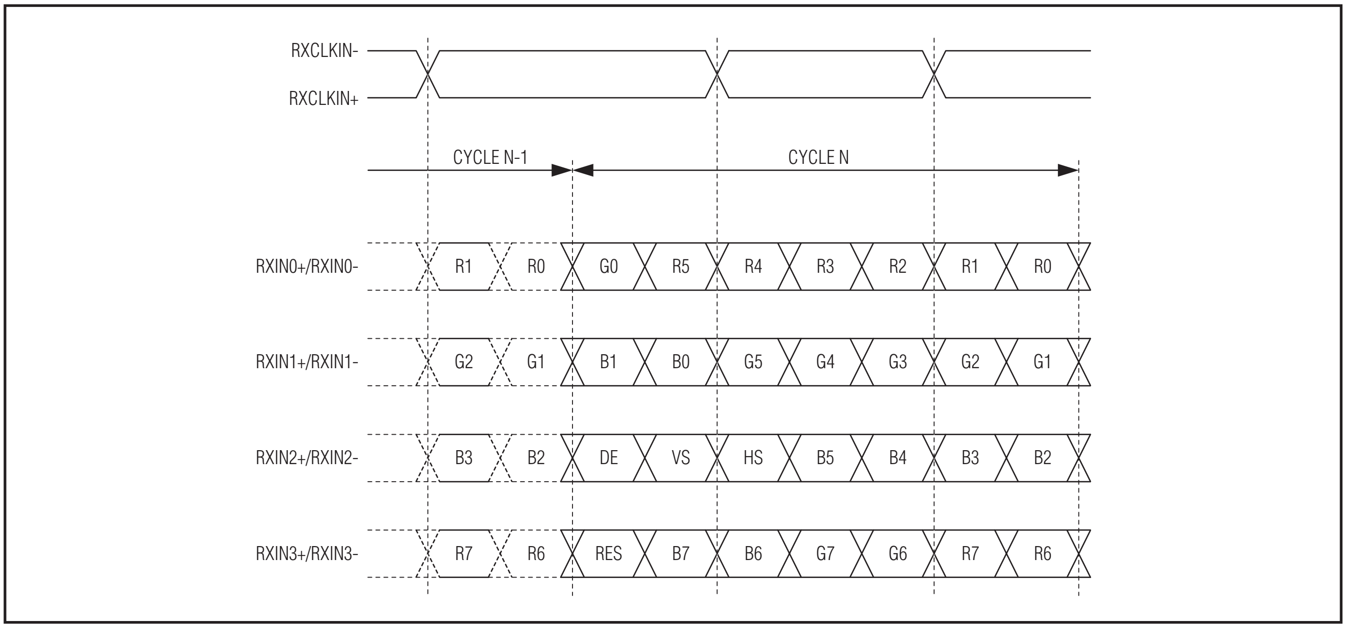


Figure 14. VESA Standard Panel Clock and Bit Assignment

the embedded serial clock and then samples, decodes, and descrambles before outputting the data. Figures 15 and 16 show the serial-data packet format before scrambling and 8B/10B coding. In 3-channel or 4-channel mode, 21 or 28 bits come from the RXIN_ _ LVDS inputs. Control bits can be mapped to DIN27 and DIN28 in 4-channel mode. The audio channel bit (ACB) contains an encoded audio signal derived from the three I²S inputs (SD/CNTL0, SCK, and WS). The forward control-channel (FCC) bit carries the forward control data. The last bit (PCB) is the parity bit of the previous 23 or 31 bits.

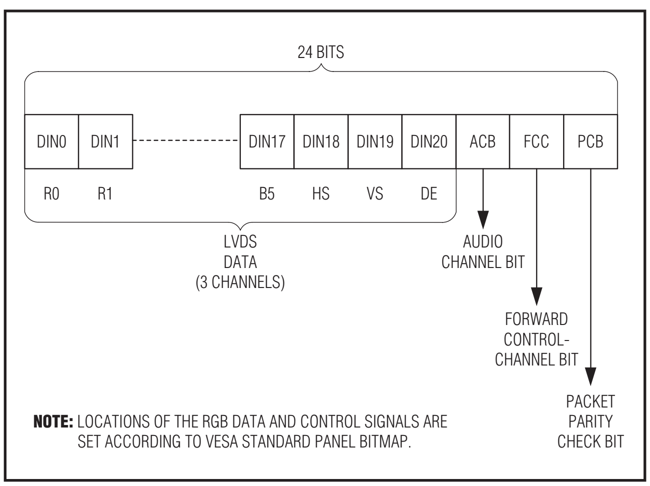


Figure 15. 3-Channel Mode Serial Link Data Format

Reserved Bit (RES)

In 4-channel mode, the MAX9249 serializes all bits of all four lanes including RES by default. Set DISRES (D4 of Register 0x0D) to 1 to map CNTL1 to DIN27 instead of RES.

Reverse Control Channel

The MAX9249 uses the reverse control channel to receive I²C/UART and interrupt signals from the GMSL deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same twisted pair forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 500µs after power-up. The MAX9249 temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Data-Rate Selection

The MAX9249 uses the DRS input to set the RXCLKIN_ frequency. Set DRS high for an RXCLKIN_ frequency of 6.25MHz to 12.5MHz (4-channel mode) or 8.33MHz to 16.66MHz (3-channel mode). Set DRS low for normal operation with an RXCLKIN_ frequency of 12.5MHz to 78MHz (4-channel mode) or 16.66MHz to 104MHz (3-channel mode).

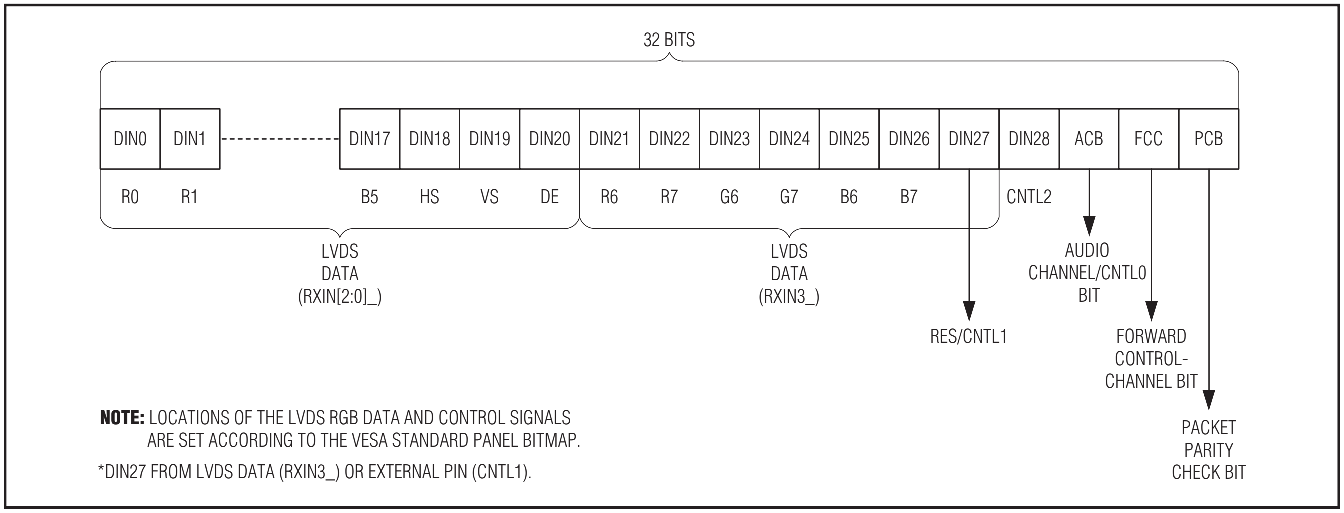


Figure 16. 4-Channel Mode Serial Link Data Format

Table 3. Maximum Audio WS Frequency (kHz) for Various RXCLKIN_ Frequencies

WORD LENGTH (BITS)	RXCLKIN_ FREQUENCY (DRS = LOW) (MHz)				RXCLKIN_ FREQUENCY (DRS = HIGH) (MHz)			
	12.5	15	16.6	> 20	6.25	7.5	8.33	> 10
8	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
16	> 192	> 192	> 192	> 192	> 192	> 192	> 192	> 192
18	185.5	> 192	> 192	> 192	185.5	> 192	> 192	> 192
20	174.6	> 192	> 192	> 192	174.6	> 192	> 192	> 192
24	152.2	182.7	> 192	> 192	152.2	182.7	> 192	> 192
32	123.7	148.4	164.3	> 192	123.7	148.4	164.3	> 192

Audio Channel

The I^2S audio channel supports audio sampling rates from 8kHz to 192kHz and audio word lengths from 4 bits to 32 bits. The audio bit clock (SCK) does not have to be synchronized with RXCLKIN_. The MAX9249 automatically encodes audio data into a single bit stream synchronous with RXCLKIN_. The GMSL deserializer decodes the audio stream and stores audio words in a FIFO. Audio rate detection uses an internal oscillator to continuously determine the audio data rate and output the audio in I^2S format. The audio channel is enabled by default. When the audio channel is disabled, the audio data on the MAX9249 and GMSL deserializer is treated as a control pin (CNTL0).

Low RXCLKIN_ frequencies limit the maximum audio sampling rate. Table 3 lists the maximum audio sampling rate for various RXCLKIN_ frequencies. Spread-spectrum settings do not affect the I^2S data rate or WS clock frequency.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. Configuring the CDS pin allows the µC to control the link from either the MAX9249 or the GMSL deserializer side to support video-display or image-sensing applications.

The control channel between the µC and MAX9249 or GMSL deserializer runs in base mode or bypass mode according to the mode selection (MS) input of the device connected to the µC. Base mode is a half-duplex control channel and the bypass mode is a full-duplex control channel. In base mode, the µC is the host and can access the registers of both the MAX9249 and GMSL deserializer from either side of the link by using the GMSL

UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the MAX9249 or GMSL deserializer, with the UART packets converted to I²C by the device on the remote side of the link (GMSL deserializer for LCD or MAX9249 for image-sensing applications). The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the MAX9249/GMSL deserializer. The device addresses of the MAX9249 and GMSL deserializer in base mode are programmable. The default values are 0x80 for the MAX9249 and 0x90 for the GMSL deserializer.

In base mode, when the peripheral interface uses I²C (default), the MAX9249/GMSL deserializer convert packets to I²C that have device addresses different from those of the MAX9249 or GMSL deserializer. The converted I²C bit rate is the same as the original UART bit rate.

In bypass mode, the MAX9249/GMSL deserializer ignore UART commands from the µC and the µC communicates with the peripherals directly using its own defined UART protocol. The µC cannot access the MAX9249/GMSL deserializer's registers in this mode. Peripherals accessed through the forward control channel using the UART interface need to handle at least one RXCLKIN_ period of jitter due to the asynchronous sampling of the UART signal by RXCLKIN_.

The MAX9249 embeds control signals going to the GMSL deserializer in the high-speed forward link. Do not send a logic-low value longer than 100µs in either base or bypass mode. The GMSL deserializer uses a proprietary differential line coding to send signals back towards the MAX9249. The speed of the control channel ranges from 100kbps to 1Mbps in both directions. The MAX9249/GMSL deserializer automatically detect the control channel bit rate in base mode. Packet bit rates can vary up to 3.5x from the previous bit rate (see the *Changing the Clock Frequency* section). Figure 17 shows the UART protocol for writing and reading in base mode between the µC and the MAX9249/GMSL deserializer.

Figure 18 shows the UART data format. Even parity is used. Figures 19 and 20 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and interrupt generate transitions on the control channel that should be ignored by the µC. Data written to the MAX9249/GMSL deserializer registers does not take effect until after the acknowledge byte is sent. This allows the µC to verify write commands received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART data rate automatically. If the INT or MS inputs of the GMSL deserializer toggles while there is control-channel communication, the control-channel communication may be corrupted. In the event of a missed acknowledge, the µC should assume there was an error in the packet when the slave device receives it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit times before starting to send a new packet.

As shown in Figure 21, the remote-side device converts the packets going to or coming from the peripherals from the UART format to the I²C format and vice versa. The remote device removes the byte number count and adds or receives the ACK between the data bytes of I²C. The I²C's data rate is the same as the UART data rate.

Interfacing Command-Byte-Only I²C Devices

The MAX9249 and GMSL deserializer UART-to-I²C conversion interfaces with devices that do not require register addresses, such as the MAX7324 GPIO expander. In this mode, the I²C master ignores the register address byte and directly reads/writes the subsequent data bytes (Figure 22). Change the communication method of the I²C master using the I2CMETHOD bit. I2CMETHOD = 1 sets command-byte-only mode, while I2CMETHOD = 0 sets normal mode where the first byte in the data stream is the register address.

Interrupt Control

The INT pin of the MAX9249 is the interrupt output and the INT pin of the GMSL deserializer is the interrupt input. The interrupt output on the MAX9249 follows the transitions at the interrupt input. This interrupt function supports remote-side functions such as touch-screen peripherals, remote power-up, or remote monitoring. Interrupts that occur during periods where the reverse control channel is disabled, such as link startup/shutdown, are automatically resent once the reverse control channel becomes available again. Bit D4 of register 0x06 in the GMSL deserializer also stores the interrupt input state. The INT output of the MAX9249 is low after power-up. In addition, the µC can set the INT output of MAX9249 by writing to the SETINT register bit. In normal operation, the state of the interrupt output changes when the interrupt input on the GMSL deserializer toggles.

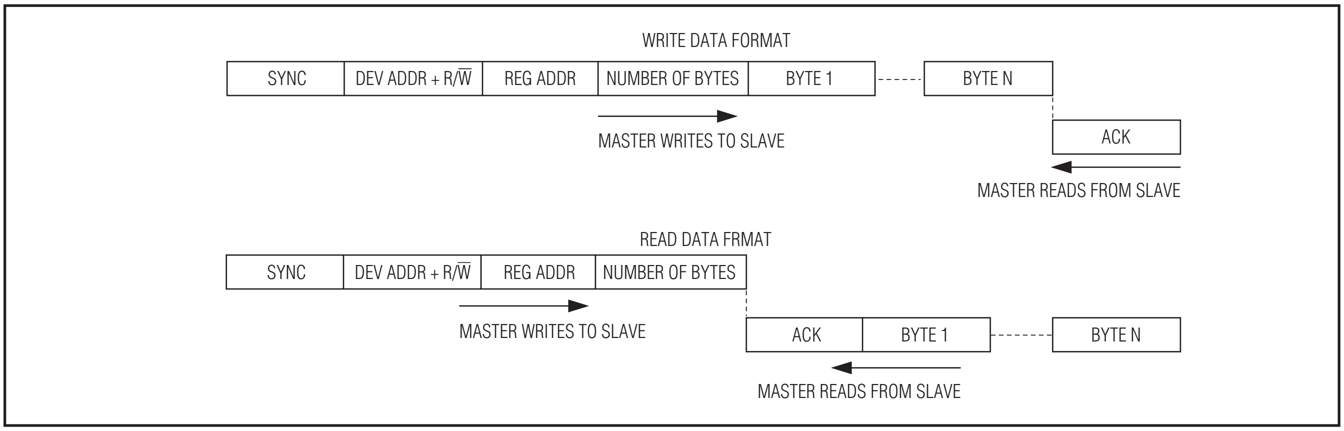


Figure 17. GMSL UART Protocol for Base Mode

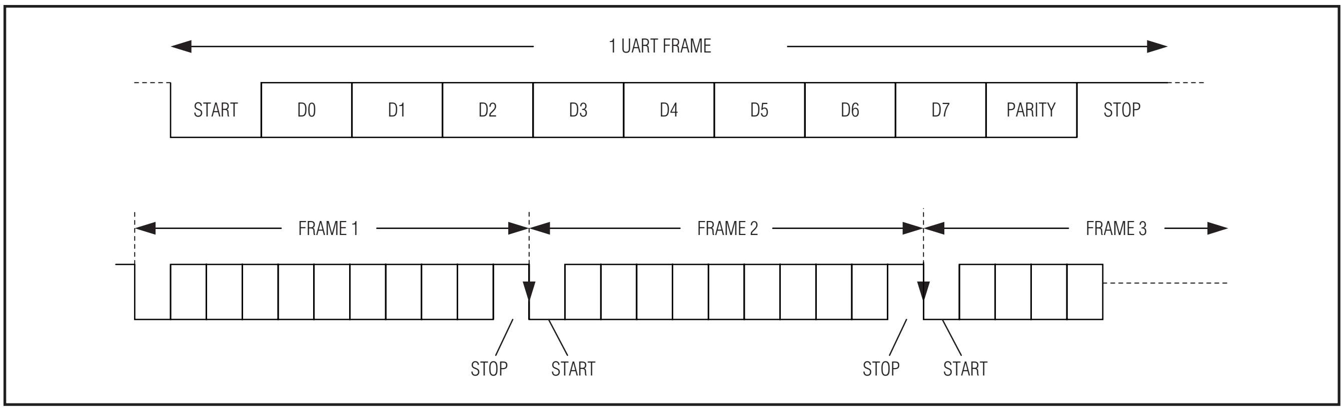


Figure 18. GMSL UART Data Format for Base Mode

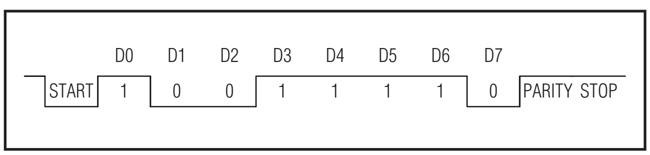


Figure 19. SYNC Byte (0x79)

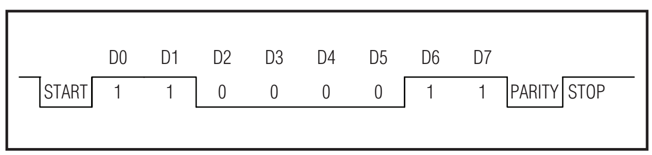


Figure 20. ACK Byte (0xC3)

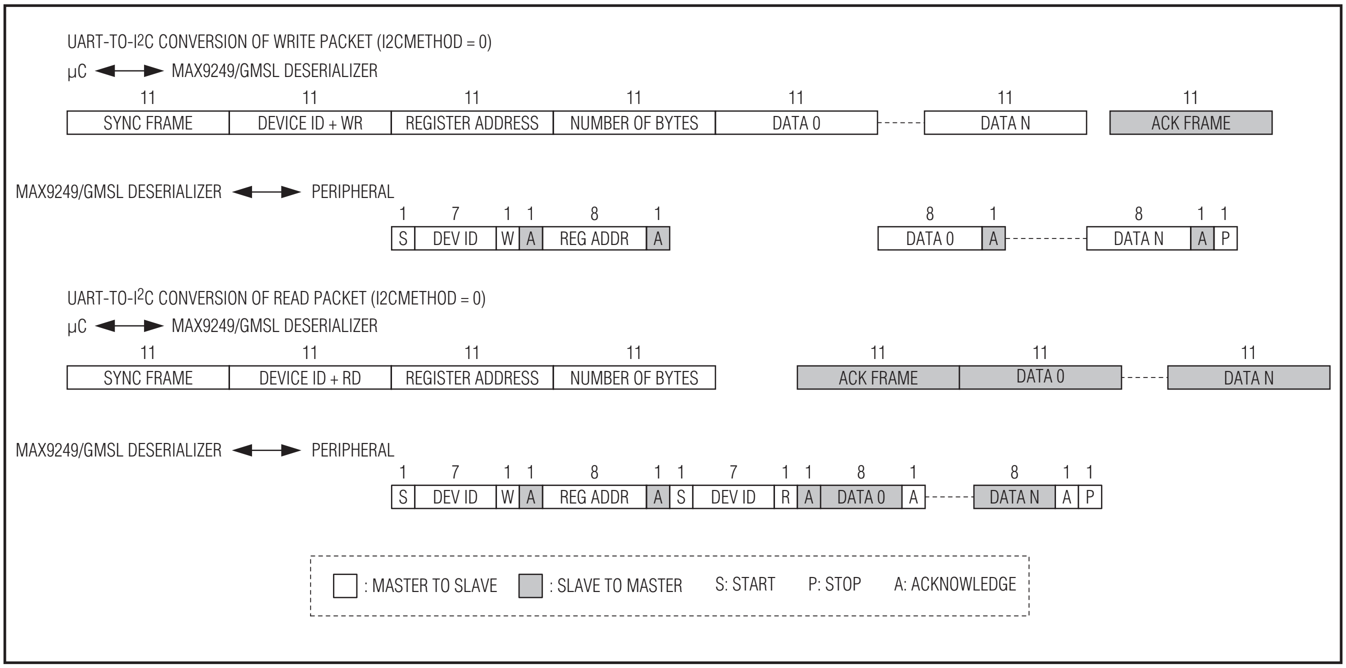


Figure 21. Format Conversion Between GMSL UART and I²C with Register Address (I2CMETHOD = 0)

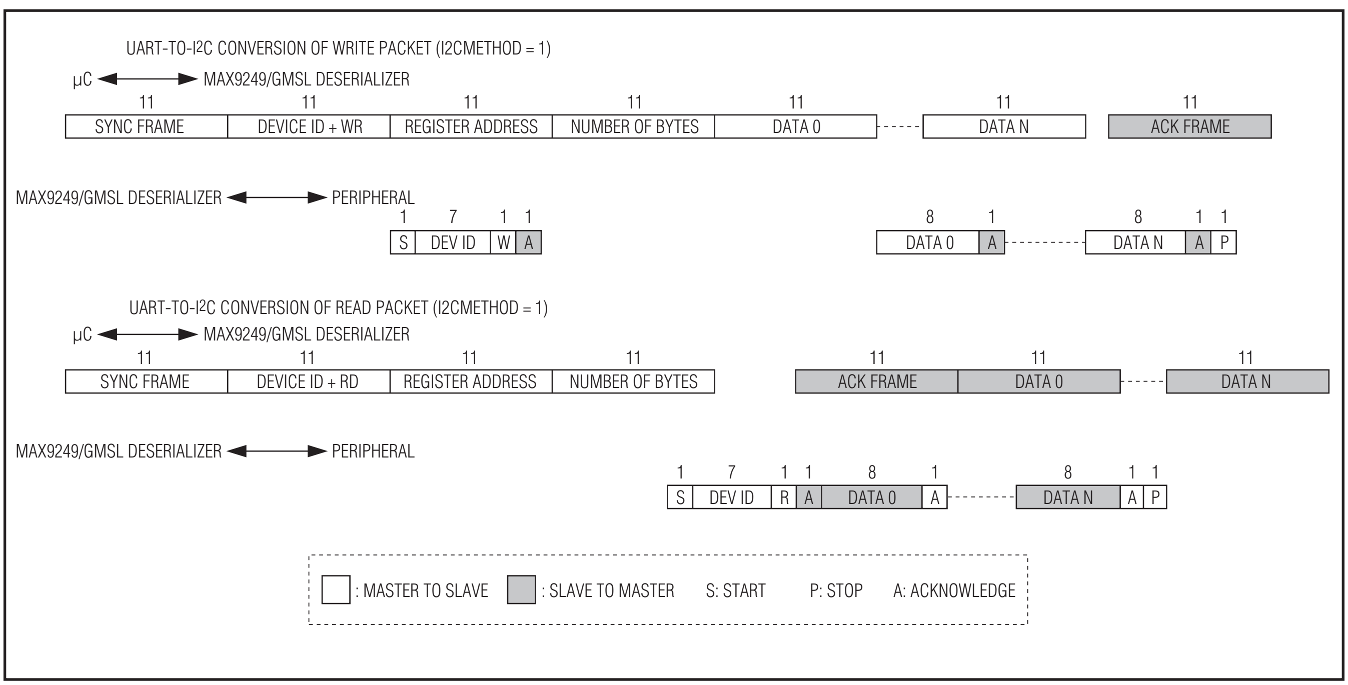


Figure 22. Format Conversion Between UART and I²C in Command-Byte-Only Mode (I2CMETHOD = 1)

Table 4. CML Driver Strength (Default Level, CMLLVL = 11)

PREEMPHASIS LEVEL (dB)*	PREEMPHASIS SETTING (0x05, D[3:0])	I_{CML} (mA)	I_{PRE} (mA)	SINGLE-ENDED VOLTAGE SWING	
				MAX (mV)	MIN (mV)
-6.0	0100	12	4	400	200
-4.1	0011	13	3	400	250
-2.5	0010	14	2	400	300
-1.2	0001	15	1	400	350
0	0000	16	0	400	400
1.1	1000	16	1	425	375
2.2	1001	16	2	450	350
3.3	1010	16	3	475	325
4.4	1011	16	4	500	300
6.0	1100	15	5	500	250
8.0	1101	14	6	500	200
10.5	1110	13	7	500	150
14.0	1111	12	8	500	100

Negative preemphasis levels denote deemphasis.

Table 5. Serial Output Spread

SS	SPREAD (%)
000	No spread spectrum. **Power-up default when SSEN = low.**
001	±0.5% spread spectrum. **Power-up default when SSEN = high.**
010	±1.5% spread spectrum
011	±2% spread spectrum
100	No spread spectrum
101	±1% spread spectrum
110	±3% spread spectrum
111	±4% spread spectrum

Preemphasis Driver

The serial line driver in the MAX9249 employs current-mode logic (CML) signaling. The driver can be programmed to generate a preemphasized waveform according to the cable length and characteristics. There are 13 preemphasis settings, as shown in Table 4. Negative preemphasis levels are deemphasis levels in which the swing is the same as normal, but the no-transition data is deemphasized. Program the preemphasis levels through register 0x05 D[3:0] of the MAX9249. This preemphasis function compensates the high-frequency loss of the cable and enables reliable transmission over longer link distances. Additionally, a lower power-drive mode can be entered by programming CMLLVL bits (0x05 D[5:4]) to reduce the driver strength down to 75% (CMLLVL = 10) or 50% (CMLLVL = 01) from 100% (CMLLVL = 11, default).

Spread Spectrum

To reduce the EMI generated by the transitions on the serial link and outputs of the GMSL deserializer, both the MAX9249 and GMSL deserializer support spread spectrum. Turning on spread spectrum on the MAX9249 spreads the serial data and the GMSL deserializer outputs. Do not enable spread for both the MAX9249 and GMSL deserializer. The six selectable spread-spectrum rates at the MAX9249 serial output are ±0.5%, ±1%, ±1.5%, ±2%, ±3%, and ±4% (Table 5). Some spread-spectrum rates can only be used at lower RXCLKIN_ frequencies (Table 6). There is no RXCLKIN_ frequency limit for the 0.5% spread rate.

Set the MAX9249 SSEN input high to select 0.5% spread at power-up and SSEN input low to select no spread at power-up. The state of SSEN is latched upon power-up or when resuming from power-down mode. Whenever the MAX9249 spread spectrum is turned on or off, the serial link automatically restarts and remains unavailable while the GMSL deserializer relocks to the serial data.

Turning on spread spectrum on the MAX9249 or GMSL deserializer does not affect the audio data stream. Changes in the MAX9249 spread settings only affect the GMSL deserializer MCLK output if it is derived from RXCLKIN_ (MCLKSRC = 0).

Table 6. Spread-Spectrum Rate Limitations

3-CHANNEL MODE RXCLKIN_ FREQUENCY (MHz)	4-CHANNEL MODE RXCLKIN_ FREQUENCY (MHz)	SERIAL LINK BIT RATE (Mbps)	AVAILABLE SPREAD RATES
< 33.3	< 25	< 1000	All rates available
33.3 to < 66.7	20 to < 50	1000 to < 2000	1.5%, 1.0%, 0.5%
≥ 66.7	≥ 50	≥ 2000	0.5%

Table 7. Modulation Coefficients and Maximum SDIV Settings

BUS-WIDTH MODE	SPREAD-SPECTRUM SETTING (%)	MODULATION COEFFICIENT (DECIMAL)	SDIV UPPER LIMIT (DECIMAL)
4-Channel	0.5	104	63
	1	104	40
	1.5	152	54
	2	204	30
	3	152	27
	4	204	15
3-Channel	0.5	80	63
	1	80	52
	1.5	112	63
	2	152	42
	3	112	37
	4	152	21

Both devices include a sawtooth divider to control the spread-modulation rate. Autodetection or manual programming of the RXCLKIN_ operation range guarantees a spread-spectrum modulation frequency within 20kHz to 40kHz. Additionally, manual configuration of the sawtooth divider (SDIV, 0x03 D[5:0]) allows the user to set a modulation frequency according to the RXCLKIN_ frequency. Always keep the modulation frequency between 20kHz to 40kHz to ensure proper operation.

Manual Programming of the Spread-Spectrum Divider

The modulation rate for the MAX9249 relates to the RXCLKIN_ frequency as follows:

$$f_M = (1 + DRS)\frac{f_{RXCLKIN\_}}{MOD \times SDIV}$$

where:

f_M = Modulation frequency

DRS = DRS pin input value (0 or 1)

$f_{RXCLKIN\_}$ = LVDS clock frequency

MOD = Modulation coefficient given in Table 7

SDIV = 6-bit SDIV setting, manually programmed by the µC

To program the SDIV setting, first look up the modulation coefficient according to the part number and desired bus-width and spread-spectrum settings. Solve the above equation for SDIV using the desired pixel clock and modulation frequencies. If the calculated SDIV value is larger than the maximum allowed SDIV value in Table 7, set SDIV to the maximum value.

Sleep Mode

The MAX9249/GMSL deserializer include low-power sleep mode to reduce power consumption on the device not attached to the µC (the GMSL deserializer in LCD applications and the MAX9249 in camera applications). Set the corresponding remote IC's SLEEP bit to 1 to initiate sleep mode. The MAX9249 sleeps immediately after

Table 8. Startup Selection for Video-Display Applications (CDS = Low)

CASE	$\overline{\text{AUTOS}}$ (MAX9249)	MAX9249 POWER-UP STATE	MS (GMSL DESERIALIZER)	GMSL DESERIALIZER POWER-UP STATE	LINK STARTUP MODE
1	Low	Serialization enabled	Low	Normal (SLEEP = 0)	Both devices power up with serial link active (autostart)
2	High	Serialization disabled	High	Sleep mode (SLEEP = 1)	Serial link is disabled and the GMSL deserializer powers up in sleep mode. Set SEREN = 1 or CLINKEN = 1 in the MAX9249 to start the serial link and wake up the GMSL deserializer.
3	High	Serialization disabled	Low	Normal (SLEEP = 0)	Both devices power up in normal mode with the serial link disabled. Set SEREN = 1 or CLINKEN = 1 in the MAX9249 to start the serial link.
4	Low	Serialization enabled	High	Sleep mode (SLEEP = 1)	GMSL deserializer starts in sleep mode. Link autostarts upon MAX9249 power-up. Use this case when the GMSL deserializer powers up before the MAX9249.

setting its SLEEP = 1. The GMSL deserializer sleeps after serial link inactivity or 8ms (whichever arrives first) after setting its SLEEP = 1. See the *Link Startup Procedure* section for details on waking up the device for different µC and starting conditions.

The µC side device cannot enter into sleep mode. If an attempt is made to program the µC side device for sleep, the SLEEP bit remains 0. Use the $\overline{\text{PWDN}}$ input pin to bring the µC side device into a low-power state.

Configuration Link Mode

The MAX9249 includes a low-speed configuration link to allow control-data connection between the two devices in the absence of a valid clock input. In either display or camera applications, the configuration link can be used to program equalizer/preemphasis or other registers before establishing the video link. An internal oscillator provides RXCLKIN_ for establishing the serial configuration link between the MAX9249 and GMSL deserializer. Set CLINKEN = 1 on the MAX9249 to turn on the configuration link. The configuration link remains active as long as the video link has not been enabled. The video link overrides the configuration link and attempts to lock when SEREN = 1.

Link Startup Procedure

Table 8 lists four startup cases for video-display applications. Table 9 lists two startup cases for image-sensing applications. In either video-display or image-sensing applications, the control link is always available after the high-speed data link or the configuration link is established and the MAX9249/GMSL deserializer registers or the peripherals are ready for programming.

Video-Display Applications

For the video-display application, with a remote display unit, connect the µC to the serializer (MAX9249) and set CDS = low for both the MAX9249 and GMSL deserializer. Table 8 summarizes the four startup cases based on the settings of $\overline{\text{AUTOS}}$ and MS.

Case 1: Autostart Mode

After power-up or when $\overline{\text{PWDN}}$ transitions from low to high for both the serializer and deserializer, the serial link establishes if a stable RXCLKIN_ is present. The MAX9249 locks to RXCLKIN_ and sends the serial data to the GMSL deserializer. The GMSL deserializer then detects activity on the serial link and locks to the input serial data.