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19-1044; Rev 1; 3/09

EVALUATION KIT AVAILABLE

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

General Description

The MAX9257 serializer pairs with the MAX9258 deserializer to form a complete digital video serial link. The MAX9257/MAX9258 feature programmable parallel data width, parallel clock frequency range, spread spectrum, and preemphasis. An integrated control channel transfers data bidirectionally at power-up during video blanking over the same differential pair used for video data. This feature eliminates the need for external CAN or LIN interface for diagnostics or programming. The clock is recovered from input serial data at MAX9258, hence eliminating the need for an external reference clock.

The MAX9257 serializes 10, 12, 14, 16, and 18 bits with the addition of two encoding bits for AC-coupling. The MAX9258 deserializer links with the MAX9257 to deserialize a maximum of 20 (data + encoding) bits per pixel/parallel clock period for a maximum serial-data rate of 840Mbps. The word length can be adjusted to accommodate a higher pixel/parallel clock frequency. The pixel clock can vary from 5MHz to 70MHz, depending on the serial-word length. Enabling parity adds two parity bits to the serial word. The encoding bits reduce ISI and allow AC-coupling.

The MAX9258 receives programming instructions from the electronic control unit (ECU) during the control channel and transmits to the MAX9257 over the serial video link. The instructions can program or update the MAX9257, MAX9258, or an external peripheral device, such as a camera. The MAX9257 communicates with the peripheral device with I²C or UART.

The MAX9257/MAX9258 operate from a +3.3V core supply and feature separate supplies for interfacing to +1.8V to +3.3V logic levels. These devices are available in 40-lead TQFN or 48-pin LQFP packages. These devices are specified over the -40°C to +105°C temperature range.

Applications

Automotive Cameras

Industrial Cameras

Navigation Systems Display

In-Vehicle Entertainment Systems

Features

- **10/12/14/16/18-Bit Programmable Parallel Data Width**
- **MAX9258 Does Not Require Reference Clock**
- **Parity Protection for Video and Control Channels**
- **Programmable Spread Spectrum**
- **Programmable Rising or Falling Edge for HSYNC, VSYNC, and Clock**
- **Up to 10 Remotely Programmable GPIO on MAX9257**
- **Automatic Resynchronization in Case of Loss of Lock**
- **MAX9257 Parallel Clock Jitter Filter PLL with Bypass**
- **DC-Balanced Coding Allows AC-Coupling**
- **5 Levels of Preemphasis for Up to 20m STP Cable Drive**
- **Integrity Test Using On-Chip Programmable PRBS Generator and Checker**
- **LVDS I/O Meet ISO 10605 ESD Protection (±10kV Contact and ±30kV Air Discharge)**
- **LVDS I/O Meet IEC 61000-4-2 ESD Protection (±8kV Contact and ±20kV Air Discharge)**
- **LVDS I/O Meet ±200V Machine Model ESD Protection**
- **-40°C to +105°C Operating Temperature Range**
- **Space-Saving, 40-Pin TQFN (5mm x 5mm) with Exposed Pad or 48-Pin LQFP Packages**
- **+3.3V Core Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9257GTL/V+	-40°C to +105°C	40 TQFN-EP*
MAX9257GCM/V+	-40°C to +105°C	48 LQFP
MAX9258GCM/V+	-40°C to +105°C	48 LQFP

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit and Pin Configurations appear at end of data sheet.

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND .....-0.5V to +4.0V
Any Ground to Any Ground.....-0.5V to +0.5V
SDI+, SDI-, SDO+, SDO- to GND.....-0.5V to +4.0V
SDO+, SDO- Short Circuit to GND or V_{CCLVDS} .....Continuous
DIN[0:15], GPIO[0:9], PCLK_IN, HSYNC_IN, VSYNC_IN, SCL/TX, SDA/RX, REM to GND .....-0.5V to (V_{CCIO} + 0.5V)
DOUT[0:15], PCLK_OUT, HSYNC_OUT, VSYNC_OUT, RX, LOCK, TX, $\overline{PD}$, $\overline{ERROR}$ to GND .....-0.5V to (V_{CCOUT} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
40-Lead TQFN
Multilayer PCB (derate 35.7mW/°C above +70°C) 2857mW
48-Lead LQFP
Multilayer PCB (derate 21.7mW/°C above +70°C) 1739mW
Junction-to-Case Thermal Resistance (θ_{JC}) (Note 1)
40-Lead TQFN .....1.7°C/W
48-Lead LQFP.....10°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
40-Lead TQFN .....28°C/W
48-Lead LQFP.....46°C/W
ESD Protection
Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
All Pins to GND .....±3kV
IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
Contact Discharge
(SDI+, SDI-, SDO+, SDO-) to GND.....±8kV
Air Discharge
(SDI+, SDI-, SDO+, SDO-) to GND.....±20kV
ISO 10605 (R_D = 2kΩ, C_S = 330pF)
Contact Discharge
(SDI+, SDI-, SDO+, SDO-) to GND.....±10kV
Air Discharge
(SDI+, SDI-, SDO+, SDO-) to GND.....±30kV
Machine Model (R_D = 0Ω, C_S = 200pF)
All Pins to GND .....±200V
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JDEC specification JESD51-7, using a 4-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX9257 DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS						
High-Level Input Voltage	V_{IH}	V_{CCIO} = +1.71V to +3V	0.65 x V_{CCIO}		V_{CCIO} + 0.3	V
		V_{CCIO} = +3V to +3.6V	2		V_{CCIO} + 0.3	
		REM input	2		V_{CC} + 0.3	
Low-Level Input Voltage	V_{IL}	V_{CCIO} = +1.71V to +3V	0		0.3 x V_{CCIO}	V
		V_{CCIO} = +3V to +3.6V	0		0.8	
		REM input	0		0.8	
Input Current	I_{IN}	V_{IN} = 0 to V_{CCIO}, V_{CCIO} = +1.71V to +3.6V	-20		+20	µA
		V_{IN} = 0 to V_{CC}, REM input	-20		+20	
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA			-1.5	V
SINGLE-ENDED OUTPUTS						
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA	V_{CCIO} - 0.1			V
		I_{OH} = -2mA	V_{CCIO} - 0.35			

MAX9257 DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA			0.1	V
		I_{OL} = 2mA			0.3	
Output Short-Circuit Current	I_{OS}	Shorted to GND	-44		-10	mA
		Shorted to $V_{CC\_}$	10		44	
I²C/UART I/O						
Input Leakage Current	I_{ILKG}	V_I = V_{CC}	-1		+1	µA
High-Level Input Voltage SDA/RX	V_{IH2}		0.7 x V_{CC}			V
Low-Level Input Voltage SDA/RX	V_{IL2}				0.3 x V_{CC}	V
Low-Level Output Voltage SCL, SDA	V_{OL2}	R_{PULLUP} = 1.6kΩ			0.4	V
LVDS OUTPUTS (SDO+, SDO-)						
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)	250	350	460	mV
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				20	mV
Common-Mode Voltage	V_{OS}		1.050	1.25	1.375	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}				20	mV
Output Short-Circuit Current	I_{OS}	V_{SDO+} or V_{SDO-} = 0 or 3.6V	-15		+15	mA
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0			15	mA
CONTROL CHANNEL TRANSCEIVER						
Differential Output Voltage	V_{OD}		250	350	460	mV
Input Hysteresis (Figure 2)	V_{HYST+}	Differential low-to-high threshold	25	90	135	mV
	V_{HYST-}	Differential high-to-low threshold	-25	-90	-135	

MAX9257 DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Worst-Case Supply Current (Figure 3) C_L = 8pF, 12 bits	I_{CCW}	±2% spread, preemphasis off, PRATE = 60MHz, SRATE = 840Mbps		104	126	mA
		No spread, preemphasis off, PRATE = 60MHz, SRATE = 840Mbps		99	121	
		No spread, preemphasis = 20%, PRATE = 60MHz, SRATE = 840Mbps		99	120	
		No spread, preemphasis = 60%, PRATE = 60MHz, SRATE = 840Mbps		108	127	
		No spread, preemphasis = 100%, PRATE = 60MHz, SRATE = 840Mbps		110	129	
		±2% spread, preemphasis off, PRATE = 28.57MHz, SRATE = 400Mbps		78	96	
		No spread, preemphasis off, PRATE = 28.57MHz, SRATE = 400Mbps		77	94	
		No spread, preemphasis = 100%, PRATE = 28.57MHz, SRATE = 400Mbps		86	105	
		±2% spread, preemphasis off, PRATE = 14.29MHz, SRATE = 200Mbps		55	68	
		No spread, preemphasis off, PRATE = 14.29MHz, SRATE = 200Mbps		54	67	
		No spread, preemphasis = 100%, PRATE = 14.29MHz, SRATE = 200Mbps		59	73	
		±2% spread, preemphasis off, PRATE = 7.14MHz, SRATE = 100Mbps		44	55	
		No spread, preemphasis off, PRATE = 7.14MHz, SRATE = 100Mbps		43	54	
		No spread, preemphasis = 100%, PRATE = 7.14MHz, SRATE = 100Mbps		46	57	
		±2% spread, preemphasis off, PRATE = 5MHz, SRATE = 70Mbps		34	43	
		No spread, preemphasis off, PRATE = 5MHz, SRATE = 70Mbps		34	42	
		No spread, preemphasis = 100%, PRATE = 5MHz, SRATE = 70Mbps		36	45	
Sleep Mode Supply Current	I_{CCS}	Sleep mode			92	µA

MAX9257 AC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 5, 9)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PCLK_IN TIMING REQUIREMENTS							
Clock Period	t_T			14.28		200.00	ns
Clock Frequency	f_{CLK}	$1/t_T$		5		70	MHz
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T		35	50	65	%
Clock Transition Time	t_R, t_F	(Figure 7)				4	ns
SWITCHING CHARACTERISTICS							
LVDS Output Rise Time	t_R	20% to 80% (Figure 4)			315	370	ps
LVDS Output Fall Time	t_F	20% to 80% (Figure 4)			315	370	ps
Control Transceiver Transition Time	t_{R1A}, t_{F1A}	20% to 80% (Figure 16)		642	970	1390	ps
	t_{R2}, t_{F2}			810	1140	1420	
	t_{R1B}, t_{F1B}			290	386	490	
Input Setup Time	t_S	(Figure 5)		0			ns
Input Hold Time	t_H	(Figure 5)		3			ns
Parallel-to-Serial Delay	t_{PSD1}	Spread off (Figure 6)				$(4.55 \times t_T) + 11$	ns
	t_{PSD2}	±4% spread				$(36.55 \times t_T) + 11$	
PLL Lock Time	t_{LOCK}	Combined FPLL and SPLL; PCLK_IN stable				$32,768 \times t_T$	ns
Random Jitter	t_{RJ}	420MHz LVDS output, spread off, FPLL = bypassed				12	ps (RMS)
Deterministic Jitter	t_{DJ}	2^{18} - 1 PRBS, SRATE = 840Mbps, 18 bits, no spread				142	ps (P-P)
SCL/TX, SDA/RX							
Rise Time	t_{RS}	0.3 x V_{CC} to 0.7 x V_{CC}, C_L = 30pF	R_{PULLUP} = 10kΩ			400	ns
			R_{PULLUP} = 1.6kΩ			60	
Fall Time	t_{FS}	0.7 x V_{CC} to 0.3 x V_{CC}, C_L = 30pF				40	ns
Pulse Width of Spike Suppressed in SDA	t_{SPK}	95kbps to 400kbps		100			ns
		400kbps to 1000kbps		50			
		1000kbps to 4250kbps		10			
		DC to 10Mbps (bypass mode)		10			
Data Setup Time	t_{SETUP}	400kbps		100			ns
		4.25Mbps, C_L = 10pF		60			
Data Hold Time	t_{HOLD}	400kbps		100			ns
		4.25Mbps, C_L = 10pF		0			
I²C TIMING (Note 8)							
Maximum SCL Clock Frequency	f_{SCL}				4.25		MHz
Minimum SCL Clock Frequency	f_{SCL}				95		kHz
Start Condition Hold Time	$t_{HD:STA}$	(Figure 30)		0.6			µs

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

MAX9257 AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, T_A = +25°C.) (Notes 5, 9)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Period of SCL Clock	t_{LOW}	(Figure 30)	1.1			µs
High Period of SCL Clock	t_{HIGH}	(Figure 30)	0.6			µs
Repeated START Condition Setup Time	$t_{SU:STA}$	(Figure 30)	0.5			µs
Data Hold Time	$t_{HD:DAT}$	(Figure 30)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Figure 30)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$	(Figure 30)	0.5			µs
Bus Free Time	t_{BUF}	(Figure 30)	1.1			µs

MAX9258 DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS							
High-Level Input Voltage	V_{IH}			2.0		V_{CC}	V
Low-Level Input Voltage	V_{IL}			0		0.8	V
Input Current	I_{IN}	V_{IN} = 0 to V_{CC}	TXIN	-60		+60	µA
			$\overline{PD}$	-20		+20	
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUTS							
High-Level Output Voltage	V_{OH}	I_{OH} = -100µA		V_{CCOUT} - 0.1			V
		I_{OH} = -2mA		V_{CCOUT} - 0.35			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100µA				0.1	V
		I_{OL} = 2mA				0.3	
High-Impedance Output Current	I_{OZ}	$\overline{PD}$ = low, V_O = 0 to V_{CCOUT}		-1		+1	µA
Output Short-Circuit Current	I_{OS}	V_O = 0V (Note 4)		-16		-65	mA
		PCLK_OUT, V_O = 0V		-22		-80	
OPEN-DRAIN OUTPUTS							
Output Low Voltage	V_{OL}	V_{CCOUT} = +3V, I_{OL} = 6.4mA				0.55	V
Output Low Voltage	V_{OL}	V_{CCOUT} = +1.71V, I_{OL} = 1.95mA				0.3	V
Leakage Current	I_{LEAK}	V_O = 0 or V_{CC}				1	µA
LVDS INPUTS (SDI+, SDI-)							
Differential Input High Threshold	V_{TH}					50	mV
Differential Input Low Threshold	V_{TL}			-50			mV
Input Current	I_{IN+}, I_{IN-}			-60		+60	µA
Power-Off Input Current	I_{INO+}, I_{INO-}	$V_{CC\_}$ = 0 or open		-70		+70	µA
CONTROL CHANNEL TRANSCEIVER							
Differential Output Voltage	V_{OD}			250		460	mV

MAX9258 DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, differential input voltage $|V_{ID}|$ = 0.05V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Hysteresis (Figure 2)	V_{HYST+}	Differential low-to-high threshold	25	90	135	mV
	V_{HYST-}	Differential high-to-low threshold	-25	-90	-135	
POWER SUPPLY						
Worst-Case Supply Current C_L = 8pF, 12 bits (Figure 8)	I_{CCW}	±4% spread, PRATE = 60MHz, SRATE = 840Mbps		85	128	mA
		Spread off, PRATE = 60MHz, SRATE = 840Mbps		71	115	
		±4% spread, PRATE = 28.57MHz, SRATE = 400Mbps		67	102	
		Spread off, PRATE = 28.57MHz, SRATE = 400Mbps		57	84	
		±4% spread, PRATE = 14.29MHz, SRATE = 200Mbps		55	82	
		Spread off, PRATE = 14.29MHz, SRATE = 200Mbps		46	67	
		±4% spread, PRATE = 5MHz, SRATE = 70Mbps		42	57	
		Spread off, PRATE = 5MHz, SRATE = 70Mbps		34	49	
Power-Down Supply Current	I_{CCZ}	$\overline{PD}$ = low		10	50	µA

MAX9258 AC ELECTRICAL CHARACTERISTICS

$V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, C_L = 8pF, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C. (Notes 5, 6, and 7)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
Output Transition Time	t_R, t_F	(Figure 9)	0.7		2.2	ns
Output Transition Time, PCLK_OUT	t_R, t_F	(Figure 9)	0.5		1.5	ns
Output Transition Time	t_R, t_F	V_{CCOUT} = 1.71V (Figure 9)	1.0		2.8	ns
Output Transition Time, PCLK_OUT	t_R, t_F	V_{CCOUT} = 1.71V (Figure 9)	0.7		2.2	ns
Control Channel Transition Time	t_{R1A}, t_{F1A}, t_{R1B}, t_{F1B}	(Figure 16)	0.5		1.2	ns
Control Channel Transition Time	t_{R2}, t_{F2}	(Figure 16)	0.6		1.3	ns
PCLK_OUT High Time	t_{HIGH}	(Figure 10)	0.4 x t_T		0.6 x t_T	ns
PCLK_OUT Low Time	t_{LOW}	(Figure 10)	0.4 x t_T		0.6 x t_T	ns

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

MAX9258 AC ELECTRICAL CHARACTERISTICS (continued)

$V_{CC\_}$ = +3.0V to +3.6V, R_L = 50Ω ±1%, C_L = 8pF, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to V_{CC} - $|V_{ID}/2|$, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at $V_{CC\_}$ = +3.3V, $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, T_A = +25°C. (Notes 5, 6, and 7)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Valid Before PCLK_ OUT	t_{DVB}	(Figure 11)		0.35 x t_T			ns
Data Valid After PCLK_OUT	t_{DVA}	(Figure 11)		0.35 x t_T			ns
Serial-to-Parallel Delay	t_{SPD1}	Spread off (Figure 14)				$8t_T$	ns
	t_{SPD2}	±4% spread				$40t_T$	
Power-Up Delay	t_{PUD}	(Figure 12)				100	ns
Power-Down to High Impedance	t_{PDD}	(Figure 13)				100	ns
Jitter Tolerance	t_{JT}	Each half of the UI, 12 bit, SRATE = 840Mbps, PRBS pattern (Figure 15)	No spread	0.25	0.30		UI

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except V_{TH} and VTL.

Note 3: Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at T_A = +105°C.

Note 4: One output at a time.

Note 5: AC parameters are guaranteed by design and characterization, and are not production tested.

Note 6: C_L includes probe and test jig capacitance.

Note 7: t_T is the period of the PCLK_OUT.

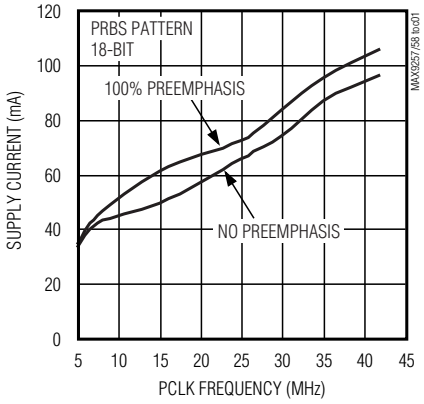
Note 8: For high-speed mode timing, see the *Detailed Description* section.

Note 9: I²C timing parameters are specified for fast-mode I²C. Max data rate = 400kbps.

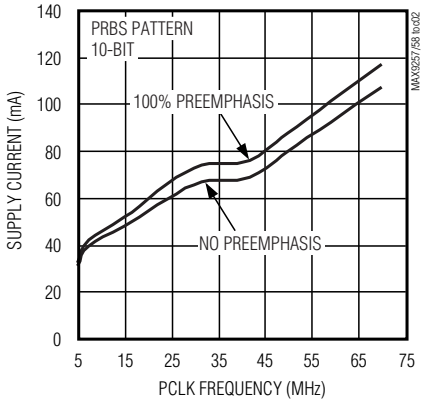
Typical Operating Characteristics

($V_{CC\_}$ = +3.3V, R_L = 50Ω, C_L = 8pF, T_A = +25°C, unless otherwise noted.)

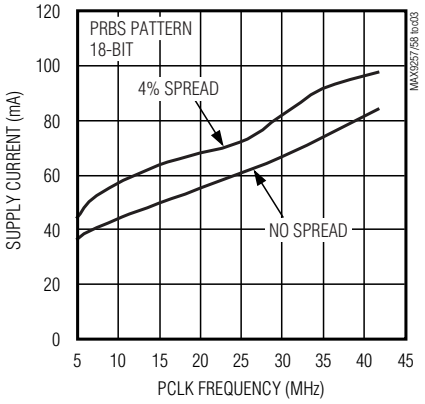
MAX9257 SUPPLY CURRENT vs. FREQUENCY



MAX9257 SUPPLY CURRENT vs. FREQUENCY



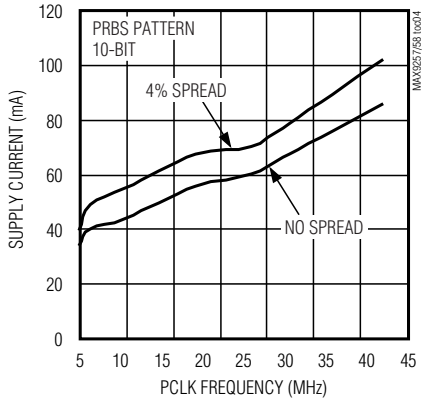
MAX9258 SUPPLY CURRENT vs. FREQUENCY



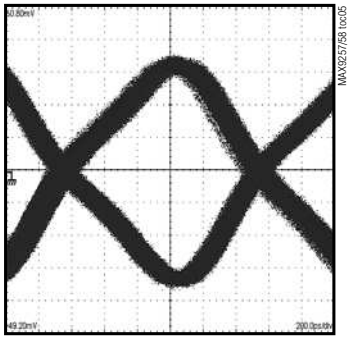
Typical Operating Characteristics (continued)

($V_{CC\_}$ = +3.3V, R_L = 50Ω, C_L = 8pF, T_A = +25°C, unless otherwise noted.)

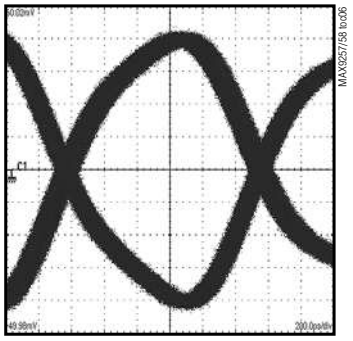
MAX9258 SUPPLY CURRENT vs. FREQUENCY



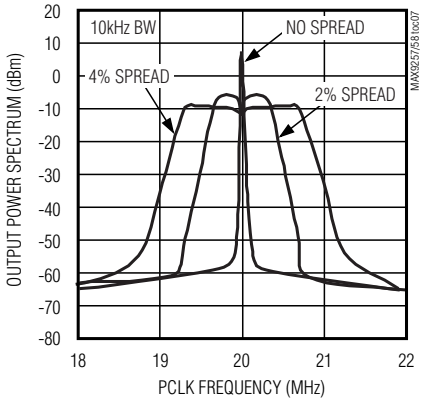
SERIAL LINK SWITCHING PATTERN WITHOUT PREEMPHASIS (BIT RATE = 840MHz, 2m STP CABLE)



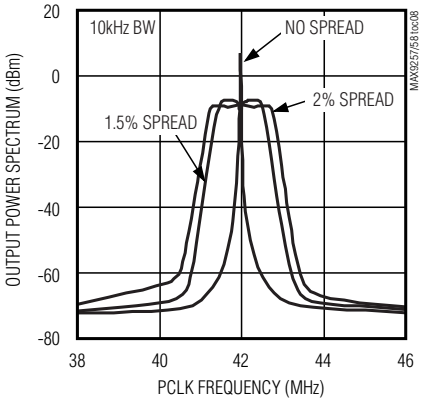
SERIAL LINK SWITCHING PATTERN WITH PREEMPHASIS (BIT RATE = 840MHz, 2m STP CABLE) (PREEMPHASIS = 100%)



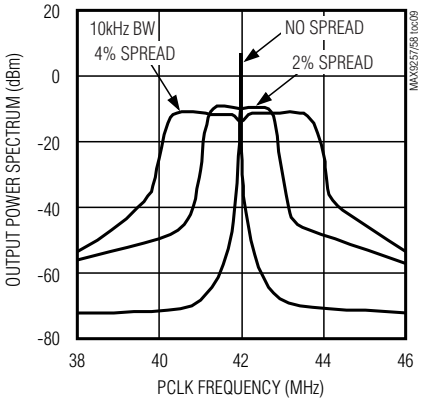
MAX9257 OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY



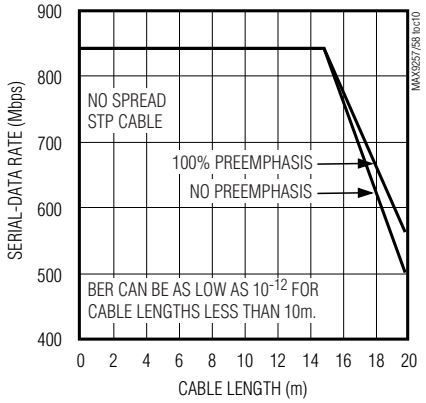
MAX9257 OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY



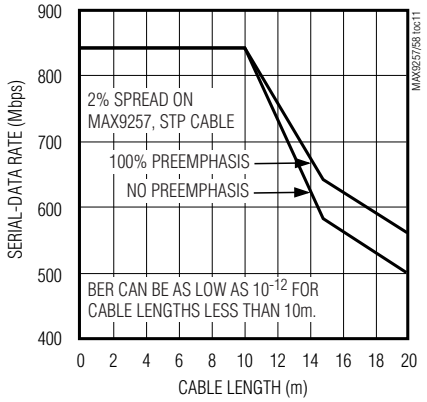
MAX9258 OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY



BIT ERROR RATE (< 10^{-9}) vs. CABLE LENGTH



BIT ERROR RATE (< 10^{-9}) vs. CABLE LENGTH



Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

MAX9257 Pin Description

PIN		NAME	FUNCTION
TQFN	LQFP		
1, 18	2, 21	V_{CCIO}	Single-Ended Input/Output Buffer Supply Voltage. Bypass V_{CCIO} to GND with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCIO}.
2, 11, 19, 34	3, 14, 22, 41	GND	Digital Supply Ground
3–8	4–9	DIN[9:14]/ GPIO[1:6]	Data Input/General Purpose Input/Output. When a serial-data word is less than 18 bits word length, DIN_ not programmed as data inputs becomes GPIO (Table 22). DIN[9:14] are internally pulled down to ground.
9	10	GND_{FPLL}	Filter PLL Ground
10	11	V_{CCFPLL}	Filter PLL Supply Voltage. Bypass V_{CCFPLL} to GND_{FPLL} with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCFPLL}.
12	15	DIN15/GPIO7	Data Input/General Purpose Input/Output. When a serial-data word is less than 18 bits word length, DIN_ not programmed as data input becomes GPIO (Table 22). DIN15 is internally pulled down to ground.
13	16	HSYNC_IN	Horizontal SYNC Input. HSYNC_IN is internally pulled down to ground.
14	17	VSYNC_IN	Vertical SYNC Input. VSYNC_IN is internally pulled down to ground.
15	18	PCLK_IN	Parallel Clock Input. PCLK_IN latches data and sync inputs and provides the PLL reference clock. PCLK_IN is internally pulled down to ground.
16	19	SCL/TX	Open-Drain Control Channel Output. SCL/TX becomes SCL output when UART-to-I²C is active. SCL/TX becomes TX output when UART-to-I²C is bypassed. Externally pull up to V_{CC}.
17	20	SDA/RX	Open-Drain Control Channel Input/Output. SDA/RX becomes bidirectional SDA when UART-to-I²C is active. SDA/RX becomes RX input when UART-to-I²C is bypassed. SDA output requires a pullup to V_{CC}.
20, 33	23, 40	V_{CC}	Digital Supply Voltage. Bypass V_{CC} to ground with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CC}.
21	26	GPIO8	General Purpose Input/Output
22	27	GPIO9	General Purpose Input/Output
23	28	V_{CCSPLL}	Spread PLL Supply Voltage. Bypass V_{CCSPLL} to GND_{SPLL} with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCSPLL}.
24	29	GND_{SPLL}	SPLL Ground
25	30	GND_{LVDS}	LVDS Ground
26	31	SDO-	Serial LVDS Inverting Output
27	32	SDO+	Serial LVDS Noninverting Output
28	33	V_{CCLVDS}	LVDS Supply Voltage. Bypass V_{CCLVDS} to GND_{LVDS} with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCLVDS}.

MAX9257 Pin Description (continued)

PIN		NAME	FUNCTION
TQFN	LQFP		
29	34	REM	Remote Power-Up/Power-Down Select Input. Connect REM to ground for power-up to follow V_{CC}. Connect REM high to V_{CC} through 10kΩ resistor for remote power-up. REM is internally pulled down to GND.
30, 31, 32, 35–39	35, 38, 39, 42–46	DIN[0:7]	Data Inputs. DIN[0:7] are internally pulled down to ground.
40	47	DIN8/GPIO0	Data Input/General Purpose Input/Output. When a serial-data word is less than 18 bits word length, DIN_ not programmed as data input becomes GPIO (Table 22). DIN8 is internally pulled down to ground.
—	1, 12, 13 24, 25, 36, 37, 48	N.C.	No Connection. Not internally connected.
—	—	EP	Exposed Pad for Thin QFN Package Only. Connect EP to ground.

MAX9258 Pin Description

PIN	NAME	FUNCTION
1, 12, 13, 24, 25, 36, 37	N.C.	No Connection. Not internally connected.
2	V_{CC}	Digital Supply Voltage. Bypass V_{CC} to GND with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest V_{CC}.
3, 14	GND	Digital Supply Ground
4	$\overline{PD}$	LVCMOS/LVTTL Power-Down Input. Drive $\overline{PD}$ high to power up the device and enable all outputs. Drive $\overline{PD}$ low to put all outputs in high impedance and reduce supply current. $\overline{PD}$ is internally pulled down to ground.
5	V_{CCLVDS}	LVDS Supply Voltage. Bypass V_{CCLVDS} to GND_{LVDS} with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCLVDS}.
6	SDI-	Serial LVDS Inverting Input
7	SDI+	Serial LVDS Noninverting Input
8	GND_{LVDS}	LVDS Supply Ground
9	GND_{PLL}	PLL Supply Ground
10	V_{CCPLL}	PLL Supply Voltage. Bypass V_{CCPLL} to GND_{PLL} with 0.1µF and 0.001µF capacitors in parallel as close to the device as possible with the smallest value capacitor closest to V_{CCPLL}.
11	$\overline{ERROR}$	Active-Low, Open-Drain Error Output. $\overline{ERROR}$ asserts low to indicate a data transfer error was detected (parity, PRBS, or UART control channel error). $\overline{ERROR}$ is high to indicate no error detected. $\overline{ERROR}$ resets when the error registers are read for parity, control channel errors, and when PRBS enable bit is reset for PRBS errors. Pull up to V_{CCOUT} with a 1kΩ resistor.
15	RX	LVCMOS/LVTTL Control Channel UART Output

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

MAX9258 Pin Description (continued)

PIN	NAME	FUNCTION
16	TX	LVCMOS/LVTTL Control Channel UART Input. TX is internally pulled up to V_{CCOUT}.
17	LOCK	Open-Drain Lock Output. LOCK asserts high to indicate PLLs are locked with correct serial-word boundary alignment. LOCK asserts low to indicate PLLs are not locked or incorrect serial-word boundary alignment was detected. Pull up to V_{CCOUT} with a 1kΩ resistor.
18	PCLK_OUT	LVCMOS/LVTTL Recovered Clock Output
19	VSYNC_OUT	LVCMOS/LVTTL Vertical SYNC Output
20	HSYNC_OUT	LVCMOS/LVTTL Horizontal SYNC Output
21, 28–35, 40–46	DOUT[15:0]	LVCMOS/LVTTL Data Outputs
22, 39	V_{CCOUT}	Output Supply Voltage. V_{CCOUT} is the supply for all output buffers. Bypass V_{CCOUT} to GND_{OUT} with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCOUT}.
23, 38, 48	GND_{OUT}	Output Supply Ground
26	V_{CCSPLL}	Spread-Spectrum PLL Supply Voltage. Bypass V_{CCSPLL} to GND_{SPLL} with 0.1µF and 0.001µF capacitors in parallel as close as possible to the device with the smallest value capacitor closest to V_{CCSPLL}.
27	GND_{SPLL}	SPLL Ground
47	CCEN	LVCMOS/LVTTL Control Channel Enabled Output. CCEN asserts high to indicate that control channel is enabled.

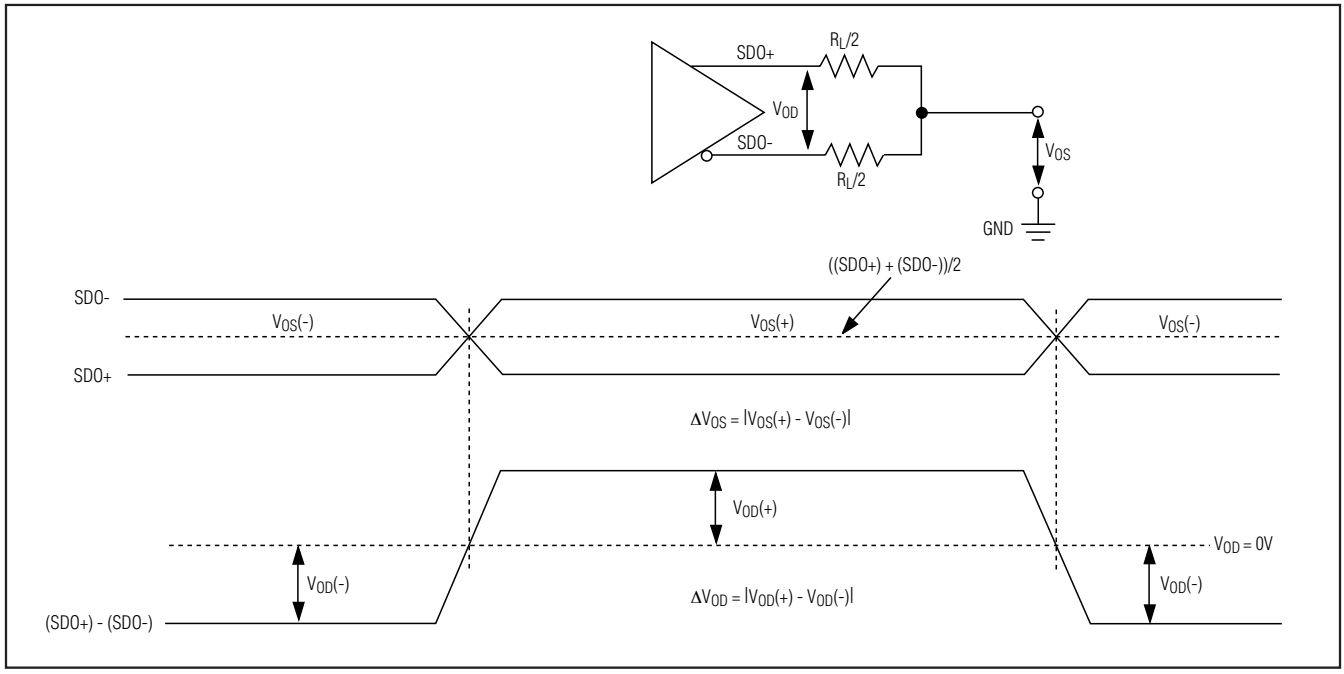


Figure 1. MAX9257 LVDS DC Output Parameters

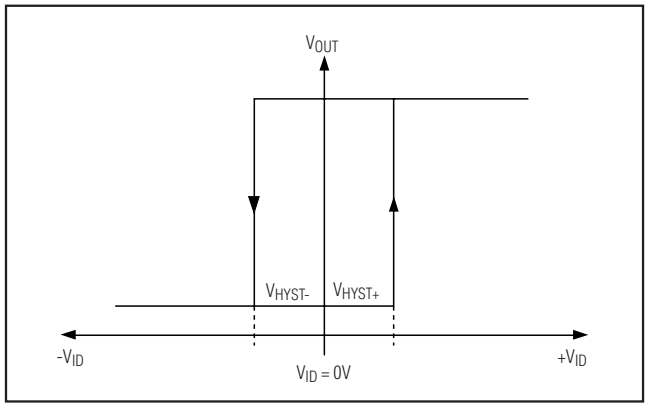


Figure 2. Input Hysteresis

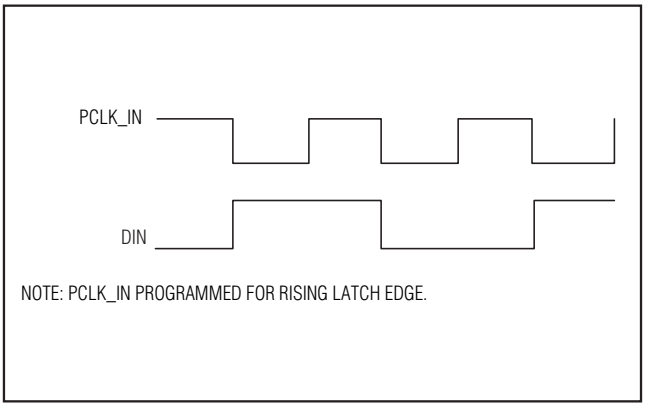


Figure 3. MAX9257 Worst-Case Pattern Input

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

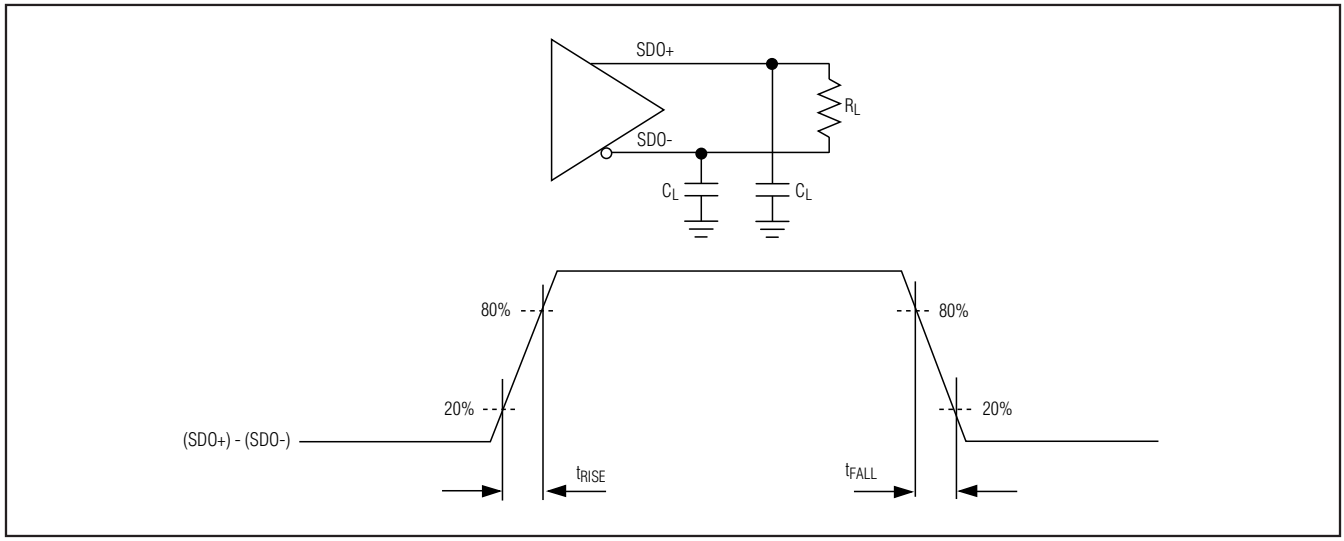


Figure 4. MAX9257 LVDS Control Channel Output Load and Output Rise/Fall Times

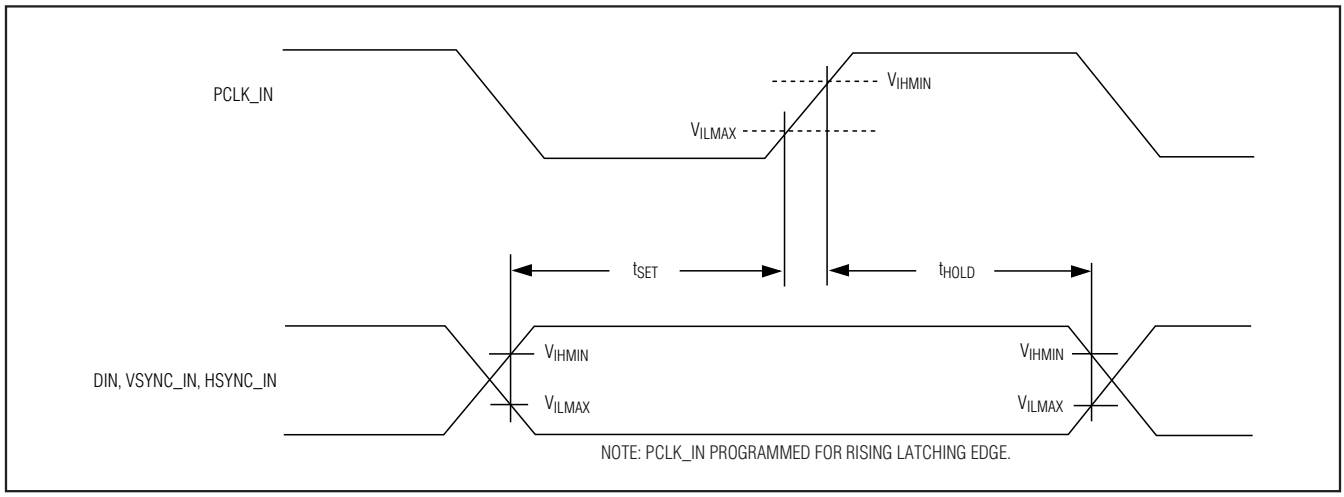


Figure 5. MAX9257 Input Setup and Hold Times

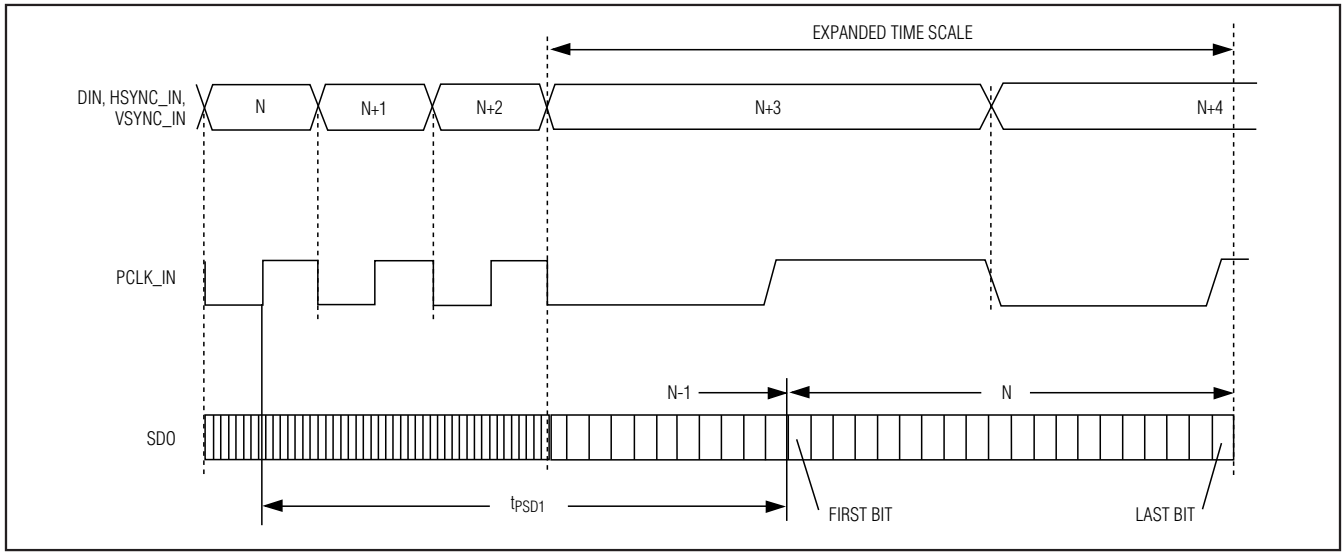


Figure 6. MAX9257 Parallel-to-Serial Delay

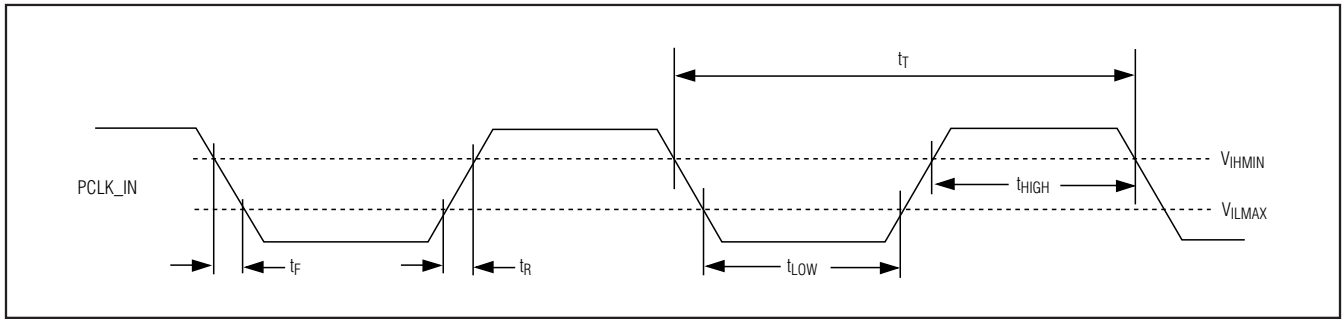


Figure 7. MAX9257 Parallel Input Clock Requirements

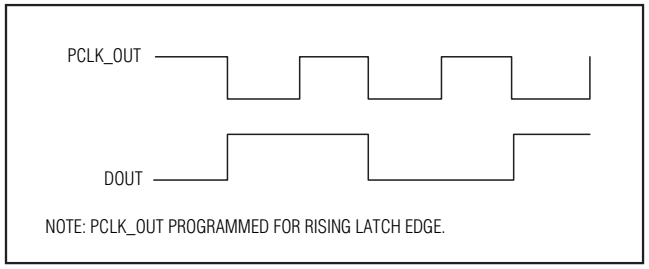


Figure 8. MAX9258 Worst-Case Pattern Output

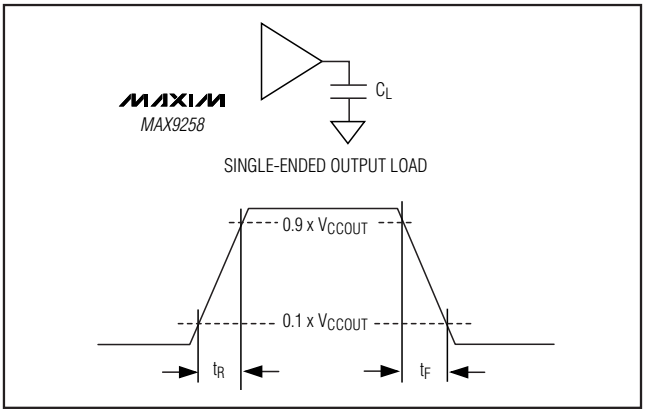


Figure 9. MAX9258 Output Rise and Fall Times

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

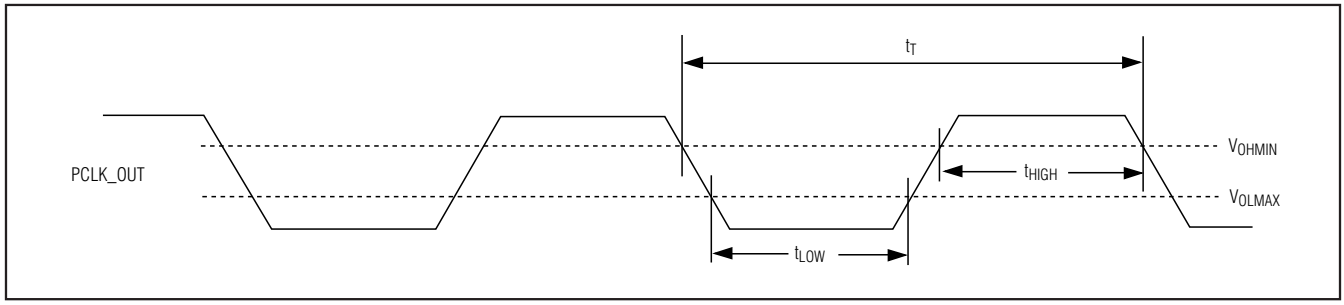


Figure 10. MAX9258 Clock Output High and Low Time

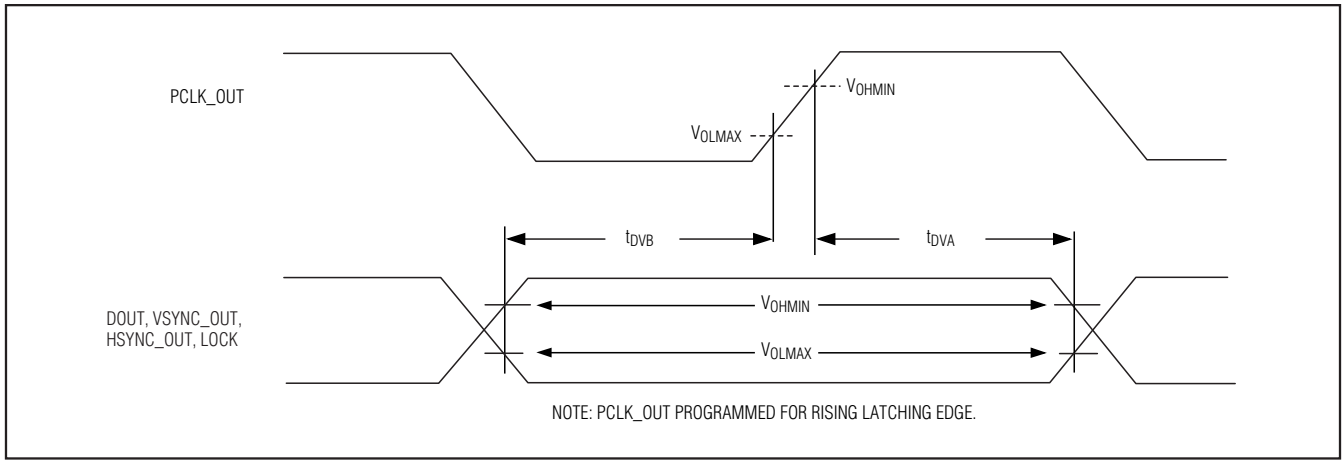


Figure 11. MAX9258 Output Data Valid Times

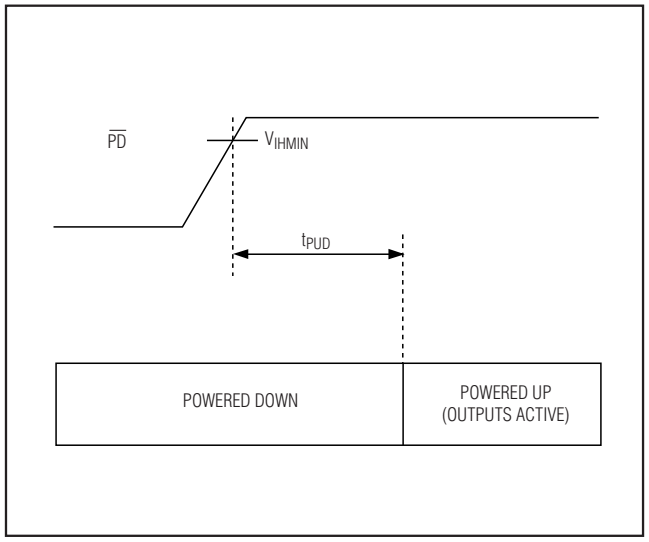


Figure 12. MAX9258 Power-Up Delay

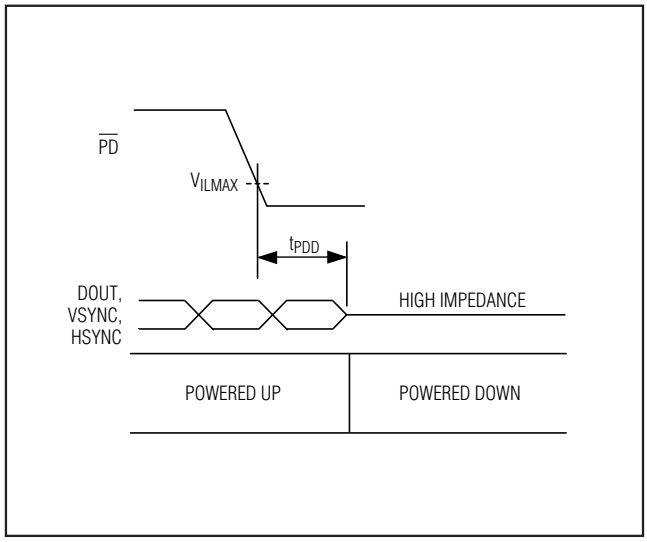


Figure 13. MAX9258 Power-Down Delay

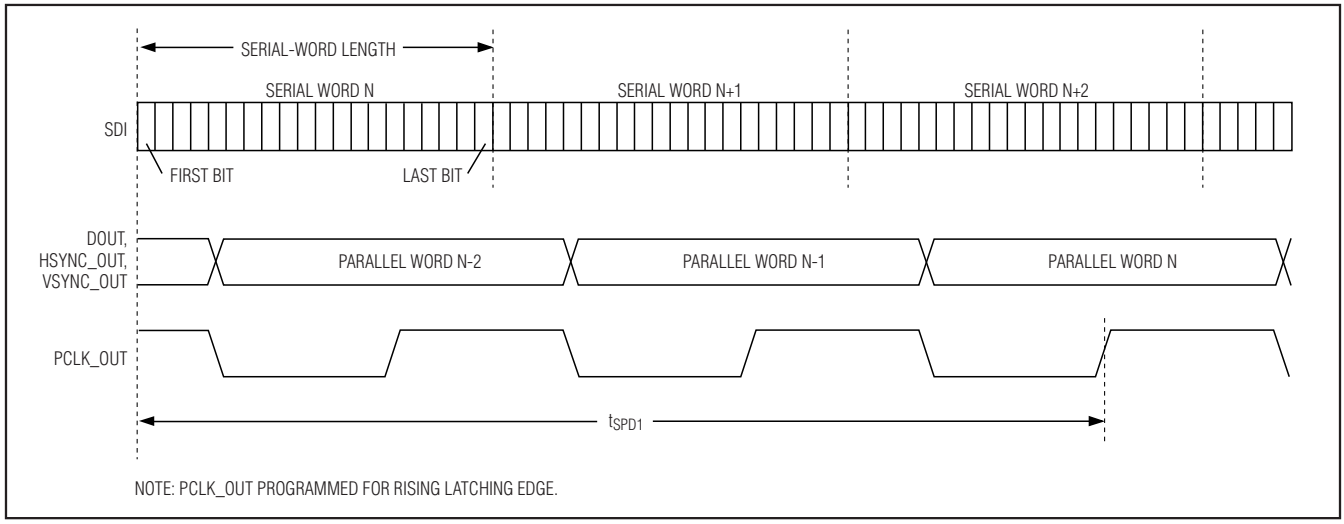


Figure 14. MAX9258 Serial-to-Parallel Delay

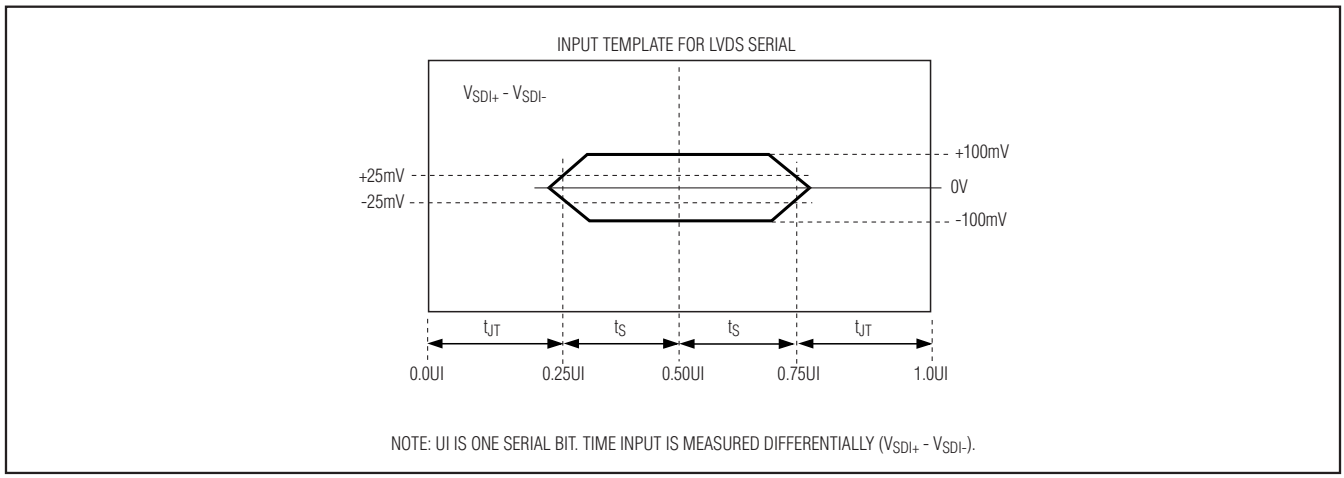


Figure 15. MAX9258 Jitter Tolerance

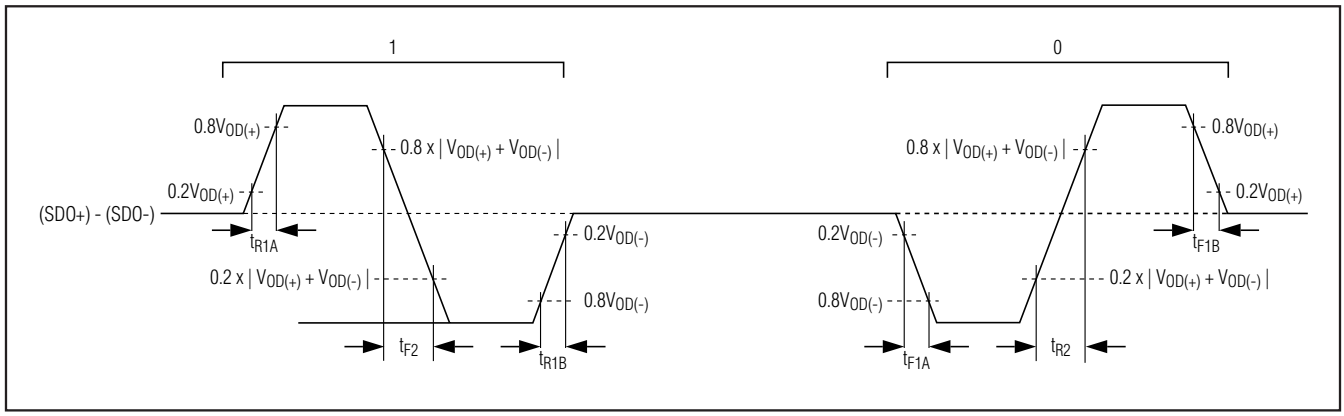


Figure 16. Control Channel Transition Time

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

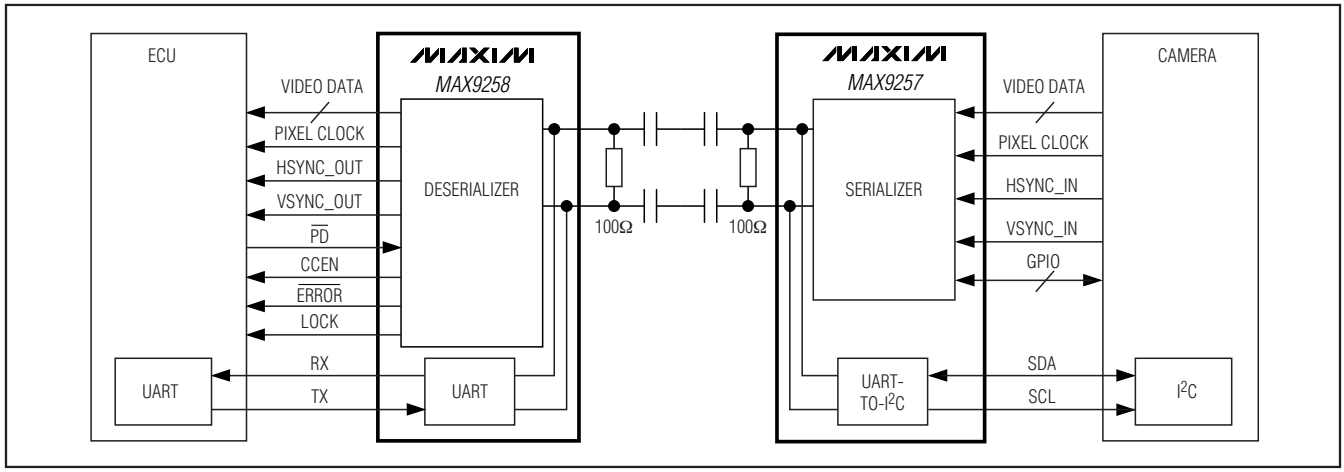


Figure 17. Serial Link with I²C Camera Programming Interface (Base Mode)

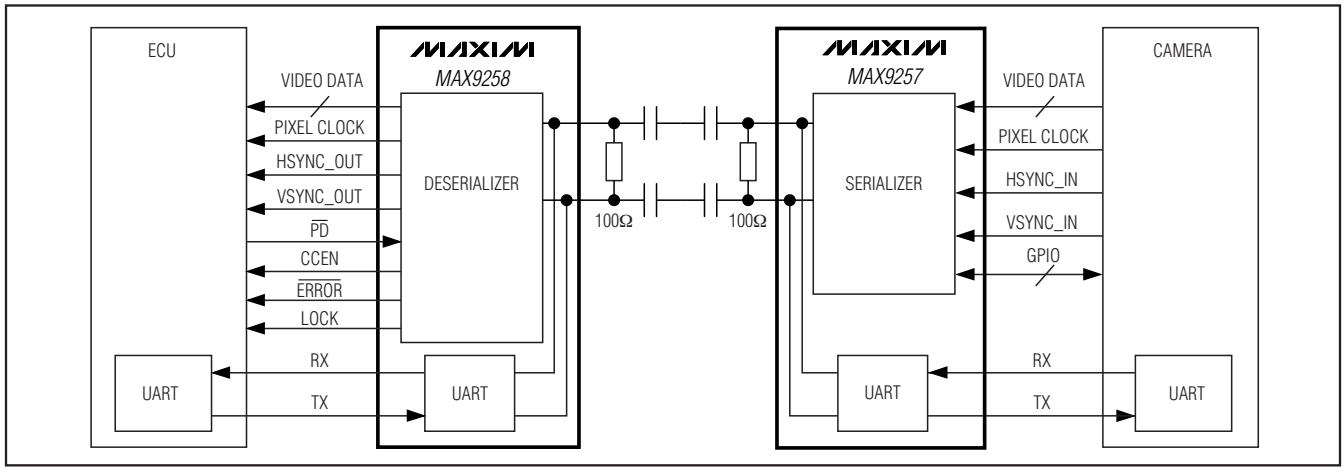


Figure 18. Serial Link with UART Camera Programming Interface (Bypass Mode)

Detailed Description

The MAX9257 serializer pairs with the MAX9258 deserializer to form a complete digital video serial link. The electronic control unit (ECU) programs the registers in the MAX9257, MAX9258, and peripheral devices, such as a camera, during the control channel phase that occurs at startup or during the vertical blanking time. All control channel communication is half-duplex. The UART communication between the MAX9258 and the MAX9257 is encoded to allow transmission through AC-coupling capacitors. The MAX9257 communicates to the peripheral device through UART or I²C.

The MAX9257/MAX9258 DC-balanced serializer and deserializer operate from a 5MHz-to-70MHz parallel clock frequency, and are capable of serializing and deserializing programmable 10, 12, 14, 16, and 18 bits parallel data during the video phase. The MAX9257/MAX9258 have two phases of operation: video and control channel (Figures 19 and 20). During the video phase, the MAX9257 accepts parallel video data and transmits serial encoded data over the LVDS link. The MAX9258 accepts the encoded serial LVDS data and converts it back to parallel output data. The MAX9257 has dedicated inputs for HSYNC and VSYNC. The selected VSYNC edge causes the MAX9257/MAX9258 to enter the control channel phase. Nonactive VSYNC edge can be asserted after eight pixel clock cycles.

The video data are coded using two overhead bits (EN0 and EN1) resulting in a serial-word length of N+2 bits. The MAX9257/MAX9258 feature programmable

parity encoding that adds two parity bits to the serial word. Bit 0 (EN0) is the LSB that is serialized first without parity enabled. The parity bits are serialized first when parity is enabled.

The ECU programs the MAX9258, MAX9257, and peripheral devices at startup and during the control channel phase. In a digital video system, the control channel phase occurs during the vertical blanking time and synchronizes to the VSYNC signal. The programmable active edge of VSYNC initiates the control channel phase. Nonactive edge of VSYNC can transition at any time after 8 x t_T if MAX9257 spread is not enabled and 0.5/f_{SSM} when enabled. At the end of video phase, the MAX9258 drives CCEN high to indicate to the ECU that the control channel is open. Programmable timers and ECU signal activity determine how long the control channel stays open. The timers are reset by ECU signal activity. ECU programming must not exceed the vertical blanking time to avoid loss of video data.

After the control channel phase closes, the MAX9257 sends a 546 or 1090 word pattern as handshaking (HSK) to synchronize the MAX9258's internal clock recovery circuit to the MAX9257's transmitted data. Following the handshaking, the control channel is closed and the video phase begins. The serial LVDS data is recovered and parallel data is valid on the programmed edge of the recovered pixel clock.

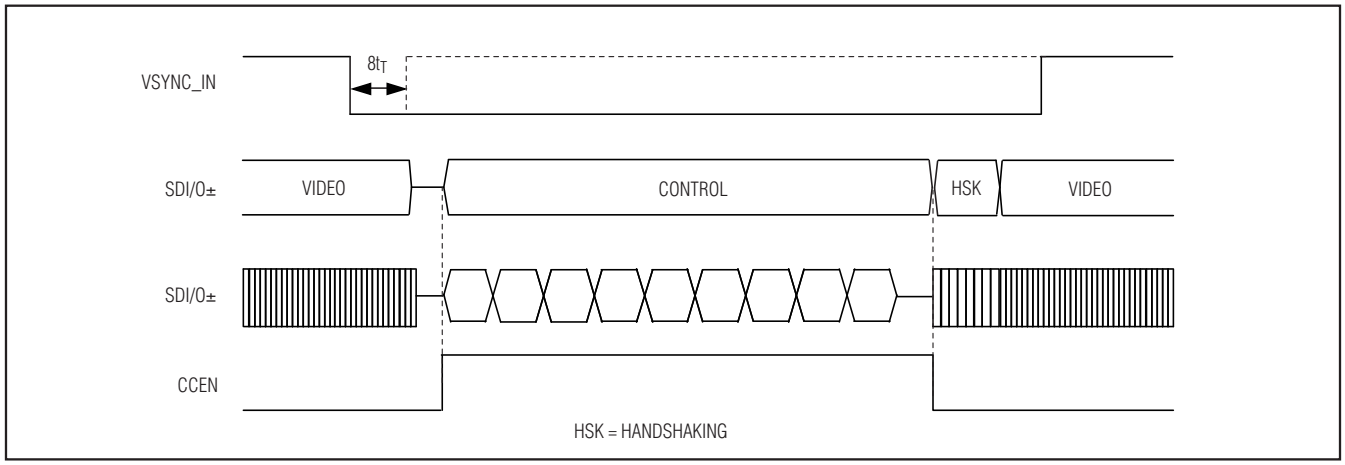


Figure 19. Video and Control Channel Phases (Spread Off)

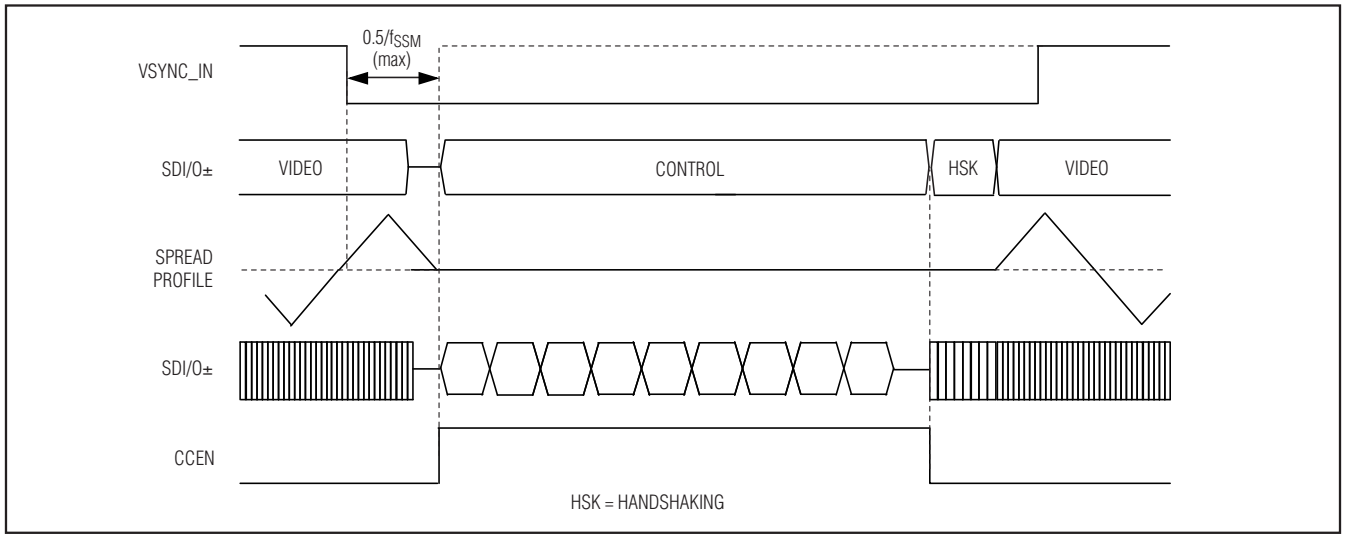


Figure 20. Video and Control Channel Phases (MAX9257 Spread is Enabled)

Fully Programmable Serializer/Deserializer with UART/I²C Control Channel

Table 1. MAX9257 Power-Up Default Register Map (see the *MAX9257 Register Table*)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG0	0x00	0xB5	PRATE = 10, 20MHz to 40MHz SRATE = 11, 400Mbps to 840Mbps PAREN = 0, parity disabled PWIDTH = 101, parallel data width = 18
REG1	0x01	0x1F	SPREAD = 000, spread = off Reserved = 11111
REG2	0x02	0xA0	STODIV = 1010, STO clock is pixel clock divided by 1024 STOCNT = 0000, STO counter counts to 1
REG3	0x03	0xA0	ETODIV = 1010, ETO clock is pixel clock divided by 1024 ETOCNT = 0000, ETO counter counts to 1
REG4	0x04	1) REM = 0, 0x28 2) REM = 1, 0x30	VEDGE = 0, VSYNC active edge is falling Reserved = 0 CKEDGE = 1, pixel clock active edge is rising PD: 1) If REM = 0, PD = 0 2) If REM = 1, PD = 1 SEREN: 1) If REM = 0, SEREN = 1 2) If REM = 1, SEREN = 0 BYPFPLL = 0, filter PLL is active Reserved = 0 PRBSEN = 0, PRBS test disabled
REG5	0x05	0xFA	MAX9257 address = 1111 1010
REG6	0x06	0xFF	End frame = 1111 1111
REG7	0x07	0xF8	MAX9258 address = 1111 1000
REG8	0x08	0x00	INTMODE = 0, interface with peripheral is UART INTEN = 0, interface with peripheral is disabled FAST = 0, UART bit rate = DC to 4.25Mbps CTO = 000, never come back BITRATE = 00, base mode bit rate = 95kbps to 400kbps
REG9	0x09	0x00	PRBSLEN = 0000, PRBS word length = 2^{21} GPIO9DIR = 0, GPIO9 = input GPIO8DIR = 0, GPIO8 = input GPIO9 = 0 GPIO8 = 0
REG10	0x0A	0x00	GPIO7DIR = 0, GPIO7 = input GPIO6DIR = 0, GPIO6 = input GPIO5DIR = 0, GPIO5 = input GPIO4DIR = 0, GPIO4 = input GPIO3DIR = 0, GPIO3 = input GPIO2DIR = 0, GPIO2 = input GPIO1DIR = 0, GPIO1 = input GPIO0DIR = 0, GPIO0 = input

Table 1. MAX9257 Power-Up Default Register Map (continued)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG11	0x0B	0x00	GPIO7 = 0 GPIO6 = 0 GPIO5 = 0 GPIO4 = 0 GPIO3 = 0 GPIO2 = 0 GPIO1 = 0 GPIO0 = 0
REG12	0x0C	0xE0	PREEMP = 111, preemphasis = 0% Reserved = 00000
REG13	0x0D	0x00	Reserved = 000000 I2CFILT = 00, I²C glitch filter settings: 1) 95kbps to 400kbps = 100ns 2) 400kbps to 1000kbps = 50ns 3) 1000kbps to 4250kbps = 10ns
REG14	0x0E	0x00	Reserved = 0000 000 LOCKED = read only

Table 2. MAX9258 Power-Up Default Register Map (see the *MAX9258 Register Table*)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG0	0x00	0xB5	PRATE = 10, 20MHz to 40MHz SRATE = 11, 400Mbps to 840Mbps PAREN = 0, parity disabled PWIDTH = 101, parallel data width = 18
REG1	0x01	0x00	SPREAD = 00, spread spectrum = off AER = 0, error count is reset by reading error registers Reserved = 0 0000
REG2	0x02	0xA0	STODIV = 1010, STO clock is pixel clock divided by 1024 STOCNT = 0000, STO counter counts to 1
REG3	0x03	0xA0	ETODIV = 1010, ETO clock is pixel clock divided by 1024 ETOCNT = 0000, ETO counter counts to 1
REG4	0x04	0x20	VEDGE = 0, VSYNC active edge is falling HEDGE = 0, HSYNC active edge is falling CKEDGE = 1, pixel clock active edge is rising Reserved = 0000 PRBSEN = 0, PRBS test disabled
REG5	0x05	0xF8	MAX9258 address = 1111 1000
REG6	0x06	0xFF	End frame = 1111 1111
REG7	0x07	0x00	INTMODE = 0, interface with peripheral is UART INTEN = 0, interface with peripheral is disabled FAST = 0, UART bit rate = DC to 4.25Mbps CTO = 000, never come back BITRATE = 00, base mode bit rate = 95kbps to 400kbps

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Table 2. MAX9258 Power-Up Default Register Map (continued)

REGISTER NAME	REGISTER ADDRESS (hex)	POWER-UP VALUE (hex)	POWER-UP DEFAULT SETTINGS
REG8	0x08	0x10	PATHRLO = 0001 0000 parity threshold = 16
REG9	0x09	0x00	PATHRHI = 0000 0000, parity threshold = 16
REG10	0x0A	0x00	Parity errors video (8 LSBs) = read only
REG11	0x0B	0x00	Parity errors video (8 MSBs) = read only
REG12	0x0C	0x00	PRBS bit errors = read only
REG13	0x0D	0x00	Reserved = 000 Parity error, communication with MAX9258 = read only Frame error, communication with MAX9258 = read only Parity error, communication with MAX9257 = read only Frame error, communication with MAX9257 = read only I²C error, communication with peripheral = read only

Tables 1 and 2 show the default power-up values for the MAX9257/MAX9258 registers. Tables 3 and 4 show the input and output supply references.

Parallel-Word Width

The parallel-word width is made up of the video data bits, HSYNC, and VSYNC. The video data bits are programmable from 8 to 16 depending on the pixel clock, serial-data rate, and parity. Table 16 shows the parallel-word width.

Serial-Word Length

The serial-word length is made up of the parallel-word width, encoding bits, and parity bits. Tables 5–9 show the serial video format and serial-word lengths without parity. Tables 10–13 show with parity bits included.

LVDS Serial Data

Serial LVDS data is transmitted least significant bit (LSB) to most significant bit (MSB) as shown in Tables 5 through 13. The ECU at startup can program the parallel word width, serial frequency range, parity, spread-spectrum, and pixel clock frequency range *(see the MAX9257 Register Table* and the *MAX9258 Register Table).*

Table 3. MAX9257 I/O Supply

INPUTS/OUTPUTS	SUPPLY
PCLK_IN, HSYNC_IN, VSYNC_IN, DIN[0:7], DIN[8:15]/GPIO[0:7], GPIO8, GPIO9	V_{CCIO}
SDO+, SDO-	V_{CCLVDS}
SCL/TX, SDA/RX, REM	V_{CC}

Table 4. MAX9258 I/O Supply

INPUTS/OUTPUTS	SUPPLY
All inputs and outputs	V_{CCOUT}
SDI+, SDI-	V_{CCLVDS}

Table 5. Serial Video Data Format for 20-Bit Serial-Word Length (Parallel-Word Width = 18)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15

Table 6. Serial Video Data Format for 18-Bit Serial-Word Length (Parallel-Word Width = 16)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13

Table 7. Serial Video Data Format for 16-Bit Serial-Word Length (Parallel-Word Width = 14)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

Table 8. Serial Video Data Format for 14-Bit Serial-Word Length (Parallel-Word Width = 12)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

Table 9. Serial Video Data Format for 12-Bit Serial-Word Length (Parallel-Word Width = 10)

BIT	1	2	3	4	5	6	7	8	9	10	11	12
NAME	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7

Table 10. Format for 20-Bit Serial-Word Length with Parity (Parallel-Word Width = 16)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13

Table 11. Format for 18-Bit Serial-Word Length with Parity (Parallel-Word Width = 14)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

Table 12. Format for 16-Bit Serial-Word Length with Parity (Parallel-Word Width = 12)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9

Table 13. Format for 14-Bit Serial-Word Length with Parity (Parallel-Word Width = 10)

BIT	1	2	3	4	5	6	7	8	9	10	11	12	13	14
NAME	PR	PRB	EN0	EN1	HSYNC	VSYNC	D0	D1	D2	D3	D4	D5	D6	D7

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Pixel Clock Frequency Range

The MAX9257/MAX9258 each have registers that can be configured at startup. Depending on the word length, the MAX9257 multiplies PCLK_IN (pixel clock) by 12, 14, 16, 18, or 20 using an internal PLL to generate the serial clock. Use Table 20 for proper selection of available PCLK frequency and serial-data ranges. Parallel data is serialized using the serial-clock and serialized bits are transmitted at the MAX9257 LVDS outputs. The MAX9257/MAX9258 support a wide range for PCLK_IN (Table 14). If the pixel clock frequency needs to change to a frequency outside the programmed range, the ECU must program both the MAX9257 and the MAX9258 in the same control channel session.

Serial-Data Rate Range

The word length and pixel clock is limited by the maximum serial-data rate of 840Mbps. The following formula shows the relation between word length, pixel clock, and serial clock:

Serial-word length x pixel clock = serial-data rate ≤ 840Mbps

For example, if PCLK_IN is 70MHz, the serial-word length has to be 12 bits including DC balance bits if parity is not enabled to keep the serial-data rate under 840Mbps. If the serial-word length is 20 bits, the maximum PCLK_IN frequency is 42MHz. The serial-data rate can vary from 60Mbps to 840Mbps and can be programmed at power-up (Table 15). Use Table 20 for proper selection of available PCLK frequency and serial data ranges. Operating in the incorrect range for either the serial-data rate or PCLK_IN can result in excessive current dissipation and failure of the MAX9258 to lock to the MAX9257.

LVDS Common-Mode Bias

The output common-mode bias is 1.2V at the LVDS inputs on the MAX9258 and LVDS outputs on the MAX9257. No external resistors are required to provide bias for AC-coupling the LVDS inputs and outputs.

LVDS Termination

Terminate the LVDS link at both ends with the characteristic impedance of the transmission line (typically 100Ω differential). The LVDS inputs and outputs are high impedance to GND and differentially.

Spread-Spectrum Selection

The MAX9257/MAX9258 each have spread-spectrum options. Both should not be turned on at the same time. When the MAX9257 is programmed for spread spectrum, the MAX9258 tracks and passes the spread to its clock and data outputs. The MAX9257/MAX9258 are both center spread (Figure 21). The control channel does not use spread spectrum, but has slower transition times.

Table 14. MAX9257 Pixel Clock Range (PCLK_IN)

FREQUENCY (MHz)	PRATE (REG0[7:6])
5–10	00
10–20	01
20–40	10
40–70	11

Table 15. Serial-Data Rate Range

SERIAL-DATA RATE (Mbps)	SRATE (REG0[5:4])
60–100	00
100–200	01
200–400	10
400–840	11

Table 16. Parallel-Word Width

PARALLEL-WORD WIDTH	PWIDTH (REG0[2:0])
10	000
12	001
14	010
16	011
18	1XX

MAX9258 Spread Spectrum

The MAX9258 features a programmable spread-spectrum clock and data outputs for reduced EMI. The single-ended data outputs are programmable for no spread, ±2%, or ±4% (see the *Typical Operating Characteristics*) around the recovered pixel clock frequency. The output spread is programmed in register REG1[7:6]. Table 17 shows the spread options, and Table 18 shows the various modulation rates.

MAX9257 Spread Spectrum

The MAX9257 features programmable spread spectrum for the LVDS outputs. Table 19 shows various spread options, and Table 20 shows the various modulation rates. Only one device (the MAX9257 or the MAX9258) should be programmed for spread spectrum at a time. If the MAX9257 is programmed for spread, the MAX9258

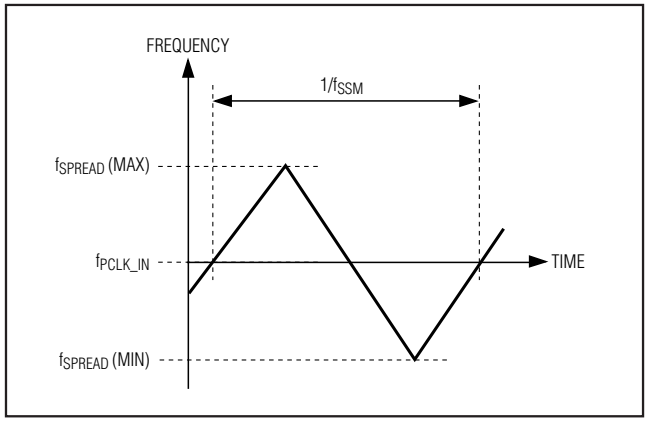

Figure 21. Simplified Modulation Profile for the MAX9257/MAX9258

tracks and passes the spread to the data and clock outputs. The PRATE range of 00 and 01 (5MHz ≤ PCLK ≤ 20MHz) supports all the spread options. The PRATE range of 10 and 11 (20MHz ≤ PCLK ≤ 70MHz) requires that the spread be 2% or less.

Pixel Clock Jitter Filter

The MAX9257 has a PLL to filter high-frequency pixel clock jitter on PCLK_IN. The FPLL can be bypassed by writing 1 to REG4[2]. The FPLL improves the MAX9258's data recovery by filtering out the high-frequency components from the pixel clock that the MAX9258 cannot track. The 3dB bandwidth of the FPLL is 100kHz (typ).

LVDS Output Preemphasis (SDO±)

The MAX9257 features programmable preemphasis where extra current is added when the LVDS outputs transition on the serial link. Preemphasis provides additional current to the normal drive current. For example, 20% preemphasis provides 20% greater current than the normal drive current. Current is boosted only on the transitions and returns to the normal drive current after switching. Select the preemphasis level to optimize the eye diagram. Preemphasis boosts the high-frequency content of the LVDS outputs to enable driving greater cable lengths. The amount of preemphasis is programmed in REG12[7:5] (Table 21).

VSYNC, HSYNC, and Pixel Clock Polarity

PCLK: The MAX9257 is programmable to latch data on either rising or falling edge of PCLK. The polarity of PCLKOUT at the MAX9258 can be independent of the MAX9257 PCLK active edge. The polarity of PCLK can be programmed using REG4[5] of the MAX9257 and the MAX9258.

Table 17. MAX9258 Spread

PRATE (REG1[7:6])	SPREAD (%)
00	Off
01	±2
10	Off
11	±4

Table 18. MAX9258 Modulation Rate

PRATE (REG1[7:6])	MODULATION RATE	f_{SSM} RANGE (kHz)
00	PCLK/312	16 to 32
01	PCLK/520	19.2 to 38.5
10	PCLK/1040	19.2 to 38.5
11	PCLK/1248	32 to 56

Table 19. MAX9257 LVDS Output Spread

REG1[7:5]	SPREAD (%)
000	Off
001	±1.5
010	±1.75
011	±2
100	Off
101	±3
110	±3.5
111	±4

VSYNC: The MAX9257 and the MAX9258 enter control channel on the falling edge of VSYNC. The default register settings are VSYNC active falling edge for both the MAX9257 and the MAX9258. If the VSYNC active edge is programmed for rising edge at the MAX9257, the MAX9258 VSYNC active edge must also be programmed for rising edge to reproduce VSYNC rising edge at the MAX9258 output. However, matching the polarity of the VSYNC active edge between the MAX9257 and the MAX9258 is not a requirement for proper operation.

HSYNC: HSYNC active-edge polarity is programmable for the MAX9258.

General Purpose I/Os (GPIOs)

The MAX9257 has up to 10 GPIOs available. GPIO8 and GPIO9 are always available while GPIO[0:7] are available depending on the parallel-word width (Table 22). If GPIOs are not available, the corresponding GPIO bits are not used.