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EVALUATION KIT AVAILABLE

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

General Description

The MAX9259/MAX9260 chipset presents Maxim's gigabit multimedia serial link (GMSL) technology. The MAX9259 serializer pairs with the MAX9260 deserializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data.

The MAX9259/MAX9260 allow a maximum serial payload data rate of 2.5Gbps for a 15m shielded twisted-pair (STP) cable. The 24-bit or 32-bit width parallel interface operates up to a maximum bus clock of 104MHz or 78MHz, respectively. This serial link supports display panels from QVGA (320 x 240) up to XGA (1280 x 768), or dual-view WVGA (2 x 854 x 480).

The 24-bit or 32-bit mode handles 21 or 29 bits of data, along with an I²S input, supporting 4- to 32-bit audio word lengths and an 8kHz to 192kHz sample rate. The embedded control channel forms a full-duplex, differential 100kbps to 1Mbps UART link between the serializer and deserializer. The host electronic control unit (ECU) or microcontroller (µC) resides either on the MAX9259 (for video display) or on the MAX9260 (for image sensing). In addition, the control channel enables ECU/µC control of peripherals in the remote side of the serial link through I²C (base mode) or a user-defined full-duplex UART format (bypass mode).

The MAX9259 serializer driver preemphasis and channel equalizer on the MAX9260 extend the link length and enhance the link reliability. Spread spectrum is available on the MAX9259/MAX9260 to reduce EMI on the serial and parallel output data signals. The differential link complies with the ISO 10605 and IEC 61000-4-2 ESD-protection standards.

The core supplies for the MAX9259/MAX9260 are 1.8V and 3.3V, respectively. Both devices use an I/O supply from 1.8V to 3.3V. These devices are available in a 64-pin TQFP package (10mm x 10mm) and a 56-pin TQFN package (8mm x 8mm x 0.75mm) with an exposed pad. Electrical performance is guaranteed over the -40°C to +105°C automotive temperature range.

Applications

High-Speed Serial-Data Transmission for Display

High-Speed Serial-Data Transmission for Image Sensing

Automotive Navigation, Infotainment, and Image-Sensing Systems

Features

- **2.5Gbps Payload Rate, AC-Coupled Serial Link with 8B/10B Line Coding**
- **24-Bit or 32-Bit Programmable Parallel Input Bus Supports Up to XGA (1280 x 768) or Dual-View WVGA (2 x 854 x 480) Panels with 18-Bit or 24-Bit Color**
- **8.33MHz to 104MHz (24-Bit Bus) or 6.25MHz to 78MHz (32-Bit Bus) Parallel Data Rate**
- **Support Two/Three 10-Bit Camera Links at 104MHz/78MHz Maximum Pixel Clock**
- **4-Bit to 32-Bit Word Length, 8kHz to 192kHz I²S Audio Channel Supports High-Definition Audio**
- **Embedded Half-/Full-Duplex Bidirectional Control Channel (100kbps to 1Mbps)**
- **Separate Interrupt Signal Supports Touch-Screen Functions for Display Panels**
- **Remote-End I²C Master for Peripherals**
- **Preemphasis Line Driver (MAX9259)/Line Equalizer (MAX9260)**
- **Programmable Spread Spectrum on the Serial or Parallel Data Outputs Reduce EMI**
- **Deserializer Does Not Require an External Clock**
- **Auto Data-Rate Detection Allows "On-The-Fly" Data-Rate Change**
- **Input Clock PLL Jitter Attenuator (MAX9259)**
- **Built-In PRBS Generator/Checker for BER Testing**
- **Line-Fault Detector Detects Wire Shorts to Ground, Battery, or Open Link**
- **ISO 10605 and IEC 61000-4-2 ESD Protection**
- **-40°C to +105°C Operating Temperature Range**
- **Patent Pending**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9259GCB/V+	-40°C to +105°C	64 TQFP-EP*
MAX9259GCB/V+T	-40°C to +105°C	64 TQFP-EP*
MAX9259GTN/V+T	-40°C to +105°C	56 TQFN-EP*
MAX9260GCB/V+	-40°C to +105°C	64 TQFP-EP*
MAX9260GCB/V+T	-40°C to +105°C	64 TQFP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

Typical Applications Circuit appears at end of data sheet.

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND
- MAX9259 ..... -0.5V to +1.9V
- MAX9260 ..... -0.5V to +3.9V

DVDD to GND (MAX9259) ..... -0.5V to +1.9V
DVDD to DGND (MAX9260) ..... -0.5V to +3.9V
IOVDD to GND (MAX9259) ..... -0.5V to +3.9V
IOVDD to IOGND (MAX9260) ..... -0.5V to +3.9V
Any Ground to Any Ground ..... -0.5V to +0.5V
OUT+, OUT- to AGND (MAX9259) ..... -0.5V to +1.9V
IN+, IN- to AGND (MAX9260) ..... -0.5V to +1.9V
LMN_ to GND (MAX9259)
- (60kΩ source impedance) ..... -0.5V to +3.9V

All Other Pins to GND (MAX9259) ..... -0.5V to (IOVDD + 0.5V)
All Other Pins to IOGND (MAX9260) ... -0.5V to (IOVDD + 0.5V)
OUT+, OUT- Short Circuit to Ground or
- Supply (MAX9259) ..... Continuous

IN+, IN- Short Circuit to Ground or
- Supply (MAX9260) ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
- 64-Pin TQFP (derate 31.3mW/°C above +70°C) 2508mW
- 56-Pin TQFN (derate 47.6mW/°C above +70°C) 3809.5mW

ESD Protection
- Human Body Model (R_D = 1.5kΩ, C_S = 100pF)
  - (OUT+, OUT-) to AGND (MAX9259) ..... ±8kV
  - (IN+, IN-) to AGND (MAX9260) ..... ±8kV
  - All Other Pins to Any Ground (MAX9259) ..... ±4kV
  - All Other Pins to Any Ground (MAX9260) ..... ±4kV
- IEC 61000-4-2 (R_D = 330Ω, C_S = 150pF)
  - Contact Discharge
    - (OUT+, OUT-) to AGND (MAX9259) ..... ±10kV
    - (IN+, IN-) to AGND (MAX9260) ..... ±8kV
  - Air Discharge
    - (OUT+, OUT-) to AGND (MAX9259) ..... ±12kV
    - (IN+, IN-) to AGND (MAX9260) ..... ±10kV
- ISO 10605 (R_D = 2kΩ, C_S = 330pF)
  - Contact Discharge
    - (OUT+, OUT-) to AGND (MAX9259) ..... ±10kV
    - (IN+, IN-) to AGND (MAX9260) ..... ±8kV
  - Air Discharge
    - (OUT+, OUT-) to AGND (MAX9259) ..... ±25kV
    - (IN+, IN-) to AGND (MAX9260) ..... ±20kV

Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

64 TQFP
- Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 31.9°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

56 TQFN
- Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 21°C/W
- Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAX9259 DC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, PWDN, SSEN, BWS, ES, DRS, MS, CDS, AUTOS, SD, SCK, WS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}		-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA				-1.5	V
SINGLE-ENDED OUTPUT (INT)							
High-Level Output Voltage	V_{OH1}	I_{OH} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

MAX9259 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)		-110		+5	µA
Low-Level Open-Drain Output Voltage	V_{OL2}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV_{P-P}
		3.3dB preemphasis setting, $V_{OD(P)}$ (Figure 2)		350		610	
		3.3dB deemphasis setting, $V_{OD(D)}$ (Figure 2)		240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}					15	mV
Output Offset Voltage, (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}					15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}					27	mV
Low Switching Threshold	V_{CLR}			-27			mV
LINE-FAULT-DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 3				0.3	V
Normal Thresholds	V_{TN}	Figure 3		0.57		1.07	V
Open Thresholds	V_{TO}	Figure 3		1.45		V_{IO+} 0.06	V
Open Input Voltage	V_{IO}	Figure 3		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 3		2.47			V
POWER SUPPLY							
Worst-Case Supply Current (Figure 4)	I_{WCS}	BWS = GND	f_{PCLKIN} = 16.6MHz		100	125	mA
			f_{PCLKIN} = 33.3MHz		105	145	
			f_{PCLKIN} = 66.6MHz		116	155	
			f_{PCLKIN} = 104MHz		135	175	
Sleep-Mode Supply Current	I_{CCS}				40	110	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			5	70	µA

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

MAX9259 AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PARALLEL CLOCK INPUT (PCLKIN)							
Clock Frequency	f_{PCLKIN}	V_{BWS} = V_{GND}, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		V_{BWS} = V_{GND}, V_{DRS} = V_{GND}		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{GND}		12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 5)		35	50	65	%
Clock Transition Time	t_R, t_F	(Figure 5)				4	ns
Clock Jitter	t_J	3.125Gbps, 300kHz sinusoidal jitter				800	$ps_{(P-P)}$
I²C/UART PORT TIMING (Note 3)							
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Input Setup Time	t_{SET}	I²C only (Figure 6)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 6)		0			ns
SWITCHING CHARACTERISTICS (Note 3)							
Differential Output Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial-data rate = 3.125Gbps			90	150	ps
Total Serial Output Jitter	t_{TSOJ1}	3.125Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.125Gbps PRBS signal			0.15		UI
Parallel Data Input Setup Time	t_{SET}	(Figure 8)		1			ns
Parallel Data Input Hold Time	t_{HOLD}	(Figure 8)		1.5			ns
Serializer Delay (Note 4)	t_{SD}	(Figure 9)	Spread spectrum enabled			2830	Bits
			Spread spectrum disabled			270	
Link Start Time	t_{LOCK}	(Figure 10)				3.5	ms
Power-Up Time	t_{PU}	(Figure 11)				3.5	ms
I²S INPUT TIMING							
WS Frequency	f_{WS}	(Table 4)		8		192	kHz
Sample Word Length	n_{WS}	(Table 4)		4		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x 2		(8 x 4) x 2		(192 x 32) x 2	kHz
SCK Clock High Time (Note 3)	t_{HC}	V_{SCK} ≥ V_{IH}, t_{SCK} = $1/f_{SCK}$		0.35 x t_{SCK}			ns
SCK Clock Low Time (Note 3)	t_{LC}	V_{SCK} ≤ V_{IL}, t_{SCK} = $1/f_{SCK}$		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Figure 12, Note 3)		2			ns
SD, WS Hold Time	t_{HOLD}	(Figure 12, Note 3)		2			ns

MAX9260 DC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS ($\overline{ENABLE}$, INT, $\overline{PWDN}$, SSEN, BWS, ES, DRS, MS, CDS, EQS, DCS)								
High-Level Input Voltage	V_{IH1}				0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}						0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}			-10		+10	µA
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA					-1.5	V
SINGLE-ENDED OUTPUTS (DOUT_, SD, WS, SCK, PCLKOUT)								
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA	V_{DCS} = V_{IOGND}		V_{IOVDD} - 0.3			V
			V_{DCS} = V_{IOVDD}		V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA	V_{DCS} = V_{IOGND}				0.3	V
			V_{DCS} = V_{IOVDD}				0.2	
Output Short-Circuit Current	I_{OS}	DOUT_, SD, WS, SCK	V_O = 0V, V_{DCS} = V_{IOGND}	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, V_{DCS} = V_{IOGND}	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, V_{DCS} = V_{IOVDD}	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
I²C AND UART I/O, OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL, $\overline{ERR}$, GPIO_, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2)	RX/SDA, TX/SCL		-110		+1	µA
			GPIO, $\overline{ERR}$, LOCK		-80		+1	
Low-Level Open-Drain Output Voltage	V_{OL2}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V				0.4	V
			V_{IOVDD} = 3.0V to 3.6V				0.3	V

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

MAX9260 DC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIFFERENTIAL OUTPUTS FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROH}	No high-speed data transmission (Figure 13)		30		60	mV
Differential Low Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROL}	No high-speed data transmission (Figure 13)		-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)							
Differential High Input Threshold (Peak), (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	(Figure 14)			40	90	mV
Differential Low Input Threshold (Peak), (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	(Figure 14)		-90	-40		mV
Input Common-Mode Voltage, ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}			1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I			80	100	130	Ω
POWER SUPPLY							
Worst-Case Supply Current (Figure 15)	I_{WCS}	V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 16.6MHz	2% spread spectrum active		113	166	mA
			Spread spectrum disabled		105	155	
		V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 33.3MHz	2% spread spectrum active		122	181	
			Spread spectrum disabled		110	165	
		V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 66.6MHz	2% spread spectrum active		137	211	
			Spread spectrum disabled		120	188	
		V_{BWS} = V_{IOGND}, $f_{PCLKOUT}$ = 104MHz	2% spread spectrum active		159	247	
			Spread spectrum disabled		135	214	
Sleep-Mode Supply Current	I_{CCS}				80	130	µA
Power-Down Supply Current	I_{CCZ}	$V_{\overline{PWDN}}$ = V_{IOGND}			19	70	µA

MAX9260 AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)							
Clock Frequency	$f_{PCLKOUT}$	V_{BWS} = V_{IOGND}, V_{DRS} = V_{IOVDD}		8.33		16.66	MHz
		V_{BWS} = V_{IOGND}, V_{DRS} = V_{IOGND}		16.66		104	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOVDD}		6.25		12.5	
		V_{BWS} = V_{IOVDD}, V_{DRS} = V_{IOGND}		12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 16)		40	50	60	%
Clock Jitter	t_J	Period jitter, RMS, spread off, 3.125Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$			0.05		UI
I²C/UART PORT TIMING							
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		150	ns
Input Setup Time	t_{SET}	I²C only		100			ns
Input Hold Time	t_{HOLD}	I²C only		0			ns
SWITCHING CHARACTERISTICS							
PCLKOUT Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.4		2.2	ns
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.25		1.7	
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.3		2.0	
Parallel Data Rise-and-Fall Time (Figure 17)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.5		3.1	ns
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		2.2	
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	Spread spectrum enabled (Figure 18)				2880	Bits
		Spread spectrum disabled (Figure 18)				750	
Lock Time	t_{LOCK}	Spread spectrum enabled (Figure 19)				1500	µs
		Spread spectrum off (Figure 19)				1000	
Power-Up Time	t_{PU}	(Figure 20)				2500	µs
Reverse Control-Channel Output Rise Time	t_R	No high-speed transmission (Figure 13)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No high-speed transmission (Figure 13)		180		400	ns

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

MAX9260 AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)

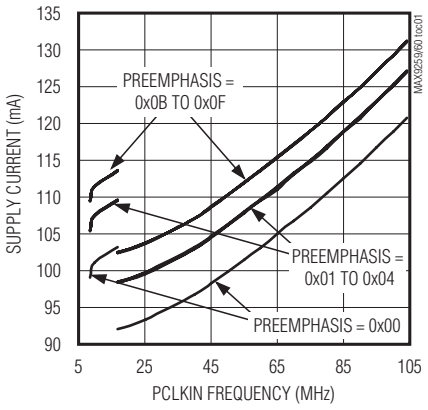
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²S OUTPUT TIMING							
WS Jitter	t_{AJ-WS}	t_{WS} = 1/f_{WS}, rising (falling) edge to falling (rising) edge (Note 5)	f_{WS} = 48kHz or 44.1kHz		0.4e - 3 x t_{WS}	0.5e - 3 x t_{WS}	ns
			f_{WS} = 96kHz		0.8e - 3 x t_{WS}	1e - 3 x t_{WS}	
			f_{WS} = 192kHz		1.6e - 3 x t_{WS}	2e - 3 x t_{WS}	
SCK Jitter	t_{AJ-SCK}	t_{SCK} = 1/f_{SCK}, rising edge to rising edge	n_{WS} = 16 bits, f_{WS} = 48kHz or 44.1kHz		13e - 3 x t_{SCK}	16e - 3 x t_{SCK}	ns
			n_{WS} = 24 bits, f_{WS} = 96kHz		39e - 3 x t_{SCK}	48e - 3 x t_{SCK}	
			n_{WS} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
Audio Skew Relative to Video	ASK	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	V_{DCS} = V_{IOVDD}, C_L = 10pF	0.3		3.1	ns
			V_{DCS} = V_{IOGND}, C_L = 5pF	0.4		3.8	ns
SD, WS Valid Time Before SCK	t_{DVB}	t_{SCK} = 1/f_{SCK} (Figure 21)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK	t_{DVA}	t_{SCK} = 1/f_{SCK} (Figure 21)		0.35 x t_{SCK}	0.5 x t_{SCK}		ns

Note 2: Minimum I_{IN} due to voltage drop across the internal pullup resistor.
Note 3: Not production tested.
Note 4: Bit time = 1/(30 x $f_{RXCLKIN}$) (BWS = 0), = 1/(40 x $f_{RXCLKIN}$) (BWS = V_{IOVDD}).
Note 5: Rising to rising edge jitter can be twice as large.

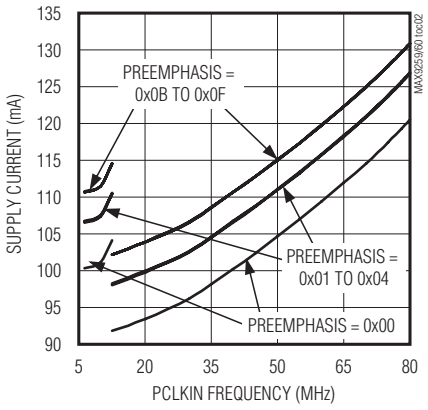
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V (MAX9259), V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V (MAX9260), T_A = +25°C, unless otherwise noted.)

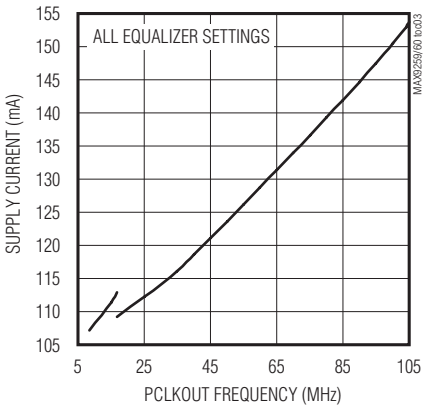
MAX9259 SUPPLY CURRENT vs. PCLKIN FREQUENCY (24-BIT MODE)



MAX9259 SUPPLY CURRENT vs. PCLKIN FREQUENCY (32-BIT MODE)



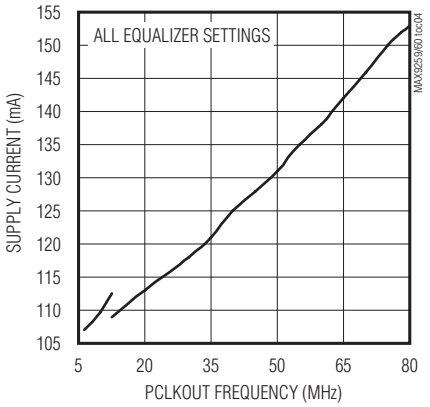
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (24-BIT MODE)



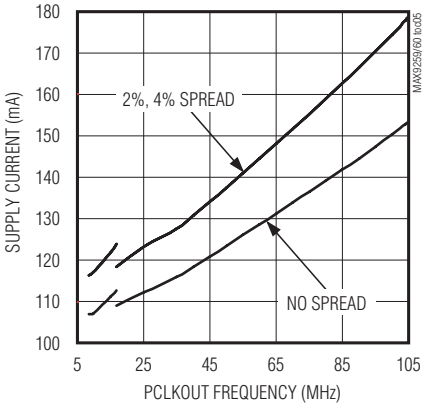
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V (MAX9259), V_{DVDD} = V_{AVDD} = V_{IOVDD} = 3.3V (MAX9260), T_A = +25°C, unless otherwise noted.)

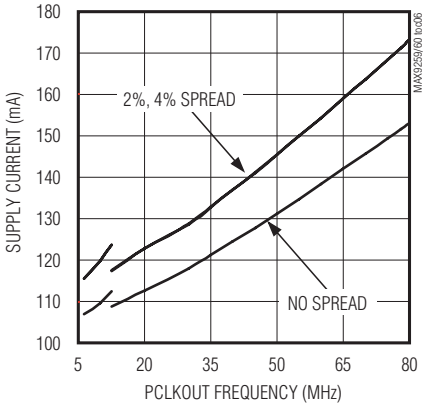
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (32-BIT MODE)



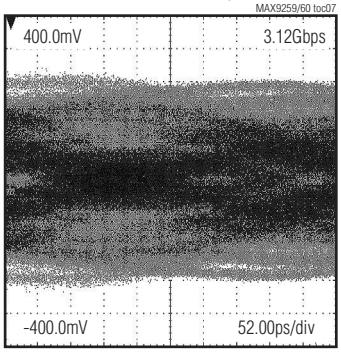
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (24-BIT MODE)



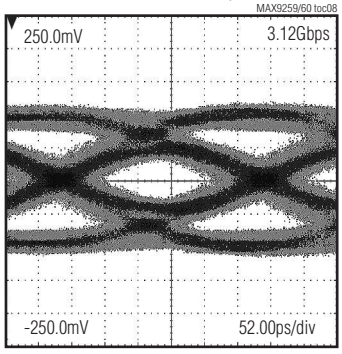
MAX9260 SUPPLY CURRENT vs. PCLKOUT FREQUENCY (32-BIT MODE)



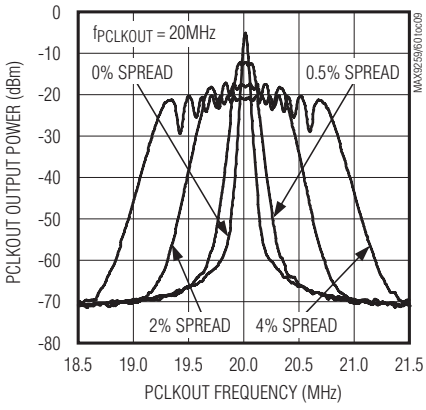
SERIAL LINK SWITCHING PATTERN WITHOUT PREEMPHASIS (PARALLEL BIT RATE = 104MHz, 10m STP CABLE)



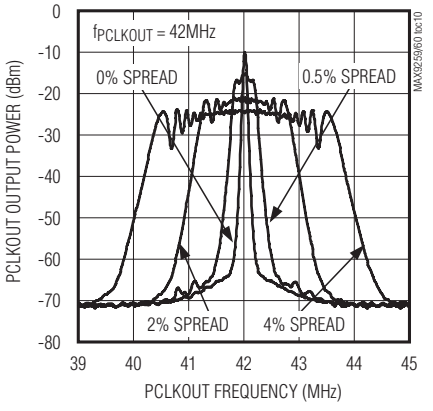
SERIAL LINK SWITCHING PATTERN WITH 14dB PREEMPHASIS (PARALLEL BIT RATE = 104MHz, 10m STP CABLE)



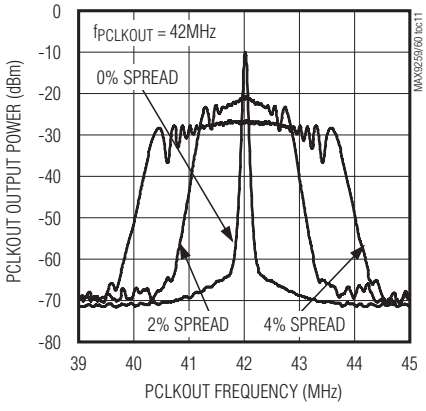
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (MAX9259 SPREAD ON, MAX9260 SPREAD OFF)



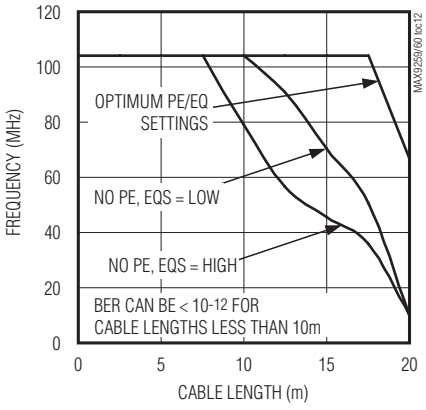
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (MAX9259 SPREAD ON, MAX9260 SPREAD OFF)



OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (MAX9260 SPREAD ON, MAX9259 SPREAD OFF)

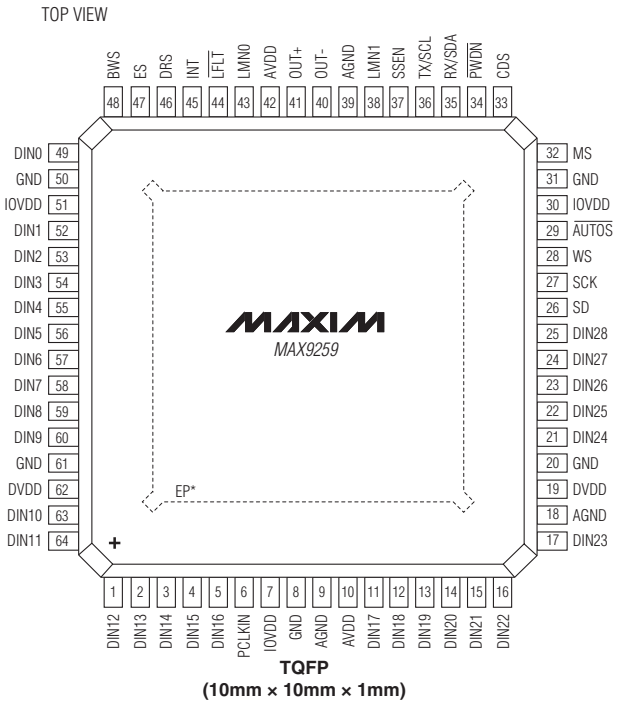


MAXIMUM PCLKIN FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-9})

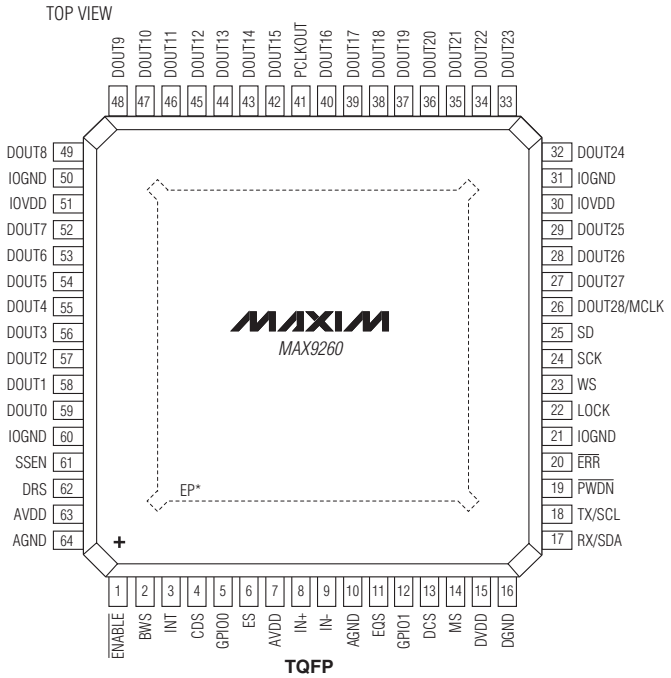


Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

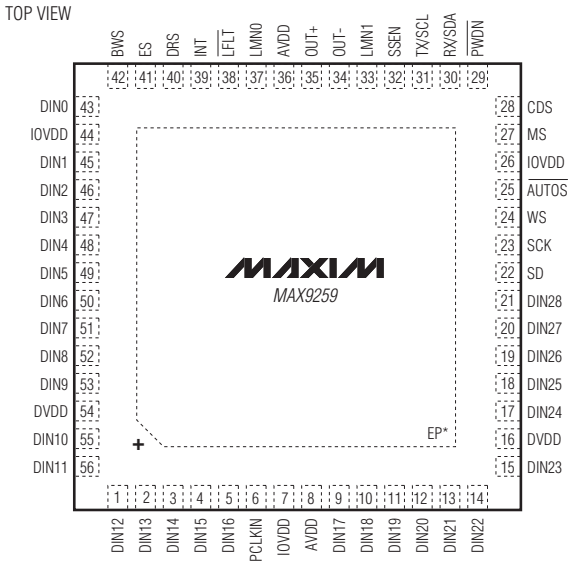
Pin Configurations



TQFP
(10mm × 10mm × 1mm)



TQFP
(10mm × 10mm × 1mm)



TQFN
(8mm x 8mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

MAX9259 Pin Description

PIN		NAME	FUNCTION
TQFP	TQFN		
1–5, 11–17, 21–25, 49, 52–60, 63, 64	1–5, 9–15, 17–21, 43, 45–53, 55, 56	DIN0–DIN28	Data Input[0:28]. Parallel data inputs. All pins internally pulled down to GND. Selected edge of PCLKIN latches input data. Set BWS = low (24-bit mode) to use DIN0–DIN20 (RGB and SYNC). DIN21–DIN28 are not used in 24-bit mode. Set BWS = high (32-bit mode) to use DIN0–DIN28 (RGB, SYNC, and two extra inputs).
6	6	PCLKIN	Parallel Clock Input. Latches parallel data inputs and provides the PLL reference clock.
7, 30, 51	7, 26, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to IOVDD.
8, 20, 31, 50, 61	—	GND	Digital and I/O Ground
9, 18, 39	—	AGND	Analog Ground
10, 42	8, 36	AVDD	1.8V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to AVDD.
19, 62	16, 54	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
26	22	SD	I^2S Serial-Data Input with Internal Pulldown to GND. Disable I^2S to use SD as an additional data input latched on the selected edge of PCLKIN.
27	23	SCK	I^2S Serial-Clock Input with Internal Pulldown to GND
28	24	WS	I^2S Word-Select Input with Internal Pulldown to GND
29	25	$\overline{\text{AUTOS}}$	Autostart Setting. Active-low power-up mode selection input requires external pulldown or pullup resistors. Set $\overline{\text{AUTOS}}$ = high to power up the device with no link active. Set $\overline{\text{AUTOS}}$ = low to have the MAX9259 power up the serial link with autorange detection (see Tables 13 and 14).
32	27	MS	Mode Select. Control-link mode-selection input requires external pulldown or pullup resistors. Set MS = low, to select base mode. Set MS = high to select the bypass mode.
33	28	CDS	Control-Direction Selection. Control-link-direction selection input requires external pulldown or pullup resistors. Set CDS = low for µC use on the MAX9259 side of the serial link. Set CDS = high for µC use on the MAX9260 side of the serial link.
34	29	$\overline{\text{PWDN}}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistors.
35	30	RX/SDA	Receive/Serial Data. UART receive or I^2C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9259's UART. In I^2C mode, RX/SDA is the SDA input/output of the MAX9259's I^2C master.

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

MAX9259 Pin Description (continued)

PIN		NAME	FUNCTION
TQFP	TQFN		
36	31	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9259's UART. In I²C mode, TX/SCL is the SCL output of the MAX9259's I²C master.
37	32	SSEN	Spread-Spectrum Enable. Serial link spread-spectrum enable input requires external pulldown or pullup resistors. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
38	33	LMN1	Line-Fault Monitor Input 1 (see Figure 3 for details)
40, 41	34, 35	OUT-, OUT+	Differential CML Output −/+. Differential outputs of the serial link.
43	37	LMN0	Line-Fault Monitor Input 0 (see Figure 3 for details)
44	38	$\overline{LFLT}$	Line Fault. Active-low open-drain line-fault output with a 60kΩ internal pullup resistor. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is high impedance when $\overline{PWDN}$ = low.
45	39	INT	Interrupt Output to Indicate Remote Side Requests. INT = low upon power-up and when $\overline{PWDN}$ = low. A transition on the INT input of the MAX9260 toggles the MAX9259's INT output.
46	40	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistors. Set DRS = high for parallel input data rates of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for parallel input data rates of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
47	41	ES	Edge Select. PCLKIN trigger edge-selection input requires external pulldown or pullup resistors. Set ES = low to trigger on the rising edge of PCLKIN. Set ES = high to trigger on the falling edge of PCLKIN.
48	42	BWS	Bus-Width Select. Parallel input bus-width selection input requires external pulldown or pullup resistors. Set BWS = low for 24-bit bus mode. Set BWS = high for 32-bit bus mode.
—	—	EP	Exposed Pad. EP internally connected to AGND (TQFP package) or AGND and GND (TQFN package). **MUST** externally connect EP to the AGND plane to maximize thermal and electrical performance.

MAX9260 Pin Description

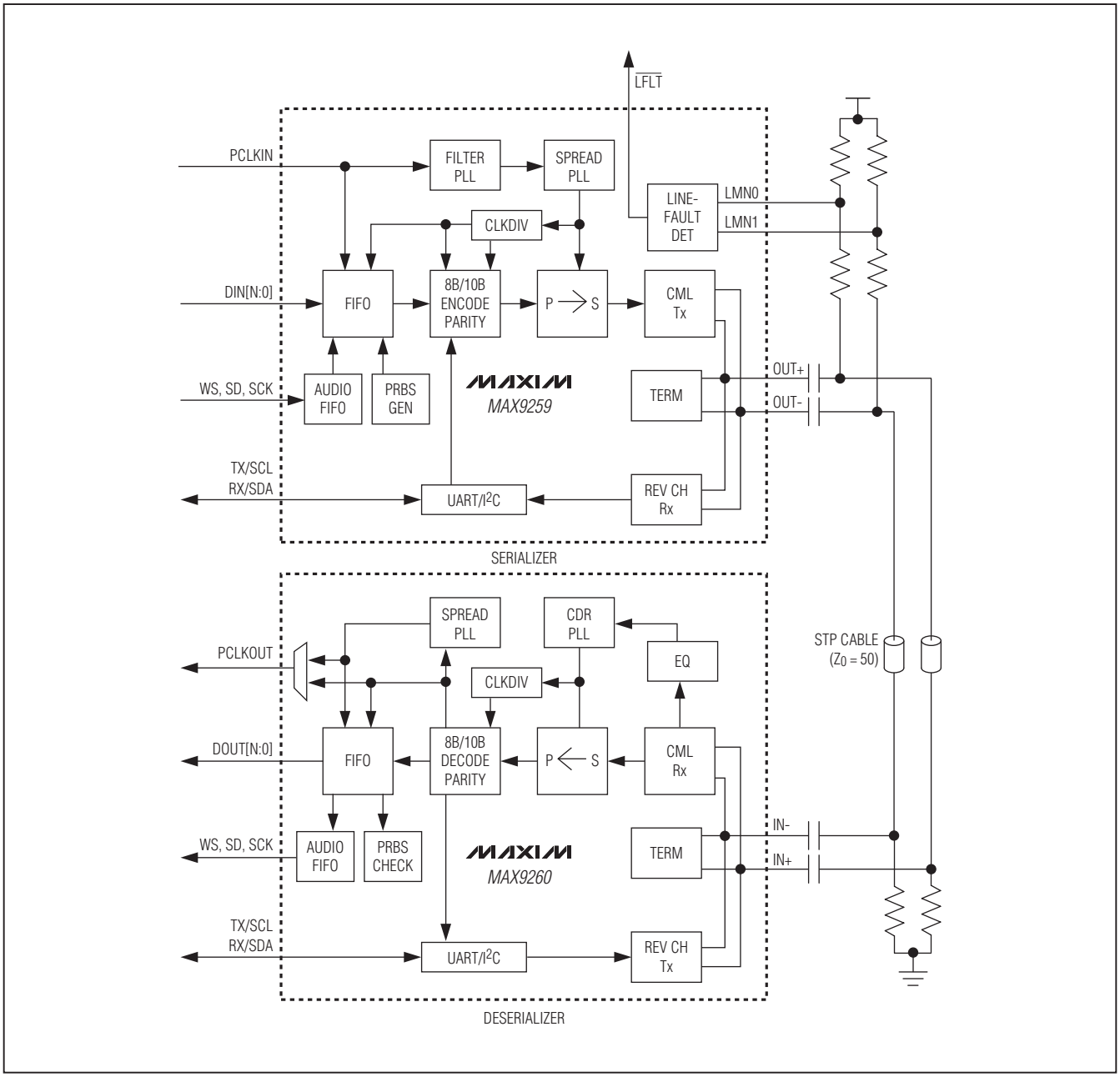
PIN	NAME	FUNCTION
1	$\overline{\text{ENABLE}}$	Enable. Active-low parallel output-enable input requires external pulldown or pullup resistors. Set $\overline{\text{ENABLE}}$ = low to enable PCLKOUT, SD, SCK, WS, and the parallel outputs, DOUT_. Set $\overline{\text{ENABLE}}$ = high to put PCLKOUT, SD, SCK, WS, and DOUT_ to high impedance.
2	BWS	Bus-Width Select. Parallel output bus-width selection input requires external pulldown or pullup resistors. Set BWS = low for 24-bit bus mode. Set BWS = high for 32-bit bus mode.
3	INT	Interrupt. Interrupt input requires external pulldown or pullup resistors. A transition on the INT input of the MAX9260 toggles the MAX9259's INT output.
4	CDS	Control-Direction Selection. Control-link-direction selection input requires external pulldown or pullup resistors. Set CDS = low for µC use on the MAX9259 side of the serial link. Set CDS = high for µC use on the MAX9260 side of the serial link.
5	GPIO0	GPIO0. Open-drain general-purpose input/output with internal 60kΩ pullup resistors to IOVDD. GPIO0 is high impedance during power-up and when $\overline{\text{PWDN}}$ = low.
6	ES	Edge Select. PCLKOUT edge-selection input requires external pulldown or pullup resistors. Set ES = low for a rising-edge trigger. Set ES = high for a falling-edge trigger.
7, 63	AVDD	3.3V Analog Power Supply. Bypass AVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to AVDD.
8 , 9	IN+, IN-	Differential CML Input +/−. Differential inputs of the serial link.
10, 64	AGND	Analog Ground
11	EQS	Equalizer Select. Deserializer equalizer-selection input requires external pulldown or pullup resistors. The state of EQS latches upon power-up or rising edge of $\overline{\text{PWDN}}$. Set EQS = low for 10.7dB equalizer boost (EQTUNE = 1001). Set EQS = high for 5.2dB equalizer boost (EQTUNE = 0100).
12	GPIO1	GPIO1. Open-drain general-purpose input/output with internal 60kΩ pullup resistors to IOVDD. GPIO1 is high impedance during power-up and when $\overline{\text{PWDN}}$ = low.
13	DCS	Drive Current Select. Driver current-selection input requires external pulldown or pullup resistors. Set DCS = high for stronger parallel data and clock output drivers. Set DCS = low for normal parallel data and clock drivers (see the *MAX9260 DC Electrical Characteristics* table).
14	MS	Mode Select. Control-link mode-selection/autostart mode selection input requires external pulldown or pullup resistors. MS sets the control-link mode when CDS = high (see the *Control-Channel and Register Programming* section). Set MS = low to select base mode. Set MS = high to select the bypass mode. MS sets autostart mode when CDS = low (see Tables 13 and 14).
15	DVDD	3.3V Digital Power Supply. Bypass DVDD to DGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
16	DGND	Digital Ground
17	RX/SDA	Receive/Serial Data. UART receive or I^2C serial-data input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9260's UART. In I^2C mode, RX/SDA is the SDA input/output of the MAX9259's I^2C master.

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

MAX9260 Pin Description (continued)

PIN	NAME	FUNCTION
18	TX/SCL	Transmit/Serial Clock. UART transmit or I²C serial-clock output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9259's UART. In I²C mode, TX/SCL is the SCL output of the MAX9260's I²C master.
19	$\overline{PWDN}$	Power-Down. Active-low power-down input requires external pulldown or pullup resistors.
20	$\overline{ERR}$	Error. Active-low open-drain video data error output with internal pullup to IOVDD. $\overline{ERR}$ goes low when the number of decoding errors during normal operation exceed a programmed error threshold or when at least one PRBS error is detected during PRBS test. $\overline{ERR}$ is high impendence when $\overline{PWDN}$ = low.
21, 31, 50, 60	IOGND	Input/Output Ground
22	LOCK	Open-Drain Lock Output with Internal Pullup to IOVDD. LOCK = high indicates PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates PLLs are not locked or incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active. LOCK is high impedance when $\overline{PWDN}$ = low.
23	WS	Word Select. I²S word-select output.
24	SCK	Serial Clock. I²S serial-clock output
25	SD	Serial Data. I²S serial-data output. Disable I²S to use SD as an additional data output latched on the selected edge of PCLKOUT.
26–29, 32–40, 42–49, 52–59	DOUT0–DOUT27, DOUT28/MCLK	Data Output[0:28]. Parallel data outputs. Output data can be strobed on the selected edge of PCLKOUT. Set BWS = low (24-bit mode) to use DOUT0–DOUT20 (RGB and SYNC). DOUT21–DOUT28 are not used in 24-bit mode and are set to low. Set BWS = high (32-bit mode) to use DOUT0–DOUT28 (RGB, SYNC, and two extra outputs). DOUT28 can be used to output MCLK (see the *Additional MCLK Output for Audio Applications* section).
30, 51	IOVDD	1.8V to 3.3V Logic I/O Power Supply. Bypass IOVDD to IOGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to IOVDD.
41	PCLKOUT	Parallel Clock Output. Used for DOUT0–DOUT28.
61	SSEN	Spread-Spectrum Enable. Parallel output spread-spectrum enable input requires external pulldown or pullup resistors. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±2% spread spectrum on the parallel outputs. Set SSEN = low to use the parallel outputs without spread spectrum.
62	DRS	Data-Rate Select. Data-rate range-selection input requires external pulldown or pullup resistors. Set DRS = high for parallel input data rates of 8.33MHz to 16.66MHz (24-bit mode) or 6.25MHz to 12.5MHz (32-bit mode). Set DRS = low for parallel input data rates of 16.66MHz to 104MHz (24-bit mode) or 12.5MHz to 78MHz (32-bit mode).
—	EP	Exposed Pad. EP internally connected to AGND. **MUST** externally connect EP to the AGND plane to maximize thermal and electrical performance.

Functional Diagram



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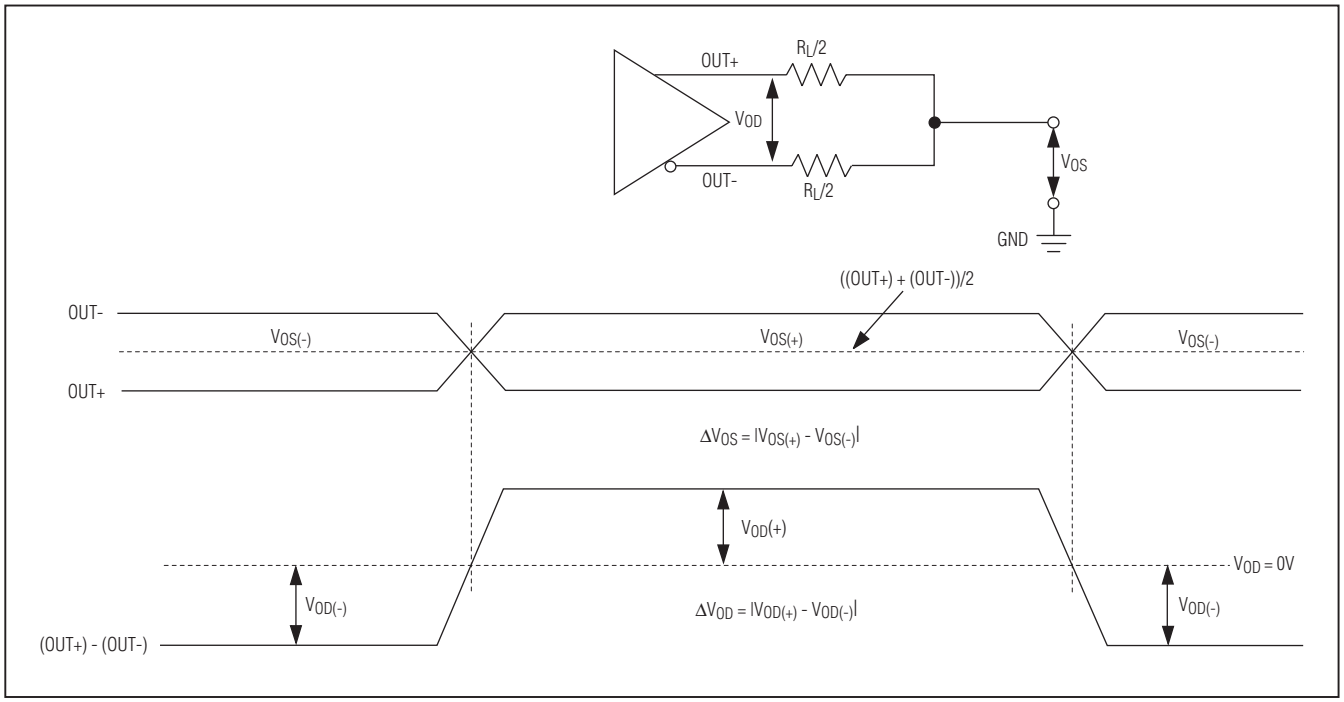

Figure 1. MAX9259 Serial Output Parameters

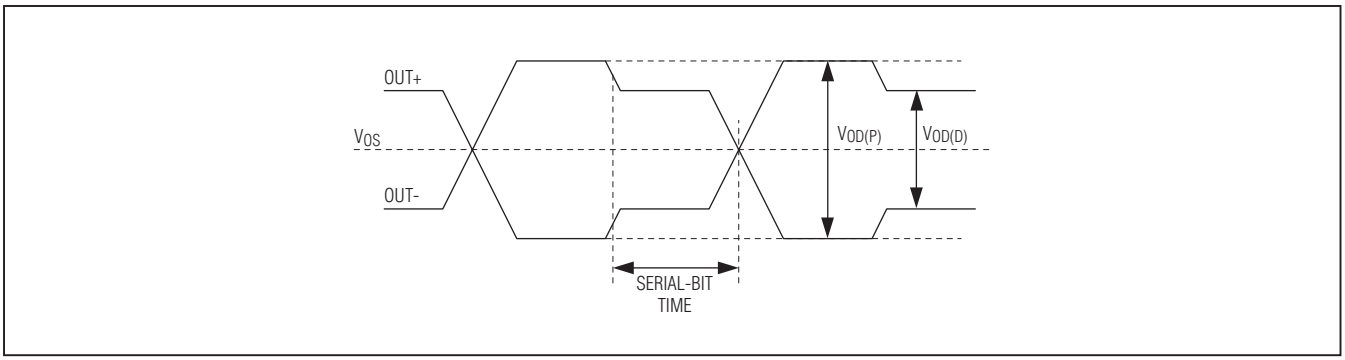

Figure 2. Output Waveforms at OUT+ and OUT-

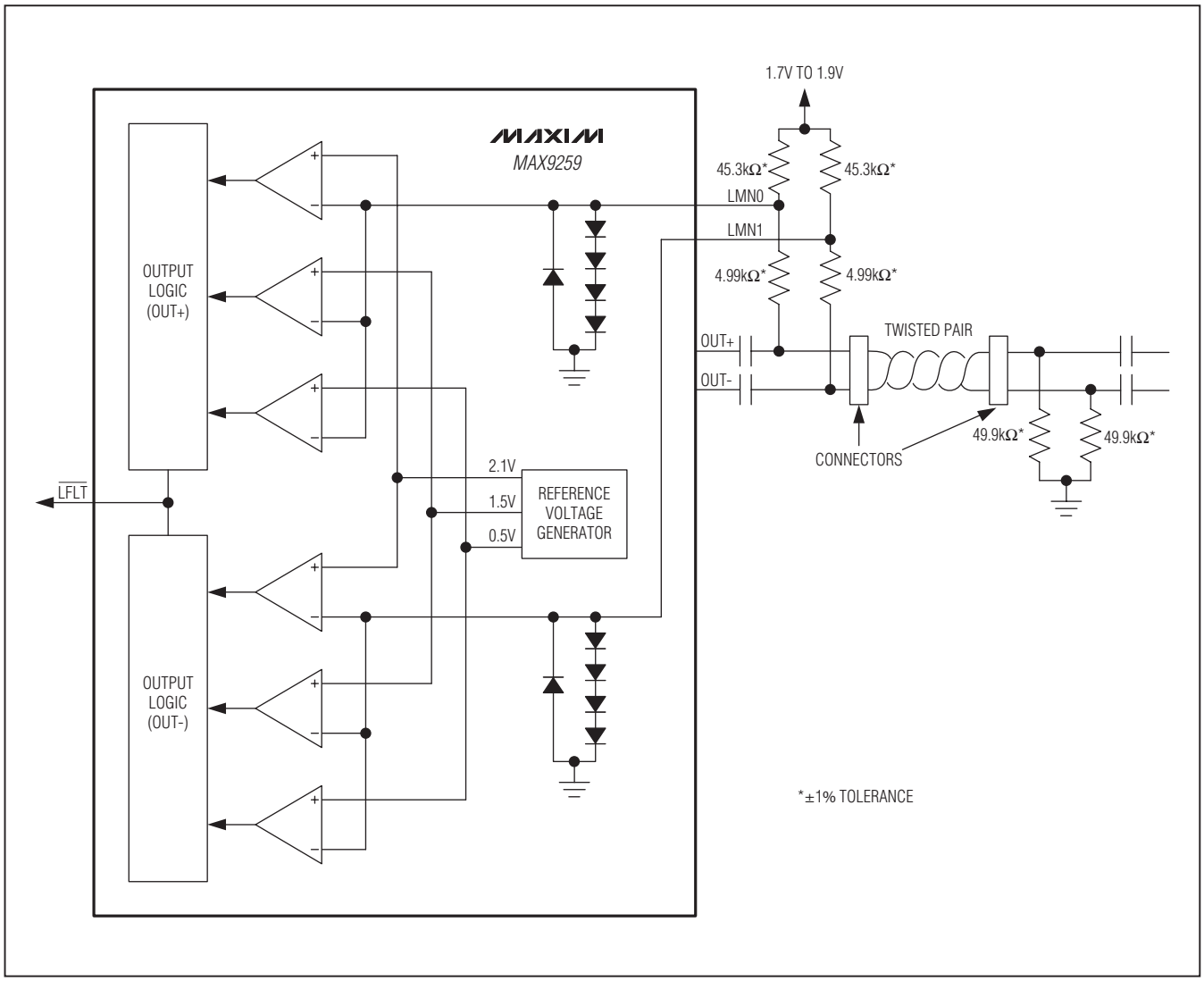

Figure 3. Fault-Detector Circuit

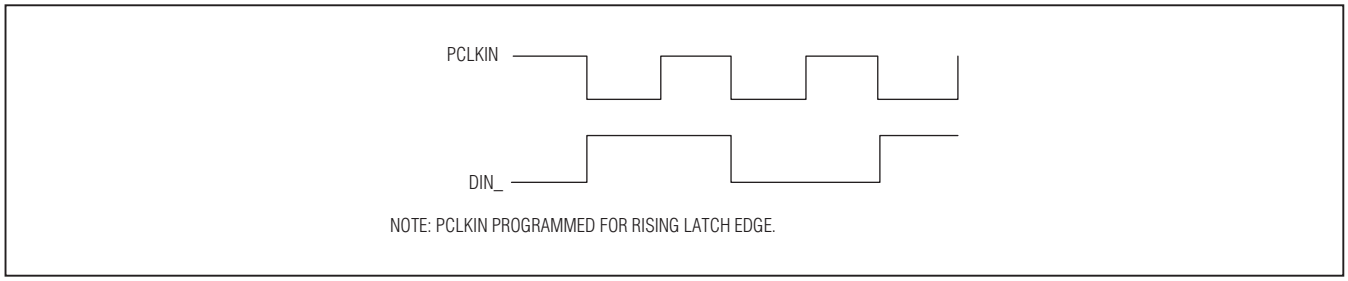

Figure 4. MAX9259 Worst-Case Pattern Input

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

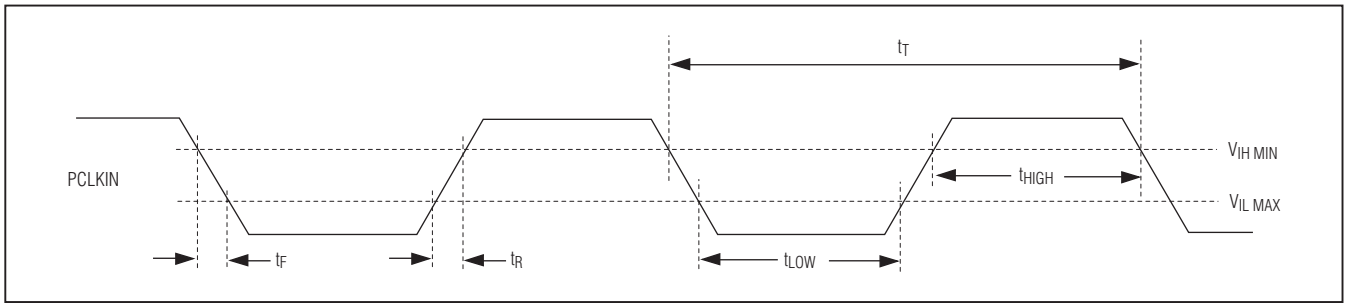

Figure 5. MAX9259 Parallel Input Clock Requirements

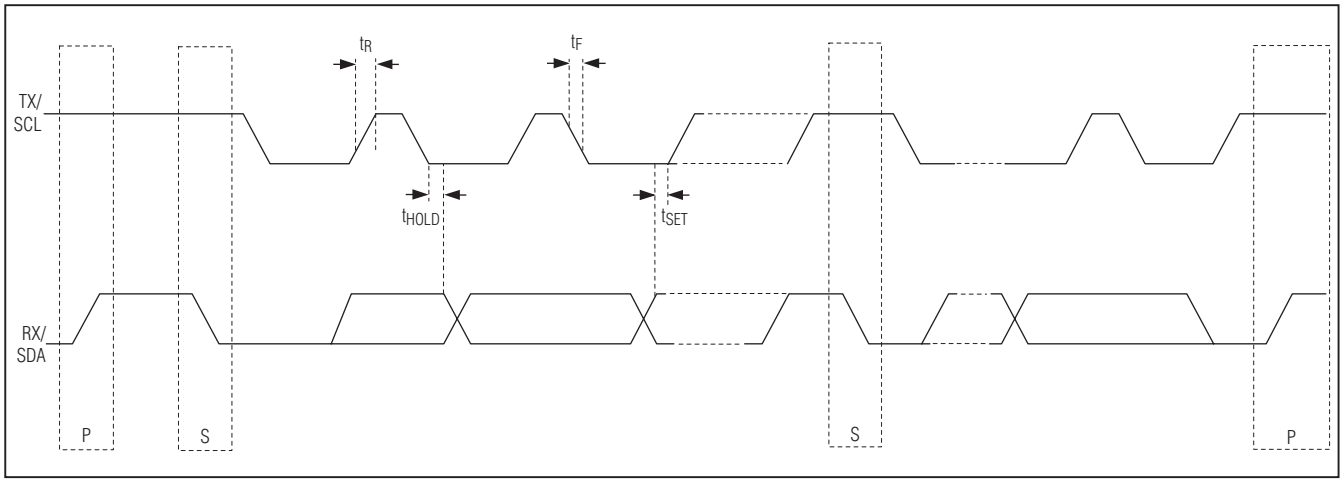

Figure 6. I²C Timing Parameters

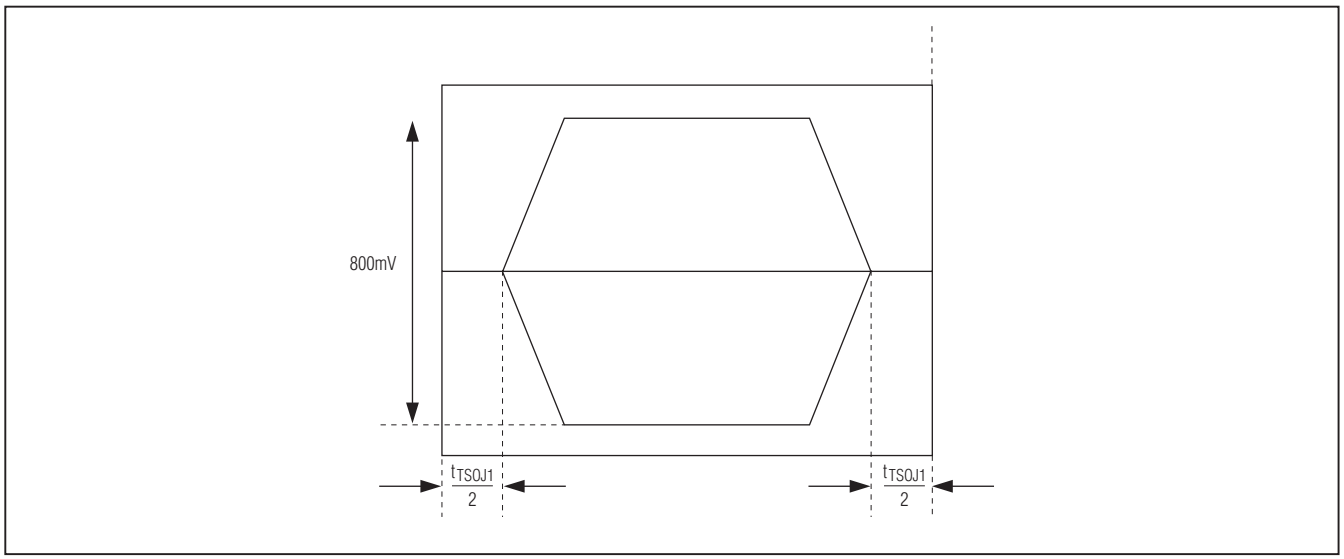

Figure 7. Differential Output Template

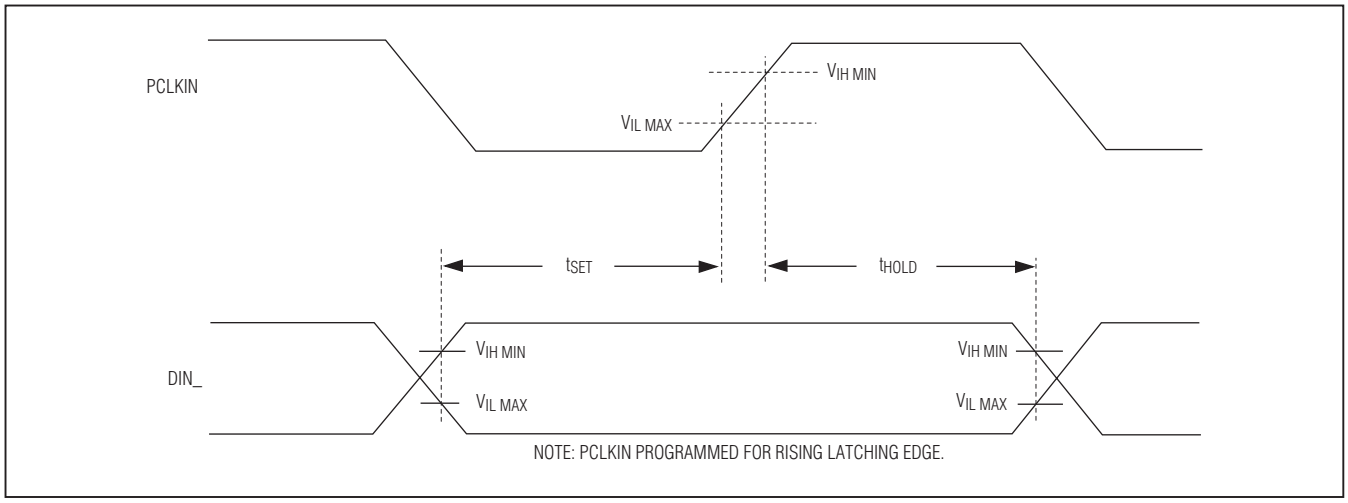

Figure 8. MAX9259 Input Setup-and-Hold Times

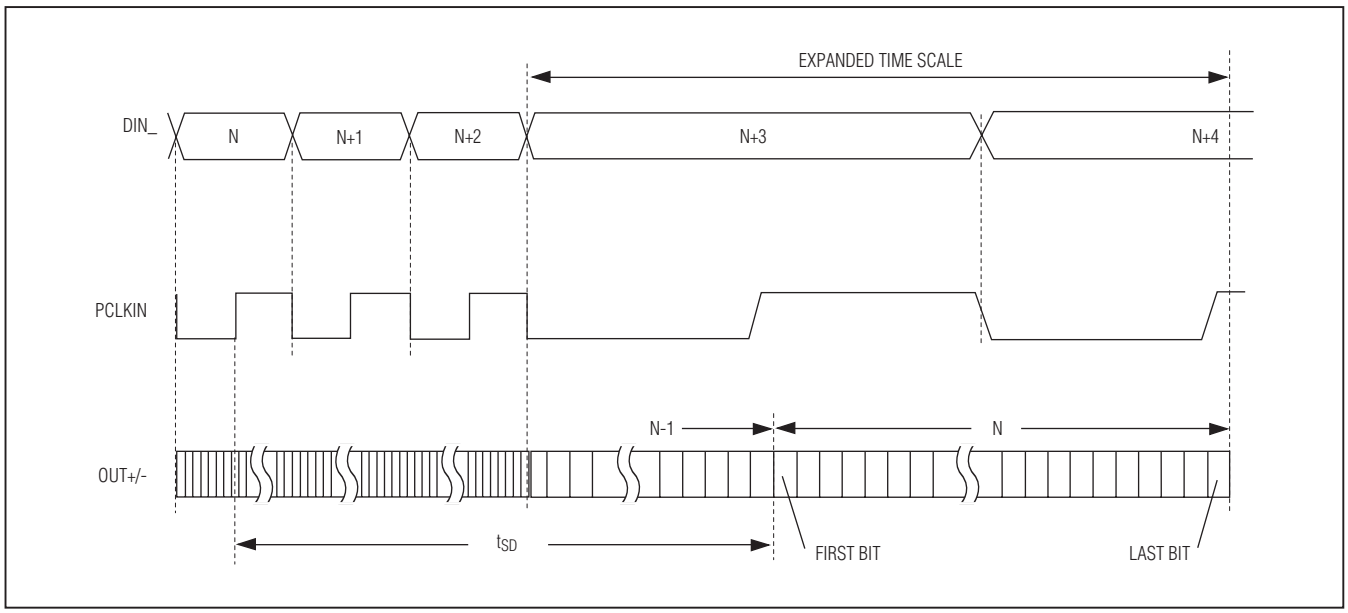

Figure 9. MAX9259 Serializer Delay

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

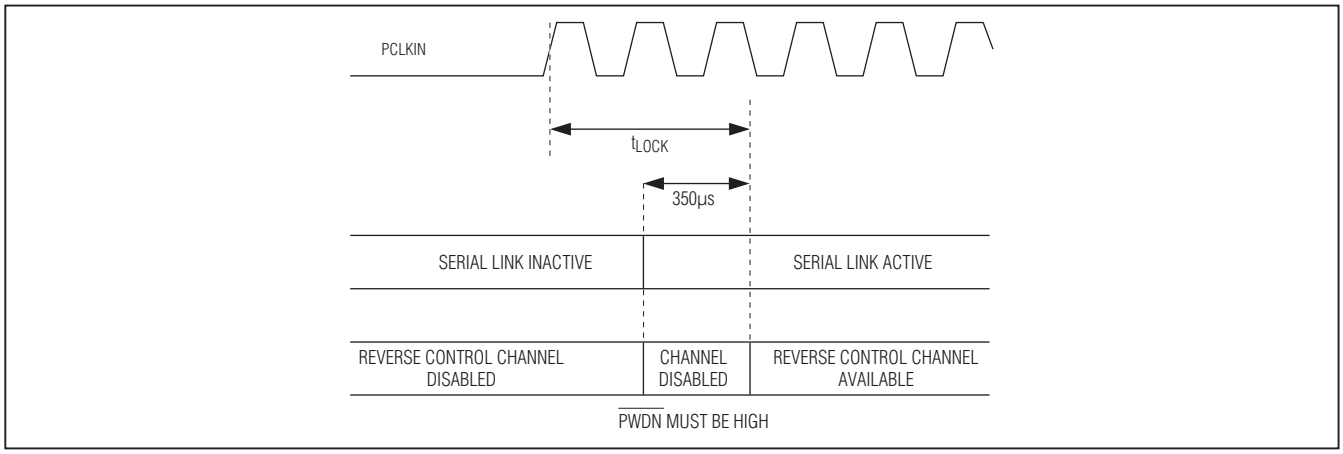

Figure 10. MAX9259 Link Startup Time

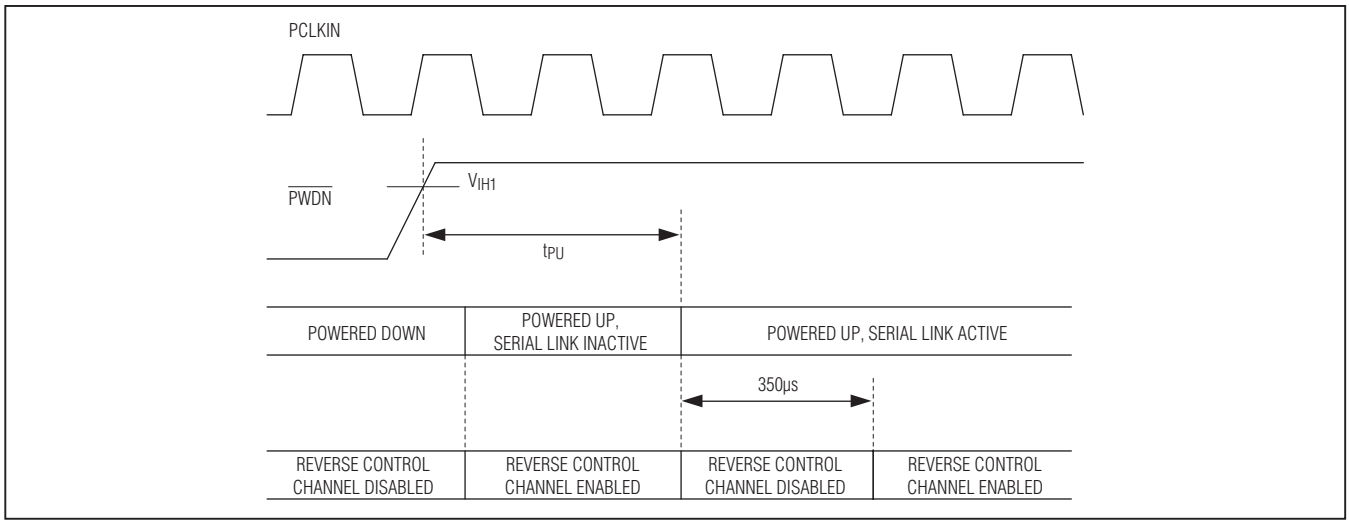

Figure 11. MAX9259 Power-Up Delay

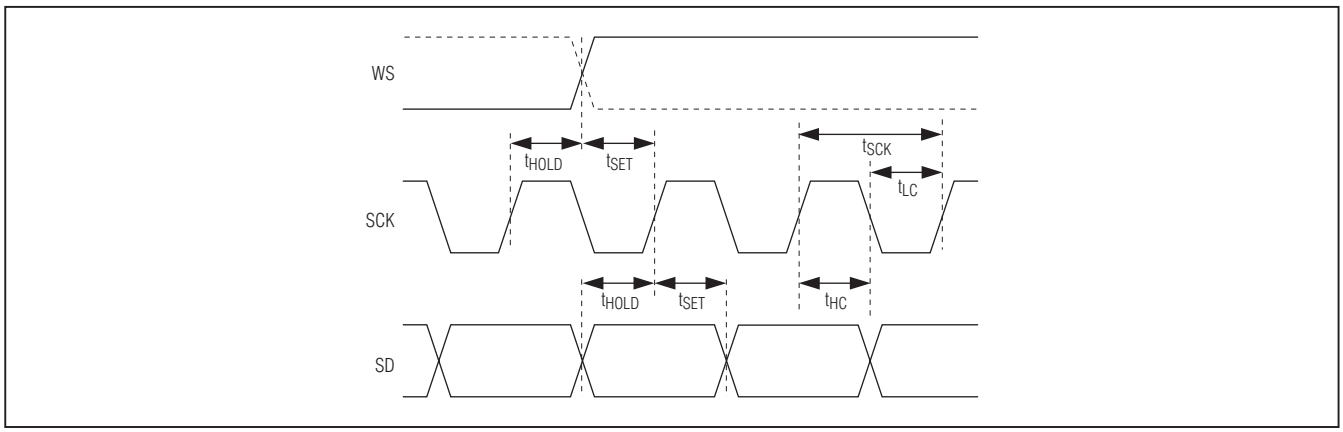

Figure 12. MAX9259 Input I²S Timing Parameters

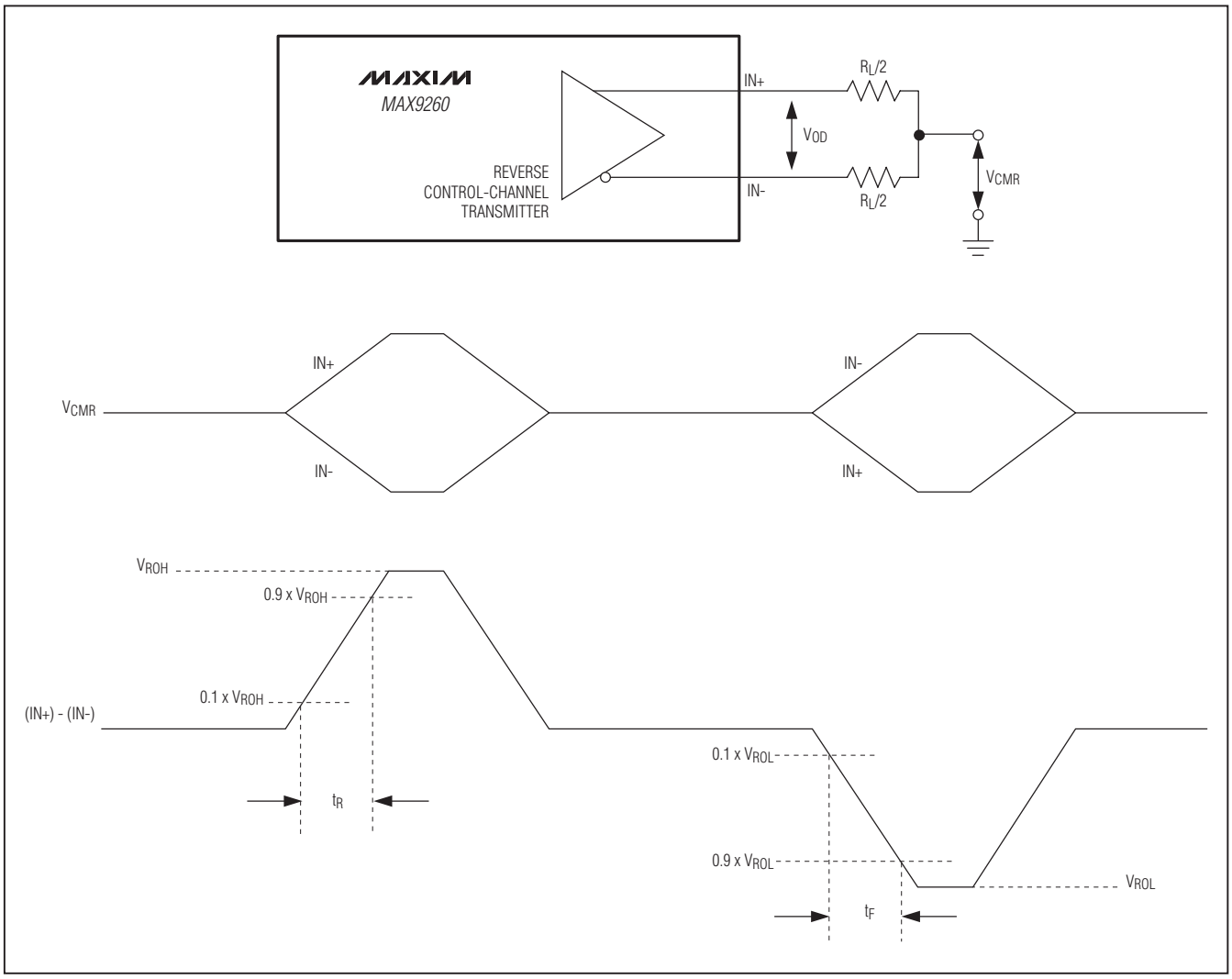

Figure 13. MAX9260 Reverse Control-Channel Output Parameters

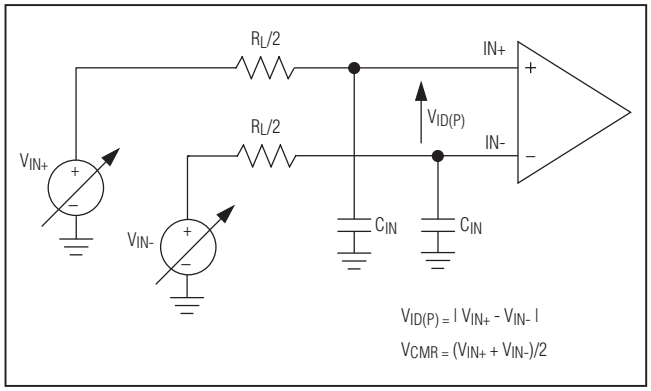

Figure 14. MAX9260 Test Circuit for Differential Input Measurement

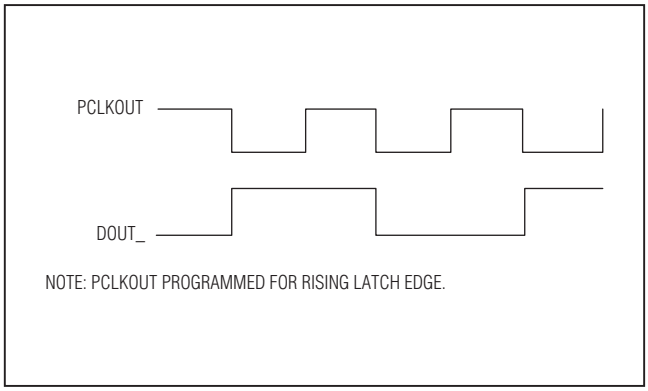

Figure 15. MAX9260 Worst-Case Pattern Output

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

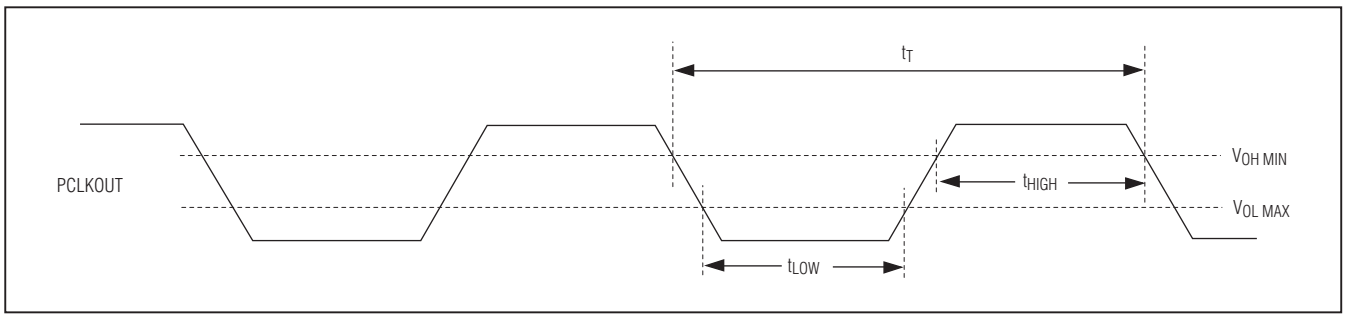

Figure 16. MAX9260 Clock Output High-and-Low Times

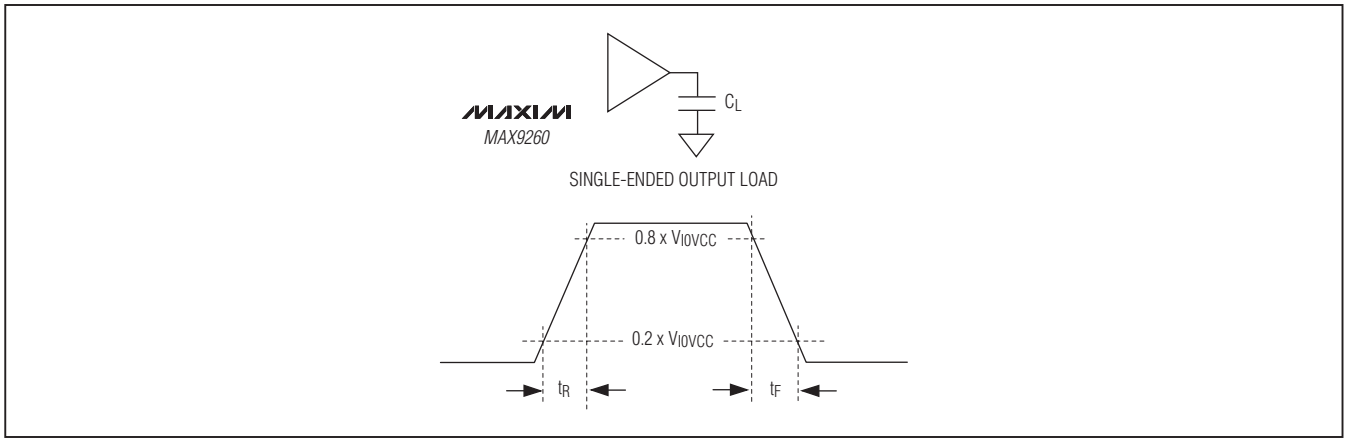

Figure 17. MAX9260 Output Rise-and-Fall Times

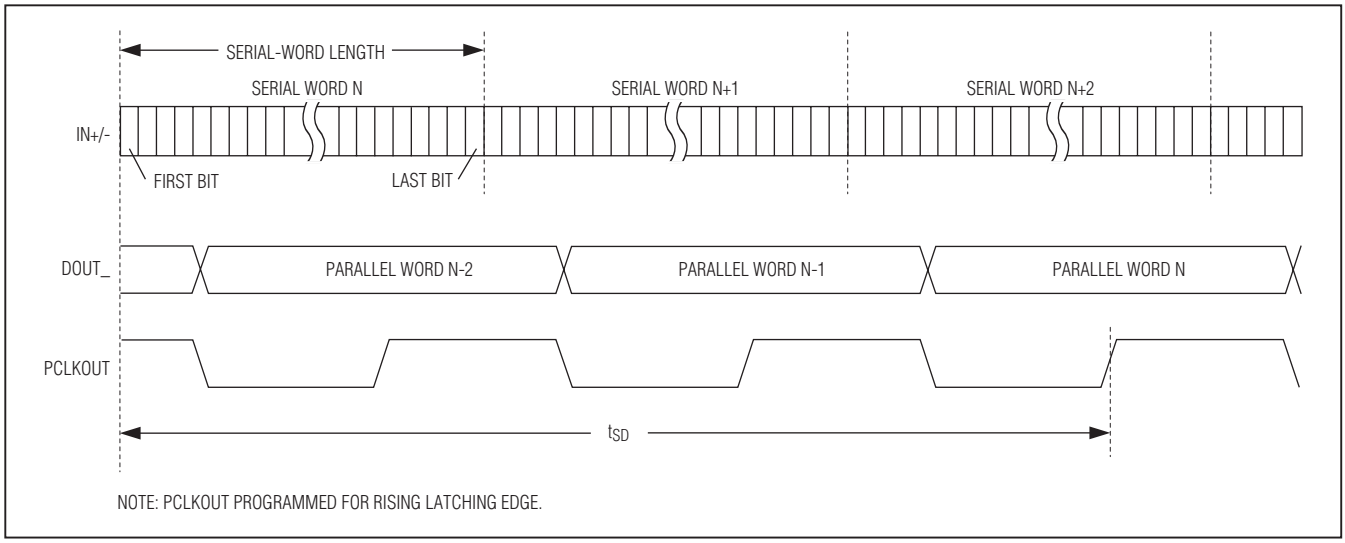

Figure 18. MAX9260 Deserializer Delay

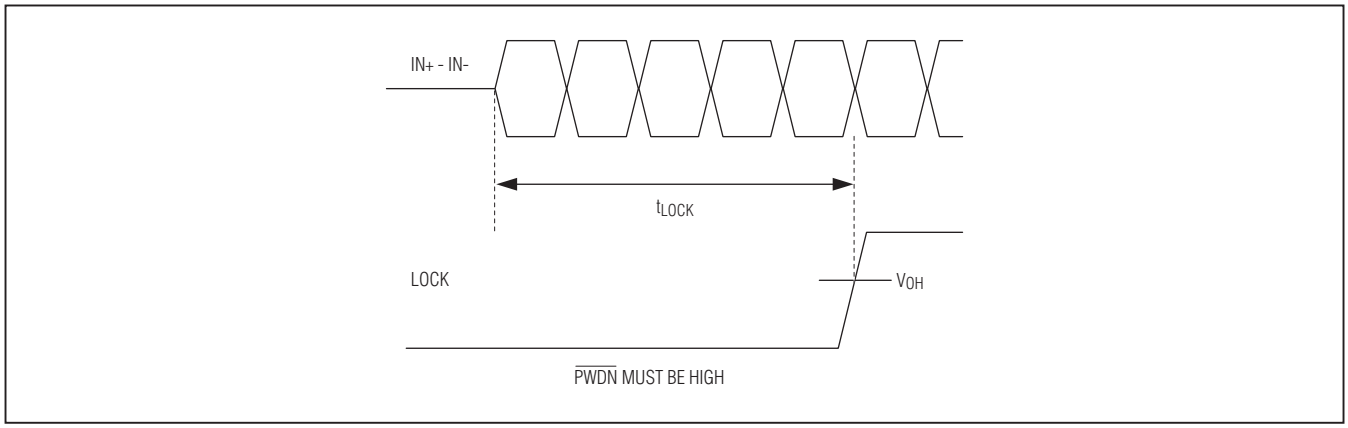

Figure 19. MAX9260 Lock Time

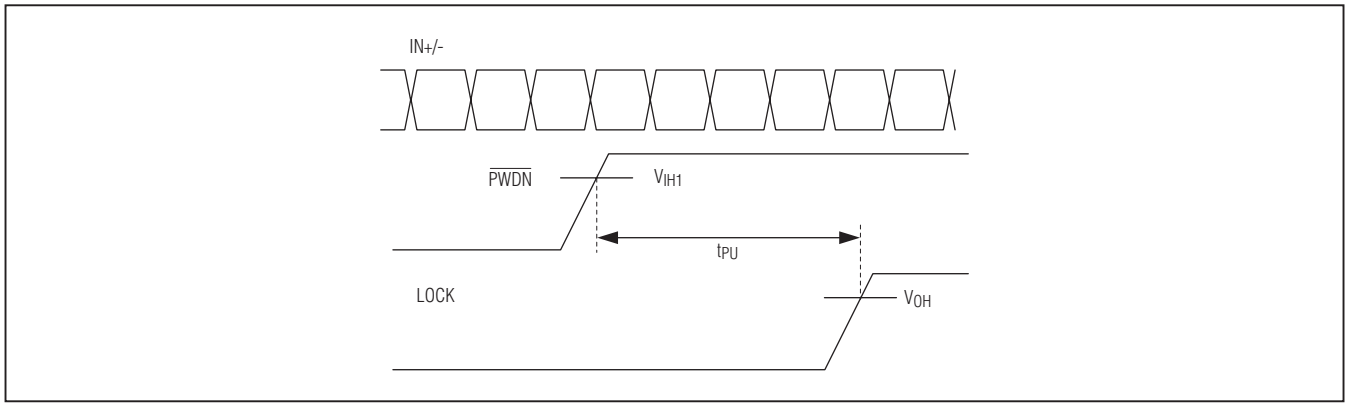

Figure 20. MAX9260 Power-Up Delay

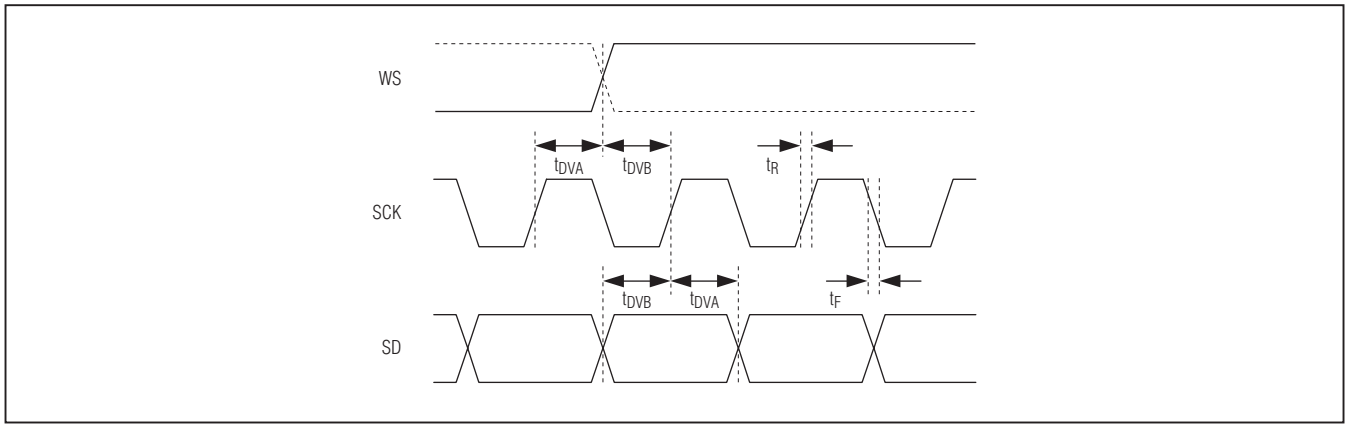

Figure 21. MAX9260 Output I²S Timing Parameters

Gigabit Multimedia Serial Link with Spread Spectrum and Full-Duplex Control Channel

Detailed Description

The MAX9259/MAX9260 chipset presents Maxim's GMSL technology. The MAX9259 serializer pairs with the MAX9260 deserializer to form a complete digital serial link for joint transmission of high-speed video, audio, and control data for video-display or image-sensing applications. The serial-payload data rate can reach up to 2.5Gbps for a 15m STP cable. The parallel interface is programmable for 24-bit or 32-bit width modes at the maximum bus clock of 104MHz or 78MHz, respectively. The minimum bus clock is 6.25MHz for the 32-bit mode and 8.33MHz for the 24-bit mode. With such a flexible data configuration, the GMSL is able to support XGA (1280 x 768) or dual-view WVGA (2 x 854 x 480) display panels. For image sensing, it supports three 10-bit camera links simultaneously with a pixel clock up to 78MHz. The 24-bit mode handles 21-bit data and control signals plus an I²S audio signal. The 32-bit mode handles 29-bit data and control signals plus an I²S audio signal. Any combination and sequence of color video data, video sync, and control signals make up the 21-bit or 29-bit parallel data on DIN_ and DOUT_. The I²S port supports the sampled audio data at a rate from 8kHz to 192kHz and the audio word length of anywhere between 4 to 32 bits. The embedded control channel forms a UART link between the serializer and deserializer. The UART link can be set to half-duplex mode or full-duplex mode depending on the application. The GMSL supports UART rates from 100kbps to 1Mbps. Using this control link, a host ECU or µC communicates with the serializer and deserializer, as well as the peripherals in the remote side, such as backlight control, grayscale gamma correction, camera module, and touch screen. All serial communication (forward and reverse) uses differential signaling. The peripheral programming uses I²C format or the default GMSL UART format. A separate bypass mode enables communication using a full-duplex, user-defined UART format. The control link between the MAX9259 and MAX9260 allows µC connectivity to either device or peripherals to support video-display or image-sensing applications.

The AC-coupled serial link uses 8B/10B coding. The MAX9259 serializer features a programmable driver preemphasis and the MAX9260 deserializer features a programmable channel equalizer to extend the link length and enhance the link reliability. Both devices have a programmable spread-spectrum feature for reducing EMI on the serial link output (MAX9259) and parallel data outputs (MAX9260). The differential serial link input and output pins comply with the ISO 10605 and IEC 61000-4-2 ESD-protection standards. The core supplies for the MAX9259/MAX9260 are 1.8V and 3.3V, respectively. Both devices use an I/O supply from 1.8V to 3.3V

Register Mapping

The µC configures various operating conditions of the GMSL through registers in the MAX9259/MAX9260. The default device addresses stored in the R0 and R1 registers of the MAX9259/MAX9260 are 0x80 and 0x90, respectively. Write to the R0/R1 registers in both devices to change the device address of the MAX9259 or MAX9260.

Table 1. MAX9259 Power-Up Default Register Map (see Table 18)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID =1000000, serializer device address is 1000 000 RESERVED = 0
0x01	0x90	DESID =1001000, deserializer device address is 1001 000 RESERVED = 0
0x02	0x1F, 0x3F	SS = 000 (SSEN = low), SS = 001 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up AUDIOEN = 1, I²S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking SDIV = 000000, auto calibrate sawtooth divider

Table 1. MAX9259 Power-Up Default Register Map (see Table 18) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x04	0x03, 0x13, 0x83, or 0x93	SEREN = 0 ($\overline{AUTOS}$ = high), SEREN = 1 ($\overline{AUTOS}$ = low), serial link enable default depends on $\overline{AUTOS}$ pin state at power-up CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0 or 1, sleep mode state depends on CDS and $\overline{AUTOS}$ pin state at power-up (see the *Link Startup Procedure* section) INTTYPE = 00, base mode uses I^2C REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)
0x05	0x70	I2CMETHOD = 0, I^2C packets include register address DISFPLL = 1, filter PLL disabled CMLLVL = 11, 400mV CML signal level PREEMP = 0000, preemphasis disabled
0x06	0x40	RESERVED = 01000000
0x07	0x22	RESERVED = 00100010
0x08	0x0A (read only)	RESERVED = 0000 LFNEG = 10, no faults detected LFPOS = 10, no faults detected
0x0D	0x0F	SETINT = 0, interrupt output set to low RESERVED = 0001111
0x1E	0x01 (read only)	ID = 00000001, device ID is 0x01
0x1F	0x0X (read only)	RESERVED = 0000 REVISION = XXXX, revision number

Table 2. MAX9260 Power-Up Default Register Map (see Table 19)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID =1000000, serializer device identifier is 1000 000 RESERVED = 0
0x01	0x90	DESID =1001000, deserializer device identifier is 1001 000 RESERVED = 0
0x02	0x1F or 0x5F	SS = 00 (SSEN = low), SS = 01 (SSEN = high), spread-spectrum settings depend on SSEN pin state at power-up RESERVED = 0 AUDIOEN = 1, I^2S channel enabled PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate