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EVALUATION KIT AVAILABLE

MAX9271

16-Bit GMSL Serializer with Coax or STP Cable Drive

General Description

The MAX9271 compact serializer is designed to drive 50Ω coax or 100Ω shielded twisted-pair (STP) cable. The device pairs with the MAX9272 deserializer.

The parallel input is programmable for single or double input. Double input allows higher pixel clock input frequency by registering two pixels of typical image-sensor video data before serializing. This doubles the maximum pixel clock frequency compared to single input.

The device features an embedded control channel that operates at 9.6kbps to 1Mbps in UART and mixed UART/I²C modes, and up to 400kbps in I²C mode. Using the control channel, a microcontroller (µC) is capable of programming serializer, deserializer, and camera (or any peripheral) registers at any time, independent of video timing. There is one dedicated GPIO, four optional GPIOs, and a GPO output, allowing remote power-up of a camera module, camera frame synchronization, and other uses. Error-detection and correction coding are programmable.

For driving longer cables, the device has programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 32-pin (5mm x 5mm) TQFN-EP package with 0.5mm lead pitch and operates over the -40°C to +105°C temperature range.

Applications

Automotive Camera Systems

***Ordering Information* and *Typical Application Circuit* appear at end of data sheet.**

Benefits and Features

- **Ideal for Camera Applications**
  - **Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP**
  - **Error Detection/Correction**
  - **9.6kbps to 1Mbps Control Channel in I²C-to-I²C Mode with Clock Stretch Capability**
  - **Best-in-Class Supply Current: 75mA (max)**
  - **Double-Rate Clock for Megapixel Cameras**
  - **Serializer Pre/Deemphasis Allows 15m Cable at Full Speed**
  - **32-Pin (5mm x 5mm) TQFN Package with 0.5mm Lead Pitch**
- **High-Speed Data Serialization for Megapixel Cameras**
  - **Up to 1.5Gbps Serial-Bit Rate with Single or Double Input: 6.25MHz to 100MHz Clock**
- **Multiple Control-Channel Modes for System Flexibility**
  - **9.6kbps to 1Mbps Control Channel in UART-to-UART or UART-to-I²C Modes**
- **Reduces EMI and Shielding Requirements**
  - **Output Programmable for 100mV to 500mV Single-Ended or 100mV to 400mV Differential**
  - **Programmable Spread Spectrum on the Serial Output Reduces EMI**
  - **Bypassable Input PLL for Parallel Clock Jitter Attenuation**
  - **Tracks Spread Spectrum on Parallel Input**
- **Peripheral Features for Camera Power-Up and Verification**
  - **Built-In PRBS Generator for BER Testing of the Serial Link**
  - **Up to Five GPIO Ports**
  - **Dedicated "Up/Down" GPO for Camera Frame Sync Trigger and Other Uses**
  - **Remote/Local Wake-Up from Sleep Mode**
- **Meets Rigorous Automotive and Industrial Requirements**
  - **-40°C to +105°C Operating Temperature**
  - **±10kV Contact and ±15kV IEC 61000-4-2 ESD Protection**
  - **±10kV Contact and ±30kV Air ISO 10605 ESD Protection**

For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX9271.related.**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6385; Rev 1; 11/12

MAX9271

16-Bit GMSL Serializer with Coax or STP Cable Drive

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ABSOLUTE MAXIMUM RATINGS*

AVDD to EP ..... -0.5V to +1.9V
DVDD to EP ..... -0.5V to +1.9V
IOVDD to EP ..... -0.5V to +3.9V
OUT+, OUT- to EP ..... -0.5V to +1.9V
All other pins to EP ..... -0.5V to (V_{IOVDD} + 0.5V)
OUT+, OUT- short circuit to ground or supply ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.5mW/°C above +70°C) 2758.6mW
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**EP connected to PCB ground.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (LCCEN, DIN_, PCLKIN, HS, VS, MS/HVEN, $\overline{PWDN}$)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		20	µA
THREE-LEVEL LOGIC INPUTS (CONF0, CONF1)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Midlevel Input Current	I_{INM}	(Note 2)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUT (GPO)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN INPUTS/OUTPUTS (RX/SDA/EDC, TX/SCL/DBL, GPIO_)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 3)	RX/SDA, TX/SCL	-110		+1	µA
			GPIO_	-80		+1	
			EDC, DBL, BWS	-10		+20	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
DIFFERENTIAL SERIAL OUTPUTS (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV
		3.3dB preemphasis setting (Figure 2)		350		610	
		3.3dB deemphasis setting (Figure 2)		240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}					25	mV
Output Offset Voltage, (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}					25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From V_{OUT+}, V_{OUT-} to V_{AVDD}		45	54	63	Ω
SINGLE-ENDED SERIAL OUTPUTS (OUT+, OUT-)							
Single-Ended Output Voltage	V_{OUT}	Preemphasis off, high drive (Figure 3)		375	500	625	mV
		3.3dB preemphasis setting, high drive (Figure 2)		435		765	
		3.3dB deemphasis setting, high drive (Figure 2)		300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V				32	
Output Termination Resistance (Internal)	R_O	From V_{OUT+}, V_{OUT-} to V_{AVDD}		45	54	63	Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L= 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REVERSE CONTROL-CHANNEL RECEIVER OUTPUTS (OUT+, OUT-)							
High Switching Threshold	V_{CHR}					27	mV
Low Switching Threshold	V_{CLR}			-27			mV
POWER SUPPLY							
Worst-Case Supply Current (Figure 4)	I_{WCS}	Single input, BWS = 0	f_{PCLKIN} = 25MHz		44	65	mA
			f_{PCLKIN} = 50MHz		46	75	
		Double input, BWS = 0	f_{PCLKIN} = 50MHz		45	65	
			f_{PCLKIN} = 100MHz		56	75	
Sleep Mode Supply Current	I_{CCS}	Single wake-up receiver enabled			40	100	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = EP			5	70	µA
ESD PROTECTION							
OUT+, OUT- (Note 4)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±10			
			Air discharge	±15			
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±10			
			Air discharge	±30			
All Other Pins (Note 5)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4			kV

AC ELECTRICAL CHARACTERISTICS

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (PCLKIN)						
Clock Frequency	f_{PCLKIN}	BWS = 1, DRS = 1	6.25		12.5	MHz
		BWS = 0, DRS = 1	8.33		16.66	
		BWS = 1, DRS = 0	12.5		37.5	
		BWS = 0, DRS = 0	16.66		50	
		BWS = 1, DRS = 0, 15-bit double input	25		75	
		BWS = 0, DRS = 0, 11-bit double input	33.33		100	
Clock Duty Cycle	DC_	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 5, Note 6)	35	50	65	%
Clock Transition Time	t_R, $t_{F\_}$	(Figure 5, Note 6)			4	ns
Clock Jitter	t_J	1.5Gbps bit rate, 300kHz sinusoidal jitter			800	ps (pk-pk)

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C)

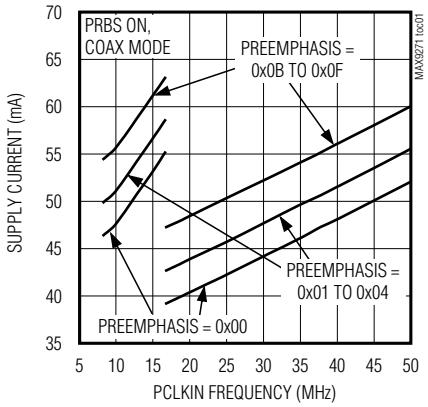
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C/UART AND GPIO PORT TIMING							
I²C/UART Bit Rate				9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD		20		120	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD.		20		120	ns
Input Setup Time	t_{SET}	I²C only (Figure 6, Note 6)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 6, Note 6)		0			ns
SWITCHING CHARACTERISTICS (Note 6)							
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400Mv, R_L = 100Ω, serial-bit rate = 1.5Gbps				250	ps
Total Serial Output Jitter (Differential Output)	t_{TSOJ1}	1.5Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)			0.25		UI
Deterministic Serial Output Jitter (Differential Output)	t_{DSOJ2}	1.5Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)			0.15		UI
Total Serial Output Jitter (Single-Ended Output)	t_{TSOJ1}	1.5Gbps PRBS signal, measured at V_O/2, preemphasis disabled (Figure 3)			0.25		UI
Deterministic Serial Output Jitter (Single-Ended Output)	t_{DSOJ2}	1.5Gbps PRBS signal, measured at V_O/2, preemphasis disabled (Figure 3)			0.15		UI
Parallel Data Input Setup Time	t_{SET}	(Figure 8)		2			ns
Parallel Data Input Hold Time	t_{HOLD}	(Figure 8)		1			ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (Figure 9)				350	µs
Serializer Delay (Note 7)	t_{SD}	(Figure 10)	Spread spectrum enabled			6880	Bits
			Spread spectrum disabled			3040	
Link Start Time	t_{LOCK}	(Figure 11)				2	ms
Power-Up Time	t_{PU}	(Figure 12)				7	ms

Note 2: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.
Note 3: I_{IN} min due to voltage drop across the internal pullup resistor.
Note 4: Specified pin to ground.
Note 5: Specified pin to all supply/ground.
Note 6: Guaranteed by design and not production tested.
Note 7: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = 0. Bit time = 1/(40 x f_{PCLKIN}) for BWS = 1.

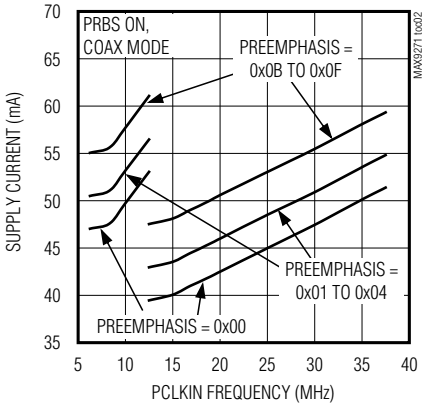
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, DBL = low, T_A = +25°C, unless otherwise noted.)

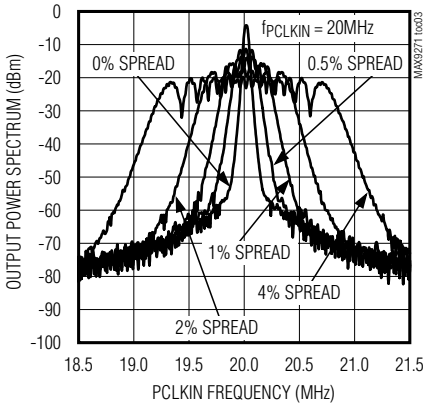
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = 0)



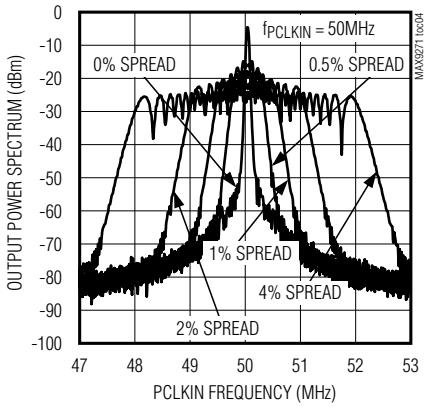
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = 1)



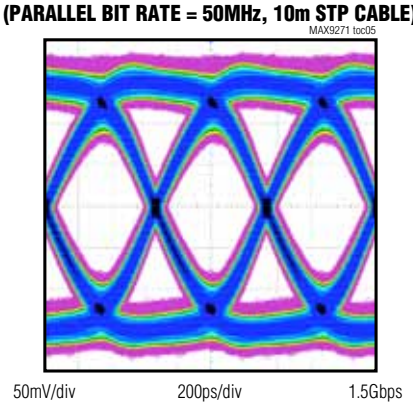
OUTPUT POWER SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)



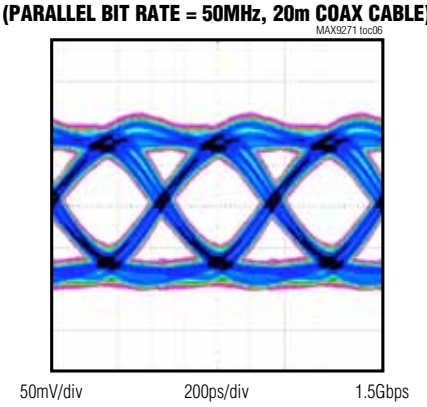
OUTPUT POWER SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)



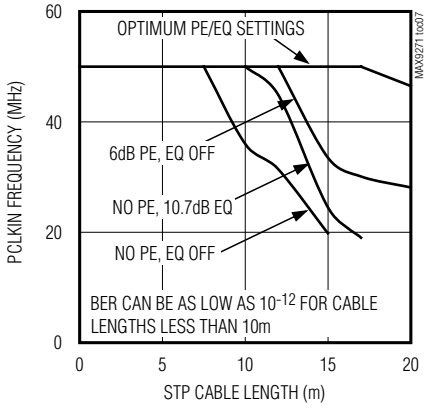
SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALLEL BIT RATE = 50MHz, 10m STP CABLE)



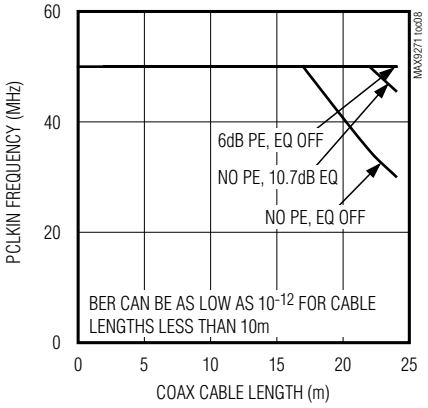
SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALLEL BIT RATE = 50MHz, 20m COAX CABLE)



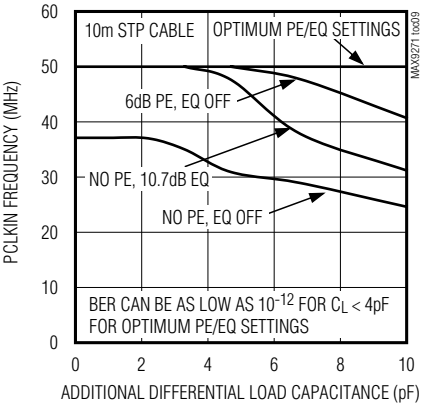
MAXIMUM PCLKIN FREQUENCY vs. STP CABLE LENGTH (BER ≤ 10^{-10})



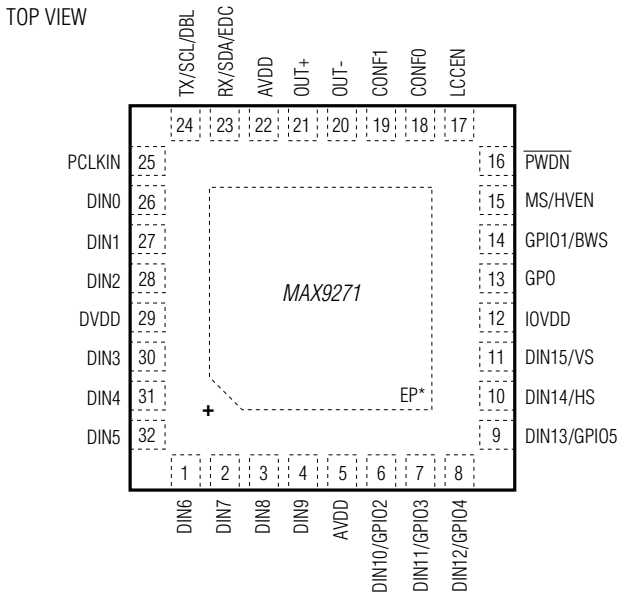
MAXIMUM PCLKIN FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



MAXIMUM PCLKIN FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER < 10^{-10})



Pin Configuration



TQFN
(5mm x 5mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

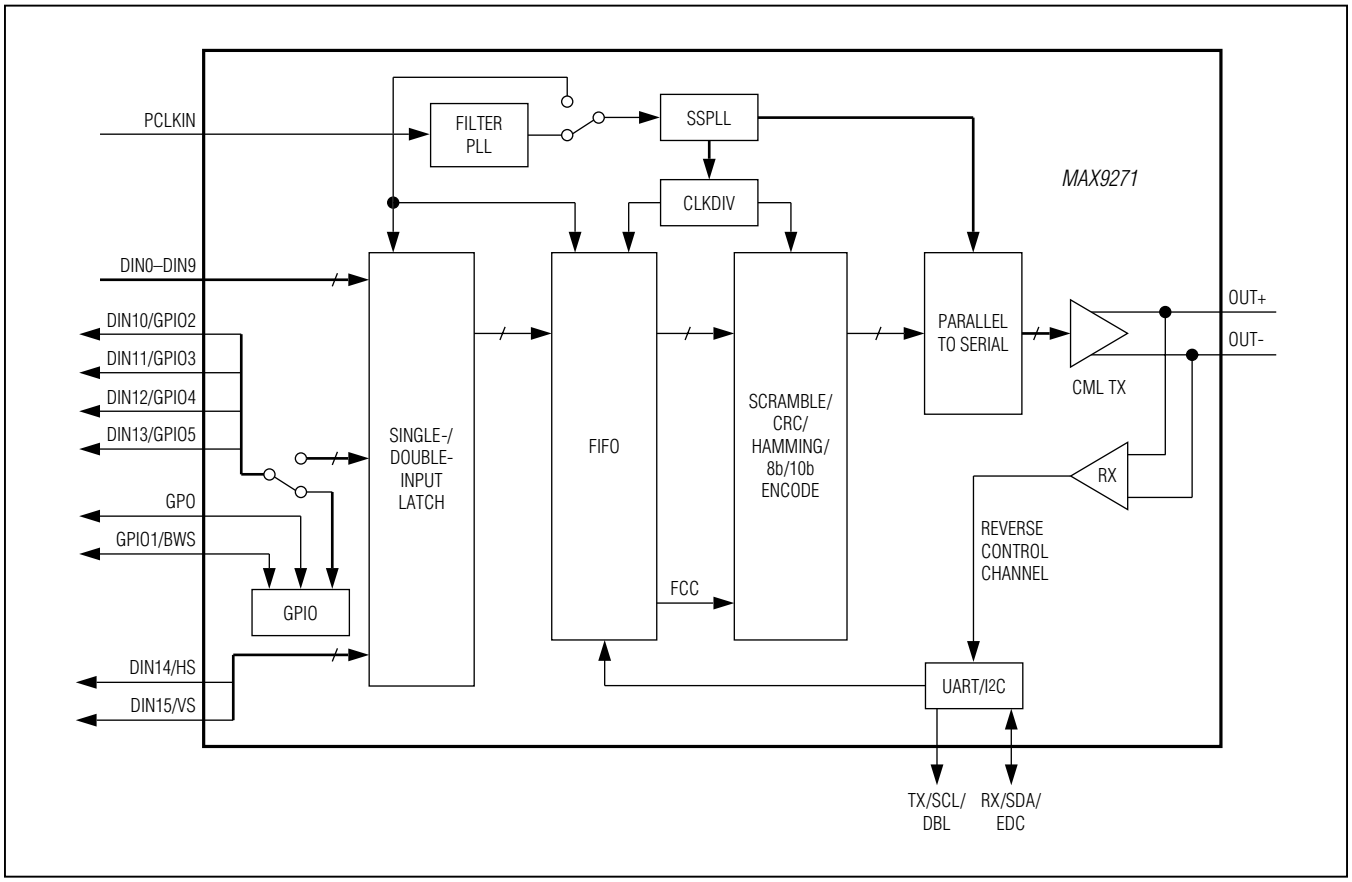
Pin Description

PIN	NAME	FUNCTION
1–4, 26, 27, 28, 30, 31, 32	DIN0–DIN9	Parallel Data Inputs with Internal Pulldown to EP
5, 22	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
6–9	DIN10/ GPIO2–DIN13/ GPIO5	Parallel Data Inputs/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to EP. GPIO_ has an open-drain output with internal 60kΩ pullup to IOVDD. See Table 1 for programming details.
10	DIN14/HS	Parallel Data Input/Horizontal Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Horizontal sync input when VS/HS encoding is enabled (Table 2).
11	DIN15/VS	Parallel Data Input/Vertical Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Vertical sync input when VS/HS encoding is enabled (Table 2).
12	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.

Pin Description (continued)

PIN	NAME	FUNCTION
13	GPO	General-Purpose Output. GPO follows the GMSL deserializer GPI (or INT) input. GPO = low upon power-up and when $\overline{PWDN}$ = low.
14	GPIO1/BWS	GPIO/Bus Width Select Input. Function is determined by the state of LCCEN (Table 13). GPIO1 (LCCEN = high): Open-drain, general-purpose input/output with internal 60kΩ pullup to IOVDD. BWS (LCCEN = low): Input with internal pulldown to EP. Set BWS = low for 22-bit input latch. Set BWS = high for 30-bit input latch.
15	MS/HVEN	Mode Select/HS and VS Encoding Enable with Internal Pulldown to EP. Function is determined by the state of LCCEN (Table 13). MS (LCCEN = high): Set MS = low to select base mode. Set MS = high to select the bypass mode. HVEN (LCCEN = low): Set HVEN = high to enable HS/VS encoding on DIN14/HS and DIN15/VS. Set HVEN = low to use DIN14/HS and DIN15/VS as parallel data inputs.
16	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
17	LCCEN	Local Control-Channel Enable Input with Internal Pulldown to EP. LCCEN = high enables the control-channel interface pins. LCCEN = low disables the control-channel interface pins and selects an alternate function on the indicated pins (Table 13).
18	CONF0	Configuration 0. Three-level configuration input (Table 9).
19	CONF1	Configuration 1. Three-level configuration input (Table 9).
20	OUT-	Inverting Coax/Twisted-Pair Serial Output
21	OUT+	Noninverting Coax/Twisted-Pair Serial Output
23	RX/SDA/EDC	Receive/Serial Data/Error-Detection/Correction. Function is determined by the state of LCCEN (Table 13). RX/SDA (LCCEN = high): Input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In I²C mode, RX/SDA is the SDA input/output of the serializer's I²C master/slave. RX/SDA has an open-drain driver and requires a pullup resistor. EDC (LCCEN = low): Input with internal pulldown to EP. Set EDC = high to enable error-detection correction. Set EDC = low to disable error-detection correction.
24	TX/SCL/DBL	Transmit/Serial Clock/Double Mode. Function is determined by the state of LCCEN (Table 13). TX/SCL (LCCEN = high): Input/output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In the I²C mode, TX/SCL is the SCL input/output of the serializer's I²C master/slave. TX/SCL has an open-drain driver and requires a pullup resistor. DBL (LCCEN = low): Input with internal pulldown to EP. Set DBL = high to use double-input mode. Set DBL = low to use single-input mode.
25	PCLKIN	Parallel Clock Input with Internal Pulldown to EP. Latches parallel data inputs and provides the PLL reference clock.
29	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
—	EP	Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



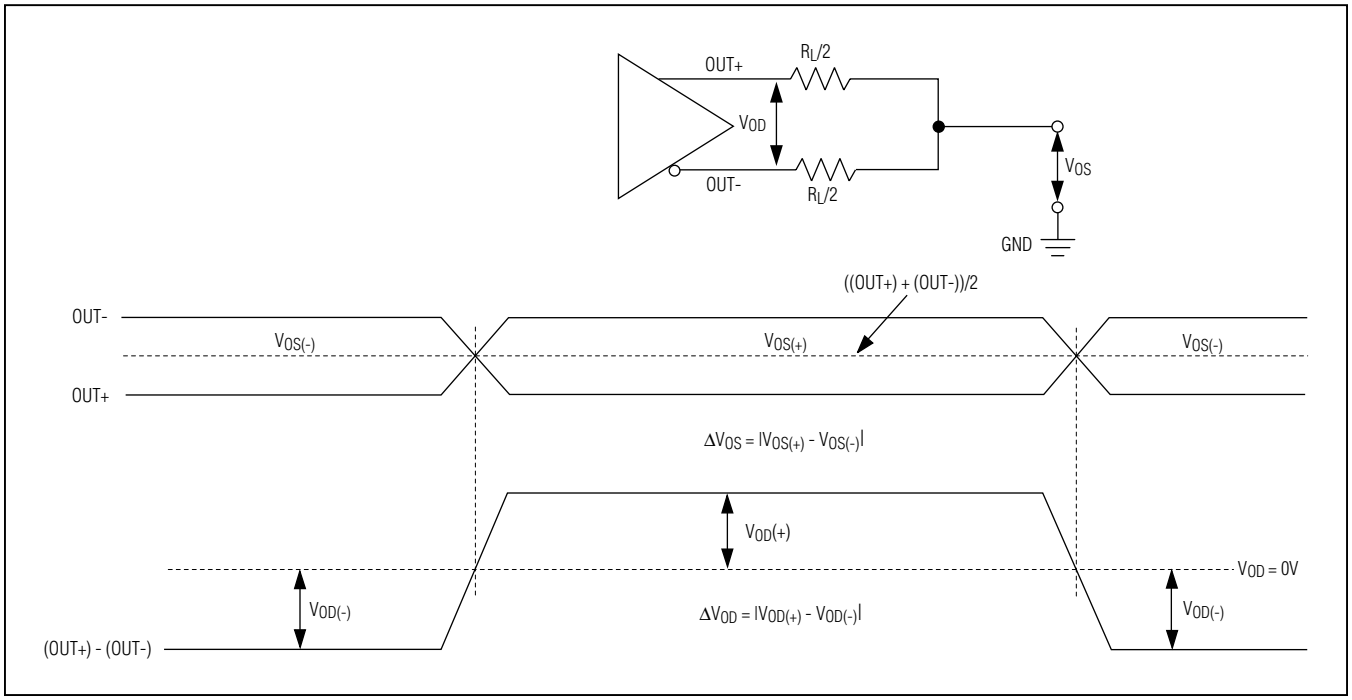


Figure 1. Serial-Output Parameters

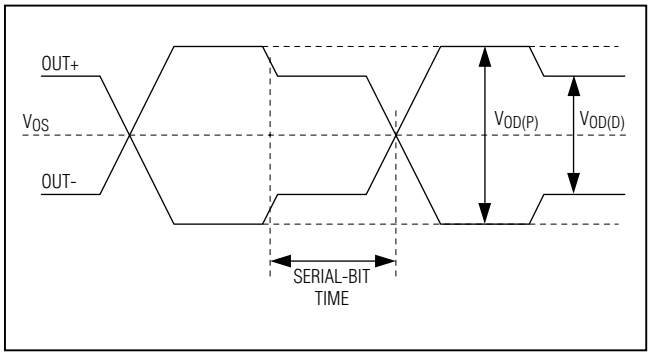


Figure 2. Output Waveforms at OUT+, OUT-

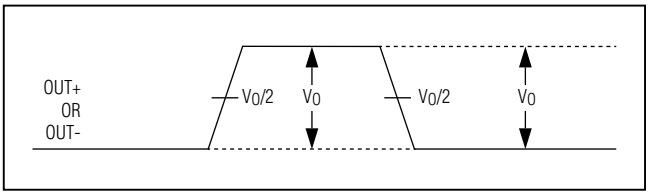


Figure 3. Single-Ended Output Template

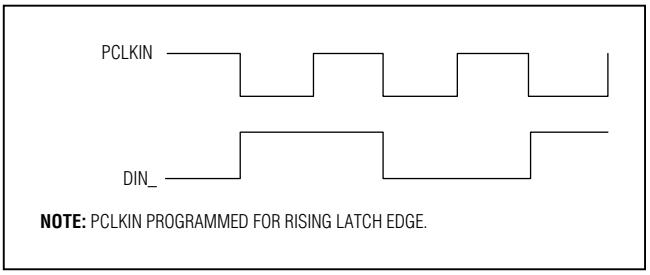


Figure 4. Worst-Case Pattern Input

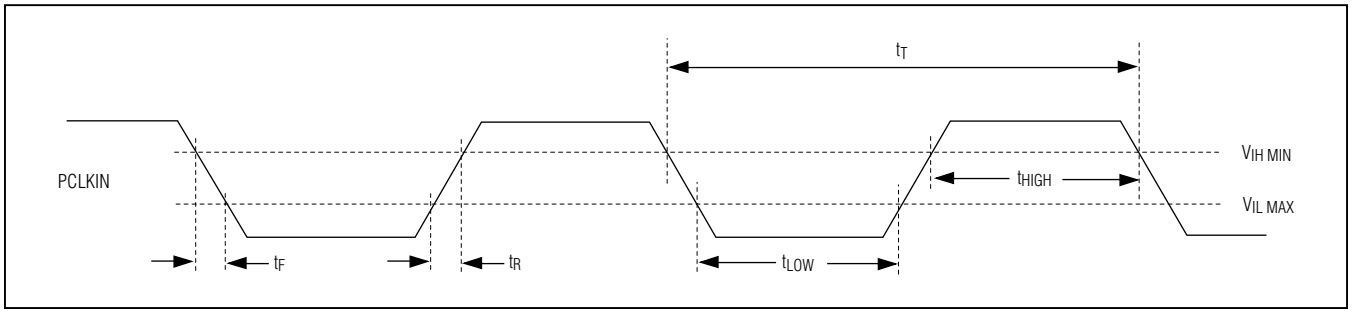


Figure 5. Parallel Clock Input Requirements

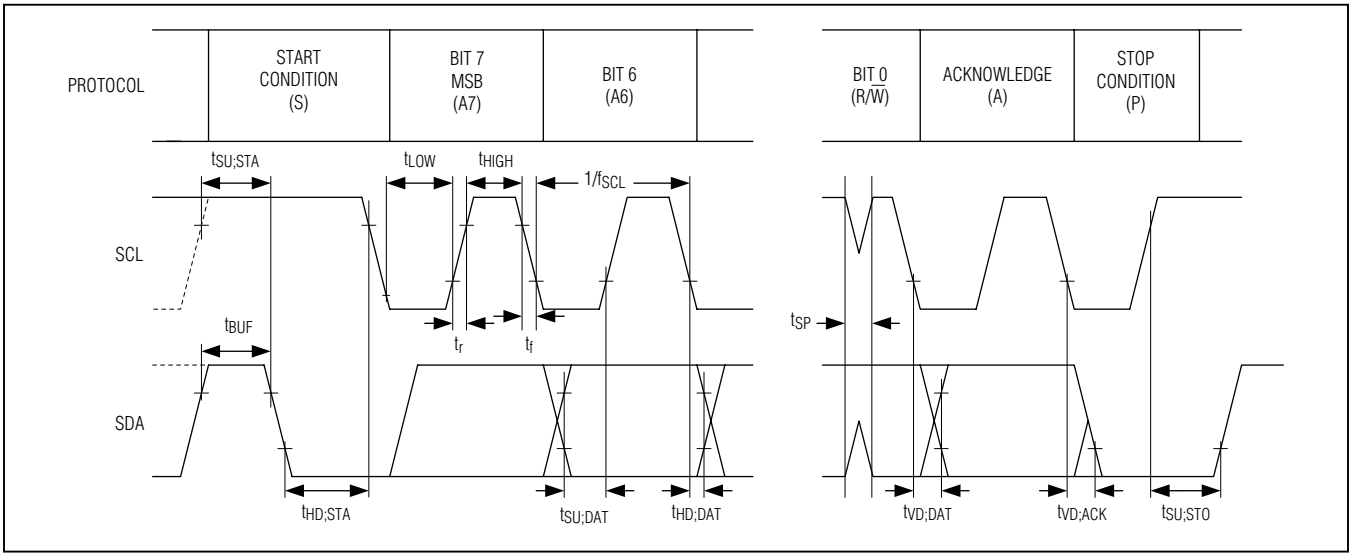


Figure 6. I^2C Timing Parameters

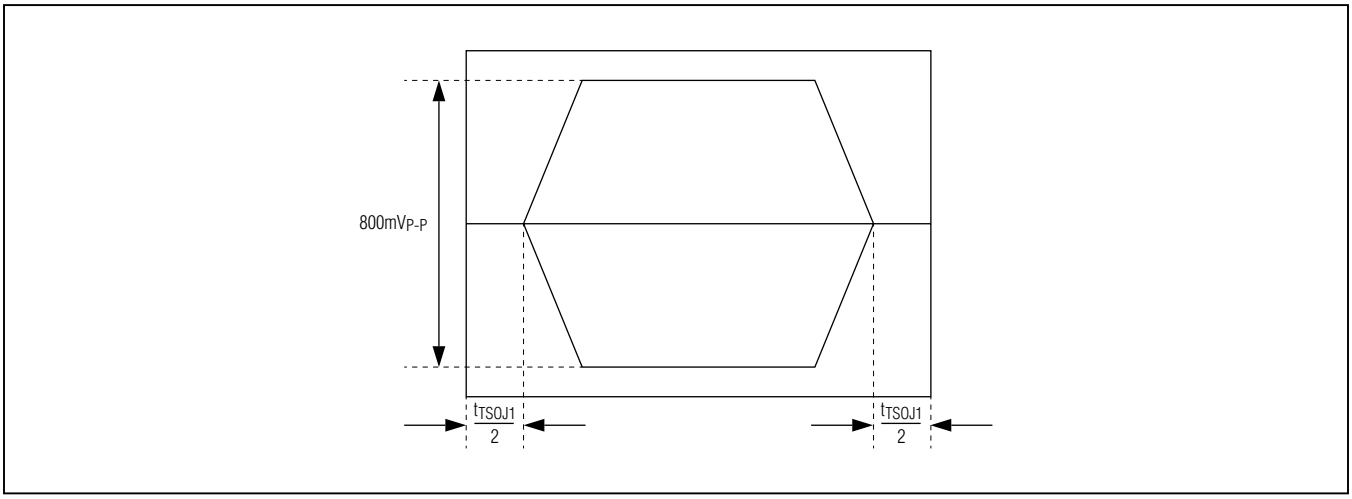


Figure 7. Differential Output Template

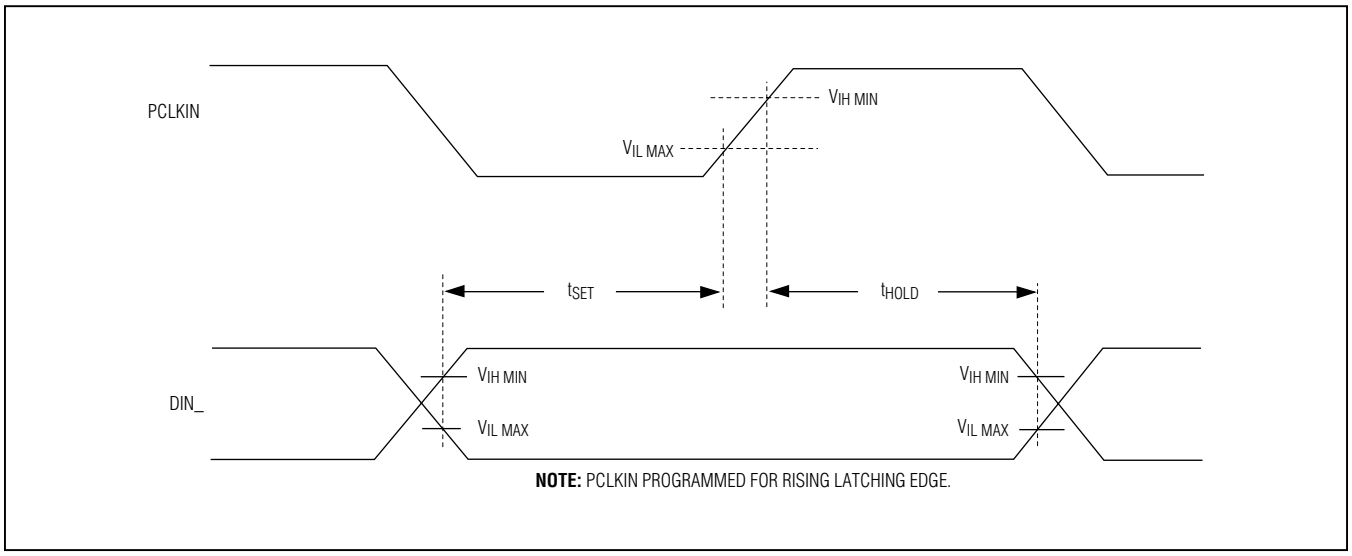


Figure 8. Input Setup and Hold Times

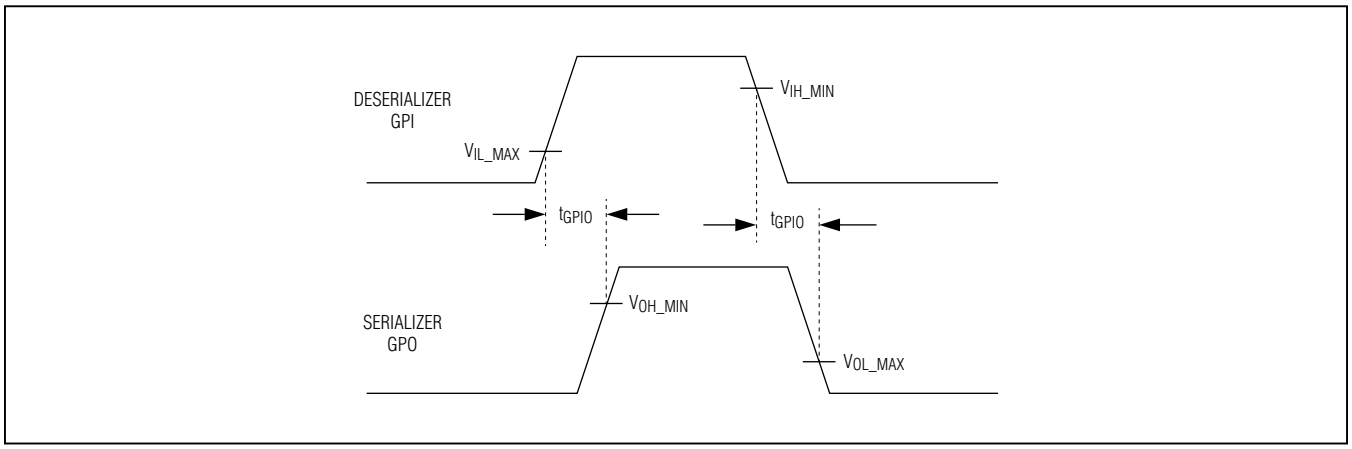


Figure 9. GPI-to-GPO Delay

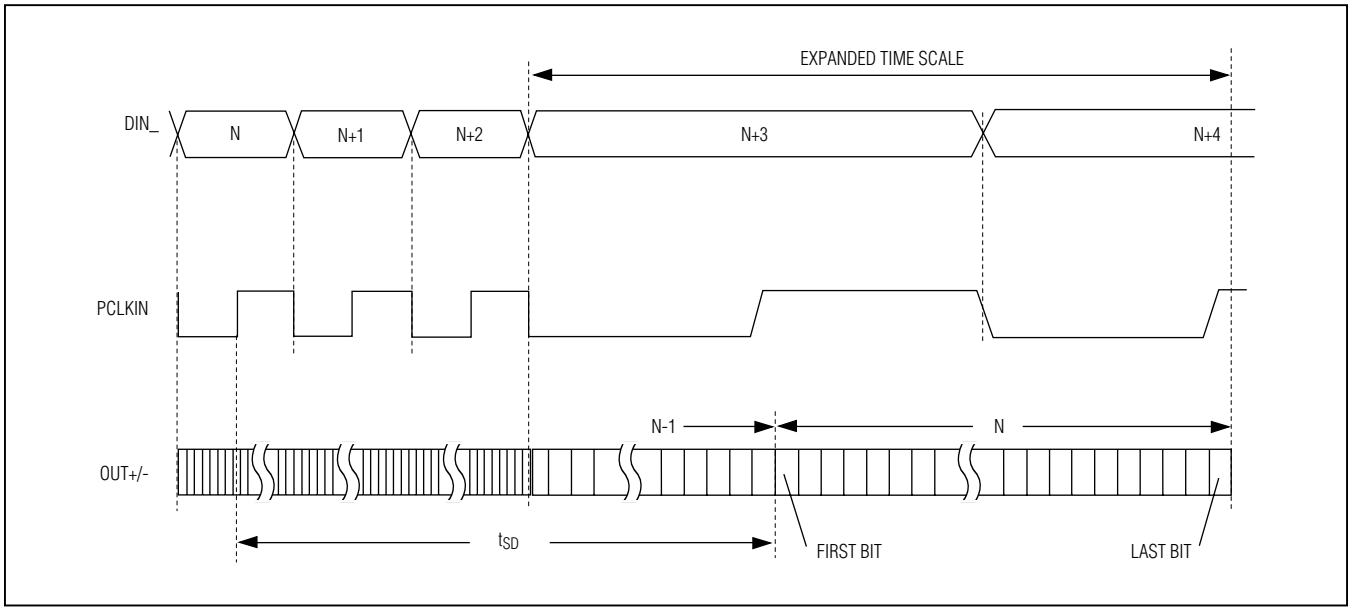


Figure 10. Serializer Delay

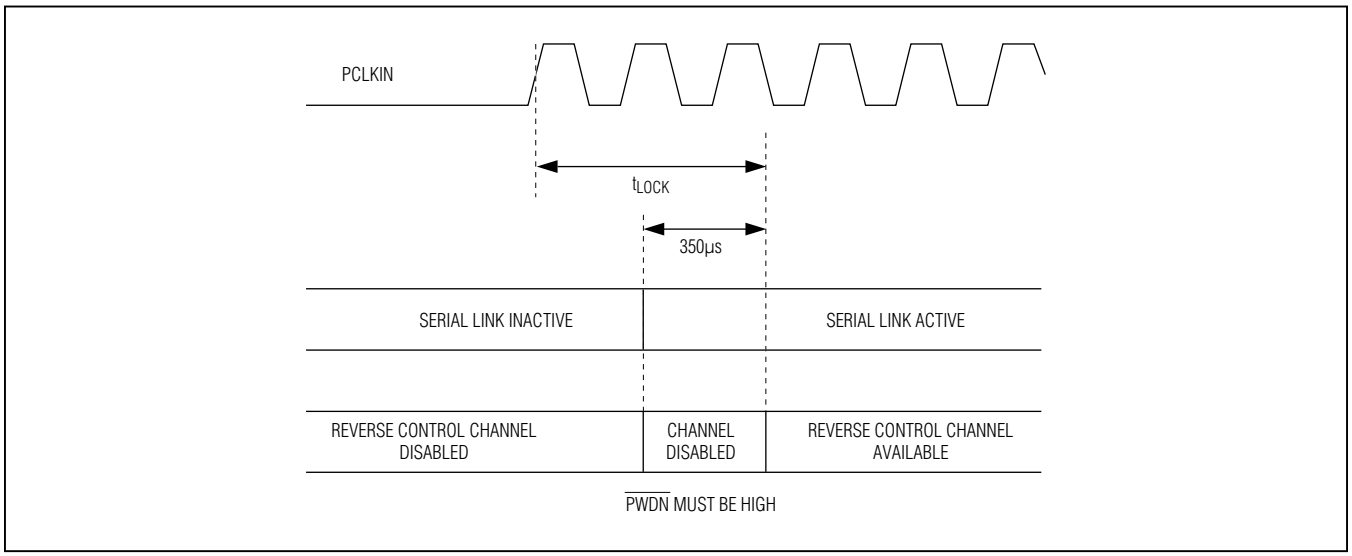


Figure 11. Link Startup Time

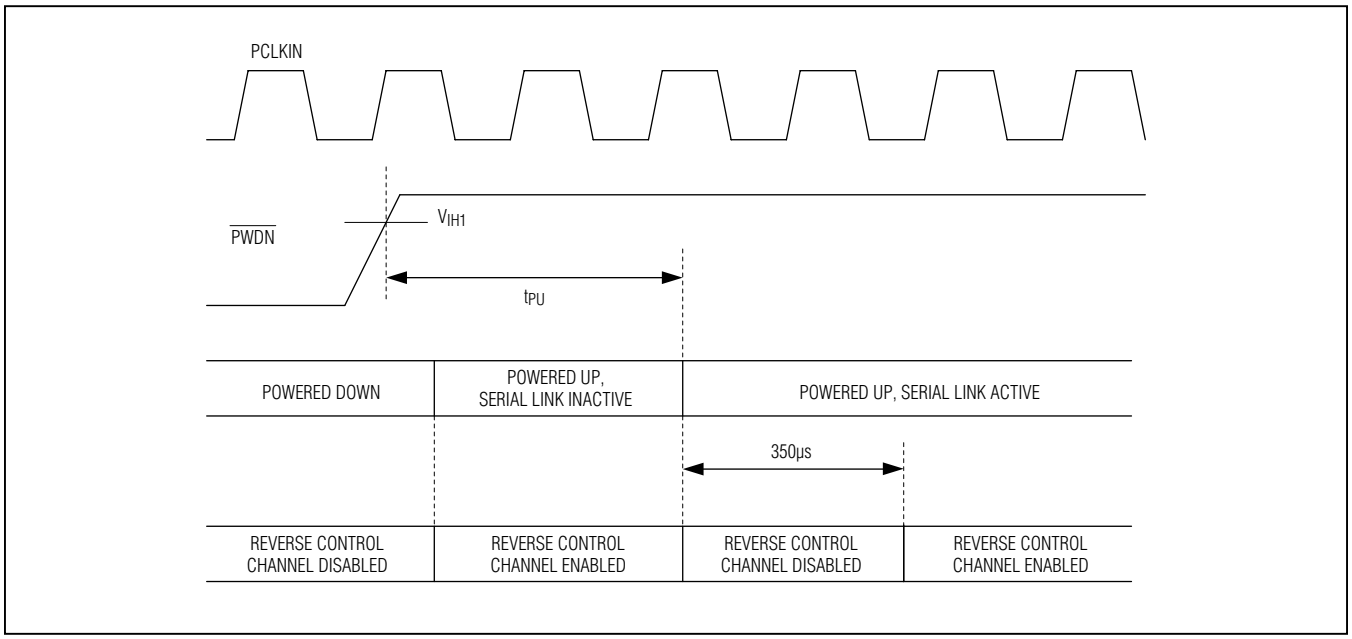


Figure 12. Power-Up Delay

Detailed Description

The MAX9271 serializer, when paired with the MAX9272 deserializer, provides the full set of operating features, but offers basic functionality when paired with any GMSL deserializer.

The serializer has a maximum serial-bit rate of 1.5Gbps for 15m or more of cable and operates up to a maximum input clock of 50MHz in 16-bit, single-input mode, or 75MHz/100MHz in 15-bit/11-bit, double-input mode, respectively. Pre/deemphasis, along with the GMSL deserializer channel equalizer, extends the link length and enhances link reliability.

The control channel enables a µC to program serializer and deserializer registers and program registers on peripherals. The µC can be located at either end of the link or at both ends. Two modes of control-channel operation are available with associated protocols and data formats. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol.

Spread spectrum is available to reduce EMI on the serial output. The serial output complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the serializer and are programmed using the control channel in base mode. The serializer holds its device address and the device address of the deserializer it is driving. Similarly, the driven deserializer holds its device address and the address of the serializer by which it is driven. Whenever a device address is changed, the new address should be written to both devices. The default device address of the MAX9271 serializer (or any GMSL serializer) is 0x80 and the default device address of any GMSL deserializer is 0x90 (Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses.

Input Bit Map

The parallel input functioning and width depends on settings of the double-/single-input mode (DBL), HS/VS encoding (HVEN), error correction (EDC), and bus width (BWS) pins. DINA is the input latched by the pixel clock in single-input mode, or the inputs latched on the first pixel clock in double-input mode. DINB are the inputs latched on the second pixel clock in double-input mode. Table 2 lists the bit map for the control pin settings.

Table 1. Power-Up Default Register Map (see Table 16)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID = 1000000, serializer device address CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x01	0x90	DESID = 1001000, deserializer device address RESERVED = 0
0x02	0x1F	SS = 000 no spread spectrum RESERVED = 1 PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking SDIV = 000000, autocalibrate sawtooth divider
0x04	0x87	SEREN = 1, serial link enabled CLINKEN = 0, configuration link disabled PRBSEN = 0, PRBS test disabled SLEEP = 0, sleep mode disabled (see the *Link Startup Procedure* section) INTTYPE = 01, local control channel uses UART REVCCEN = 1, reverse control channel active (receiving) FWDCCEN = 1, forward control channel active (sending)
0x05	0x00	I2CMETHOD = 0, I²C packets include register address ENJITFILT = 0, jitter filter disabled PRBSLEN = 00, continuous PRBS length RESERVED = 00 ENWAKEN = 0, OUT- wake-up receiver disabled ENWAKEP = 1, OUT+ wake-up receiver enabled
0x06	0x80, 0xA0	CMLLVL = 1000 or 1010, output level determined by the state of CONF1 and CONF0 at power-up PREEMP = 0000, preemphasis disabled
0x07	0xXX	DBL = 0 or 1, single-/double-input mode setting determined by the state of LCCEN and TX/SCL/DBL at startup DRS = 0, high data-rate mode BWS = 0 or 1, bit width setting determined by the state of LCCEN and GPIO1/BWS at startup ES = 0 or 1, edge-select input setting determined by the state of LCCEN and TX/SCL/ES at startup RESERVED = 0 HVEN = 0 or 1, HS/VS tracking encoding setting determined by the state of LCCEN and MS/HVEN at startup EDC = 00 or 10, error-detection/correction setting determined by the state of LCCEN and RX/SDA/EDC at startup
0x08	0x00	INVVS = 0, serializer does not invert VSYNC INVHS = 0, serializer does not invert HSYNC RESERVED = 000000

Table 1. Power-Up Default Register Map (see Table 16) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x09	0x00	I2CSRCA = 0000000, I²C address translator source A is 0x00 RESERVED = 0
0x0A	0x00	I2CDSTA = 0000000, I²C address translator destination A is 0x00 RESERVED = 0
0x0B	0x00	I2CSRCB = 0000000, I²C address translator source B is 0x00 RESERVED = 0
0x0C	0x00	I2CDSTB = 0000000, I²C address translator destination B is 0x00 RESERVED = 0
0x0D	0xB6	I2CLOCACK = 1, acknowledge generated when forward channel is not available I2CSLVSH = 01, 469ns/234ns I²C setup/hold time I2CMSTBT = 101, 339kbps (typ) I²C-to-I²C master bit-rate setting I2CSLVTO = 10, 1024µs (typ) I²C-to-I²C slave remote timeout
0x0E	0x42	DIS_REV_P = 0, OUT+ reverse channel receiver enabled DIS_REV_N = 1, OUT- reverse channel receiver disabled GPIO5EN = 0, GPIO5 disabled GPIO4EN = 0, GPIO4 disabled GPIO3EN = 0, GPIO3 disabled GPIO2EN = 0, GPIO2 disabled GPIO1EN = 1, GPIO1 enabled RESERVED = 0
0x0F	0xFE	RESERVED = 11 GPIO5OUT = 1, GPIO5 set high GPIO4OUT = 1, GPIO4 set high GPIO3OUT = 1, GPIO3 set high GPIO2OUT = 1, GPIO2 set high GPIO1OUT = 1, GPIO1 set high SETGPO = 0, GPO set low
0x10	0x3E	RESERVED = 00 GPIO5IN = 1, GPIO5 is input high GPIO4IN = 1, GPIO4 is input high GPIO3IN = 1, GPIO3 is input high GPIO2IN = 1, GPIO2 is input high GPIO1IN = 1, GPIO1 is input high GPO_L = 0, GPO is set low
0x11	0x00	ERRGRATE = 00, generate an error every 2560 bits ERRGTYPE = 0, generate single-bit errors ERRGCNT = 00, continuously generate errors ERRGPER = 0, disable periodic error generation ERRGEN = 0, disable error generation

Table 1. Power-Up Default Register Map (see Table 16) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x12	0x40	RESERVED = 01000000
0x13	0x22	RESERVED = 00100010
0x14	0xXX	RESERVED = XXXXXXXX
0x15	0x00	CXTP = 0, CXTP is low I2CSEL = 0, input is low LCCEN = 0, local control channel disabled RESERVED = 000 OUTPUTEN = 0, output disabled PCLKDET = 0, no valid PCLKIN detected
0x16	0xXX (read only)	RESERVED = XXXXXXXX
0x17	0xXX (read only)	RESERVED = XXXXXXXX
0x1E	0x09 (read only)	ID = 00001001, device ID is 0x09
0x1F	0x0X (read only)	RESERVED = 000 CAPS = 0, serializer is not HDCP capable REVISION = XXXX, revision number

X = Don't care.

Table 2. Input Map

EDC	BWS	DBL	HVEN	DINA	DINB*	SERIAL LINK WORD BITS
0	0	0	0	0:15	—	0:15
0	0	0	1	0:13, HS, VS	—	0:13
0	0	1	0	0:10	0:10	0:21
0	0	1	1	0:10, HS, VS	0:10, HS, VS	0:21
0	1	0	0	0:15	—	0:15
0	1	0	1	0:13, HS, VS	—	0:13
0	1	1	0	0:14	0:14	0:29
0	1	1	1	0:13, HS, VS	0:13, HS, VS	0:13, 15:28
1	0	0	0	0:15	—	0:15
1	0	0	1	0:13, HS, VS	—	0:13
1	0	1	0	0:7	0:7	0:15
1	0	1	1	0:7, HS, VS	0:7, HS, VS	0:13
1	1	0	0	0:15	—	0:15
1	1	0	1	0:13, HS, VS	—	0:13
1	1	1	0	0:11	0:11	0:23
1	1	1	1	0:11, HS, VS	0:11, HS, VS	0:23

**In double-input mode (DBL = 1), DINA is latched on the first cycle of PCLKIN and DINB is latched on the second cycle of PCLKIN.*

The parallel input has two input modes: single- and double-rate input. In single-input mode, LATCH A stores data from DIN_ every PCLKIN cycle (Figure 13). Parallel data from LATCH A is then sent to the scrambler for serialization (Figure 14). The device accepts pixel clocks from 6.25MHz to 50MHz.

In double-input mode, LATCH B stores two input words (Figure 15). Data from LATCH B is sent to the scrambler as a combined word. The MAX9272 deserializer outputs the combined word (single-output mode) or two half-sized words (double-output mode). The serializer/deserializer use pixel clock rates from 33.3MHz to 100MHz for 11-bit, double-input mode and 25MHz to 75MHz for 15-bit, double-input mode. See Figure 16 for timing details.

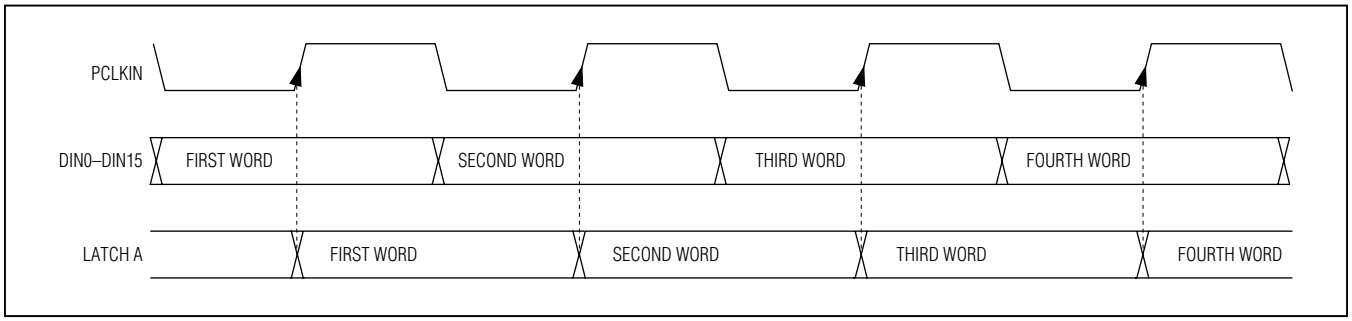


Figure 13. Single-Input Waveform (Latch on Rising Edge of PCLKIN Selected)

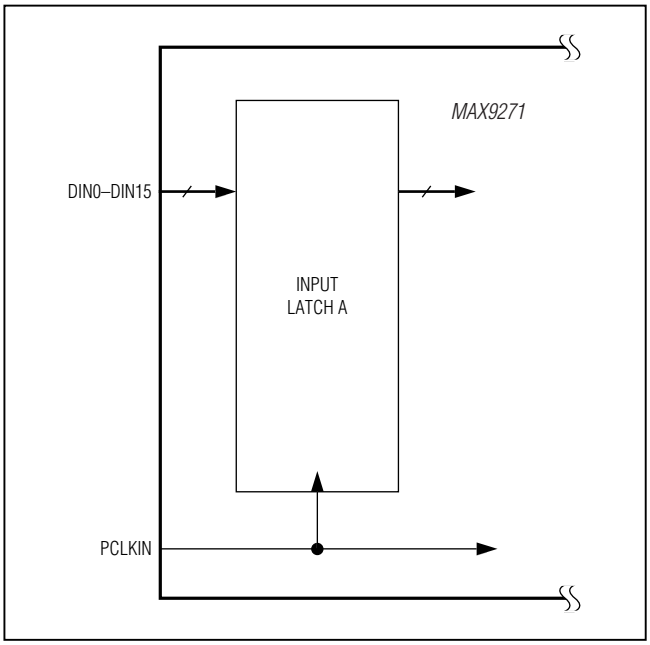


Figure 14. Single-Input Function Block

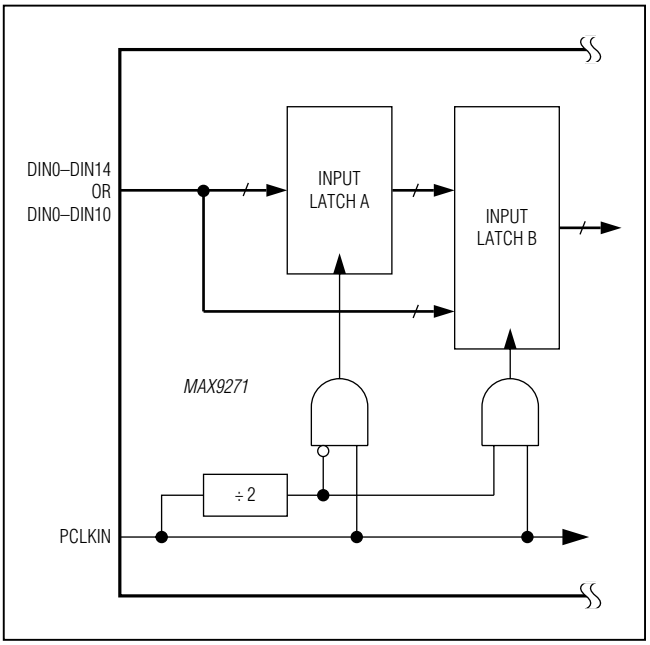


Figure 15. Double-Input Function Block

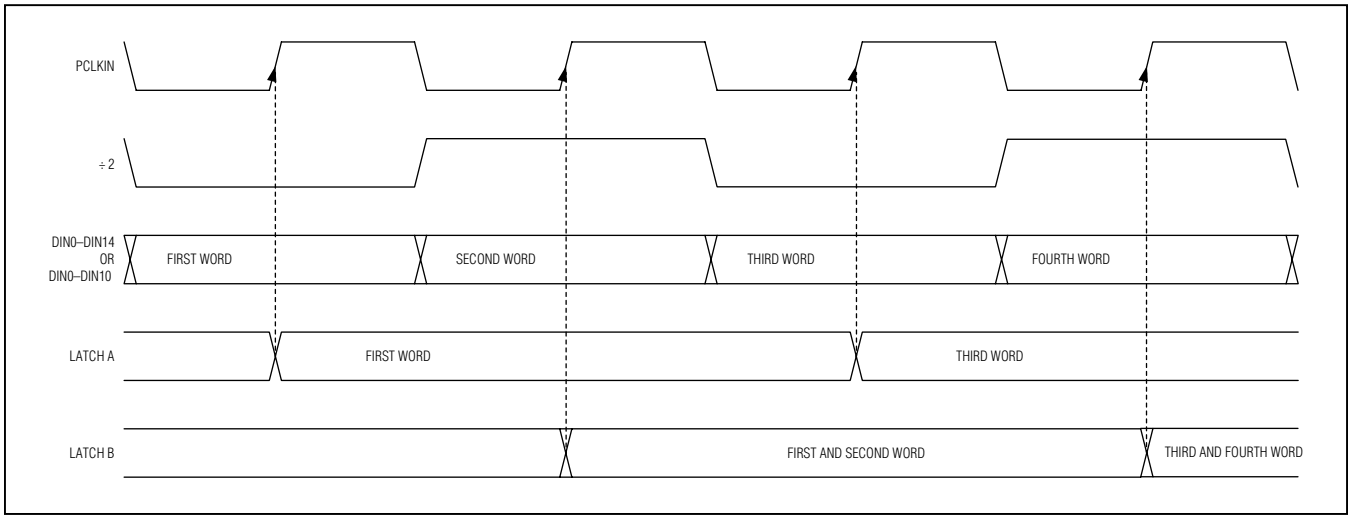


Figure 16. Double-Input Waveform (Latch on Rising Edge of PCLKIN Selected)

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coax cable. The output amplitude is programmable.

Input data is scrambled and then 8b/10b coded. The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit or 32-bit mode, 22 or 30 bits contain the video data and/or error-correction bits, if used. The 23rd or 31st bit carries the forward control-channel data. The last bit is the parity bit of the previous 23 or 31 bits. (Figure 17).

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable, forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Data-Rate Selection

The serializer/deserializer use DRS, DBL, and BWS to set the PCLKIN frequency range (Table 3). Set DRS = 1 for a PCLKIN frequency range of 6.25MHz to 12.5MHz (32-bit, single-input mode) or 8.33MHz to 16.66MHz (24-bit, single-input mode). Set DRS = 0 for normal operation. It is not recommended to use double-input mode when DRS = 1.

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode, according to the mode selection (MS/HVEN) input of the device connected to the µC. Base mode is a half-duplex control channel and bypass mode is a full-duplex control channel.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I²C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer/deserializer in base mode are programmable. The default value is 0x80 for the serializer and 0x90 for the deserializer.

When the peripheral interface is I²C, the serializer/deserializer convert UART packets to I²C that have device addresses different from those of the serializer or deserializer. The converted I²C bit rate is the same as the original UART bit rate.

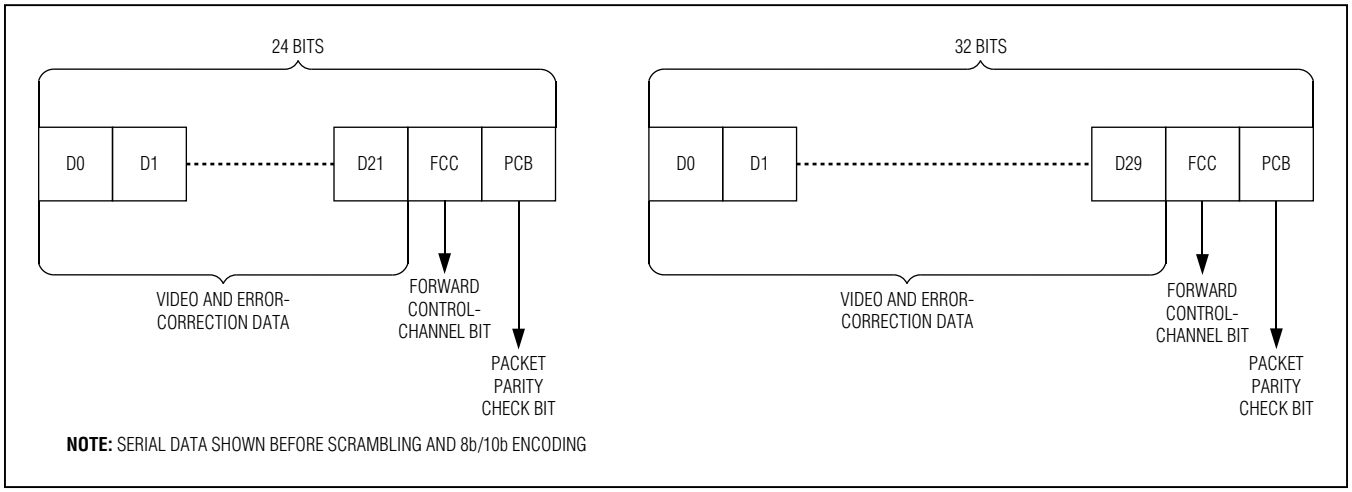


Figure 17. Serial-Data Format

Table 3. Data-Rate Selection Table

DRS SETTING	DBL SETTING	BWS SETTING	PCLKIN RANGE (MHz)
0	0 (single input)	0 (24-bit mode)	16.66 to 50
0	0	1 (32-bit mode)	12.5 to 35
0	1 (double input)	0	33.3 to 100
0	1	1	25 to 75
1	0	0	8.33 to 16.66
1	0	1	6.25 to 12.5
1	1	0	Do not use
1	1	1	Do not use

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer/deserializer automatically detect the control-channel bit rate in base mode. Packet bit-rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information on changing the control-channel bit rate.

Figure 18 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 19 shows the UART data format. Figure 20 and Figure 21 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the serializer/deserializer registers do not take effect until after the ACK byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS/HVEN inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication is corrupted. In the event of a missed or delayed acknowledge (~1ms due to control-channel timeout), the µC should assume there was an error in the packet when the slave device received it, or that an error occurred during the response from the slave device. In base mode, the µC must keep the UART Tx/Rx lines high for 16 bit times before starting to send a new packet.

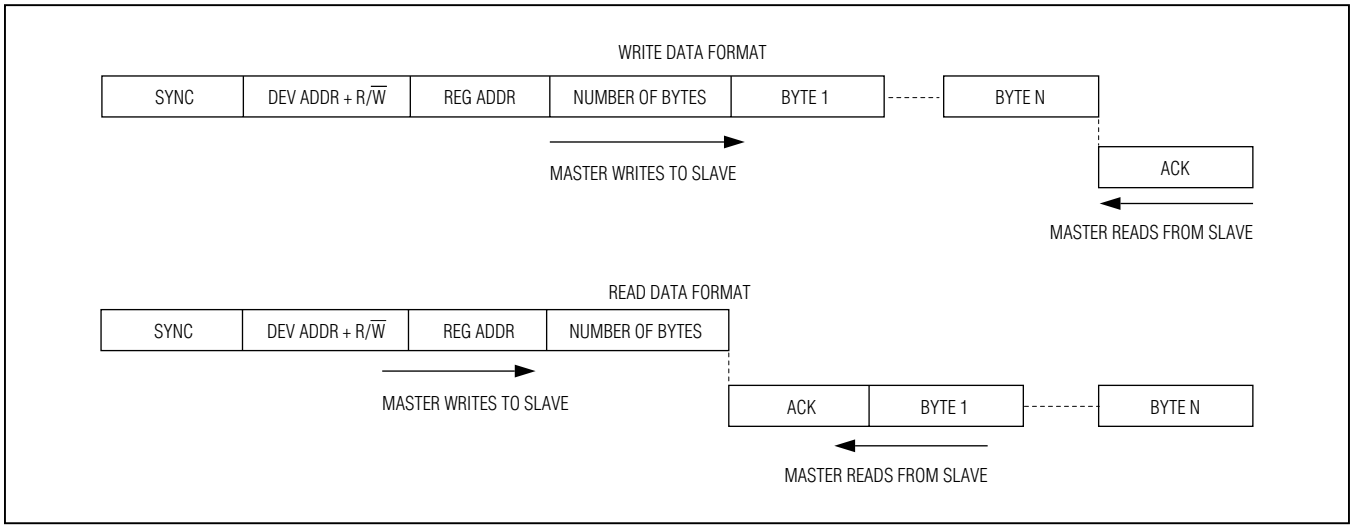


Figure 18. GMSL UART Protocol for Base Mode

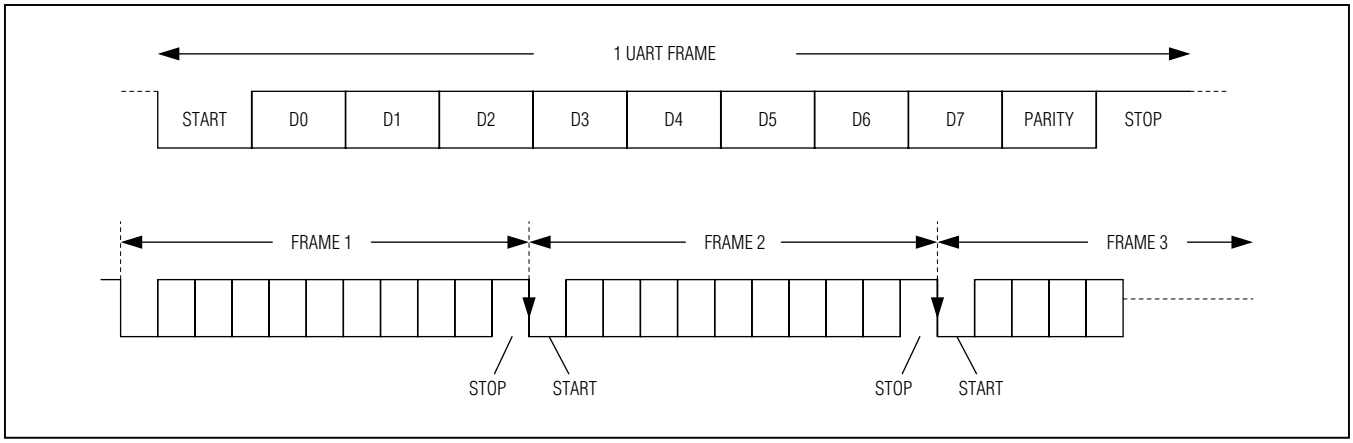


Figure 19. GMSL UART Data Format for Base Mode

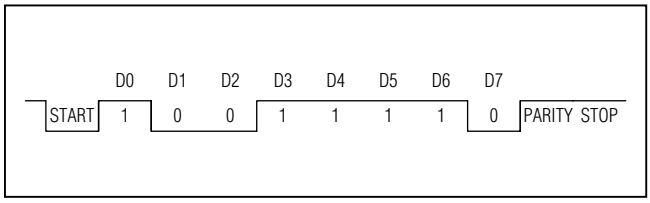


Figure 20. SYNC Byte (0x79)

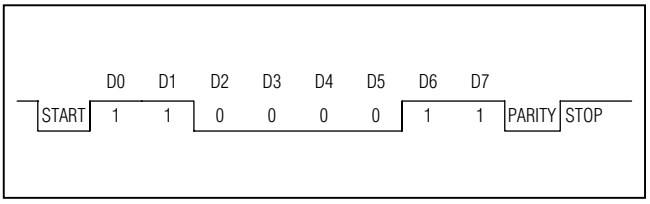


Figure 21. ACK Byte (0xC3)