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MAX9272A 28-Bit GMSL Deserializer for Coax or STP Cable

General Description

The MAX9272A compact deserializer is designed to interface with a GMSL serializer over 50Ω coax or 100Ω shielded twisted-pair (STP) cable. The device pairs with the MAX9271 or MAX9273 serializers.

The parallel output is programmable for single or double output. Double output strobes out half of a parallel word on each pixel clock cycle. Double output can be used with GMSL serializers that have the double-input feature.

The device features an embedded control channel that operates at 9.6kbps to 1Mbps. Using the control channel, a microcontroller (µC) can program the serializer/deserializer and peripheral device registers at any time, independent of video timing. Two programmable GPIO ports and a continuously sampled GPI input are available.

For use with longer cables, the device has a programmable equalizer. Programmable spread spectrum is available on the parallel output. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 48-pin (7mm x 7mm) TQFN-EP package with 0.5mm lead pitch and operates over the -40ºC to +105ºC temperature range.

Applications

- Automotive Camera Systems

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit *appears at end of data sheet.*

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX9272A.related**.*

Benefits and Features

- Ideal for Camera Applications
  - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - Error Detection/Correction
  - 9.6kbps to 1Mbps Control Channel in I²C-to-I²C Mode with Clock-Stretch Capability
  - Best-in-Class Supply Current: 90mA (max)
  - Double-Rate Clock for Megapixel Cameras
  - Cable Equalization Allows 15m Cable at Full Speed
  - 48-Pin (7mm x 7mm) TQFN-EP Package with 0.5mm Lead Pitch
- High-Speed Data Deserialization for Megapixel Cameras
  - Up to 1.5Gbps Serial-Bit Rate with Single or Double Output: 6.25MHz to 100MHz Clock
- Multiple Control-Channel Modes for System Flexibility
  - 9.6kbps to 1Mbps Control Channel in UART-to-UART or UART-to-I²C Modes
- Reduces EMI and Shielding Requirements
  - Input Programmable for 100mV to 500mV
  - Single-Ended or 50mV to 400mV Differential
  - Programmable Spread Spectrum on the Parallel Output Reduces EMI
  - Tracks Spread Spectrum on Serial Input
- Peripheral Features for Camera Power-Up and Verification
  - Built-In PRBS Checker for BER Testing of the Serial Link
  - Two GPIO Ports
  - Dedicated “Up/Down” GPI for Camera Frame Sync Trigger and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40ºC to +105ºC Operating Temperature
  - ±10kV Contact and ±15kV Air IEC 61000-4-2 ESD Protection
  - ±10kV Contact and ±30kV Air ISO 10605 ESD Protection

19-7404; Rev 0; 5/14

maxim integrated™

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF TABLES

Absolute Maximum Ratings*

AVDD to EP .....-0.5V to +1.9V
DVDD to EP .....-0.5V to +1.9V
IOVDD to EP .....-0.5V to +3.9V
IN+, IN- to EP .....-0.5V to +1.9V
All other pins to EP.....-0.5V to (V_{IOVDD} + 0.5V)
IN+, IN- short circuit to ground or supply .....Continuous
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 40mW/°C above +70°C) 3200mW

Junction Temperature.....+150°C
Operating Temperature Range..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

**EP is connected to PCB ground.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....25°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (I2CSEL, LCCEN, GPI, $\overline{PWDN}$, MS/HVEN)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+20	µA
THREE-LEVEL LOGIC INPUTS (CX/TP)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 2)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUTS (DOUT_, PCLKOUT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = 0	V_{IOVDD} - 0.3			V
			DCS = 1	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = 0			0.3	V
			DCS = 1			0.2	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	DOUT_	V_O = 0V, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
OPEN-DRAIN INPUTS/OUTPUTS (GPIO0/DBL, GPIO1/BWS, RX/SDA/EDC, TX/SCL/ES, $\overline{ERR}$, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 3)		RX/SDA, TX/SCL	-110		+1	µA
				LOCK, $\overline{ERR}$, GPIO_	-80		+1	
				DBL, BWS, EDC, ES	-10		+20	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA		V_{IOVDD} = 1.7V to 1.9V			0.4	V
				V_{IOVDD} = 3.0V to 3.6V			0.3	
OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROH}	No high-speed data transmission (Figure 1)			30		60	mV
Differential Low Output Peak Voltage, (V_{IN}+) - (V_{IN}-)	V_{ROL}	No high-speed data transmission (Figure 1)			-60		-30	mV
DIFFERENTIAL INPUTS (IN+, IN-)								
Differential High Input Threshold (Peak) Voltage, (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	(Figure 2)	Activity detector, medium threshold (0x22 D[6:5] = 01)				60	mV
			Activity detector, low threshold (0x22 D[6:5] = 00)				45	
Differential Low Input Threshold (Peak) Voltage, (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	(Figure 2)	Activity detector, medium threshold (0x22 D[6:5] = 01)		-60			mV
			Activity detector, medium threshold (0x22 D[6:5] = 00)		-45			
Input Common-Mode Voltage ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}				1	1.3	1.6	V
Differential Input Resistance (Internal)	R_I				80	105	130	Ω

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (IN+, IN-)							
Single-Ended High Input Threshold (Peak) Voltage, (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01)				43	mV
		Activity detector, low threshold (0x22 D[6:5] = 00)				33	
Single-Ended Low Input Threshold (Peak) Voltage, (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01)		-43			mV
		Activity detector, medium threshold (0x22 D[6:5] = 00)		-33			
Input Resistance (Internal)	R_I			40	52.5	65	Ω
POWER SUPPLY							
Worst-Case Supply Current (Figure 3)	I_{WCS}	BWS = 0, single output, EQ off	$f_{PCLKOUT}$ = 25MHz		42	65	mA
			$f_{PCLKOUT}$ = 50MHz		61	90	
		BWS = 0, double output, EQ off	$f_{PCLKOUT}$ = 50MHz		42	70	
			$f_{PCLKOUT}$ = 100MHz		62	90	
Sleep Mode Supply Current	I_{CCS}				40	100	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = EP			5	70	µA
ESD PROTECTION							
IN+, IN- (Note 4)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±10		
			Air discharge		±15		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±10		
			Air discharge		±30		
All Other Pins (Note 5)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±4		kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, RL = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)						
Clock Frequency	$f_{PCLKOUT}$	BWS = 0, DRS = 1	8.33		16.66	MHz
		BWS = 0, DRS = 0	16.66		50	
		BWS = 1, DRS = 1	6.25		12.5	
		BWS = 1, DRS = 0	12.5		37.5	
		BWS = 1, DRS = 0, 15-bit double input	25		75	
		BWS = 0, DRS = 0, 11-bit double input	33.33		100	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Figure 4, Note 6)	40	50	60	%
Clock Jitter	t_J	Period jitter, RMS, spread off, 1.5Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$ (Note 6)		0.05		UI

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, RL = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.)

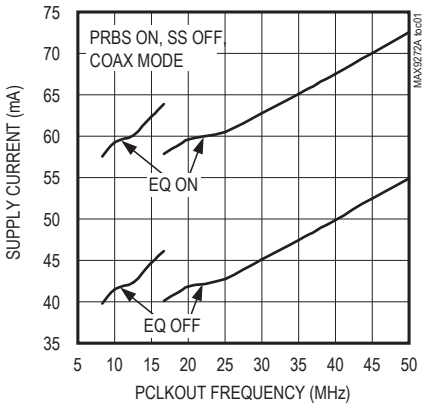
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C/UART PORT TIMING							
I²C/UART Bit Rate				9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		120	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		120	ns
Input Setup Time	t_{SET}	I²C only (Figure 5, Note 6)		100			ns
Input Hold Time	t_{HOLD}	I²C only (Figure 5, Note 6)		0			ns
SWITCHING CHARACTERISTICS							
PCLKOUT Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V (Note 6)	DCS = 1, C_L = 10pf	0.4		2.2	ns
			DCS = 0, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V (Note 6)	DCS = 1, C_L = 10pF	0.25		1.7	
			DCS = 0, C_L = 5pF	0.3		2.0	
Parallel Data Rise-and-Fall Time (Figure 6)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V (Note 6)	DCS = 1, C_L = 10pf	0.5		3.1	ns
			DCS = 0, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V (Note 6)	DCS = 1, C_L = 10pF	0.3		2.2	
			DCS = 0, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	(Figure 7, Notes 6, 7)	Spread spectrum enabled			6960	Bits
			Spread spectrum disabled			2160	
Reverse Control-Channel Output Rise Time	t_R	No forward-channel data transmission (Figure 1, Note 6)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward-channel data transmission (Figure 1, Note 6)		180		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included) (Figure 8)				350	µs
Lock Time	t_{LOCK}	(Figure 9, Note 6)	Spread spectrum enabled			1.5	ms
			Spread spectrum disabled			1	
Power-Up Time	t_{PU}	(Figure 10)				6	ms

Note 2: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.
Note 3: I_{IN} min due to voltage drop across the internal pullup resistor.
Note 4: Specified pin to ground.
Note 5: Specified pin to all supply/ground.
Note 6: Guaranteed by design and not production tested.
Note 7: Measured in serial link bit times. Bit time = 1/(30 x $f_{PCLKOUT}$) for BWS = GND. Bit time = 1/(40 x $f_{PCLKOUT}$) for BWS = 1.

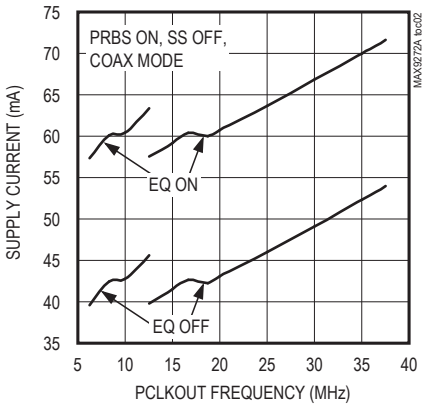
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, DBL = low, T_A = +25°C, unless otherwise noted.)

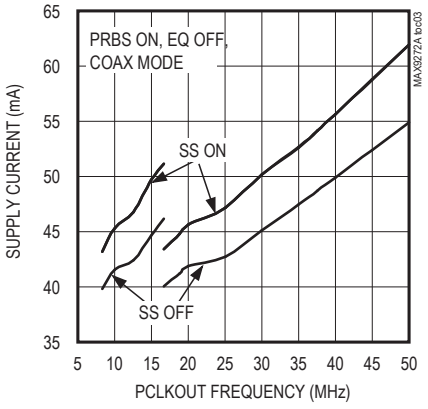
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



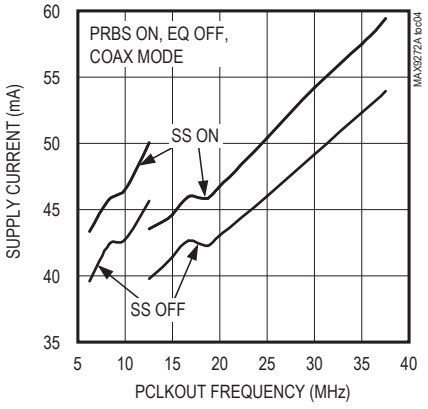
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



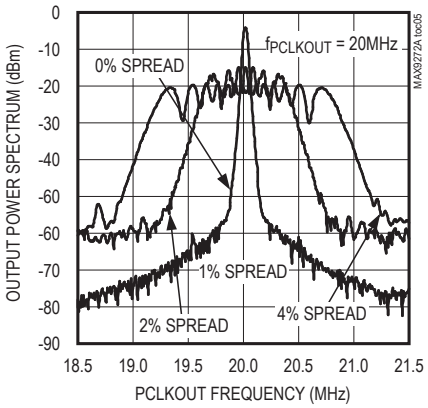
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



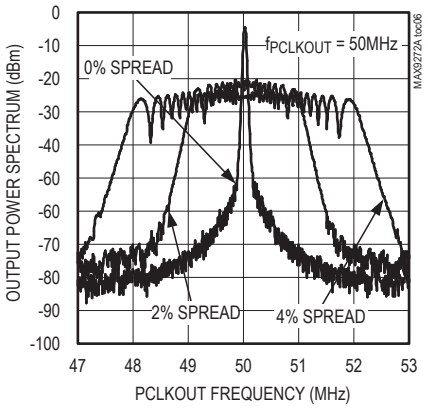
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



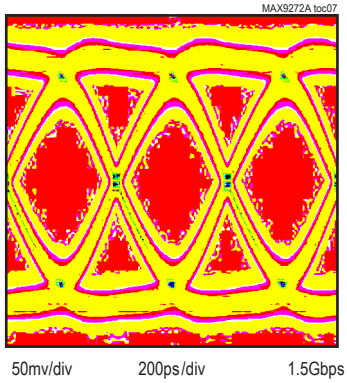
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



Typical Operating Characteristics (continued)

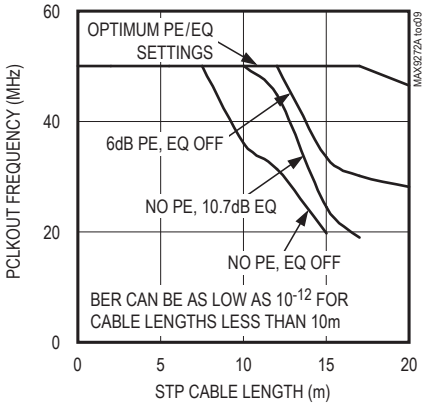
(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, DBL = low, T_A = +25°C, unless otherwise noted.)

SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALELL BIT RATE = 50MHz, 10m STP CABLE)

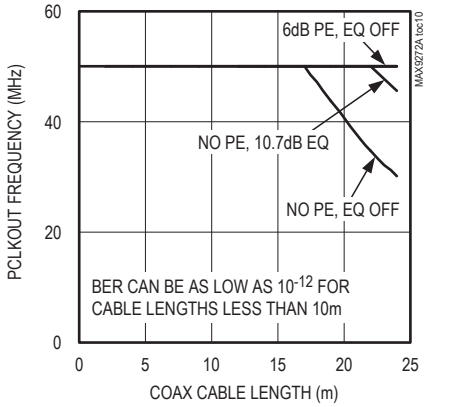


SERIAL LINK SWITCHING PATTERN WITH 6dB PREEMPHASIS (PARALELL BIT RATE = 50MHz, 20m COAX CABLE)

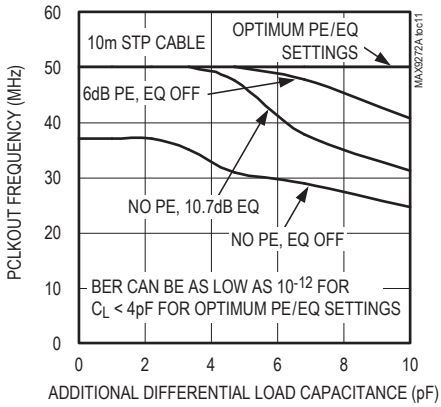
MAXIMUM PCLKOUT FREQUENCY vs. STP CABLE LENGTH (BER ≤ 10^{-10})



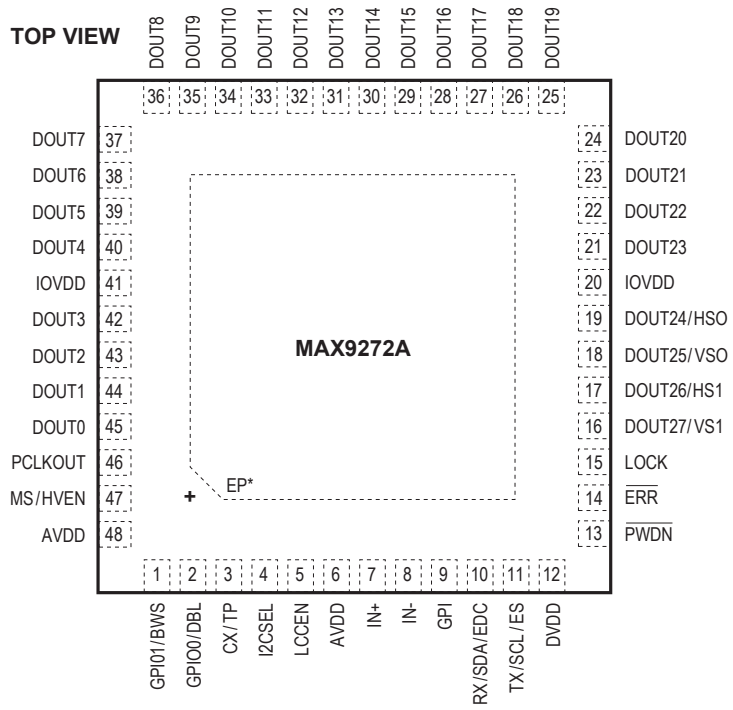
MAXIMUM PCLKOUT FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



MAXIMUM PCLKOUT FREQUENCY vs. ADDITIONAL DIFFERENTIAL C_L (BER ≤ 10^{-10})



Pin Configuration



TQFN
(7mm x 7mm X 0.75mm)
CONNECT EP TO GROUND PLANE

Pin Description

PIN	NAME	FUNCTION
1	GPIO1/BWS	GPIO/Bus Width Select Input. Function is determined by the state of LCCEN (Table 13). GPIO1 (LCCEN = high): Open-drain, general-purpose input/output with internal 60kΩ pullup to IOVDD. BWS (LCCEN = low): Input with internal pulldown to EP. Set BWS = low for 22-bit input latch. Set BWS = high for 30-bit input latch.
2	GPIO0/DBL	GPIO/Double-Mode Input. Function is determined by the state of LCCEN (Table 13). GPIO0 (LCCEN = high): Open-drain, general-purpose input/output with internal 60kΩ pullup to IOVDD. DBL (LCCEN = low): Input with internal pulldown to EP. Set DBL = high to use double-input mode. Set DBL = low to use single-input mode.
3	CX/TP	Coax/Twisted-Pair Three-Level Configuration Input (Table 8)
4	I2CSEL	I²C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I²C slave interface. Set I2CSEL = low to select UART interface.

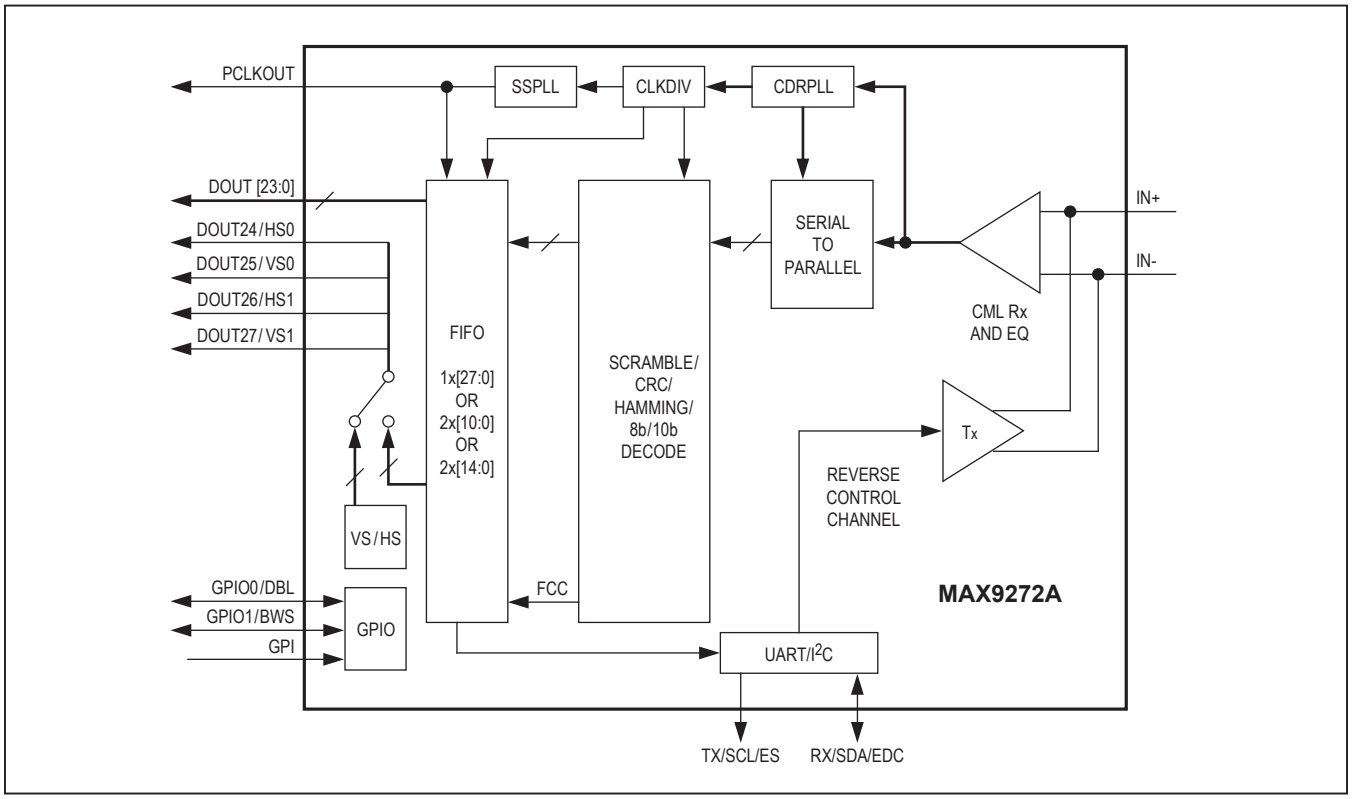
Pin Description (continued)

PIN	NAME	FUNCTION
5	LCCEN	Local Control-Channel Enable Input with Internal Pulldown to EP. LCCEN = high enables the control-channel interface pins. LCCEN = low disables the control-channel interface pins and selects an alternate function on the indicated pins (Table 13).
6, 48	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
7	IN+	Noninverting Coax/Twisted-Pair Serial Input
8	IN-	Inverting Coax/Twisted-Pair Serial Input
9	GPI	General-Purpose Input. The GMSL serializer GPI (or INT) input follows GPI.
10	RX/SDA/EDC	Receive/Serial Data/Error Detection Correction. Function is determined by the state of LCCEN (Table 13). RX/SDA (LCCEN = high): Input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the MAX9272A's UART. In the I²C mode, RX/SDA is the SDA input/output of the MAX9272A's I²C master/slave. RX/SDA has an open-drain driver and requires a pullup resistor. EDC (LCCEN = low): Input with internal pulldown to EP. Set EDC = high to enable error detection correction. Set EDC = low to disable error detection correction.
11	TX/SCL/ES	Transmit/Serial Clock/Edge Select. Function is determined by the state of LCCEN (Table 13). TX/SCL (LCCEN = high). Input/output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the MAX9272A's UART. In the I²C mode, TX/SCL is the SCL input/output of the MAX9272A's I²C master/slave. TX/SCL has an open-drain driver and requires a pullup resistor. ES (LCCEN = low): Input with internal pulldown to EP. When ES is high, PCLKOUT indicates valid data on the falling edge of PCLKOUT. When ES is low, PCLKOUT indicates valid data on the rising edge of PCLKOUT. Do not change the ES input while the pixel clock is running.
12	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
13	$\overline{\text{PWDN}}$	Active-Low Power-Down Input with Internal Pulldown to EP. Set PWDN low to enter power-down mode to reduce power consumption.
14	$\overline{\text{ERR}}$	Error Output. Open-drain data error detection and/or correction indication output with internal 60kΩ pullup to IOVDD. $\overline{\text{ERR}}$ is output high when $\overline{\text{PWDN}}$ is low.
15	LOCK	Open-Drain Lock Output with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK remains low when the configuration link is active or during PRBS test. LOCK is output high when $\overline{\text{PWDN}}$ = low.
16	DOUT27/VS1	Parallel Data/Vertical Sync 1 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded vertical sync for upper half of single output when VS/HS encoding is enabled (Table 2).
17	DOUT26/HS1	Parallel Data/Horizontal Sync 1 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded horizontal sync for upper half of single-output when VS/HS encoding is enabled (Table 2).
18	DOUT25/VS0	Parallel Data/Vertical Sync 0 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded vertical sync for lower half of single-output when VS/HS encoding is enabled (Table 2).

Pin Description (continued)

PIN	NAME	FUNCTION
19	DOUT24/HS0	Parallel Data/Horizontal Sync 0 Output. Defaults to parallel data output on power-up. Parallel data output when VS/HS encoding is disabled. Decoded horizontal sync for lower half of single-output when VS/HS encoding is enabled (Table 2).
20, 41	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
21–40, 42–45	DOUT23–DOUT0	Parallel Data Outputs
46	PCLKOUT	Parallel Clock Output. Latches parallel data into the input of another device.
47	MS/HVEN	Mode Select/HS and VS Encoding Enable with Internal Pulldown to EP. Function is determined by the state of LCCEN (Table 13). MS (LCCEN = high). Set MS = low to select base mode. Set MS = high to select the bypass mode. HVEN (LCCEN = low): Set HVEN = high to enable HS/VS encoding on DOUT_/HS_ and DOUT_/VS_. Set HVEN = low to use DOUT_/HS_ and DOUT_/VS_ as parallel data outputs.
—	EP	Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



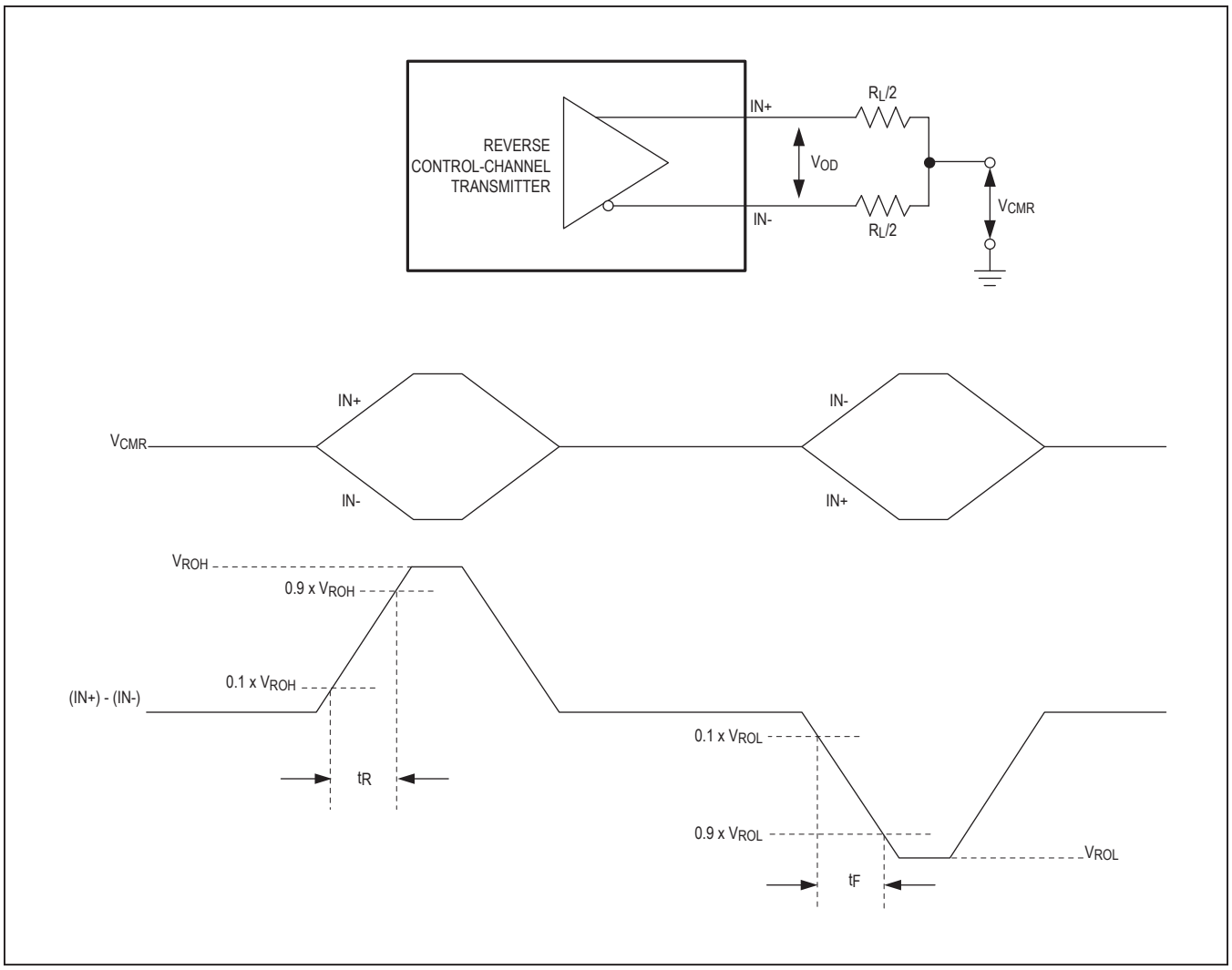


Figure 1. Reverse Control-Channel Output Parameters

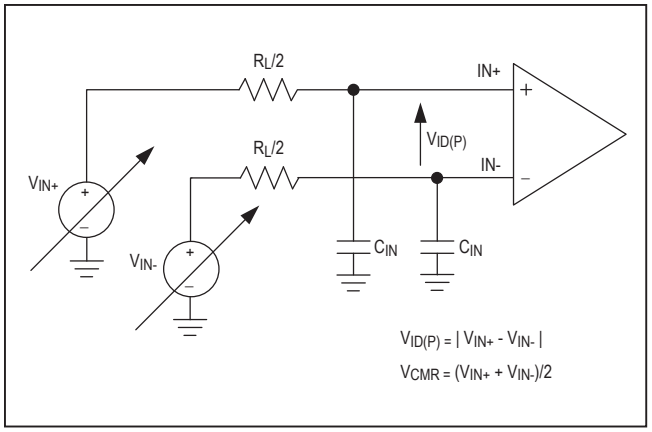


Figure 2. Test Circuit for Differential Input Measurement

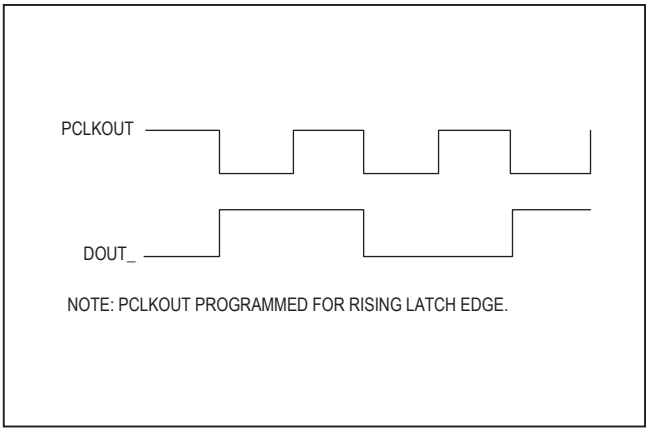


Figure 3. Worst-Case Pattern Output

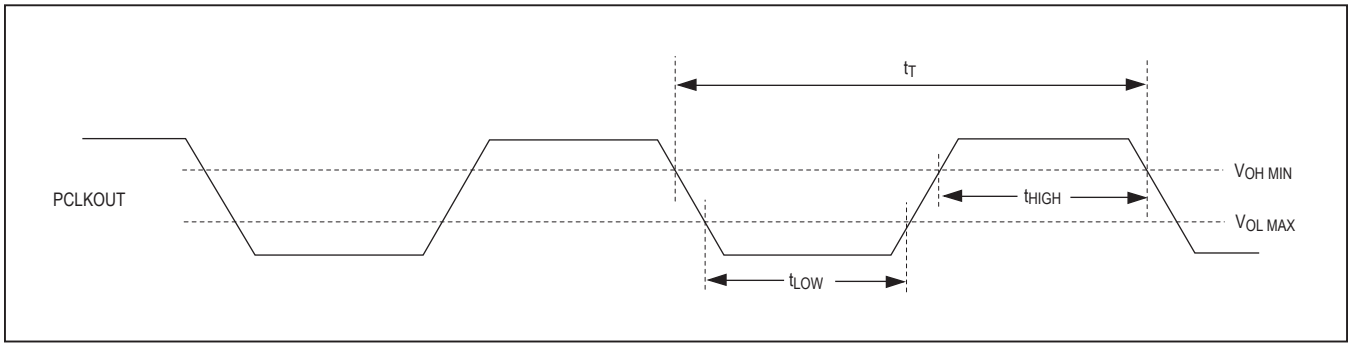


Figure 4. Parallel Clock Output High and Low Times

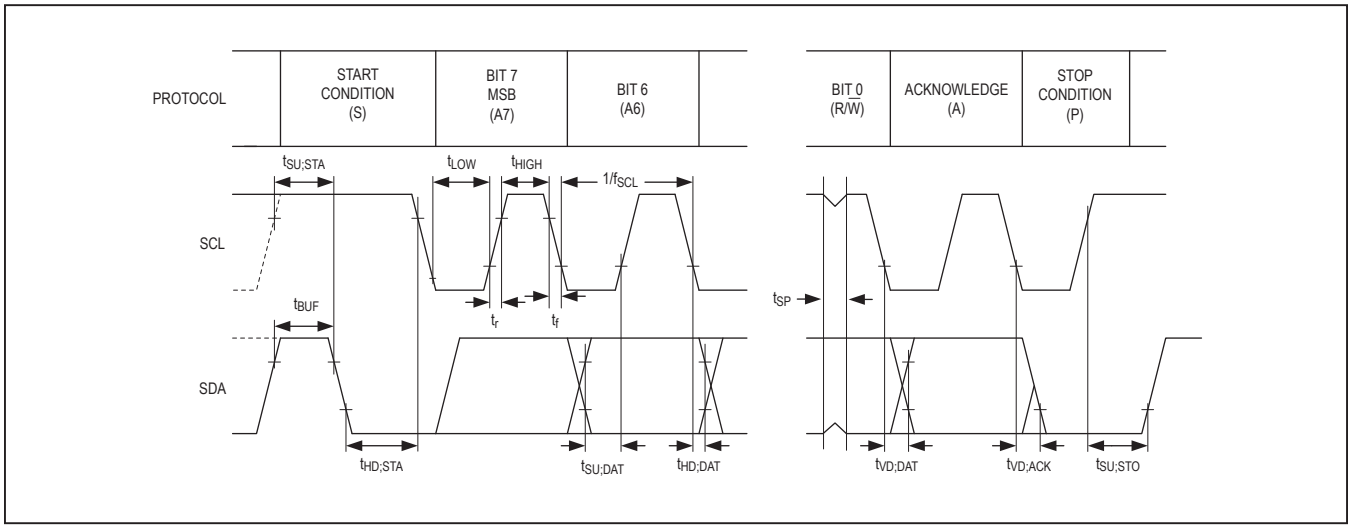


Figure 5. I²C Timing Parameters

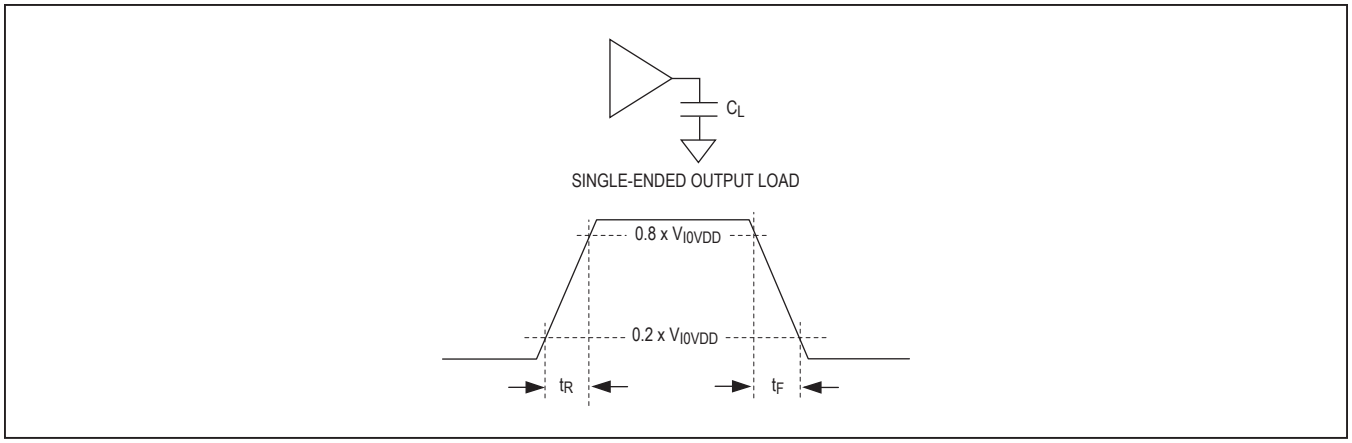


Figure 6. Output Rise-and-Fall Times

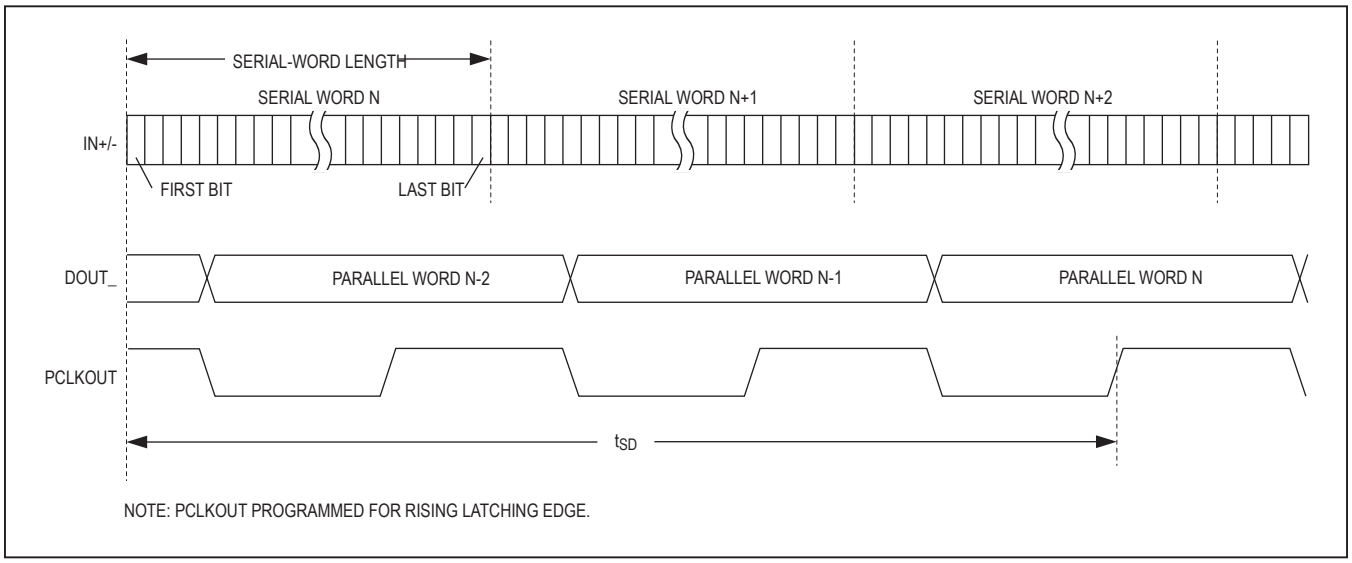


Figure 7. Deserializer Delay

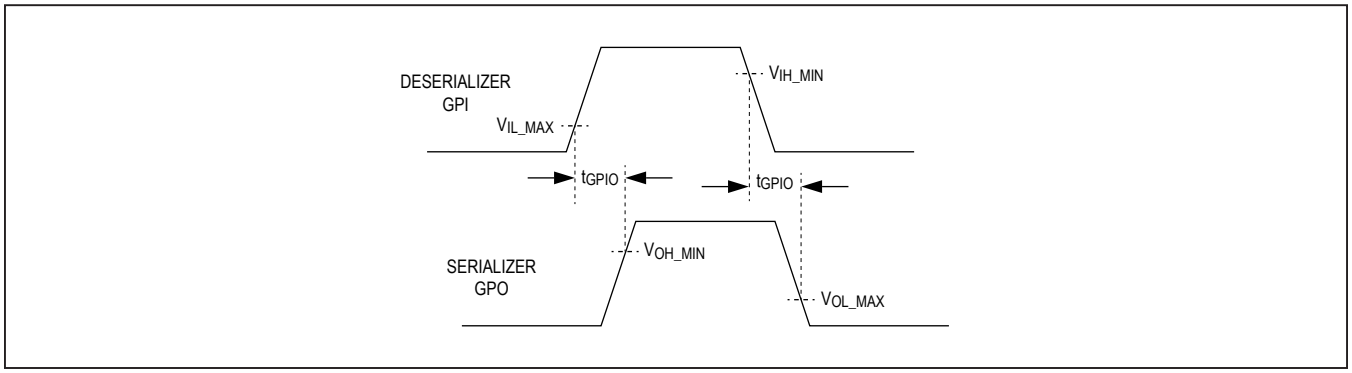


Figure 8. GPI-to-GPO Delay

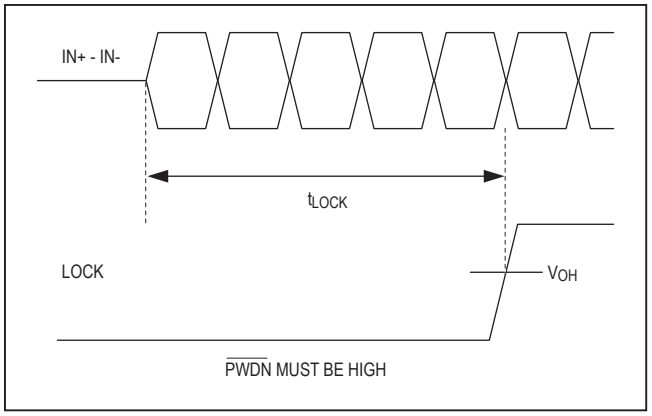


Figure 9. Lock Time

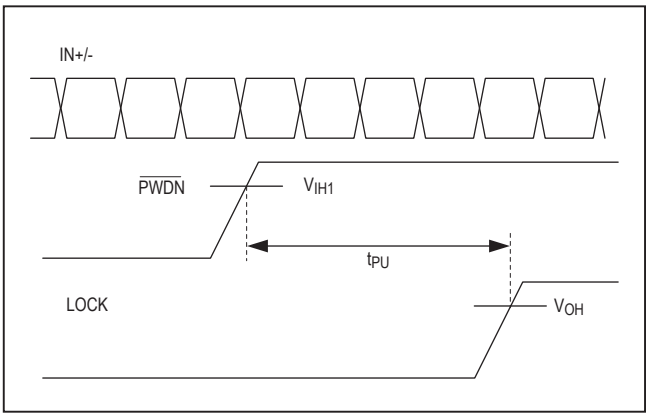


Figure 10. Power-Up Delay

Detailed Description

The MAX9272A deserializer, when paired with the MAX9271 or MAX9273 serializer, provides the full set of operating features, but offers basic functionality when paired with any GMSL serializer.

The deserializer has a maximum serial-bit rate of 1.5Gbps for 15m or more of cable and operates up to a maximum output clock of 50MHz in 28-bit, single-output mode, or 75MHz to 100MHz in 15-bit /11-bit, double-output mode, respectively. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to WVGA (800 x 480) and higher with 18-bit color, as well as megapixel image sensors. Input equalization, combined with GMSL serializer pre/deemphasis, extends the cable length and enhances link reliability

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to configure and access the GPIO. The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I²C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the parallel output. The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the deserializer and are programmed using the control channel in base mode. The deserializer holds its device address and the device address of the serializer it is paired with. Similarly, the serializer holds its device address and the address of the deserializer. Whenever a device address is changed, the new address should be written to both devices. The default device address of the deserializer is set by the CX/TP input and the default device address of any GMSL serializer is 0x80 (see Table 1 and Table 8). Registers 0x00 and 0x01 in both devices hold the device addresses.

Bit Map

The parallel output functioning and width depend on settings of the double-/single-output mode (DBL), HS/VS encoding (HVEN), error correction used (EDC), and bus width (BWS) pins. Table 2 lists the bit map for the control pin settings. Unused output bits are pulled low.

The parallel output has two output modes: single and double output. In single-output mode, the deserialized parallel data is clocked out every PCLKOUT cycle. The device accepts pixel clocks from 6.25MHz to 50MHz (Figures 11 and 12).

In double-output mode, the device splits deserialized data into two half-sized words that are output at twice the serial-word rate (Figures 13 and 14). The serializer/deserializer use pixel clock rates from 33.3MHz to 100MHz for 11-bit, double-output mode and 25MHz to 75MHz for 15-bit, double-output mode.

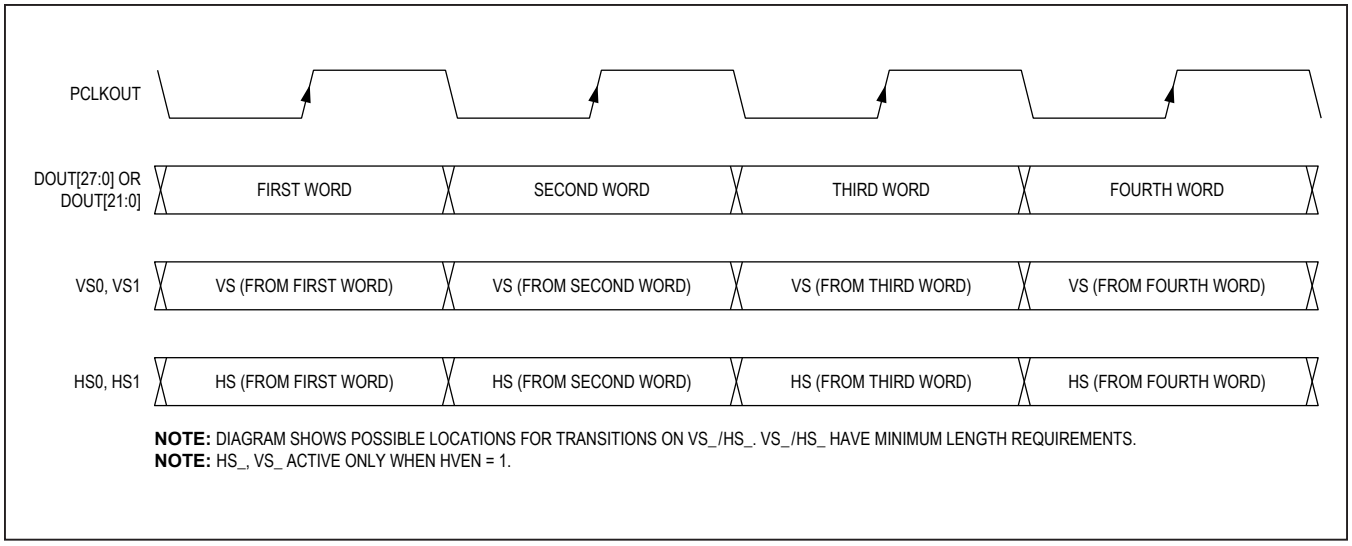


Figure 11. Single-Output Waveform (Serializer Using Single Input)

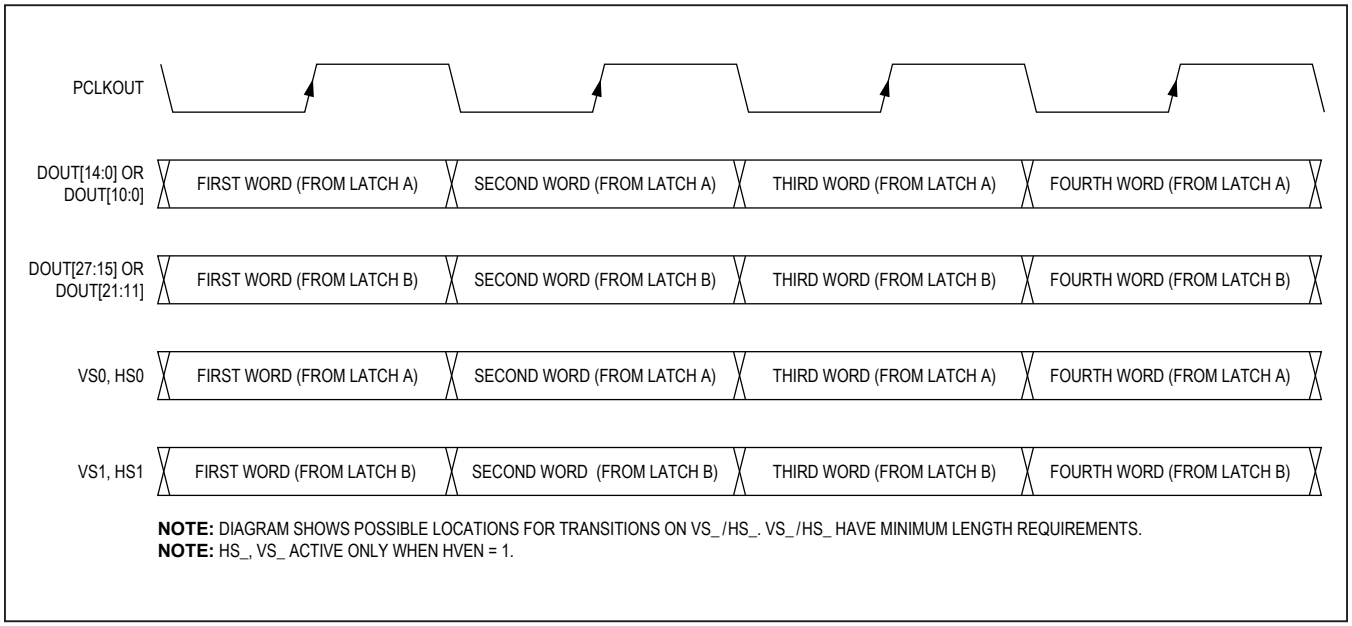


Figure 12. Single-Output Waveform (Serializer Using Double Input)

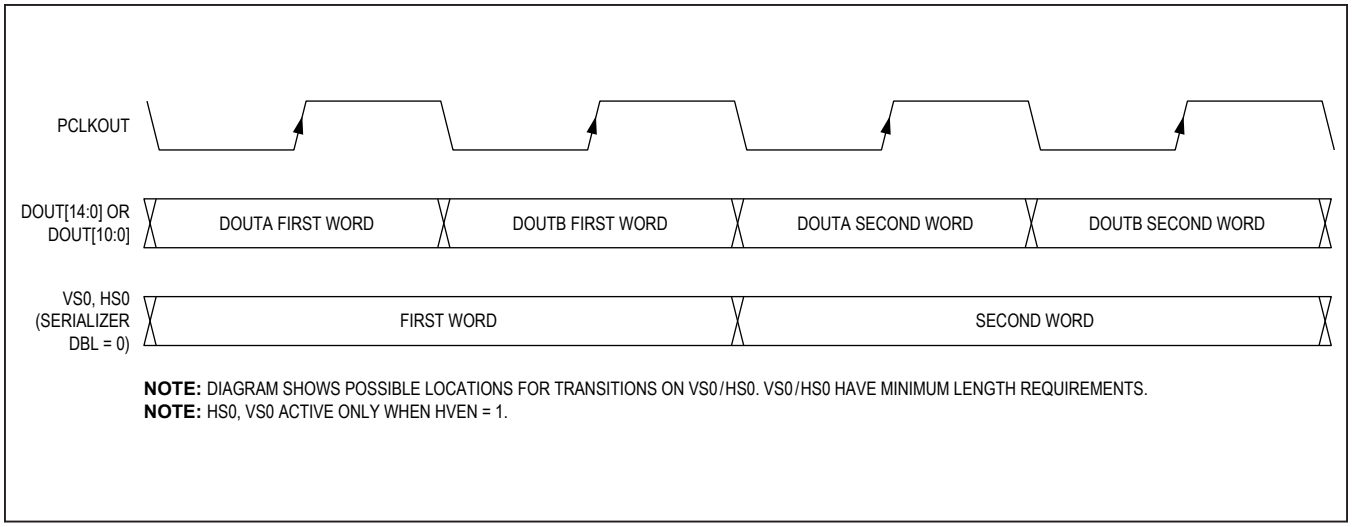


Figure 13. Double-Output Waveform (Serializer Using Single Input)

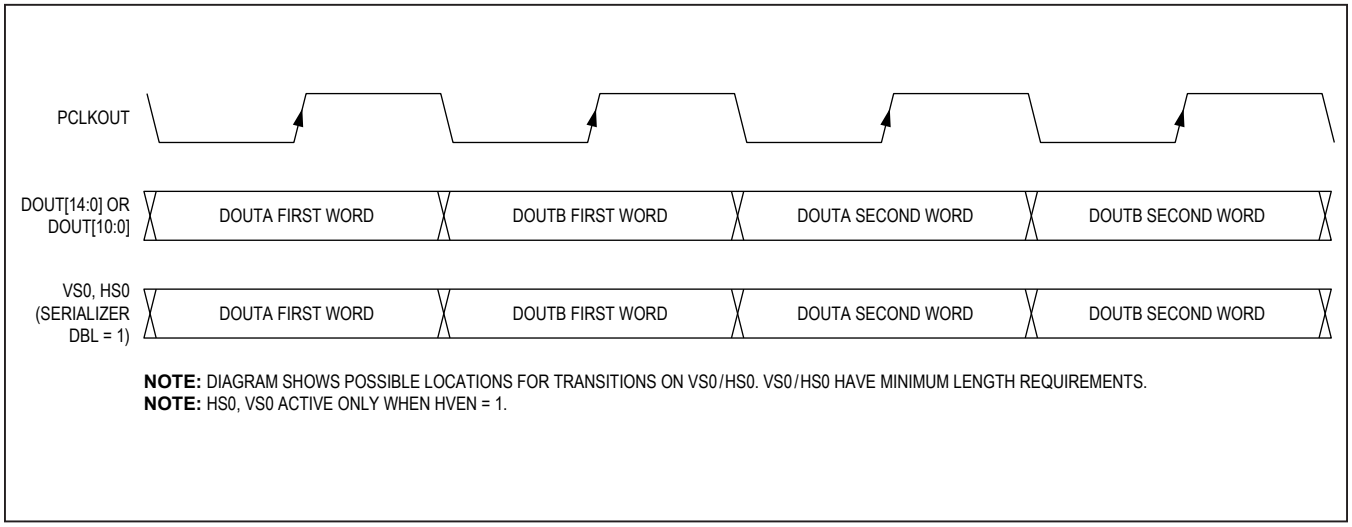


Figure 14. Double-Output Waveform (Serializer Using Double Input)

Table 1. Power-Up Default Register Map (see Table 16)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x00	0x80	SERID = 1000000, serializer device address RESERVED = 0
0x01	0x90 or 0x92	DESID = 1001000 (CX/TP = high or low), DESID = 1001001 (CX/TP = midlevel), deserializer device address is determined by the state of the CX/TP input at power-up CFGBLOCK = 0, registers 0x00 to 0x1F are read/write
0x02	0x1F	SS = 00, spread spectrum disabled RESERVED = 01 PRNG = 11, automatically detect the pixel clock range SRNG = 11, automatically detect serial-data rate
0x03	0x00	AUTOFM = 00, calibrate spread-modulation rate only once after locking RESERVED = 0 SDIV = 00000, autocalibrate sawtooth divider
0x04	0x07	LOCKED = 0, LOCK output is low (read only) OUTENB = 0, output enabled PRBSEN = 0, PRBS test disabled SLEEP = 0, sleep mode deactivated (see the Link Startup Procedure section) INTTYPE = 01, base mode uses UART REVCCEN = 1, reverse control channel active (sending) FWDCCEN = 1, forward control channel active (receiving)
0x05	0x24	I2CMETHOD = 0, I²C master sends the register address DCS = 0, normal parallel output driver current HVTRMODE = 1, full periodic HS/VS tracking ENEQ = 0, equalizer disabled EQTUNE = 1001, 10.7dB equalization
0x06	0x02 or 0x22	RESERVED = 00X00010
0x07	0xXX	DBL = 0 or 1, single-/double-input mode setting determined by the state of LCCEN and GPIO0/DBL at startup DRS = 0, high data-rate mode BWS = 0 or 1, bit width setting determined by the state of LCCEN and GPIO1/BWS at startup ES = 0 or 1, edge-select input setting determined by the state of LCCEN and TX/SCL/ES at startup HVTRACK = 0 or 1, HS/VS tracking setting determined by the state of LCCEN and MS/HVEN at startup HVEN = 0 or 1, HS/VS tracking encoding setting determined by the state of LCCEN and MS/HVEN at startup EDC = 00 or 10, error-detection/correction setting determined by the state of LCCEN and RX/SDA/EDC at startup

Table 1. Power-Up Default Register Map (see Table 16) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x08	0x00	INVVS = 0, deserializer does not invert VSYNC INVHS = 0, deserializer does not invert HSYNC RESERVED = 0 UNEQDBL = 0, serializer DBL is not the same as deserializer DISSTAG = 0, outputs are staggered AUTORST = 0, error registers/output autoreset disabled ERRSEL = 00, detected errors trigger $\overline{ERR}$
0x09	0x00	I2CSCRA = 0000000, I²C address translator source A is 0x00 RESERVED = 0
0x0A	0x00	I2CDSTA = 0000000, I²C address translator destination A is 0x00 RESERVED = 0
0x0B	0x00	I2CSCRB = 0000000, I²C address translator source B is 0x00 RESERVED = 0
0x0C	0x00	I2CDSTB = 0000000, I²C address translator destination B is 0x00 RESERVED = 0
0x0D	0xB6	I2CLOCACK = 1, acknowledge not generated when forward channel is not available I2CSLVSH = 01, 469ns/234ns I²C setup/hold time I2CMSTBT = 101, 339kbps (typ) I²C-to-I²C master bit-rate setting I2CSLVTO = 10, 1024Fs (typ) I²C-to-I²C slave remote timeout
0x0E	0x6A	RESERVED = 01 GPIEN = 1, enable GPI-to-GPO signal transmission to serializer GPIIN = 0, GPI input is low (read only) GPIO1OUT = 1, set GPIO1 to high GPIO1IN = 0, GPIO1 input is low (read only) GPIO0OUT = 1, set GPIO0 to high GPIO0IN = 0, GPIO0 input is low (read only)
0x0F	0x00	DETTHR = 00000000, error threshold set to zero for detected errors
0x10	0x00 (read only)	DETERR = 00000000, zero errors detected
0x11	0x00	CORRTHR = 00000000, error threshold set to zero for corrected errors
0x12	0x00 (read only)	CORRERR = 00000000, zero errors corrected
0x13	0x00 (read only)	PRBSERR = 00000000, zero PRBS errors detected
0x14	0x00 (read only)	PRBSOK = 0, PRBS test not completed RESERVED = 0000000
0x15	0x2X	RESERVED = 00100XXX
0x16	0x30	RESERVED = 00110000
0x17	0x54	RESERVED = 01010100
0x18	0x30	RESERVED = 00110000
0x19	0xC8	RESERVED = 11001000

Table 1. Power-Up Default Register Map (see Table 16) (continued)

REGISTER ADDRESS (hex)	POWER-UP DEFAULT (hex)	POWER-UP DEFAULT SETTINGS (MSB FIRST)
0x1A	0xXX (read only)	RESERVED = XXXXXXXX
0x1B	0xXX (read only)	RESERVED = XXXXXXXX
0x1C	0xXX (read only)	RESERVED = XXXXXXXX
0x1D	0x0X (read only)	CXTP = 0, twisted-pair input CXSEL = 0, noninverting input I2CSEL = 0, UART input LCCEN = 0, local control channel disabled RESERVED = XXXX
0x1E	0x0A (read only)	ID = 00001010, device ID is 0x0A
0x1F	0x0X (read only)	RESERVED = 000 CAPS = 0, not HDCP capable REVISION = XXXX

X = Indeterminate.

Table 2. Output Map

EDC	BWS	DBL	HVEN	OUTPUT* (PAIRED WITH MAX9271)	OUTPUT* (PAIRED WITH MAX9273)	PCLK RANGE** (MHz)
0	0	0	0	DOUT0–DOUT15	DOUT0–DOUT21	16.66 to 50
0	0	0	1	DOUT0–DOUT13, HS, VS	DOUT0–DOUT21, HS, VS	16.66 to 50
0	0	1	0	DOUT0–DOUT10	DOUT0–DOUT10	33.33 to 100
0	0	1	1	DOUT0–DOUT10, HS, VS	DOUT0–DOUT10, HS, VS	33.33 to 100
0	1	0	0	DOUT0–DOUT15	DOUT0–DOUT21	12.5 to 37.5
0	1	0	1	DOUT0–DOUT13, HS, VS	DOUT0–DOUT21, HS, VS	12.5 to 37.5
0	1	1	0	DOUT0–DOUT14	DOUT0–DOUT14	25 to 75
0	1	1	1	DOUT0–DOUT13, HS, VS	DOUT0–DOUT14, HS, VS	25 to 75
1	0	0	0	DOUT0–DOUT15	DOUT0–DOUT15	16.66 to 50
1	0	0	1	DOUT0–DOUT13, HS, VS	DOUT0–DOUT15, HS, VS	16.66 to 50
1	0	1	0	DOUT0–DOUT7	DOUT0–DOUT7	33.33 to 100
1	0	1	1	DOUT0–DOUT7, HS, VS	DOUT0–DOUT7, HS, VS	33.33 to 100
1	1	0	0	DOUT0–DOUT15	DOUT0–DOUT21	12.5 to 37.5
1	1	0	1	DOUT0–DOUT13, HS, VS	DOUT0–DOUT21, HS, VS	12.5 to 37.5
1	1	1	0	DOUT0–DOUT11	DOUT0–DOUT11	25 to 75
1	1	1	1	DOUT0–DOUT11, HS, VS	DOUT0–DOUT11, HS, VS	25 to 75

**The number of available outputs depends on the serializer attached to the MAX9272A.*

***Device is in high-speed mode (DRS = low). See Table 3 for PCLK ranges in low-speed mode (DRS = high).*

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coax cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded. The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit or 32-bit mode, 22 or 30 bits contain the video data and/or error-correction bits, if used. The 23rd or 31st bit carries the forward control-channel data. The last bit is the parity bit of the previous 23 or 31 bits (Figure 15).

Reverse Control Channel

The serializer uses the reverse control channel to receive I²C/UART and GPO signals from the deserializer in the opposite direction of the video stream. The reverse control channel and forward video data coexist on the same serial cable, forming a bidirectional link. The reverse control channel operates independently from the forward control channel. The reverse control channel is available 2ms after power-up. The serializer temporarily disables the reverse control channel for 350µs after starting/stopping the forward serial link.

Data-Rate Selection

The serializer/deserializer use DRS, DBL, and BWS to set the PCLKOUT frequency range (Table 3). Set DRS = 1 for a PCLKOUT frequency range of 6.25MHz to 12.5MHz (32-bit, single-output mode) or 8.33MHz to 16.66MHz (24-bit, single-output mode). Set DRS = 0 for normal operation. It is not recommended to use double-output mode when DRS = 1.

Table 3. Data-Rate Selection Table

DRS SETTING	DBL SETTING	BWS SETTING	PCLKOUT RANGE (MHz)
0	0 (single input)	0 (24-bit mode)	16.66 to 50
0	0	1 (32-bit mode)	12.5 to 35
0	1 (double input)	0	33.3 to 100
0	1	1	25 to 75
1	0	0	8.33 to 16.66
1	0	1	6.25 to 12.5
1	1	0	Do Not Use
1	1	1	Do Not Use

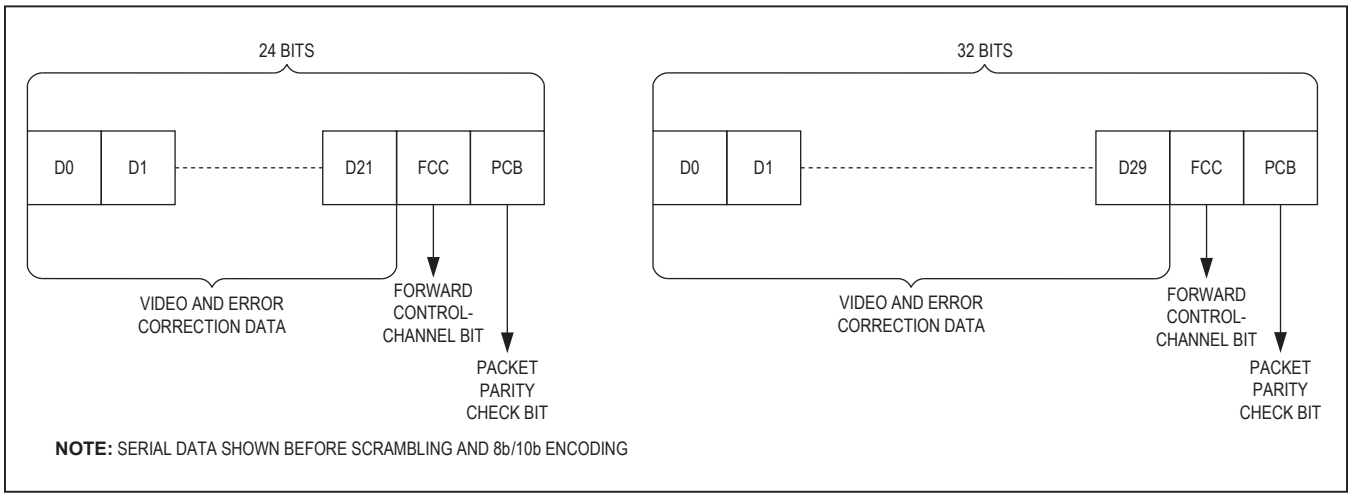


Figure 15. Serial-Data Format

Control Channel and Register Programming

The control channel is available for the µC to send and receive control data over the serial link simultaneously with the high-speed data. The µC controls the link from either the serializer or the deserializer side to support video-display or image-sensing applications. The control channel between the µC and serializer or deserializer runs in base mode or bypass mode, according to the mode selection (MS/HVEN) input of the device connected to the µC. Base mode is a half-duplex control channel and bypass mode is a full-duplex control channel.

UART Interface

In base mode, the µC is the host and can access the registers of both the serializer and deserializer from either side of the link using the GMSL UART protocol. The µC can also program the peripherals on the remote side by sending the UART packets to the serializer or deserializer, with the UART packets converted to I²C by the device on the remote side of the link. The µC communicates with a UART peripheral in base mode (through INTTYPE register settings), using the half-duplex default GMSL UART protocol of the serializer/deserializer. The device addresses of the serializer/deserializer in base mode are programmable. The default value is 0x80 for the serializer and is determined by the CX/TP input for the deserializer (Table 8).

When the peripheral interface is I²C, the serializer/deserializer convert UART packets to I²C that have device addresses different from those of the serializer or deserializer. The converted I²C bit rate is the same as the original UART bit rate.

The deserializer uses differential line coding to send signals over the reverse channel to the serializer. The bit rate of the control channel is 9.6kbps to 1Mbps in both directions. The serializer/deserializer automatically detect the control-channel bit rate in base mode. Packet bit-rate changes can be made in steps of up to 3.5 times higher or lower than the previous bit rate. See the *Changing the Clock Frequency* section for more information.

Figure 16 shows the UART protocol for writing and reading in base mode between the µC and the serializer/deserializer.

Figure 17 shows the UART data format. Even parity is used. Figure 18 and Figure 19 detail the formats of the SYNC byte (0x79) and the ACK byte (0xC3). The µC and the connected slave chip generate the SYNC byte and ACK byte, respectively. Events such as device wake-up and GPI generate transitions on the control channel that can be ignored by the µC. Data written to the serializer/deserializer registers do not take effect until after the ACK byte is sent. This allows the µC to verify that write commands are received without error, even if the result of the write command directly affects the serial link. The slave uses the SYNC byte to synchronize with the host UART's data rate. If the GPI or MS/HVEN inputs of the deserializer toggle while there is control-channel communication, or if a line fault occurs, the control-channel communication is corrupted. In the event of a missed or delayed acknowledge (~1ms due to control-channel timeout), the µC should assume there was an error in the packet slave device received it, or that an error occurred during transmission or response. In base mode, the µC must keep the UART Tx/Rx lines high no more than 4 bit times between bytes in a packet. Keep the UART Tx/Rx lines for at least 16 bit times before starting to send a new packet.

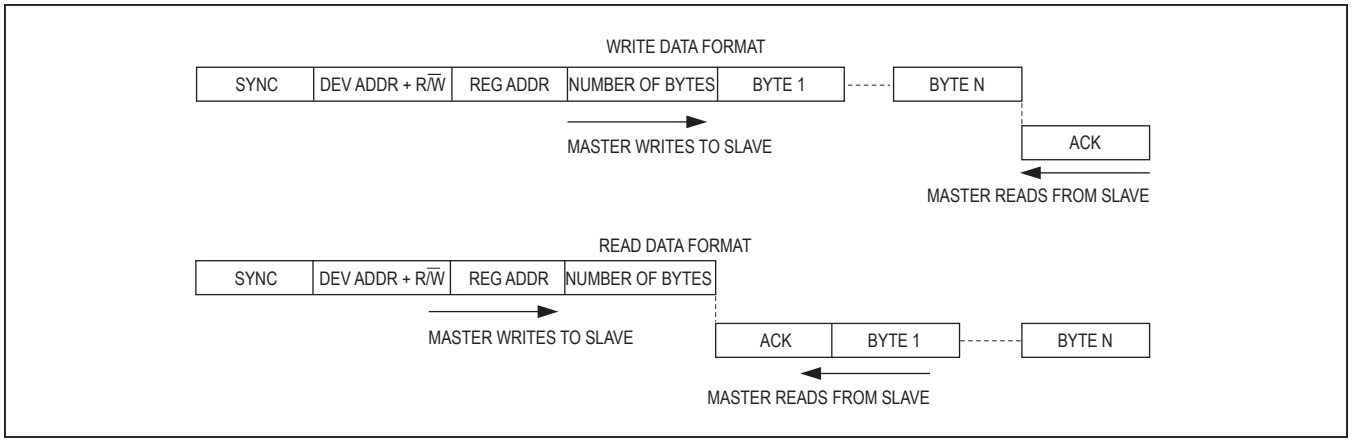


Figure 16. GMSL UART Protocol for Base Mode