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MAX9276A/MAX9280A

3.12Gbps GMSL Deserializers for Coax or STP Input and Parallel Output

General Description

The MAX9276A/MAX9280A gigabit multimedia serial link (GMSL) deserializers receive data from a GMSL serializer over 50Ω coax or 100Ω shielded twisted-pair (STP) cable and output deserialized data on the LVCMOS outputs.

The MAX9280A has HDCP content protection but otherwise is the same as the MAX9276A. The deserializers pair with any GMSL serializer capable of coax output including the MAX9293 HDMI/MHL serializer. When programmed for STP input they are backward compatible with any GMSL serializer.

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-to-UART and UART-to-I²C modes, and up to 1Mbps in I²C-to-I²C mode. Using the control channel, a μC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9280A). Two GPIO ports are included, allowing display power-up and switching of the backlight among other uses. A continuously sampled GPI input supports touch-screen controller interrupt requests in display applications.

For use with longer cables, the deserializers have a programmable cable equalizer. Programmable spread spectrum is available on the parallel output. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 3.0V to 3.6V and the I/O supply is 1.7V to 3.6V.

The devices are in lead-free, 56-pin, 8mm x 8mm TQFN and QFND packages with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Benefits and Features

- Ideal for High-Definition Video Applications
 - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
 - 104MHz High-Bandwidth Mode Supports 1920x720p/60Hz Display With 24-Bit Color
 - Equalization Allows 15m Cable at Full Speed
 - Up to 192kHz Sample Rate And 32-Bit Sample Depth For 7.1 Channel HD Audio
 - Audio Clock from Audio Source or Audio Sink
 - Color Lookup Table for Gamma Correction
 - CNTL[3:0] Control Outputs
- Multiple Data Rates for System Flexibility
 - Up to 3.12Gbps Serial-Bit Rate
 - 6.25MHz to 104MHz Pixel Clock
 - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock-Stretch Capability
- Reduces EMI and Shielding Requirements
 - Programmable Spread Spectrum Reduces EMI
 - Tracks Spread Spectrum on Input
 - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
 - Built-In PRBS Tester for BER Testing of the Serial Link
 - Programmable Choice of 8 Default Device Addresses
 - Two Dedicated GPIO Ports
 - Dedicated “Up/Down” GPI for Touch-Screen Interrupt and Other Uses
 - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
 - -40°C to +105°C Operating Temperature
 - ±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

[Ordering Information and Typical Application Circuit](#) appear at end of data sheet.

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Absolute Maximum Ratings (Note 1)

AVDD to EP	-0.5V to +3.9V
DVDD to EP	-0.5V to +3.9V
IOVDD to EP	-0.5V to +3.9V
IN+, IN- to EP	-0.5V to +1.9V
All Other Pins to EP	-0.5V to (V _{IOVDD} + 0.5V)
IN+, IN- Short Circuit to Ground or Supply	Continuous

Continuous Power Dissipation (T _A = +70°C)	
TQFN (derate 47.6mW/°C above +70°C).....	3809.5mW
QFND (derate 4.2mW/°C above +70°C).....	3418mW
Junction Temperature.....	+150°C
Storage Temperature.....	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN		QFND	
Junction-to-Ambient Thermal Resistance (θ _{JA})	21°C/W	Junction-to-Ambient Thermal Resistance (θ _{JA}).....	23.4°C/W
Junction-to-Case Thermal Resistance (θ _{JC}).....	1°C/W	Junction-to-Case Thermal Resistance (θ _{JC}).....	1.6°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (ADD_, HIM, I2CSEL, GPI, PWDN, MS)						
High-Level Input Voltage	V _{IH1}		0.65 x V _{IOVDD}			V
Low-Level Input Voltage	V _{IL1}			0.35 x V _{IOVDD}		V
Input Current	I _{IN1}	V _{IN} = 0V to V _{IOVDD}	-10		+20	µA
THREE-LEVEL LOGIC INPUTS (BWS, CX/TP)						
High-Level Input Voltage	V _{IH}		0.7 x V _{IOVDD}			V
Low-Level Input Voltage	V _{IL}			0.3 x V _{IOVDD}		V
Mid-Level Input Current	I _{INM}	(Note 4)	-10		10	µA
Input Current	I _{IN}		-150		150	µA
SINGLE-ENDED OUTPUTS (WS, SCK, SD, DOUT_, CNTL_, INTOUT, PCLKOUT)						
High-Level Output Voltage	V _{OH1}	I _{OUT} = -2mA	DCS = '0'		V _{IOVDD} - 0.3	V
			DCS = '1'		V _{IOVDD} - 0.2	
Low-Level Output Voltage	V _{OL1}	I _{OUT} = 2mA	DCS = '0'		0.3	V
			DCS = '1'		0.2	

DC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
OUTPUT Short-Circuit Current	I_{OS}	DOUT_	$V_O = 0V$, DCS = '0'	$V_{IOVDD} = 3.0V$ to $3.6V$	15	25	39	mA
				$V_{IOVDD} = 1.7V$ to $1.9V$	3	7	13	
			$V_O = 0V$, DCS = '1'	$V_{IOVDD} = 3.0V$ to $3.6V$	20	35	63	
				$V_{IOVDD} = 1.7V$ to $1.9V$	5	10	21	
		PCLKOUT	$V_O = 0V$, DCS = '0'	$V_{IOVDD} = 3.0V$ to $3.6V$	15	33	50	
				$V_{IOVDD} = 1.7V$ to $1.9V$	5	10	17	
			$V_O = 0V$, DCS = '1'	$V_{IOVDD} = 3.0V$ to $3.6V$	30	54	97	
				$V_{IOVDD} = 1.7V$ to $1.9V$	9	16	32	
OPEN-DRAIN INPUTS/OUTPUTS (GPIO0, GPIO1, RX/SDA, TX/SCL, ERR, LOCK)								
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V	
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V	
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL	-100		+5	μA	
			LOCK, ERR, GPIO_	-80		+5		
Low-Level Output Voltage	V_{OL2}	$I_{OUT} = 3mA$	$V_{IOVDD} = 1.7V$ to $1.9V$			0.4	V	
			$V_{IOVDD} = 3.0V$ to $3.6V$			0.3		
Input Capacitance	C_{IN}	Each pin (Note 6)				10	pF	
OUTPUTS FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage (V_{IN+}) - (V_{IN-})	V_{RODH}	Forward channel disabled, Figure 1	Legacy reverse control-channel mode	30		60	mV	
			High-immunity mode	50		100		
Differential Low Output Peak Voltage (V_{IN+}) - (V_{IN-})	V_{RODL}	Forward channel disabled, Figure 1	Legacy reverse control-channel mode	-60		-30	mV	
			High-immunity mode	-100		-50		
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled	Legacy reverse control-channel mode	30		60	mV	
			High-immunity mode	50		100		
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled	Legacy reverse control-channel mode	-60		-30	mV	
			High-immunity mode	-100		-50		

DC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS	
DIFFERENTIAL INPUTS (IN+, IN-)									
Differential High Input Threshold (Peak) Voltage (V_{IN+}) - (V_{IN-})	$V_{IDH(P)}$	Figure 2	Activity detector medium Threshold, (0x0B D[6:5] = 01)				60	mV	
			Activity detector low Threshold, (0x0B D[6:5] = 00)				47.5		
Differential Low Input Threshold (Peak) Voltage (V_{IN+}) - (V_{IN-})	$V_{IDL(P)}$	Figure 2	Activity detector medium Threshold, (0x0B D[6:5] = 01)		-60			mV	
			Activity detector medium Threshold, (0x0B D[6:5] = 00)		-47.5				
Input Common-Mode Voltage ($(V_{IN+}) + (V_{IN-})/2$)	V_{CMR}				1	1.3	1.6	V	
Differential Input Resistance (Internal)	R_{IN}				80	100	130	Ω	
SINGLE-ENDED INPUTS (IN+, IN-)									
Single-Ended High Input Threshold (Peak) Voltage (Figure 3)	$V_{ISH(P)}$	Activity detector medium threshold, (0x0B D[6:5] = 01)					43	mV	
		Activity detector low threshold, (0x0B D[6:5] = 00)					33		
Single-Ended Low Input Threshold (Peak) Voltage (Figure 3)	$V_{ISL(P)}$	Activity detector medium threshold, (0x0B D[6:5] = 01)			-43			mV	
		Activity detector medium threshold, (0x0B D[6:5] = 00)			-33				
Input Resistance (Internal)	R_I				40	50	65	Ω	
POWER SUPPLY									
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 4)	I_{WCS}	BWS = low, $f_{PCLKOUT} = 16.6MHz$	2% spread active	$C_L = 5pF$			131	164	mA
				$C_L = 10pF$			136	169	
			Spread spectrum disabled	$C_L = 5pF$			122	153	
				$C_L = 10pF$			127	158	
		BWS = low, $f_{PCLKOUT} = 33.3MHz$	2% spread active	$C_L = 5pF$			144	179	
				$C_L = 10pF$			153	189	
			Spread spectrum disabled	$C_L = 5pF$			133	167	
				$C_L = 10pF$			142	177	
		BWS = low, $f_{PCLKOUT} = 66.6MHz$	2% spread active	$C_L = 5pF$			175	216	
				$C_L = 10pF$			190	233	
			Spread spectrum disabled	$C_L = 5pF$			159	197	
				$C_L = 10pF$			174	214	

DC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 4)	I_{WCS}	BWS = low, $f_{PCLKOUT} = 104MHz$	2% spread active	$C_L = 5pF$	212	255	mA
				$C_L = 10pF$	234	278	
			Spread spectrum disabled	$C_L = 5pF$	190	228	
				$C_L = 10pF$	212	251	
		BWS = mid, $f_{PCLKOUT} = 36.6MHz$	2% spread active	$C_L = 5pF$	154	191	
				$C_L = 10pF$	164	203	
			Spread spectrum disabled	$C_L = 5pF$	143	177	
				$C_L = 10pF$	154	189	
		BWS = mid, $f_{PCLKOUT} = 104MHz$	2% spread active	$C_L = 5pF$	231	277	
				$C_L = 10pF$	257	305	
			Spread spectrum disabled	$C_L = 5pF$	209	249	
				$C_L = 10pF$	234	277	
Sleep Mode Supply Current	I_{CCS}			70	265	μA	
Power-Down Current	I_{CCZ}	PWDN = GND		20	195	μA	
ESD PROTECTION							
IN+, IN- (Note 8)	V_{ESD}	Human body model, $R_D = 1.5k\Omega$, $C_S = 100pF$		± 8		kV	
		IEC 61000-4-2, $R_D = 330\Omega$, $C_S = 150pF$	Contact discharge	± 10			
			Air discharge	± 12			
		ISO 10605, $R_D = 2k\Omega$, $C_S = 330pF$	Contact discharge	± 10			
Air discharge	± 20						
All Other Pins (Note 9)	V_{ESD}	Human body model, $R_D = 1.5k\Omega$, $C_S = 100pF$		± 4		kV	

AC Electrical Characteristics

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)						
Clock Frequency	$f_{PCLKOUT}$	BWS = low, DRS = '1'	8.33		16.66	MHz
		BWS = low, DRS = '0'	16.66		104	
		BWS = mid, DRS = '1'	18.33		36.66	
		BWS = mid, DRS = '0'	36.66		104	
		BWS = high, DRS = '1'	6.25		12.5	
		BWS = high, DRS = '0'	12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Note 6)	40	50	60	%
Clock Jitter	t_J	Period jitter, peak-to-peak, spread off, 3.12Gbps, PRBS pattern, $UI = 1/f_{PCLKOUT}$ (Note 6)		0.05		UI
I²C/UART PORT TIMING						
I ² C/UART Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, $C_L = 10pF$ to $100pF$, $1k\Omega$ pullup to V_{IOVDD}	20		150	ns
Output Fall Time	t_F	70% to 30%, $C_L = 10pF$ to $100pF$, $1k\Omega$ pullup to V_{IOVDD}	20		150	ns
I²C TIMING (Figure 5)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)	> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)	> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0	μs
			Mid		0.6	
			High		0.26	
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7	μs
			Mid		1.3	
			High	$V_{IOVDD} = 1.7V$ to $< 3V$ (Note 11)	0.6	
				$V_{IOVDD} = 3.0V$ to $3.6V$	0.5	
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0	μs
			Mid		0.6	
			High		0.26	
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7	μs
			Mid		0.6	
			High		0.26	

AC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low			0	μs	
			Mid			0		
			High			0		
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low			250	μs	
			Mid			100		
			High			50		
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low			4.0	μs	
			Mid			0.6		
			High			0.26		
Bus Free Time	t_{BUF}	f_{SCL} range	Low			4.7	μs	
			Mid			1.3		
			High			0.5		
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low			3.45	μs	
			Mid			0.9		
			High	$V_{IOVDD} = 1.7V$ to $< 3V$ (Note 12)				0.55
				$V_{IOVDD} = 3.0V$ to $3.6V$				0.45
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low			3.45	μs	
			Mid			0.9		
			High	$V_{IOVDD} = 1.7V$ to $< 3V$ (Note 13)				0.55
				$V_{IOVDD} = 3.0V$ to $3.6V$				0.45
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low			50	ns	
			Mid			50		
			High			50		
Capacitive Load Each Bus Line	C_b					100	pF	
SWITCHING CHARACTERISTICS								
PCLKOUT Rise-and-Fall Time (Note 6, Figure 6)	t_R, t_F	20% to 80%, $V_{IOVDD} = 1.7V$ to $1.9V$	DCS = '1', $C_L = 10pF$			0.4	ns	
			DCS = '0', $C_L = 5pF$			0.5		
		20% to 80%, $V_{IOVDD} = 3.0V$ to $3.6V$	DCS = '1', $C_L = 10pF$			0.25	1.8	
			DCS = '0', $C_L = 5pF$			0.3		
Parallel Data Rise-and-Fall Time (Note 6, Figure 7)	t_R, t_F	20% to 80%, $V_{IOVDD} = 1.7V$ to $1.9V$	DCS = '1', $C_L = 10pF$			0.5	ns	
			DCS = '0', $C_L = 5pF$			0.6		
		20% to 80%, $V_{IOVDD} = 3.0V$ to $3.6V$	DCS = '1', $C_L = 10pF$			0.3	2.2	
			DCS = '0', $C_L = 5pF$			0.4		

AC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deserializer Delay	t_{SD}	Figure 8 (Notes 6, 14)	Spread spectrum enabled			6960	Bits
			Spread spectrum disabled			2160	
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission, Figure 1 (Note 6)		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission, Figure 1 (Note 6)		180		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included), Figure 9				350	μs
Lock Time	t_{LOCK}	(Figure 10)	Spread spectrum enabled			3	ms
			Spread spectrum disabled			2	
Power-Up Time	t_{PU}	(Figure 11)				8	ms
I²S/TDM OUTPUT TIMING (Note 6)							
WS Jitter	t_{jWS}	$t_{WS} = 1/f_{WS}$, (cycle-to-cycle), rising-to-falling edge or falling-to- rising edge	$f_{WS} = 48kHz$ or 44.1kHz		$1.2e-3$	$1.5e-3$	ns
			$f_{WS} = 96kHz$		$1.6e-3$	$2e-3$	
			$f_{WS} = 192kHz$		$1.6e-3$	$2e-3$	
SCK Jitter (2-Channel I ² S)	t_{jSCK1}	$t_{SCK} = 1/f_{SCK}$, (cycle-to-cycle), rising-to-rising edge	$n_{SCK} = 16$ bits, $f_{SCK} = 48kHz$ or 44.1kHz		$13e-3$	$16e-3$	ns
			$n_{SCK} = 24$ bits, $f_{WS} = 96kHz$		$39e-3$	$48e-3$	
			$n_{SCK} = 32$ bits, $f_{WS} = 192kHz$		0.1	0.13	
SCK Jitter (8-Channel TDM)	t_{jSCK2}	$t_{SCK} = 1/f_{SCK}$, (cycle-to-cycle), rising-to-rising edge	$n_{SCK} = 16$ bits, $f_{WS} = 48kHz$ or 44.1kHz		$52e-3$	$64e-3$	ns
			$n_{SCK} = 24$ bits, $f_{WS} = 96kHz$		$156e-3$	$192e-3$	
			$n_{SCK} = 32$ bits, $f_{WS} = 192kHz$		0.4	0.52	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			$3 \times t_{WS}$	$4 \times t_{WS}$	μs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	$C_L = 10pF$, DCS = 1	0.3		3.1	ns
			$C_L = 5pF$, DCS = 0	0.4		3.8	

AC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SD, WS Valid Time Before SCK (2-Channel I ² S)	t_{DVB1}	$t_{SCK} = 1/f_{SCK}$ (Figure 12)	$0.20 \times t_{SCK}$	$0.5 \times t_{SCK}$		ns
SD, WS Valid Time After SCK (2-Channel I ² S)	t_{DVA1}	$t_{SCK} = 1/f_{SCK}$ (Figure 12)	$0.20 \times t_{SCK}$	$0.5 \times t_{SCK}$		ns
SD, WS Valid Time Before SCK (8-Channel TDM)	t_{DVB2}	$t_{SCK} = 1/f_{SCK}$ (Figure 12)	$0.20 \times t_{SCK}$	$0.5 \times t_{SCK}$		ns
SD, WS Valid Time After SCK (8-Channel TDM)	t_{DVA2}	$t_{SCK} = 1/f_{SCK}$ (Figure 12)	$0.20 \times t_{SCK}$	$0.5 \times t_{SCK}$		ns

Note 3: Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a mid level, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than $\pm 10\mu A$.

Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 6: Not production tested. Guaranteed by design.

Note 7: HDCP not enabled (MAX9280A only). IOVDD current is not production tested. See [Table 23](#) for additional supply current when HDCP is enabled

Note 8: Specified pin to ground.

Note 9: Specified pin to all supply/ground.

Note 10: Not production tested, guaranteed by bench characterization.

Note 11: The I²C bus standard t_{LOW} (min) = $0.5\mu s$.

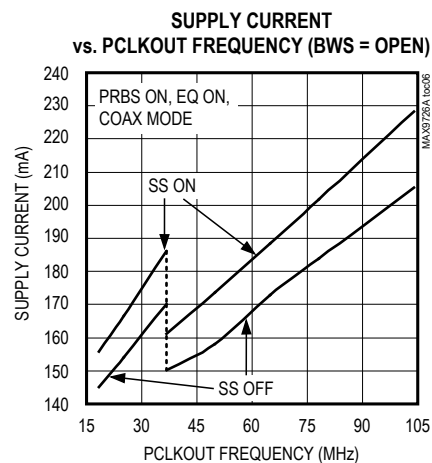
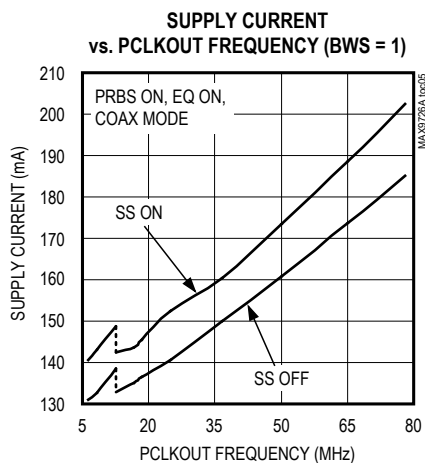
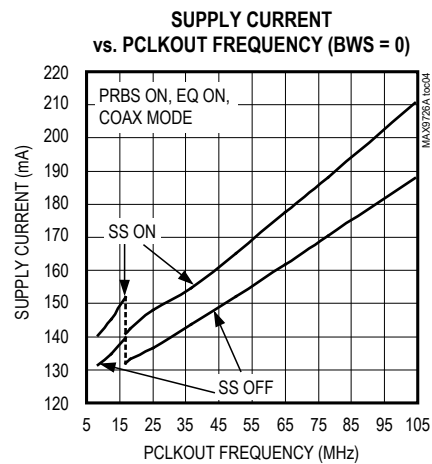
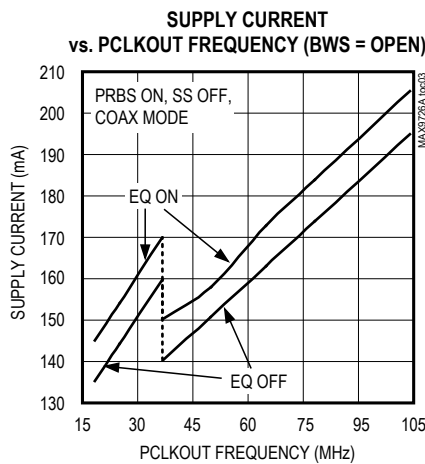
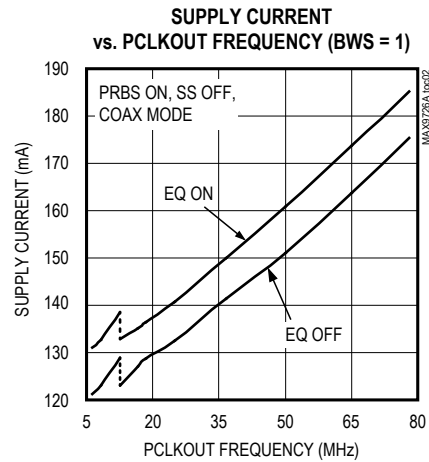
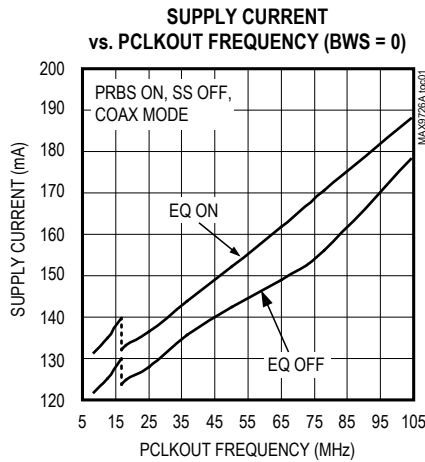
Note 12: The I²C bus standard $t_{VD:DAT}$ (max) = $0.45\mu s$.

Note 13: The I²C bus standard $t_{VD:ACK}$ (max) = $0.45\mu s$.

Note 14: Measured in serial link bit times. Bit time = $1/(30 \times f_{PCLKIN})$ for BWS = '0' or open. Bit time = $1/(40 \times f_{PCLKIN})$ for BWS = '1'.

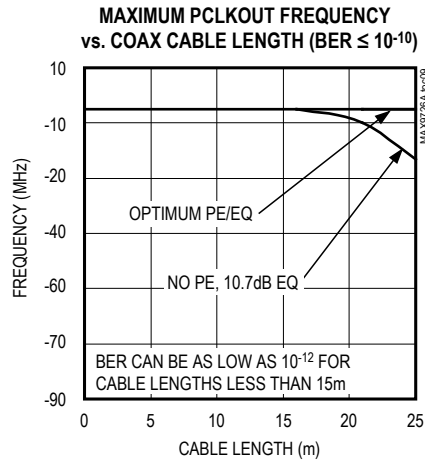
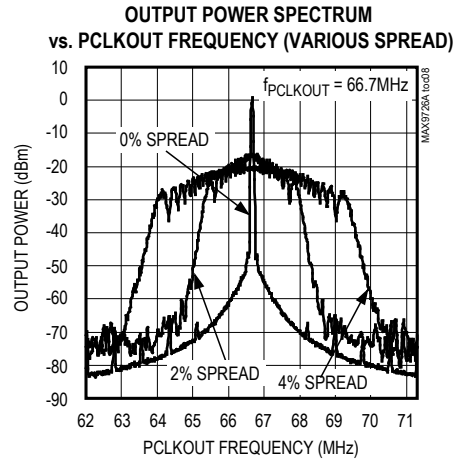
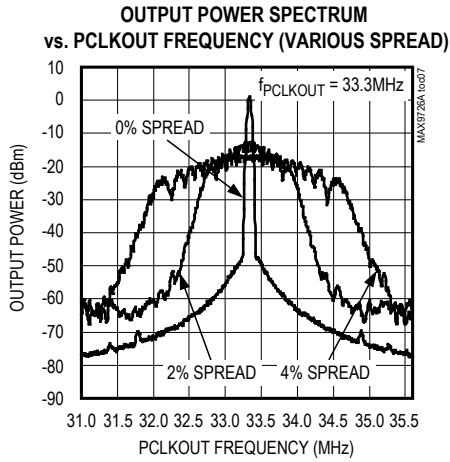
Typical Operating Characteristics

($V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

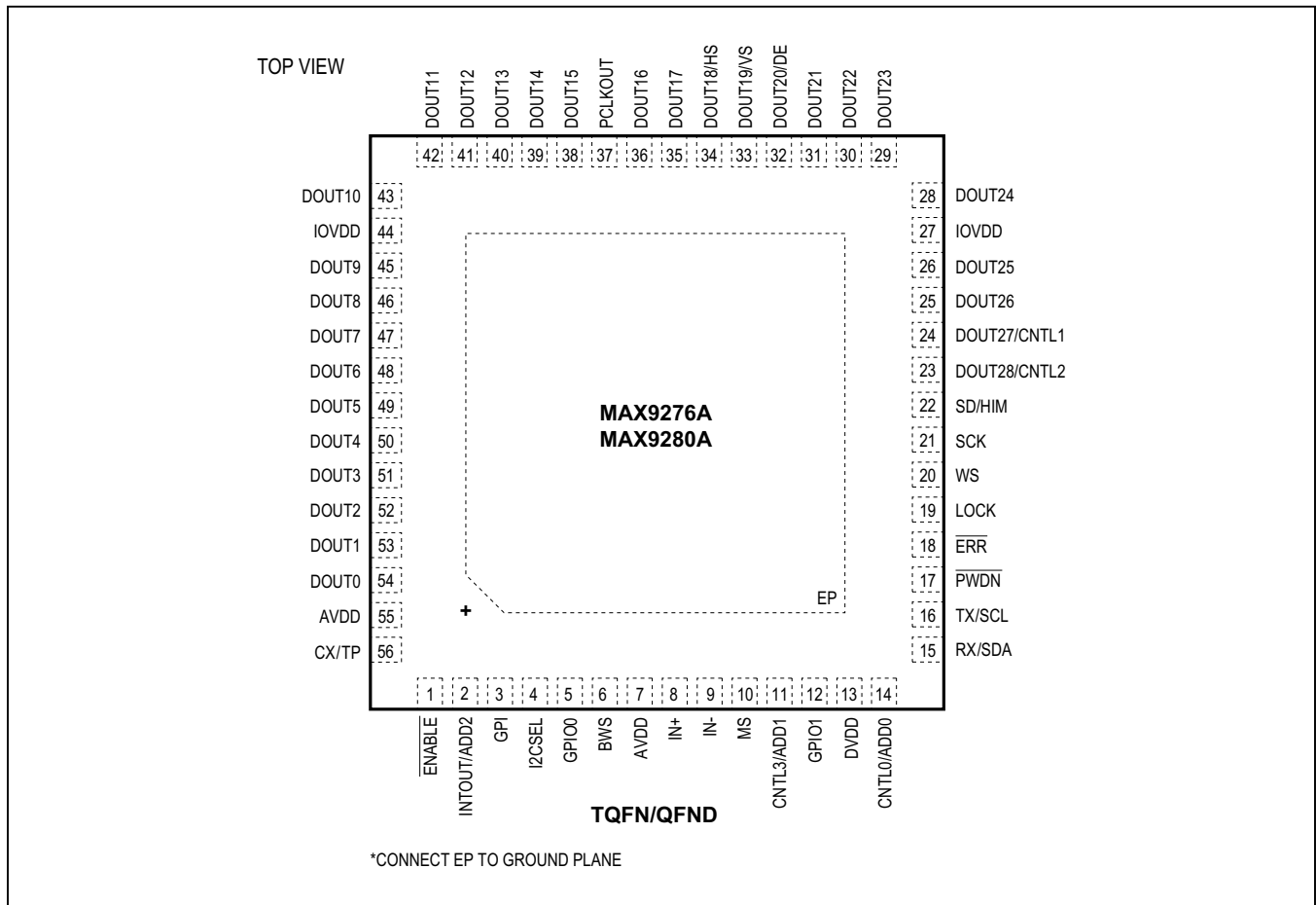


Typical Operating Characteristics (continued)

($V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{ENABLE}}$	Active-Low Parallel Output-Enable Input With Internal Pulldown to EP. Set $\overline{\text{ENABLE}}$ = low to enable PCLKOUT DOUT_ and CNTL_ outputs. Set $\overline{\text{ENABLE}}$ = high to put PCLKOUT, DOUT_ and CNTL_ into high impedance.
2	INTOUT/ADD2	A/V Status Register Interrupt Output/Address Selection Input With Internal Pulldown to EP. Functions as ADD2 input at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to INTOUT output automatically after power-up. ADD2: Bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1. Connect INTOUT/ADD2 to IOVDD with a 30kΩ resistor to set high or leave open to set low. INTOUT: Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
3	GPI	General-Purpose Input With Internal Pulldown to EP. The serializer GPO (or INT) output follows GPI.
4	I2CSEL	I ² C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I ² C interface. Set I2CSEL = low to select UART interface.
5	GPIO0	Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD

Pin Description (continued)

PIN	NAME	FUNCTION
6	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low for 24 bit mode. Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode.
7, 55	AVDD	3.3V Analog Power Supply. Bypass AVDD to EP with 0.1 μ F and 0.001 μ F capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
8	IN+	Noninverting Coax/Twisted-Pair Serial Input
9	IN-	Inverting Coax/Twisted-Pair Serial Input
10	MS	Mode Select with Internal Pulldown to EP. Set MS = low, to select base mode. Set MS = high to select the bypass mode.
11	CNTL3/ADD1	Auxiliary Control Signal Output/Address Selection Input with Internal Pulldown to EP. Functions as ADD1 input at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to CNTL3 output automatically after power-up. ADD1: Bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1. Connect CNTL3/ADD1 to IOVDD with a 30k Ω resistor to set high or leave open to set low. CNTL3: Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9280A only).
12	GPIO1	Open-Drain, General-Purpose Input/Output with Internal 60k Ω Pullup to IOVDD
13	DVDD	3.3V Digital Power Supply. Bypass DVDD to EP with 0.1 μ F and 0.001 μ F capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
14	CNTL0/ADD0	Auxiliary Control Signal Output/Address Selection Input with Internal Pulldown to EP. Functions as ADD0 input at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to CNTL0 output automatically after power-up. ADD0: Bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1. Connect CNTL0/ADD0 to IOVDD with a 30k Ω resistor to set high or leave open to set low. CNTL0: Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9280A only).
15	RX/SDA	UART Receive/I ² C Serial-Data Input/Output with Internal 30k Ω Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I ² C Master/Slave.
16	TX/SCL	UART Transmit/I ² C Serial-Clock Input/Output with Internal 30k Ω Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I ² C Master/Slave.
17	$\overline{\text{PWDN}}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{\text{PWDN}}$ low to enter power-down mode to reduce power consumption.
18	ERR	Error Output. Open-drain data error detection and/or correction indication output with internal 30k Ω pullup to IOVDD. ERR is high when $\overline{\text{PWDN}}$ is low
19	LOCK	Open-Drain Lock Output with Internal 30k Ω Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when $\overline{\text{PWDN}}$ = low.

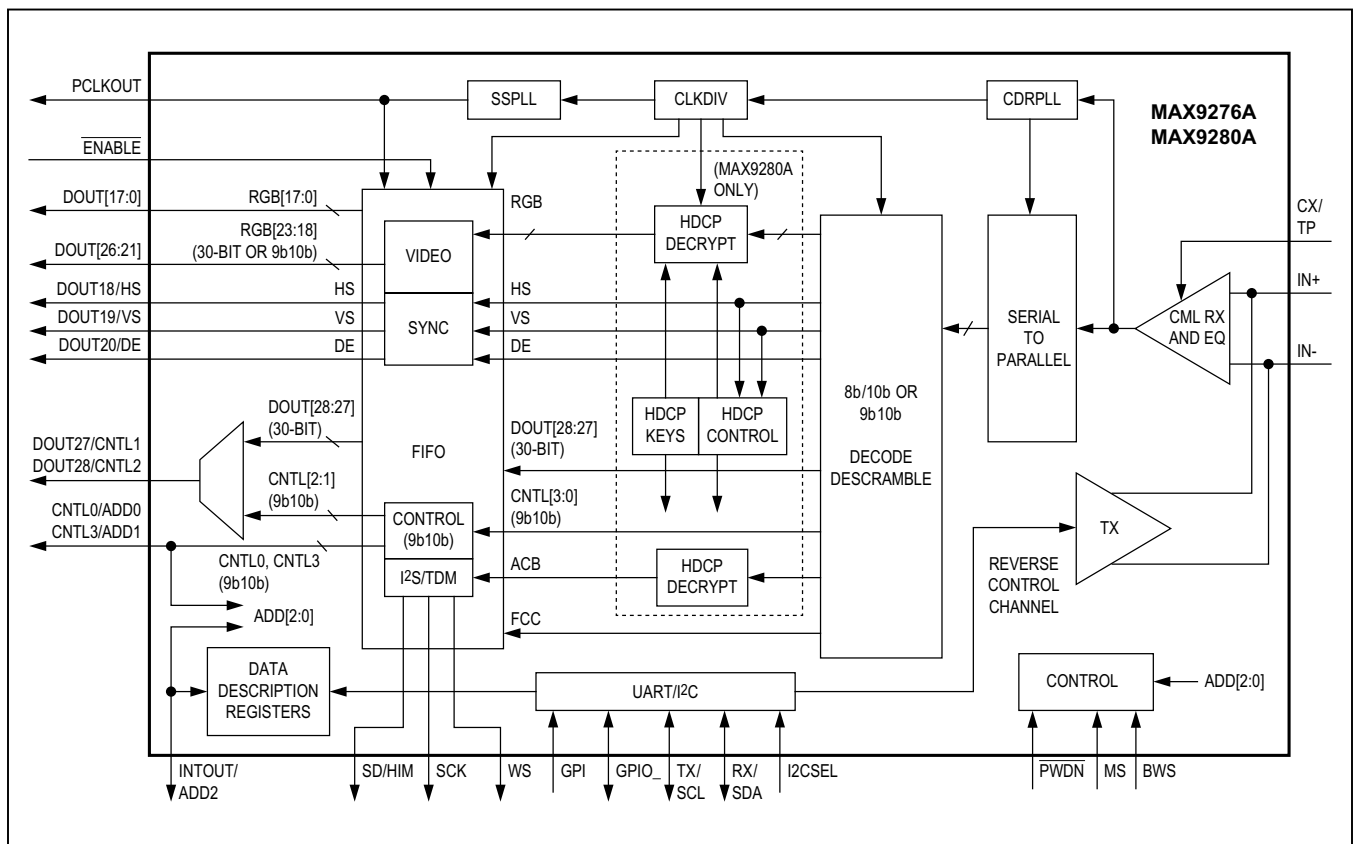
Pin Description (continued)

PIN	NAME	FUNCTION
20	WS	I ² S/TDM Word-Select Input/Output. Powers up as an I ² S output (deserializer-provided clock). Set AUDIOMODE bit = '1' to change WS to an input with internal pulldown to GND and supply WS externally (system provided clock).
21	SCK	I ² S/TDM Serial-Clock Input/Output. Powers up as an I ² S output (deserializer-provided clock). Set AUDIOMODE bit = '1' to change SCK to an input with internal pulldown to GND and supply WS externally (system provided clock).
22	SD/HIM	I ² S/TDM Serial-Data Output/High-Immunity Mode Input. Functions as HIM input with internal pulldown to EP at power-up or when resuming from power-down mode (P _W DN = low), and switches to SD output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode (P _W DN = low) and is active-high. Connect SD/HIM to IOVDD with a 30kΩ resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. SD: Disable I ² S/TDM encoding to serial data to use SD as an additional control/data output valid on the selected edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280A only).
23	DOUT28/CNTL2	Parallel Data/Auxiliary Control Signal Output Valid on the Selected Edge of PCLKOUT. DOUT28/CNTL2 remains high impedance in 24-bit mode (BWS = low) DOUT28 used only in 32-bit mode (BWS = high). DOUT28 not encrypted when HDCP is enabled (MAX9280A only). CNTL2 used only in high-bandwidth mode (BWS = open). CNTL2 not encrypted when HDCP is enabled (MAX9280A only).
24	DOUT27/CNTL1	Parallel Data/Auxiliary Control Signal Output Valid on the Selected Edge of PCLKOUT. DOUT27/CNTL1 remains high impedance in 24-bit mode (BWS = low) DOUT27 used only in 32-bit mode (BWS = high). DOUT27 not encrypted when HDCP is enabled (MAX9280A only). CNTL1 used only in high-bandwidth mode (BWS = open). CNTL1 not encrypted when HDCP is enabled (MAX9280A only)
25, 26, 28–31	DOUT[26:21]	Parallel Data Outputs Valid on the Selected Edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280A only). DOUT[26:21] used only in 32-bit and high-bandwidth modes (BWS = high or open). DOUT[26:21] remains high-impedance in 24-bit mode.
27, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1μF and 0.001μF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
32	DOUT20/DE	Parallel Data/Device Enable Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Device enable output when HDCP is enabled (MAX9280A only) or when in high-bandwidth mode (BWS = open).
33	DOUT19/VS	Parallel Data/Vertical Sync Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Vertical sync output when HDCP is enabled (MAX9280A only) or when in high-bandwidth mode (BWS = open).
34	DOUT18/HS	Parallel Data/Horizontal Sync Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Horizontal sync output when HDCP is enabled (MAX9280A only) or when in high-bandwidth mode (BWS = open).

Pin Description (continued)

PIN	NAME	FUNCTION
35, 36, 38-43, 45-54	DOUT[17:0]	Parallel Data Outputs Valid on the Selected Edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280A only)
37	PCLKOUT	Parallel Clock Output Used for DOUT[28:0]. Latches parallel data into the input of another device.
56	CX/TP	Three-Level Coax/Twisted Pair Select Input. See Table 10 for function.
—	EP	Exposed Pad. EP is internally connected to device ground. MUST connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



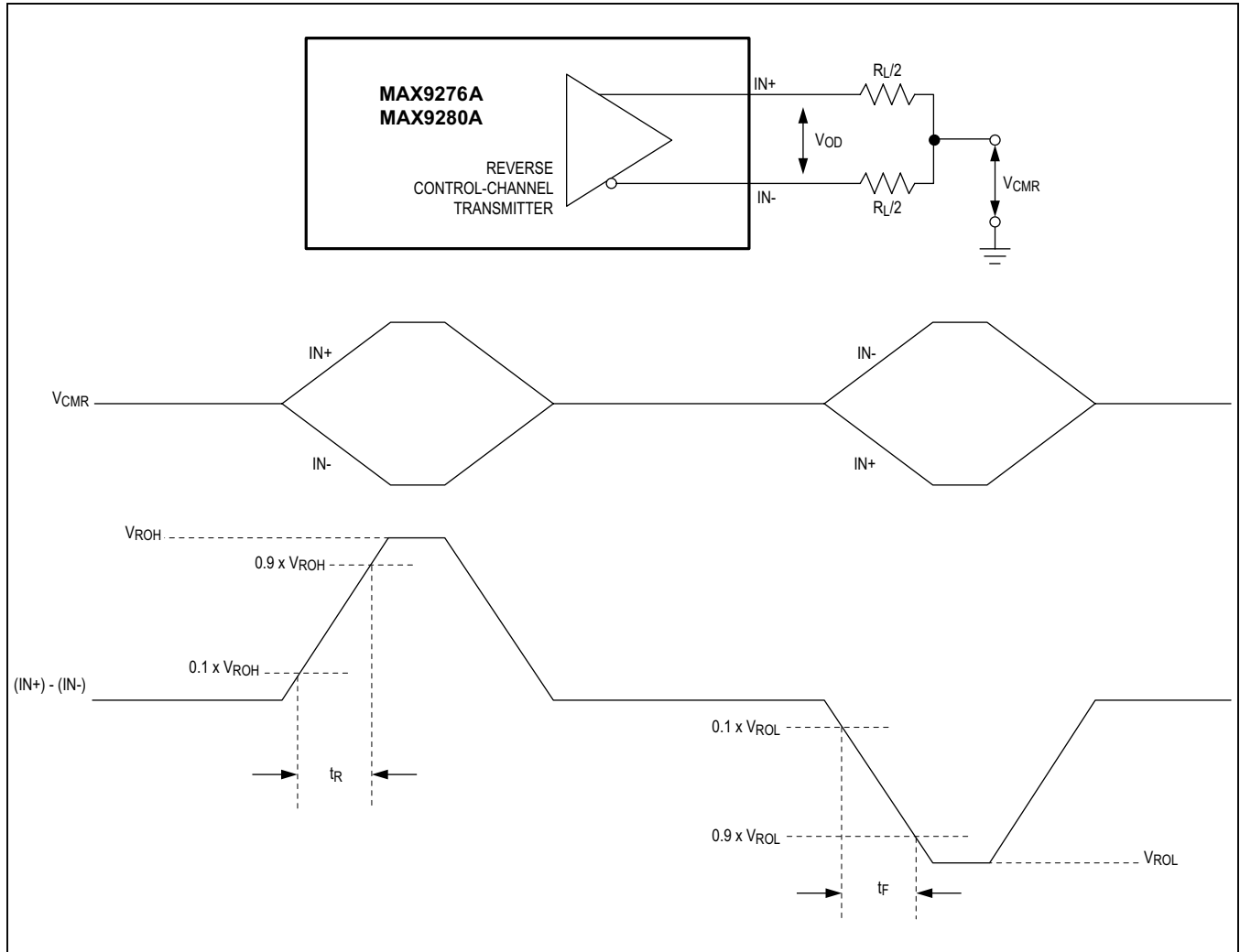


Figure 1. Reverse Control-Channel Output Parameters

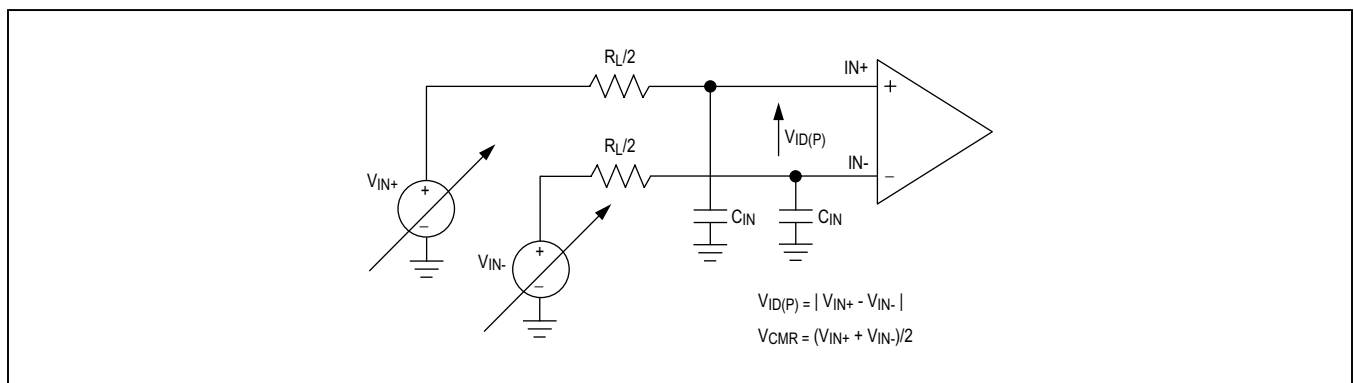


Figure 2. Test Circuit for Differential Input Measurement

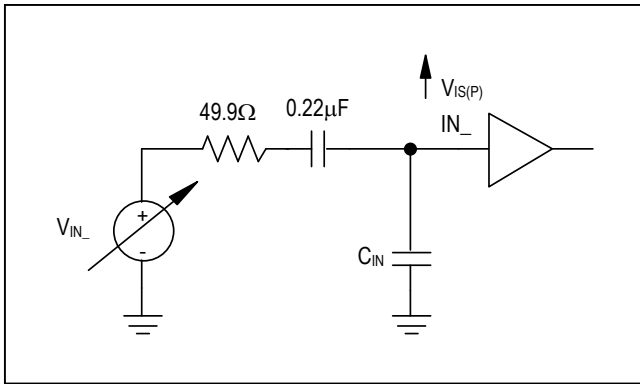


Figure 3. Test Circuit for Single-Ended Input Measurement

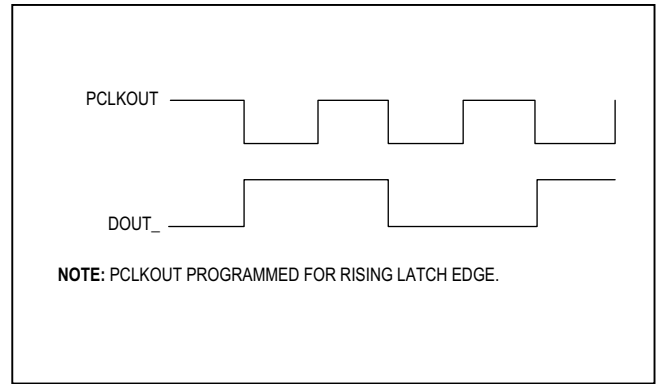


Figure 4. Worst-Case Pattern Output

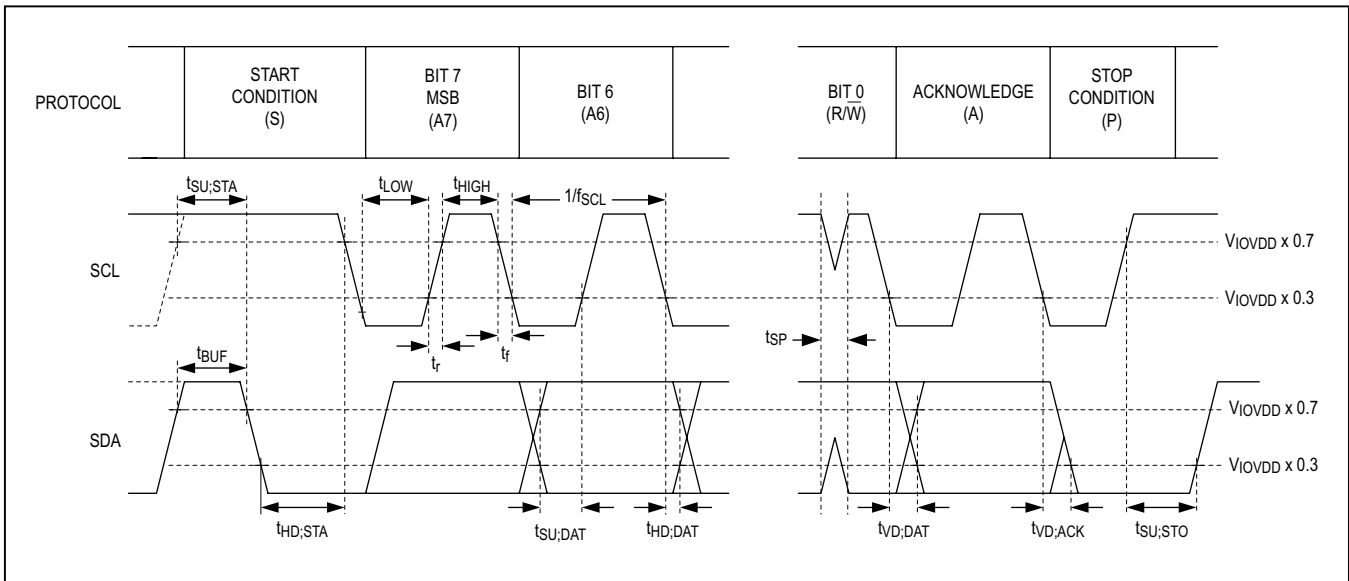


Figure 5. I²C Timing Parameters

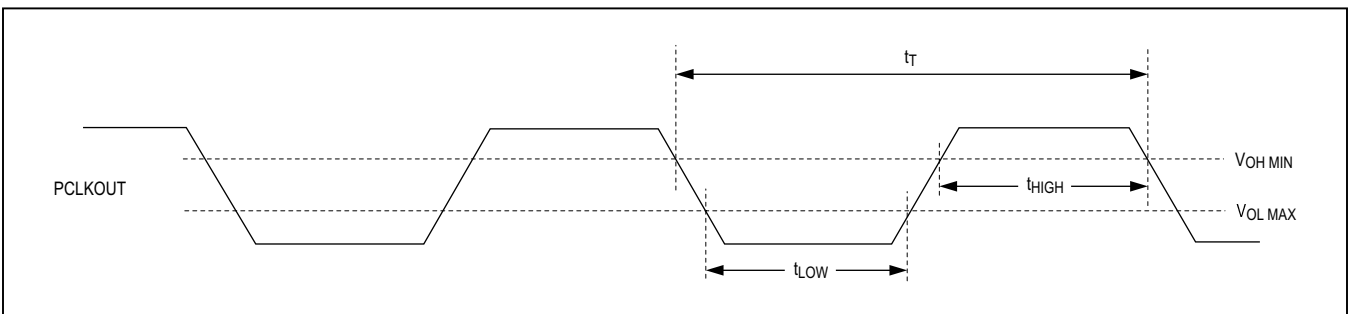


Figure 6. Parallel Clock Output Requirements

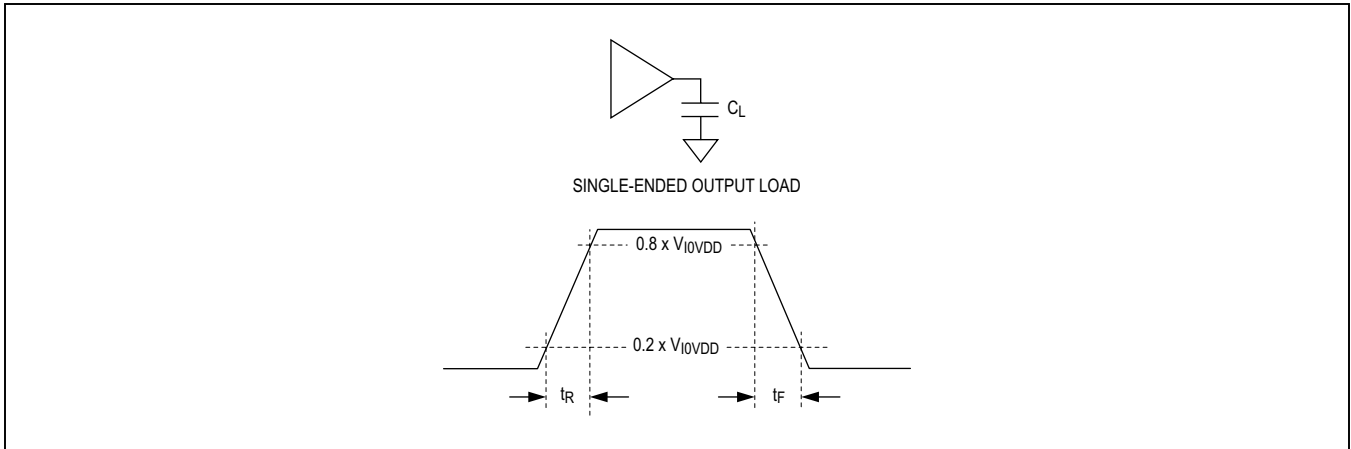


Figure 7. Output Rise-and-Fall Times

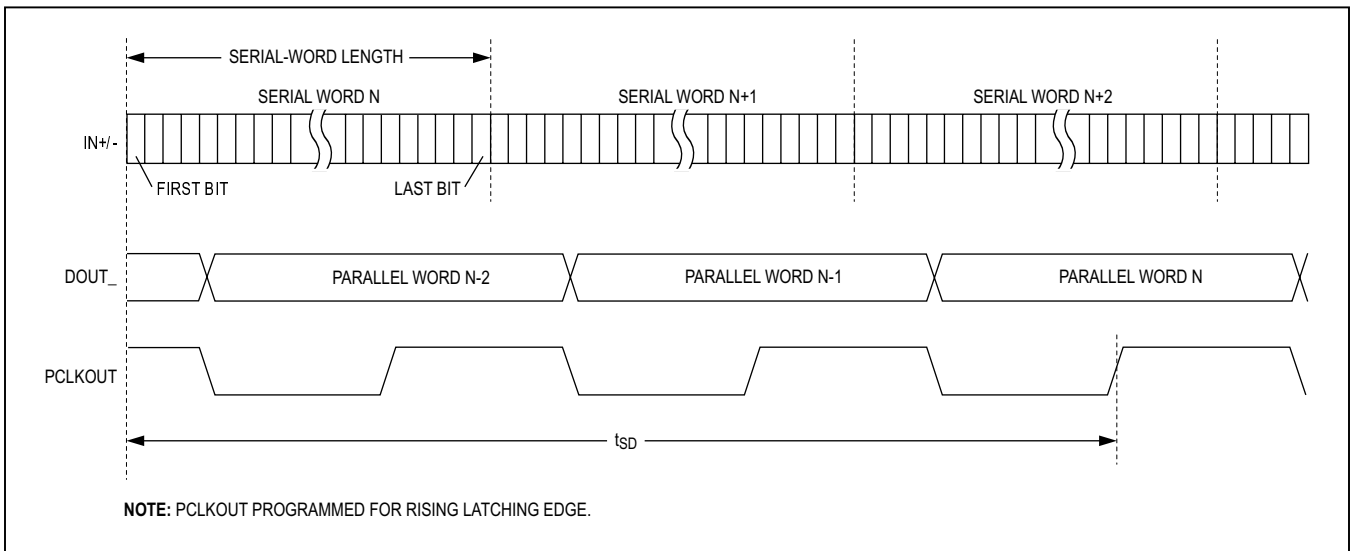


Figure 8. Deserializer Delay

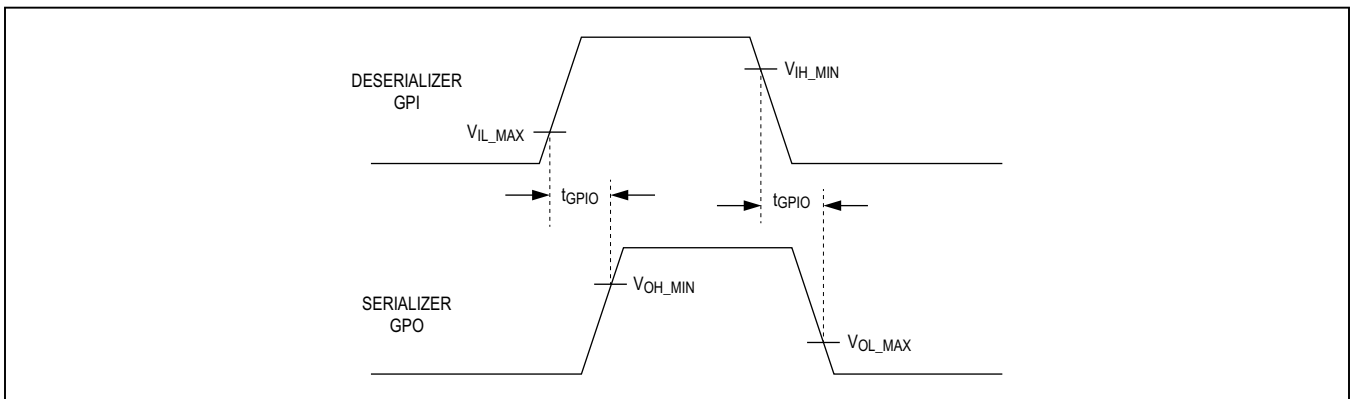


Figure 9. GPI-to-GPO Delay

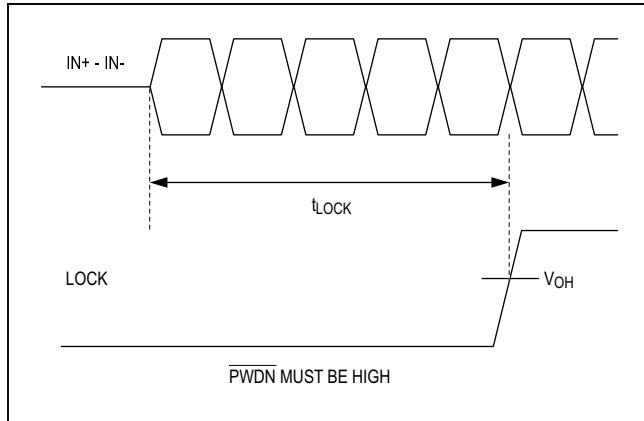


Figure 10. Lock Time

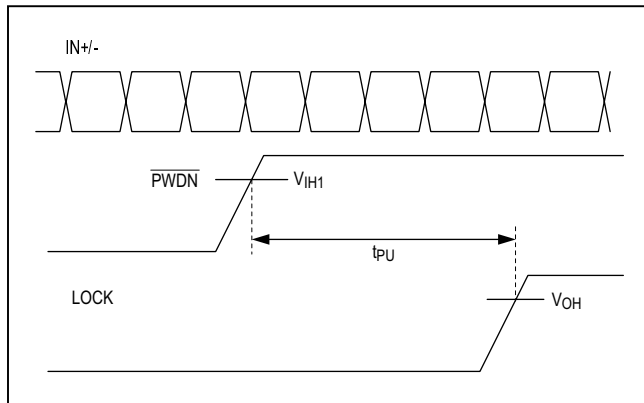


Figure 11. Power-Up Delay

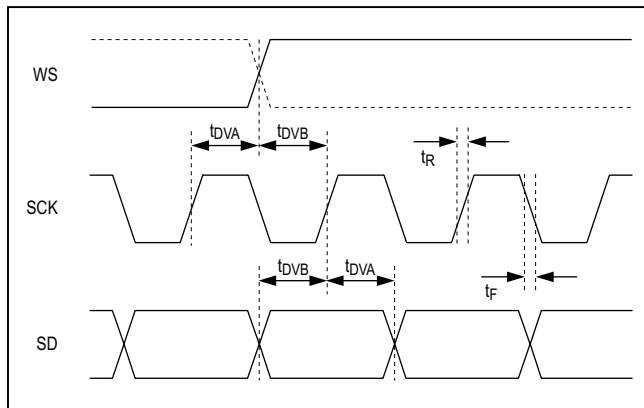


Figure 12. Output I²S Timing Parameters

Detailed Description

The MAX9276A/MAX9280A deserializers, when paired with the MAX9275/MAX9277/MAX9279/MAX9281 serializers, provides the full set of operating features, but is backward-compatible with the MAX9249–MAX9270 family of gigabit multimedia serial link (GMSL) devices, and have basic functionality when paired with any GMSL device. The MAX9280A has high-bandwidth digital content protection (HDCP) while the MAX9276A does not.

The deserializer has a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operates up to a maximum output clock of 104MHz in 24-bit mode and 27-bit high-bandwidth mode, or 78MHz in 32-bit mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Input equalization, combined with GMSL serializer pre/deemphasis, extends the cable length and enhances link reliability

The control channel enables a μ C to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9280A only). The μ C can be located at either end of the link, or when using two μ Cs, at both ends. Two modes of control-channel operation are available. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I²C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the parallel output. The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the deserializers and are programmed using the control channel in base mode. The MAX9276A/MAX9280A holds its own device address and the device address of the serializer it is paired with. Similarly, the serializer holds its own device address and the address of the MAX9276A/MAX9280A. Whenever a device address is changed be sure to write the new address to both devices. The default device address of the deserializer is set by the ADD[2:0] and CX/TP inputs (see Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses.

Table 1. Device Address Defaults (Register 0x00, 0x01)

PIN				DEVICE ADDRESS (bin)								SERIALIZER DEVICE ADDRESS (hex)	DESERIALIZER DEVICE ADDRESS (hex)
CX/TP**	ADD2	ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
High/Low	Low	Low	Low	1	0	0	X*	0	0	0	R/W	80	90
High/Low	Low	Low	High	1	0	0	X*	0	1	0	R/W	84	94
High/Low	Low	High	Low	1	0	0	X*	1	0	0	R/W	88	98
High/Low	Low	High	High	0	1	0	X*	0	1	0	R/W	44	54
High/Low	High	Low	Low	1	1	0	X*	0	0	0	R/W	C0	D0
High/Low	High	Low	High	1	1	0	X*	0	1	0	R/W	C4	D4
High/Low	High	High	Low	1	1	0	X*	1	0	0	R/W	C8	D8
High/Low	High	High	High	0	1	0	X*	1	0	0	R/W	48	58
Open	Low	Low	Low	1	0	0	X*	0	0	X*	R/W	80	92
Open	Low	Low	High	1	0	0	X*	0	1	X*	R/W	84	96
Open	Low	High	Low	1	0	0	X*	1	0	X*	R/W	88	9A
Open	Low	High	High	0	1	0	X*	0	1	X*	R/W	44	56
Open	High	Low	Low	1	1	0	X*	0	0	X*	R/W	C0	D2
Open	High	Low	High	1	1	0	X*	0	1	X*	R/W	C4	D6
Open	High	High	Low	1	1	0	X*	1	0	X*	R/W	C8	DA
Open	High	High	High	0	1	0	X*	1	0	X*	R/W	48	5A

*X = 0 for the serializer address, X = 1 for the deserializer address

**CX/TP determine the serial cable type CX/TP = open addresses only for coax mode.

Output Bit Map

The output bit width depends on settings of the bus width (BWS) pin. [Table 2](#) lists the bit map. Unused output bits are pulled low.

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded (9b/10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit mode, the first 21 bits contain video data. In 32-bit mode, the first 29 bits contain video data. In high-bandwidth mode, the first 24 bits contain video data, or special control signal packets. The last 3 bits contain the embedded audio channel, the embedded forward control channel, the parity bit of the serial word ([Figure 13](#), [Figure 14](#)).