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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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MAX9277/MAX9281

3.12Gbps GMSL Serializers for Coax or STP Output Drive and LVDS Input

General Description

The MAX9277/MAX9281 are 3.12Gbps Gigabit Multimedia Serial Link (GMSL) serializers with 3- or 4-data lane LVDS input (oLDI) and a CML serial output programmable for 50Ω coax or 100Ω shielded twisted pair (STP) cable drive. The MAX9281 has HDCP content protection but otherwise is the same as the MAX9277. The serializers pair with any GMSL deserializer capable of coax input. When programmed for STP output they are backward compatible with any GMSL deserializer. The output amplitude is programmable 100mV to 500mV single-ended (coax) or 100mV to 400mV differential (STP).

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-UART and UART-I²C modes, and up to 1Mbps in I²C-I²C mode. Using the control channel, a µC can program serializer, deserializer and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9281). A GPO output supports touch-screen controller interrupt requests from the remote end of the link.

For use with longer cables, the serializers have programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC61000-4-2 ESD standards. The core supply is 1.7 to 1.9V and the I/O supply is 1.7 to 3.6V. The package is a lead-free, 48-pin, 7mm x 7mm TQFN with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Ordering Information **appears at end of data sheet.**

Features and Benefits

- Ideal for High-Definition Video Applications
  - Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - 104MHz High-Bandwidth Mode Supports 1920x720p/60Hz Display With 24-Bit Color
  - Serializer Pre/Deemphasis Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate and 32-Bit Sample Depth For 7.1 Channel HD Audio
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 6.25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, mixed UART/I²C, or I²C Mode with Clock Stretch Capability
- Reduces EMI and Shielding Requirements
  - Serial Output Programmable for 100mV to 500mV Single-Ended or 100mV to 400mV Differential
  - Programmable Spread Spectrum Reduces EMI
  - Bypassable Input PLL for Pixel Clock Jitter Attenuation
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Generator for BER Testing of the Serial Link
  - Programmable Choice of 9 Default Device Addresses
  - Dedicated “Up/Down” GPO for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40ºC to +105ºC Operating Temperature
  - 8kV Contact and 15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

19-6764; Rev 2; 7/15

maxim integrated™

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Absolute Maximum Ratings

AVDD to AGND .....-0.5V to +1.9V
DVDD to AGND .....-0.5V to +1.9V
IOVDD to AGND.....-0.5V to +3.9V
LVDSVDD to AGND .....-0.5V to +3.9V
GND to AGND .....-0.5V to +0.5V
LMN_ to AGND (15mA current limit).....-0.5V to +3.9V
OUT+, OUT- to AGND.....-0.5V to +1.9V
All Other Pins to AGND.....-0.5V to (V_{IOVDD} + 0.5V)

OUT+, OUT- Short Circuit to Ground or Supply.....Continuous
Continuous Power Dissipation (T_A = +70ºC)
TQFN (derate 40mW/ºC above +70ºC) 3200mW
Junction Temperature.....+150ºC
Storage Temperature.....-65ºC to +150ºC
Lead Temperature (soldering, 10s) .....+300ºC
Soldering Temperature (reflow).....+260ºC

Note 1: AGND, GND connected to PCB ground.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 25°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (CX/TP, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, SD, SCK, WS, $\overline{AUTOS}$, CNTL1, CNTL2, HIM)							
High-Level Input Voltage	V_{IH1}	(CX/TP, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, $\overline{AUTOS}$, HIM)		0.65 x V_{IOVDD}			V
		SD, SCK, WS, CNTL1, CNTL2		0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+20	µA
THREE-LEVEL LOGIC INPUTS (CONF0, CONF1, ADD0, ADD1, BWS)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUT (GPO)							
High Level Output Voltage	V_{OH1}	I_{OUT} = -2mA		V_{IOVDD} - 0.2			V
Low Level Output Voltage	V_{OL1}	I_{OUT} = 2mA				0.2	V
OUTPUT Short-Circuit Current	I_{OS}	V_{OUT} = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN INPUT/OUTPUT (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL	-110		+5	µA
			LFLT	-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 9)				10	pF
DIFFERENTIAL SERIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Pre-emphasis off (Figure 1)		300	400	500	mV
		3.3dB preemphasis setting (Figure 2)		350		610	
		3.3dB deemphasis setting (Figure 2)		240		425	
Change in V_{OD} Between Complimentary Output States	ΔV_{OD}	Preemphasis off, deemphasis only				15	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} between Complimentary Output States	ΔV_{OS}					15	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_{OUT}	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
SINGLE-ENDED SERIAL OUTPUT (OUT+, OUT-)							
Single-Ended Output Voltage	V_{OUT}	Pre-emphasis off, high drive (Figure 3)		375	500	625	mV
		3.3dB preemphasis setting, high drive (Figure 2)		435		765	
		3.3dB deemphasis setting, high drive (Figure 2)		300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V				32	
Output Termination Resistance (Internal)	RO	From OUT+ or OUT- to V_{AVDD}		45	54	63	Ω

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REVERSE CONTROL CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}	Normal-immunity mode				27	mV
		High-immunity mode				40	
Low Switching Threshold	V_{CLR}	Normal-immunity mode		-27			mV
		High-immunity mode		-40			
LINE FAULT DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 4				0.3	V
Normal Threshold	V_{TN}	Figure 4		0.57		1.07	V
Open Threshold	V_{TO}	Figure 4		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	Figure 4		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 4		2.47			V
LVDS INPUTS (RXIN_, RXCLKIN_)							
Differential Input High Threshold	V_{TH}	V_{CM} = 1.2V				50	mV
Differential Input Low Threshold	V_{TL}	V_{CM} = 1.2V		-50			mV
Input Differential Termination Resistance	R_{TERM}			85	110	135	Ω
Input Current	I_{IN+}, I_{IN-}	$\overline{PWDN}$ = high or low, IN+ and IN- are shorted		-25		+25	µA
Power-Off Input Current	I_{IN0+}, I_{IN0-}	V_{AVDD} = V_{DVDD} = V_{IOVDD} = 0V		-40		+40	µA
POWER SUPPLY							
Total Supply Current (AVDD + DVDD + IOVDD) (Note 6) (Worst-Case Pattern, Figure 5)	I_{WCS}	BWS = low	$f_{PCLKIN\_}$ = 16.6MHz		100	125	mA
			$f_{PCLKIN\_}$ = 33.3MHz		106	140	
			$f_{PCLKIN\_}$ = 66.6MHz		123	155	
			$f_{PCLKIN\_}$ = 104MHz		146	190	
		BWS = mid	$f_{PCLKIN\_}$ = 36.6MHz		108	145	
			$f_{PCLKIN\_}$ = 104MHz		152	195	
LVDSVDD Worst-Case Supply Current (Figure 5, Note 6)	I_{WCS}	BWS = low	$f_{PCLKIN\_}$ = 16.6MHz		24	30	mA
			$f_{PCLKIN\_}$ = 33.3MHz		24	30	
			$f_{PCLKIN\_}$ = 66.6MHz		24	30	
			$f_{PCLKIN\_}$ = 104MHz		24	30	
		BWS = mid	$f_{PCLKIN\_}$ = 36.6MHz		29	35	
			$f_{PCLKIN\_}$ = 104MHz		29	35	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sleep Mode Supply Current	I_{CCS}	Single wake-up receiver enabled, LVDS inputs not driven			42	170	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			6	120	µA
ESD PROTECTION							
OUT+, OUT- (Note 6)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±10		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±10		
			Air discharge		±25		
RXIN_, RXCLKIN_ (Note 7)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±6		
			Air discharge		±20		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±8		
			Air discharge		±30		
All Other Pins (Note 8)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF			±4		kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUT (RXCLKIN)						
Clock Frequency	$f_{RXCLKIN\_}$	BWS = low, DRS = ‘1’	8.33		16.66	MHz
		BWS = low, DRS = ‘0’	16.66		104	
		BWS = mid, DRS = ‘1’	18.33		36.66	
		BWS = mid, DRS = ‘0’	36.66		104	
		BWS = high, DRS = ‘1’	6.25		12.5	
		BWS = high, DRS = ‘0’	12.5		78	
I²C/UART PORT TIMING						
I²C/UART Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
I²C TIMING (Figure 6)								
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)			9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)			> 100		400	kHz
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)			> 400		1000	kHz
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High	V_{IOVDD} = 1.7V to < 3V (Note 9)	0.6			
				V_{IOVDD} = 3.0V to 3.6V	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7			µs
			Mid		0.6			
			High		0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low		0			µs
			Mid		0			
			High		0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low		250			µs
			Mid		100			
			High		50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High		0.5			

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 10)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 11)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low				50	ns
			Mid				50	
			High				50	
Capacitive Load Each Bus Line	C_B	Note 12					100	pF
SWITCHING CHARACTERISTICS (Note 12)								
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps				90	150	ps
Total Serial Output Jitter (Differential Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, pre-emphasis disabled, Figure 7				0.21		UI
Deterministic Serial Output Jitter (Differential Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, pre-emphasis disabled, Figure 7				0.09		UI
Total Serial Output Jitter (Single-Ended Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_O/2, pre-emphasis disabled, Figure 3				0.19		UI
Deterministic Serial Output Jitter (Single-Ended Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_O/2, Pre-emphasis disabled, Figure 3				10		UI
CNTL_ Input Setup Time	t_{SET}	Figure 8			3			ns
CNTL_ Input Hold Time	t_{HOLD}	Figure 8			1.5			ns
RXIN_ Skew Margin	t_{RSKM}	No RXCLKIN spread, Figure 9			0.3			UI

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, $V_{LVDSVDD}$ = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), T_A = -40°C to +105°C, unless otherwise noted. Differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input common-mode voltage V_{CM} = $|V_{ID}/2|$ to 2.4V - $|V_{ID}/2|$. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GPI to GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO, Figure 10				350	µs
Serializer Delay (Note 13)	t_{SD}	Figure 11	Spread-spectrum enabled			5440	Bits
			Spread-spectrum disabled			1920	
Link Start Time	t_{LOCK}	Figure 12				3.5	ms
Power-Up Time	t_{PU}	Figure 13				8	ms
I²S/TDM INPUT TIMING							
WS Frequency	f_{WS}	See Table 5		8		192	kHz
Sample Word Length	n_{WS}	See Table 5		8		32	Bits
SCK Frequency	f_{SCK}	f_{SCK} = f_{WS} x n_{WS} x (2 or 8)		(8 x 2) x 2		(192 x 32) x 8	kHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, t_{SCK} = $1/f_{SCK}$ (Note 13)		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, t_{SCK} = $1/f_{SCK}$ (Note 13)		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	Figure 14 (Note 13)		2			ns
SD, WS Hold Time	t_{HOLD}	Figure 14 (Note 13)		2			ns

Note 3: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 6: HDCP not enabled (MAX9281 only). See Table 23 for additional supply current when HDCP is enabled.

Note 7: Specified pin to ground.

Note 8: Specified pin to all supply/ground.

Note 9: The I²C bus standard t_{LOW} min = 0.5µs.

Note 10: The I²C bus standard $t_{VD:DAT}$ max = 0.45µs.

Note 11: The I²C bus standard $t_{VD:ACK}$ max = 0.45µs.

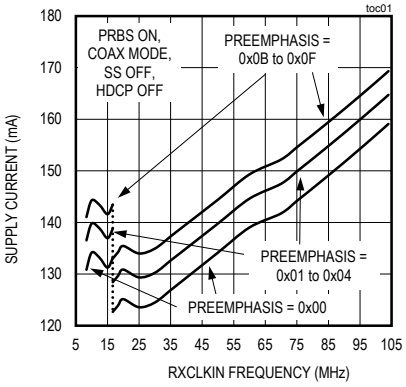
Note 12: Not production tested. Guaranteed by design.

Note 13: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = '0' or open. Bit time = 1/(40 x f_{PCLKIN}) for BWS = '1'.

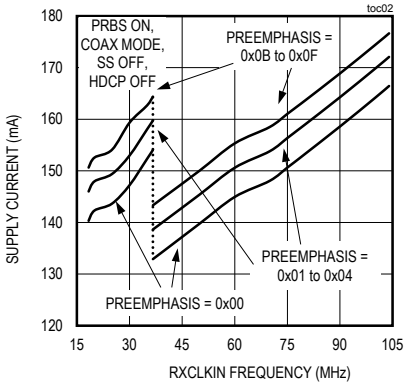
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

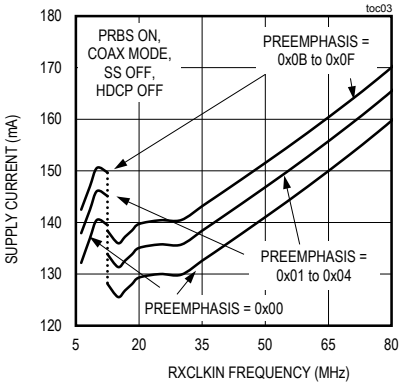
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = LOW)



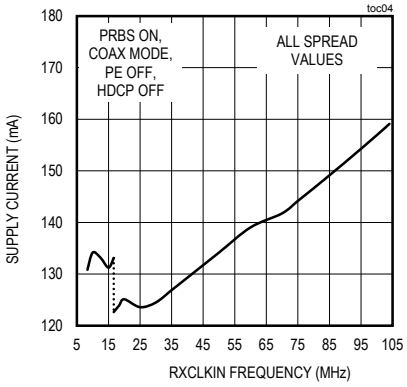
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = OPEN)



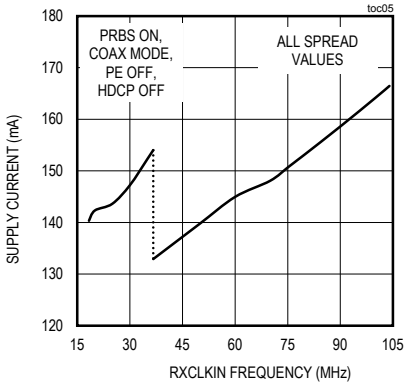
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = HIGH)



SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = LOW)



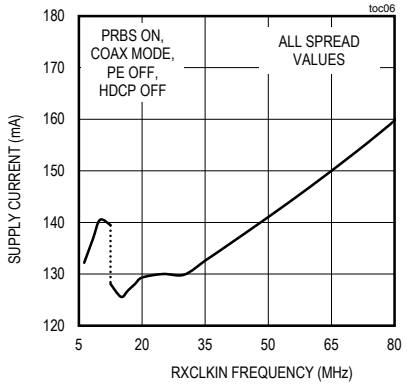
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = OPEN)



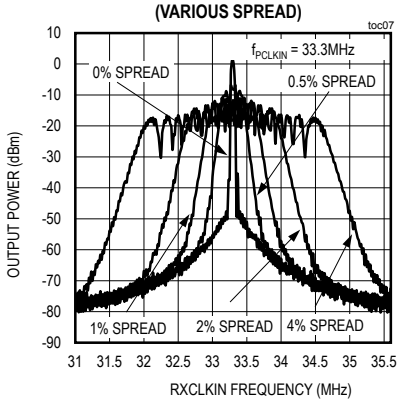
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, $V_{LVDSVDD}$ = 3.3V, T_A = +25°C, unless otherwise noted.)

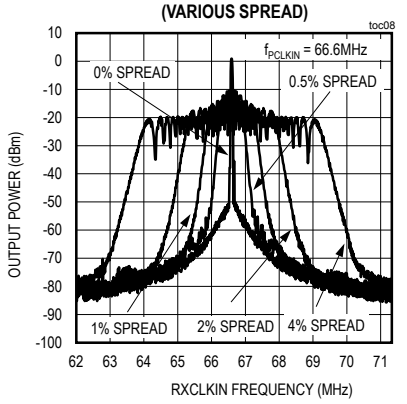
SUPPLY CURRENT vs. RXCLKIN FREQUENCY (BWS = HIGH)



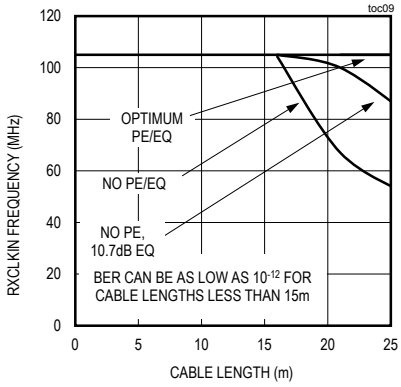
OUTPUT SPECTURM vs. RXCLKIN FREQUENCY (VARIOUS SPREAD)



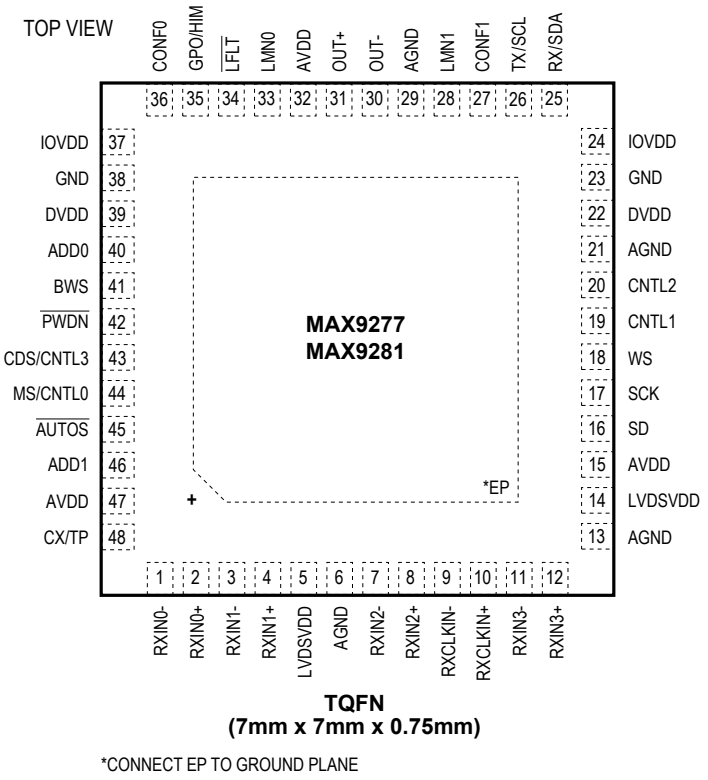
OUTPUT SPECTURM vs. RXCLKIN FREQUENCY (VARIOUS SPREAD)



MAXIMUM RXCLKIN FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



TQFN
(7mm x 7mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

Pin Description

PIN	NAME	FUNCTION
1–4, 7, 8, 11, 12	RXIN_-, RXIN_+	LVDS Data Inputs. Set BWS = low to use RXIN0_ to RXIN2_ (3-channel mode). Set BWS = high or open to use RXIN0_ to RXIN3_ (4-channel or high-bandwidth mode). Certain data bits encrypted when HDCP is enabled (MAX9281 only, Table 3)
5, 14	LVDSVDD	3.3V LVDS Power Supply. Bypass LVDSVDD to AGND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to LVDSVDD.
6, 13, 21, 29	AGND	Analog and LVDS Ground
9, 10	RXLKIN-, RXCLKIN+	LVDS Clock Input. Provides the PLL reference clock.
15, 32, 47	AVDD	1.8V Analog Power Supply. Bypass AGND to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
16	SD	I2S/TDM Serial-Data Input with Internal Pulldown to GND. Disable I2S/TDM encoding to use SD as an additional control/data input latched on the selected edge of PCLKIN. Encrypted when HDCP is enabled.
17	SCK	I2S/TDM Serial-Clock Input with Internal Pulldown to GND

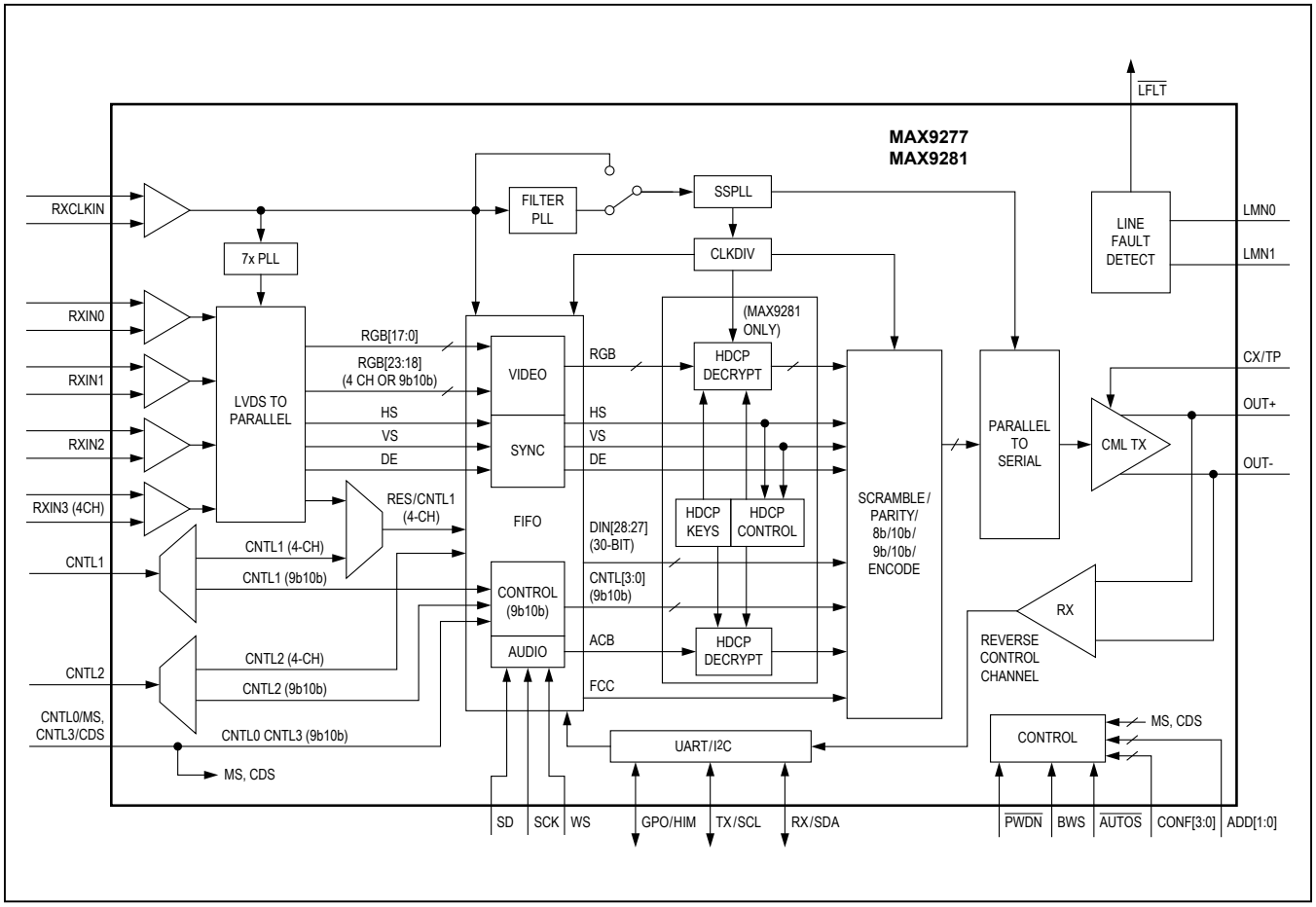
Pin Description (continued)

PIN	NAME	FUNCTION
18	WS	I2S/TDM Word-Select Input with Internal Pulldown to GND
19	CNTL1	Control Input With Internal Pulldown to GND. Input data is latched every RXCLKIN_ cycle (Figure 15). CNTL1 is not available in 3-channel mode (BWS = low). Set BWS = high or open (4-channel or high-bandwidth mode) to use this input. CNTL1 not encrypted when HDCP is on (MAX9281 only) CNTL1 or RES ("Reserved" from VESA Standard Panel Specification) is mapped to internal bit DIN27. See the *Reserved Bit (RES)/CNTL1* section.
20	CNTL2	Control Input With Internal Pulldown to GND. Input data is latched every RXCLKIN_ cycle (Figure 15). CNTL2 is not available in 3-channel mode (BWS = low). Set BWS = high or open (4-channel or high-bandwidth mode) to use this input. CNTL2 not encrypted when HDCP is on (MAX9281 only). CNTL2 is mapped to internal bit DIN28.
22, 39	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
23, 38	GND	Digital and I/O Ground
24, 37	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O Power Supply. Bypass IOVDD to GND with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD. IOVDD sets the voltage levels for all pins except for the LVDS inputs and OUT+/-
25	RX/SDA	UART Receive/I2C Serial Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 11). RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I2C Master/Slave.
26	TX/SCL	UART Transmit/I2C Serial Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 11). TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I2C Master/Slave.
27	CONF1	Three-Level Configuration Input. The state of CONF1 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 11 for details.
28	LMN1	Line-Fault Monitor Input 1 (see Figure 4 for details).
30	OUT-	Inverting CML Coax/Twisted-Pair Serial Output
31	OUT+	Noninverting CML Coax/Twisted-Pair Serial Output
33	LMN0	Line-Fault Monitor Input 0 (see Figure 4 for details).
34	$\overline{LFLT}$	Active-Low Open-Drain Line-Fault Output. $\overline{LFLT}$ has a 60kΩ internal pullup to IOVDD. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is output high when $\overline{PWDN}$ = low.
35	GPO/HIM	General-Purpose Output/High Immunity Mode Input. Functions as HIM input with internal pulldown to GND at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to GPO output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low) and is active-high. Connect HIM to IOVDD with a 30kΩ resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO: Output follows the state of the GPI (or INT) input on the deserializer. GPO is low after power-up or when $\overline{PWDN}$ is low.

Pin Description (continued)

PIN	NAME	FUNCTION
36	CONF0	Three-Level Configuration Input. The state of CONF0 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 11 for details.
40	ADD0	Three-Level Address Selection Input. The state of ADD0 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 2 for details.
41	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low for 3-channel mode. Set BWS = high for 4-channel mode. Set BWS = open for high-bandwidth mode.
42	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
43	CDS/CNTL3	Control Direction Selection/Auxiliary Control Signal Input with Internal Pulldown to GND. Function is determined by the CDSCNTL3 register bit and defaults to CDS on power-up. CDS (CDSCNTL3 = 0): Control link direction selection input with internal pulldown to GND. Set CDS = low when the control channel master µC is connected at the serializer. Set CDS = high when the control channel master µC is connected at the deserializer. CNTL3 (CDSCNTL3 = 1): Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9281 only).
44	MS/CNTL0	Mode Select/Auxiliary Control Signal Input with Internal Pulldown to GND. Function is determined by the MSCNTL0 register bit and defaults to MS on power-up. MS (MSCNTL0 = 0): Set MS = low, to select base mode. Set MS = high to select the bypass mode. CNTL0 (MSCNTL0 = 1): Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9281 only).
45	$\overline{AUTOS}$	Active-Low Auto-Start Input With Internal Pulldown to GND. Set $\overline{AUTOS}$ = high, to disable serialization at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set $\overline{AUTOS}$ = low, to enable serialization and automatic PLL range selection power-up or when resuming from power-down mode.
46	ADD1	Three-Level Address Selection Input. The state of ADD1 latches at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 2 for details.
48	CX/TP	Coax/Twisted Pair Input With Internal Pulldown to GND. Set CX/TP low for twisted-pair cable drive (differential output). Set CX/TP high for coax cable drive (single-ended output).
—	EP	Exposed Pad. EP is internally connected to AGND. MUST connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



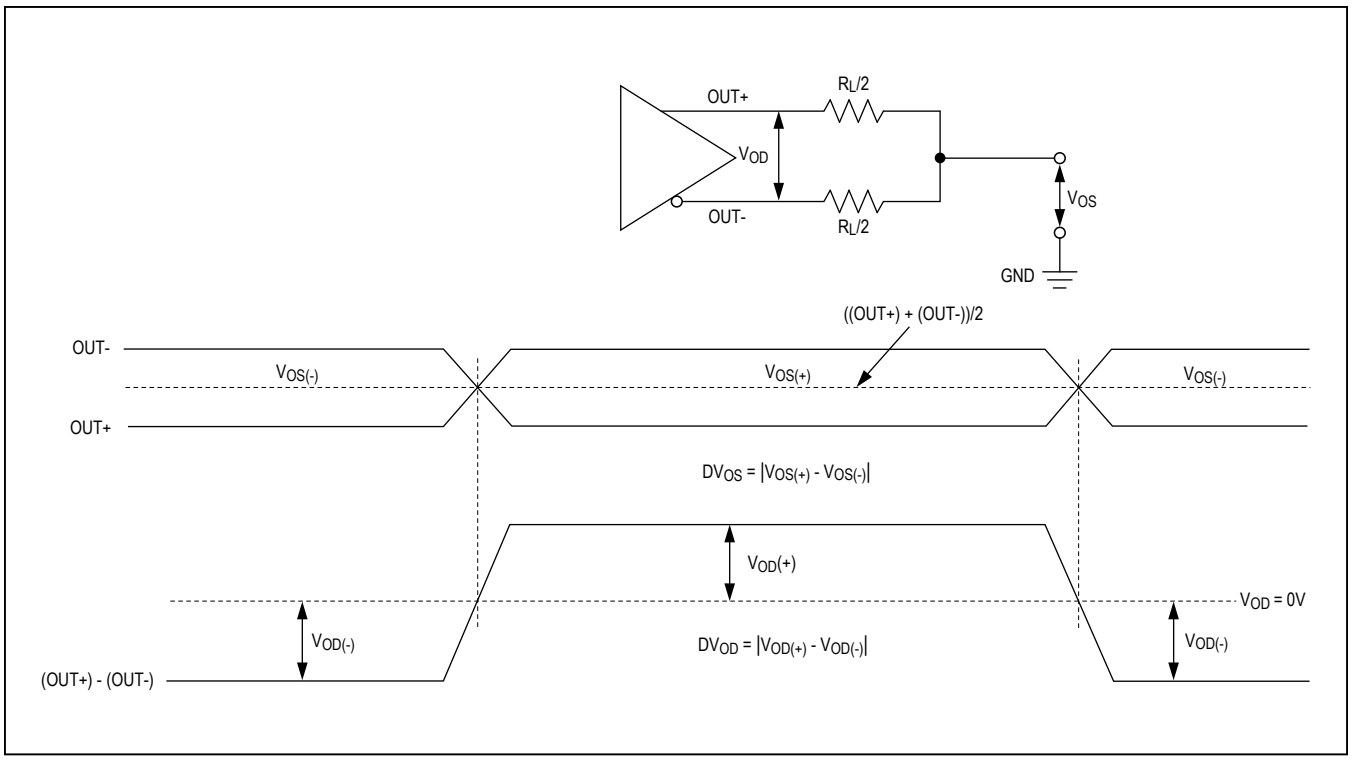


Figure 1. Serial-Output Parameters

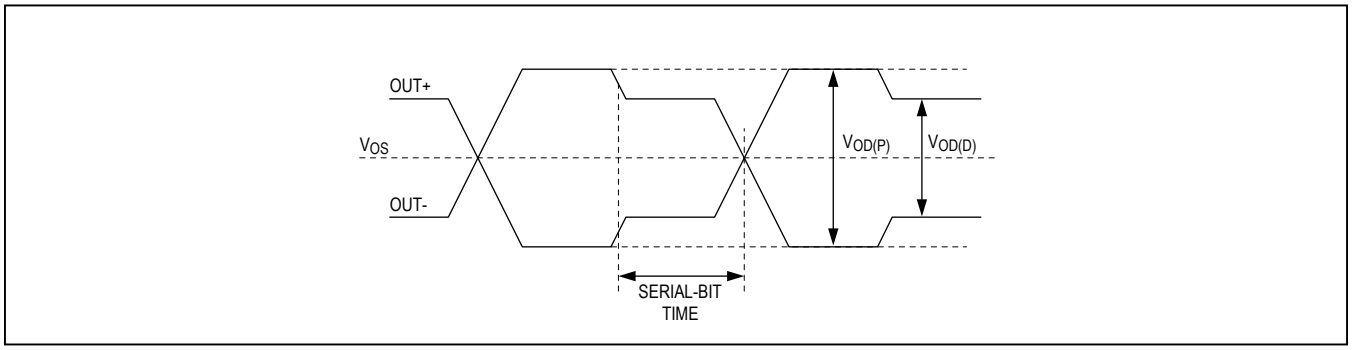


Figure 2. Output Waveforms at OUT+, OUT-

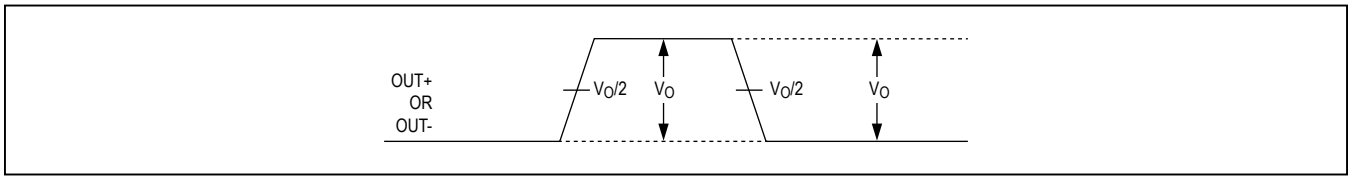


Figure 3. Single-Ended Output Template

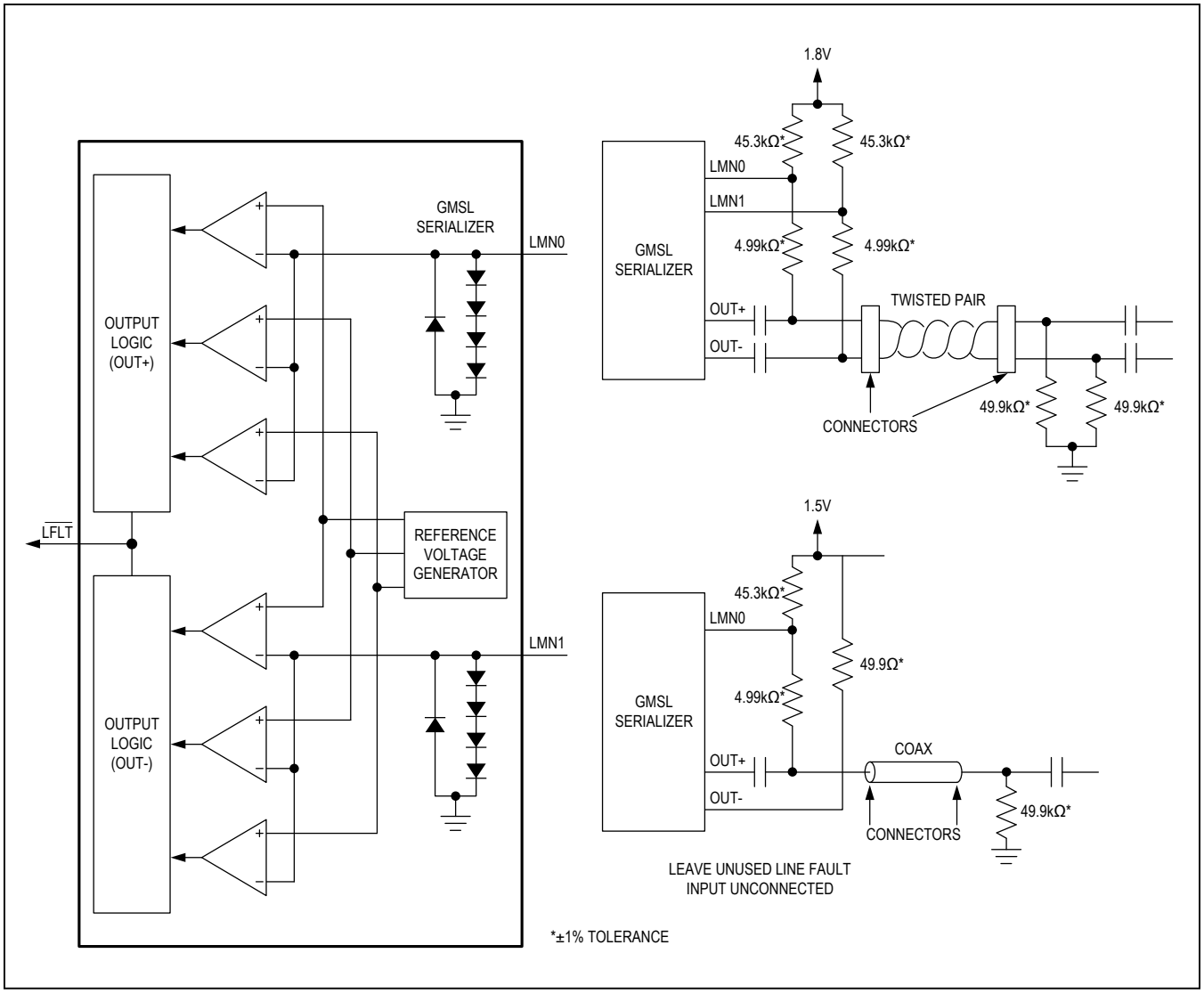


Figure 4. Line Fault Detector Circuit

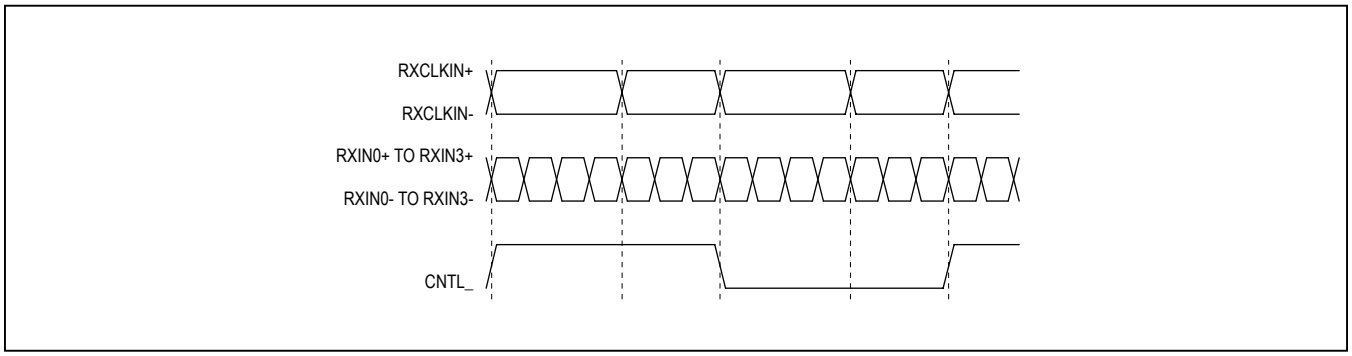


Figure 5. Worst-Case Pattern Input

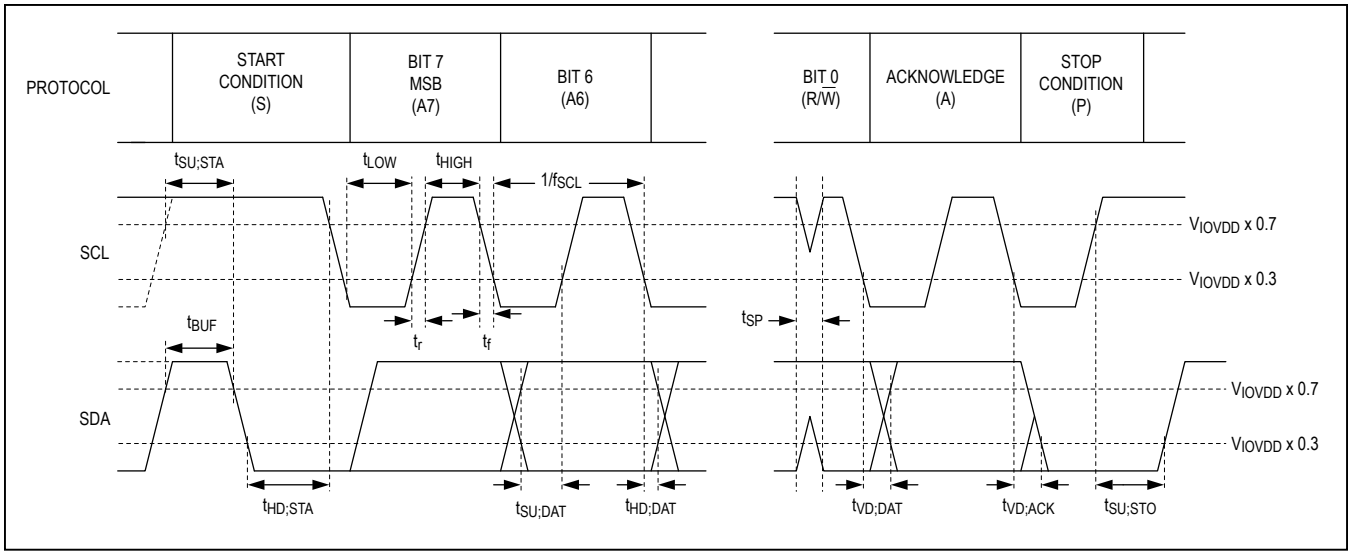


Figure 6. I²C Timing Parameters

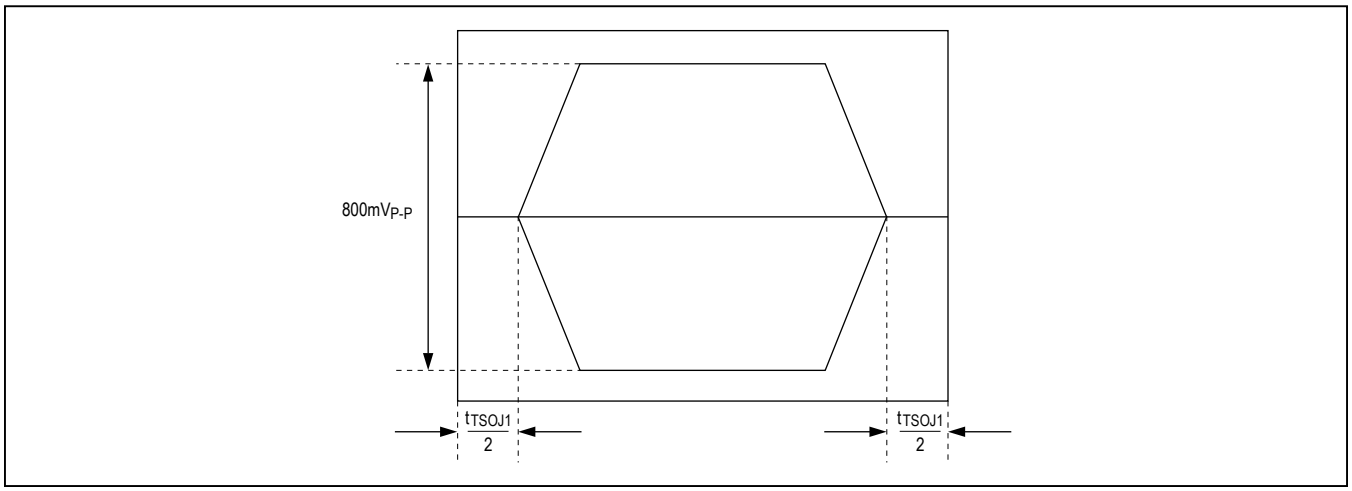


Figure 7. Differential Output Template

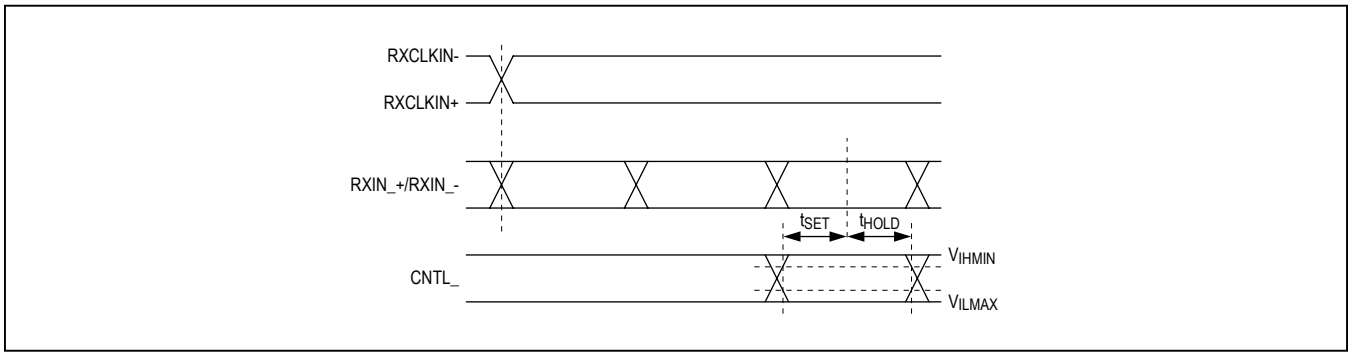


Figure 8. Input Setup and Hold Times

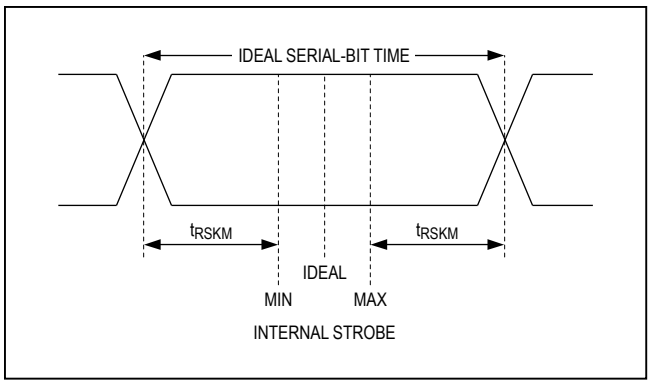


Figure 9. LVDS Receiver Input Skew Margin

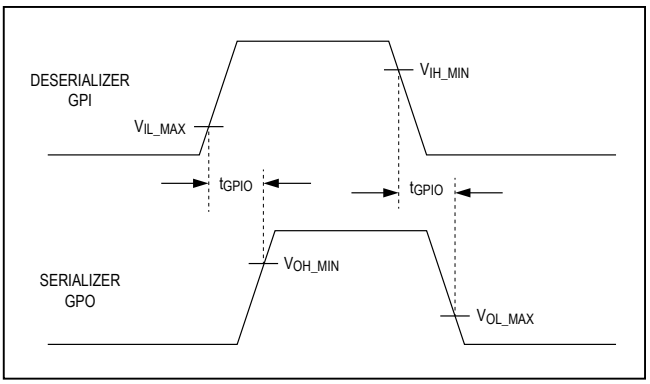


Figure 10. GPI-to-GPO Delay

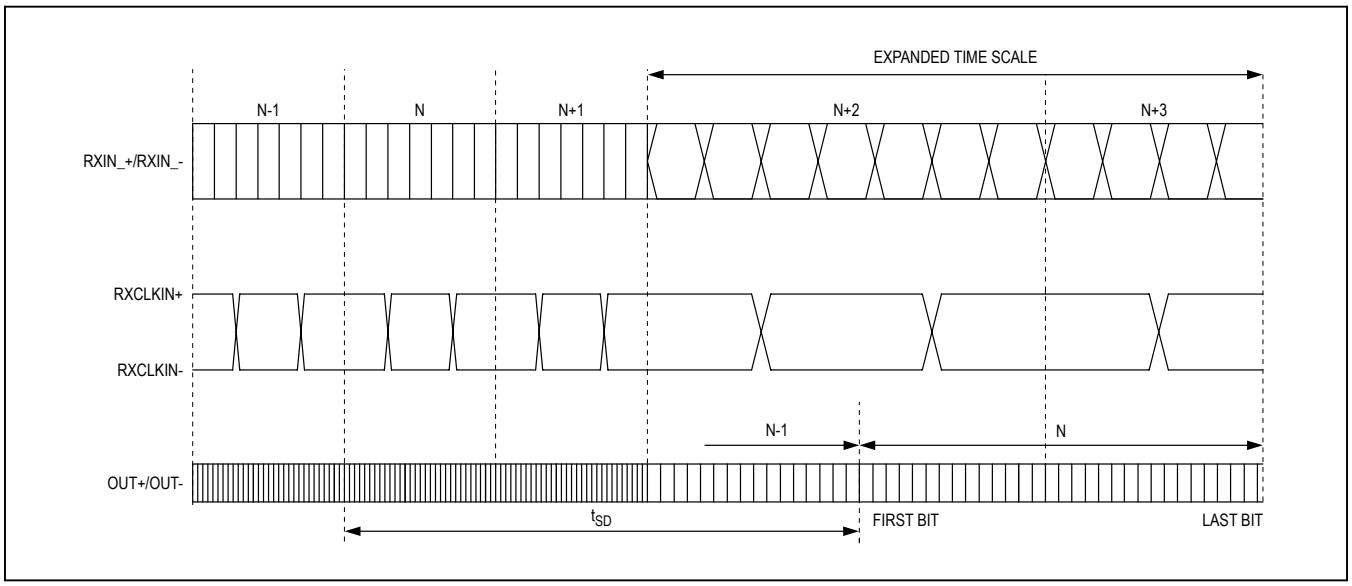


Figure 11. Serializer Delay

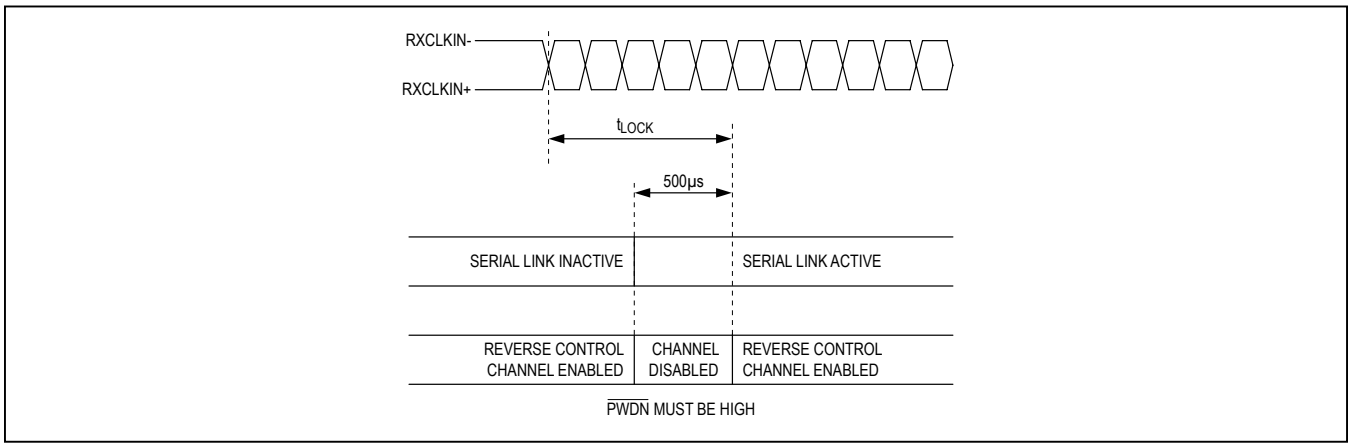


Figure 12. Link Startup Time

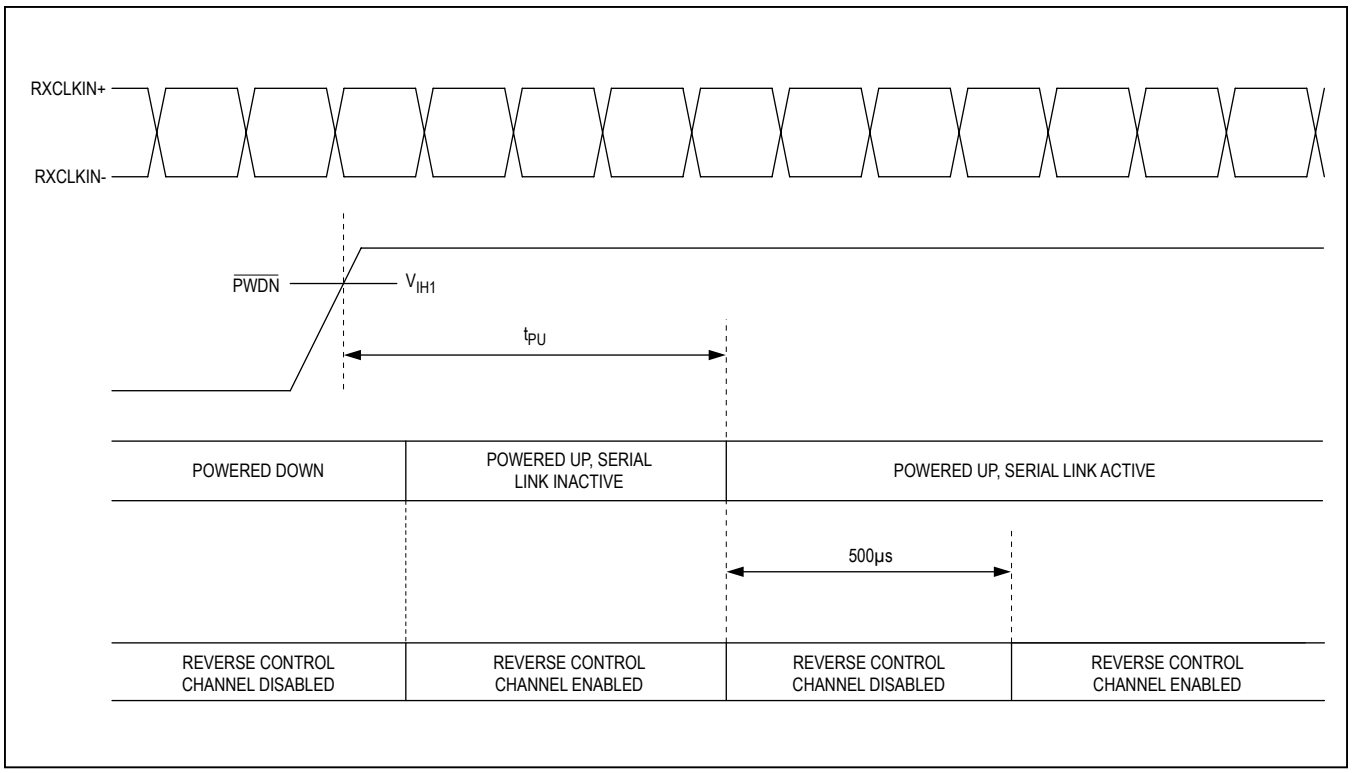


Figure 13. Power-Up Delay

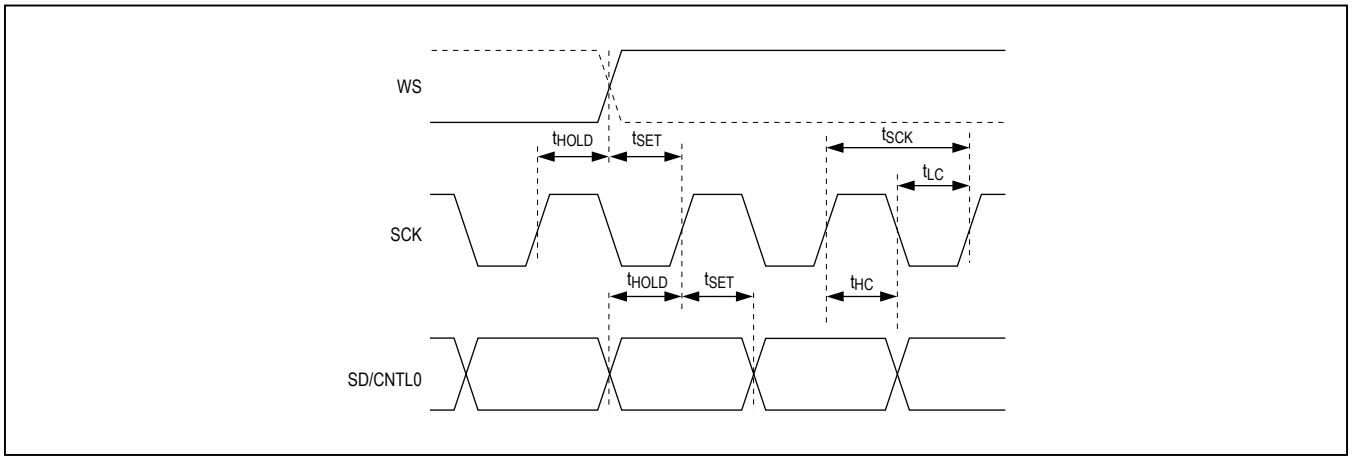


Figure 14. Input I²S Timing Parameters