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MAX9278A/MAX9282A

3.12Gbps GMSL Deserializers for Coax or STP Input and LVDS Output

General Description

The MAX9278A/MAX9282A gigabit multimedia serial link (GMSL) deserializers receive data from a GMSL serializer over 50Ω coax or 100Ω shielded twisted-pair (STP) cable and output deserialized data on 3 of 4 data-lane LVDS outputs (oLDI).

The MAX9282A has HDCP content protection but otherwise is the same as the MAX9278A. The deserializers pair with any GMSL serializer capable of coax output. When programmed for STP input, they are backward compatible with any GMSL serializer.

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-to-UART and UART-to-I²C modes, and up to 1Mbps in I²C-to-I²C mode. Using the control channel, a μC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9282A). Two GPIO ports are included, allowing display power-up and switching of the backlight among other uses. A continuously sampled GPI input supports touch-screen controller interrupt requests in display applications.

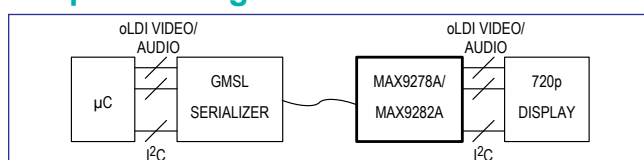
For use with longer cables, the deserializers have a programmable cable equalizer. Programmable spread spectrum is available on the LVDS output. The serial input and LVDS output meet ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 3.0V to 3.6V and the I/O supply is 1.7V to 3.6V.

The devices are in lead-free, 48-pin, 7mm x 7mm TQFN and QFND packages with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Simplified Diagram



Benefits and Features

- Ideal for High-Definition Video Applications
 - 104MHz High-Bandwidth Mode Supports 1920 x 720p/60Hz Display with 24-Bit Color
 - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
 - Equalization Allows 15m Cable at Full Speed
 - Up to 192kHz Sample Rate and 32-Bit Sample Depth for 7.1 Channel HD Audio
 - Audio Clock from Audio Source or Audio Sink
 - Color Lookup Table for Gamma Correction
 - CNTL[3:0] Control Outputs
- Multiple Data Rates for System Flexibility
 - Up to 3.12Gbps Serial-Bit Rate
 - 6.25MHz to 104MHz Pixel Clock
 - 9.6kbps to 1Mbps Control Channel in UART, UART-to-UART, UART-to-I²C, or I²C-to-I²C Modes with Clock-Stretch Capability
- Reduces EMI and Shielding Requirements
 - Programmable Spread Spectrum Reduces EMI
 - Tracks Spread Spectrum on Input
 - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
 - Built-In PRBS Tester for BER Testing of the Serial Link
 - Programmable Choice of Nine Default Device Addresses
 - Two Dedicated GPIO Ports
 - Dedicated “Up/Down” GPI for Touch-Screen Interrupt and Other Uses
 - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
 - -40°C to +105°C Operating Temperature
 - ±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

Ordering Information appears at end of data sheet.

Functional Diagram

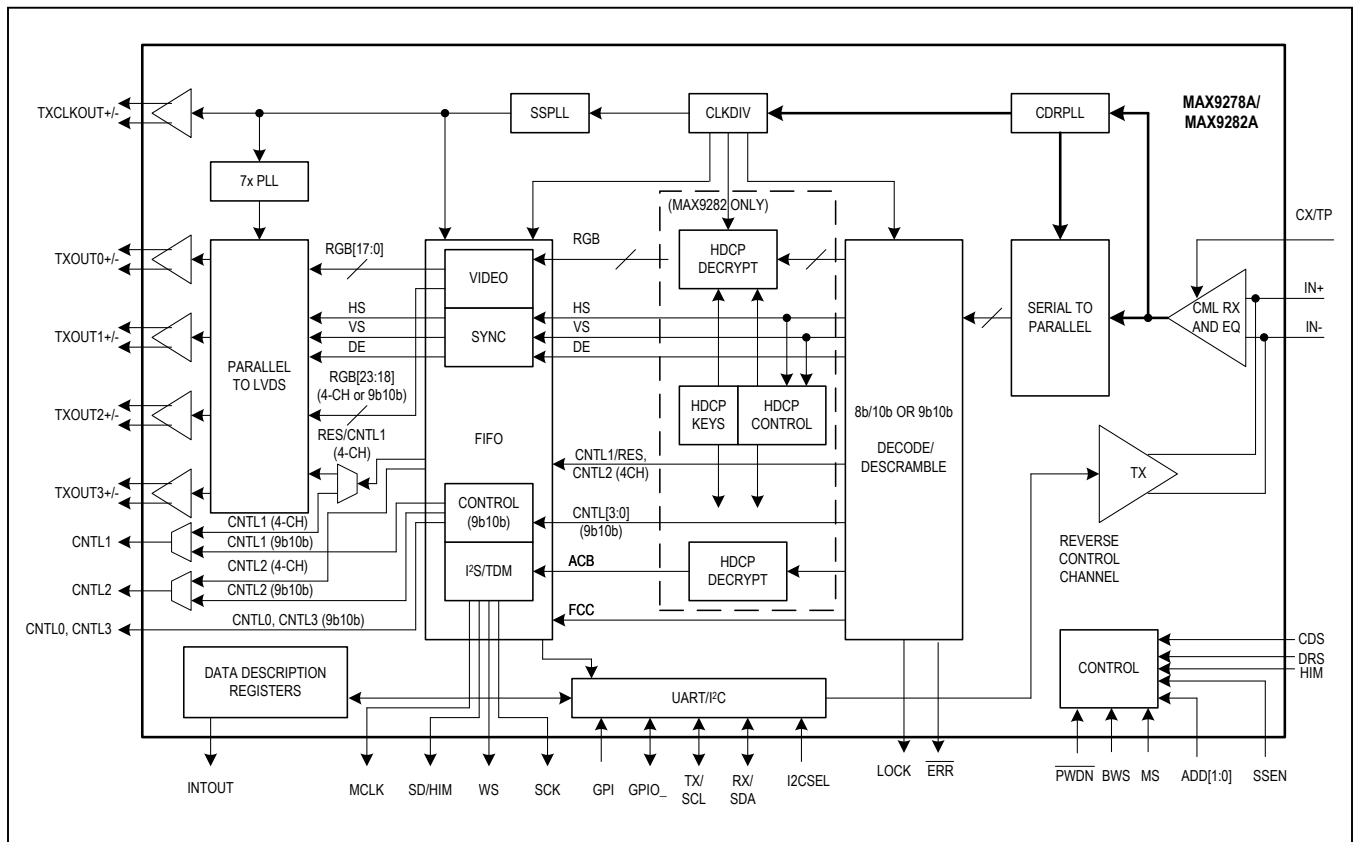


TABLE OF CONTENTS

General Description	1
Applications	1
Benefits and Features	1
Functional Diagram	2
Absolute Maximum Ratings	8
Package Thermal Characteristics	8
DC Electrical Characteristics	8
AC Electrical Characteristics	12
Typical Operating Characteristics	16
Pin Configuration	18
Pin Description	18
Detailed Description	26
Register Mapping	26
Output Bit Map	27
Serial Link Signaling and Data Format	27
High-Bandwidth Mode	31
Audio Channel	31
Audio Channel Input	31
Audio Channel Output	34
Additional MCLK Output for Audio Applications	35
Audio Output Timing Sources	35
Reverse Control Channel	35
Control Channel and Register Programming	36
UART Interface	36
Interfacing Command-Byte-Only I ² C Devices with UART	38
UART Bypass Mode	38
I ² C Interface	39
START and STOP Conditions	39
Bit Transfer	39
Acknowledge	40
Slave Address	40
Bus Reset	40
Format for Writing	41
Format for Reading	42
I ² C Communication with Remote-Side Devices	42
I ² C Address Translation	42
GPO/GPI Control	43

TABLE OF CONTENTS (continued)

Line Equalizer	43
Spread Spectrum	43
Manual Programming of the Spread-Spectrum Divider	43
HS/VIS/DE Tracking	44
Serial Input	44
Coax Splitter Mode	44
Cable Type Configuration Input	44
Color Lookup Tables	45
Programming and Verifying LUT Data	45
LUT Color Translation	45
LUT Bit Width	45
Recommended LUT Program Procedure	46
High-Immunity Reverse Control-Channel Mode	47
Sleep Mode	47
Power-Down Mode	47
Configuration Link	47
Link Startup Procedure	48
High-Bandwidth Digital Content Protection (HDCP)	51
Encryption Enable	51
Synchronization of Encryption	51
Repeater Support	51
HDCP Authentication Procedures	52
HDCP Protocol Summary	52
Example Repeater Network—Two μ Cs	56
Detection and Action Upon New Device Connection	59
Notification of Start of Authentication and Enable of Encryption to Downstream Links	59
Applications Information	60
Self PRBS Test	60
Error Checking	60
$\overline{\text{ERR}}$ Output	60
Auto Error Reset	60
Dual μ C Control	60
Changing the Clock Frequency	60
Fast Detection of Loss of Synchronization	61
Providing a Frame Sync (Camera Applications)	61
Software Programming of the Device Addresses	61
3-Level Configuration Inputs	61
Configuration Blocking	61

TABLE OF CONTENTS (continued)

Compatibility with Other GMSL Devices	61
Key Memory	61
HS/VS/DE Inversion	61
WS/SCK Inversion	62
GPIOs	62
Internal Input Pulldowns	62
Choosing I ² C/UART Pullup Resistors	62
AC-Coupling	62
Selection of AC-Coupling Capacitors	62
Power-Supply Circuits and Bypassing	63
Power-Supply Table	63
Cables and Connectors	63
Board Layout	63
ESD Protection	64
Typical Application Circuit	74
Ordering Information	74
Chip Information	74
Package Information	74
Revision History	75

LIST OF FIGURES

Figure 1. Reverse Control-Channel Output Parameters	21
Figure 2. Test Circuit for Differential Input Measurement	21
Figure 3. Test Circuit for Single-Ended Input Measurement	21
Figure 4. LVDS Output Parameters	22
Figure 5. Worst-Case Pattern Output	22
Figure 6. I ² C Timing Parameters	23
Figure 7. Parallel Clock Output Requirements	23
Figure 8. Output Pulse Positions	24
Figure 9. Enable and Disable Time Test Circuit	24
Figure 10. LVDS Enable and Disable Time	24
Figure 11. Deserializer Delay	25
Figure 12. GPI-to-GPO Delay	25
Figure 13. Lock Time	26

LIST OF FIGURES (continued)

Figure 14. Power-Up Delay	26
Figure 15. Output I ² S Timing Parameters	26
Figure 16. LVDS Input Timing	28
Figure 17. LVDS Clock and Bit Assignment	29
Figure 18. 24-Bit Mode Serial-Data Format	29
Figure 19. 32-Bit Mode Serial-Data Format	30
Figure 20. High-Bandwidth Mode Serial-Data Format	30
Figure 21. Audio Channel Input Format	31
Figure 22. 8-Channel TDM (24-Bit Samples, Padded with Zeros)	33
Figure 23. 6-Channel TDM (24-Bit Samples, No Padding)	33
Figure 24. Stereo I ² S (24-Bit Samples, Padded with Zeros)	33
Figure 25. Stereo I ² S (16-Bit Samples, No Padding)	34
Figure 26. Audio Channel Output Format	34
Figure 27. GMSL UART Protocol for Base Mode	36
Figure 28. GMSL UART Data Format for Base Mode	37
Figure 29. Sync Byte (0x79)	37
Figure 30. ACK Byte (0xC3)	37
Figure 31. Format Conversion Between GMSL UART and I ² C with Register Address (I ² CMETHOD = 0)	37
Figure 32. Format Conversion Between GMSL UART and I ² C with Register Address (I ² CMETHOD = 1)	38
Figure 33. START and STOP Conditions	39
Figure 34. Bit Transfer	39
Figure 35. Acknowledge	40
Figure 36. Slave Address	40
Figure 37. Format for I ² C Write	41
Figure 38. Format for Write to Multiple Registers	41
Figure 39. Format for I ² C Read	42
Figure 40. 2:1 Coax Splitter Connection Diagram	44
Figure 41. Coax Connection Diagram	44
Figure 42. LUT Dataflow	46
Figure 43. State Diagram, CDS = Low (Display Application)	49
Figure 44. State Diagram, CDS = High (Camera Application)	50
Figure 45. Example Network with One Repeater and Two μ Cs (Tx = GMSL Serializer's, Rx = Deserializer's)	56
Figure 46. Human Body Model ESD Test Circuit	64
Figure 47. IEC 61000-4-2 Contact Discharge ESD Test Circuit	64
Figure 48. ISO 10605 Contact Discharge ESD Test Circuit	64

LIST OF TABLES

Table 1. Device Address Defaults (Register 0x00, 0x01)	27
Table 2. Output Map (See Figure 16 and Figure 17)	28
Table 3. Data-Rate Selection Table	31
Table 4. Maximum Audio WS Frequency (kHz) for Various TXCLKOUT Frequencies	32
Table 5. fSRC Settings	35
Table 6. I ² C Bit Rate Ranges	42
Table 7. Cable Equalizer Boost Levels	43
Table 8. Output Spread	43
Table 9. Modulation Coefficients and Maximum SDIV Settings	43
Table 10. Configuration Input Map	44
Table 11. Pixel Data Format	45
Table 12. Reverse Control-Channel Modes	47
Table 13. Fast High-Immunity Mode Requirements	47
Table 14. Startup Procedure for Video-Display Applications (CDS = Low)	48
Table 15. Startup Procedure for Image-Sensing Applications (CDS = High)	50
Table 16. Startup, HDCP Authentication, and Normal Operation (Deserializer is Not a Repeater)—First Part of the HDCP Authentication Protocol	52
Table 17. Link Integrity Check (Normal)—Performed Every 128 Frames After Encryption is Enabled	54
Table 18. Optional Enhanced Link Integrity Check—Performed Every 16 Frames After Encryption is Enabled	55
Table 19. HDCP Authentication and Normal Operation (One Repeater, Two μ Cs)—First and Second Parts of the HDCP Authentication Protocol	56
Table 20. MAX9278A/MAX9282A Feature Compatibility	61
Table 21. Additional Supply Current from HDCP (MAX9282A Only)	63
Table 22. Suggested Connectors and Cables for GMSL	63
Table 23. Register Table	65
Table 24. HDCP Register Table (MAX9282A Only)	72

Absolute Maximum Ratings (Note 1)

AVDD to EP-0.5V to +3.9V
 DVDD to EP-0.5V to +3.9V
 IOVDD to EP-0.5V to +3.9V
 IN+, IN- to EP-0.5V to +1.9V
 TXOUT_, TCLKOUT_ to EP.....-0.5V to +3.9V
 All Other Pins to EP-0.5V to (V_{IOVDD} + 0.5V)
 IN+, IN- Short Circuit to Ground or Supply Continuous

Continuous Power Dissipation (T_A = +70°C)
 TQFN (derate 40mW/°C above +70°C).....3200mW
 QFND (derate 38.5mW/°C above +70°C)3076.9mW
 Operating Temperature Range -40°C to +105°C
 Junction Temperature +150°C
 Storage Temperature Range -65°C to +150°C
 Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow) +260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN	Junction-to-Ambient Thermal Resistance (θ _{JA})25°C/W	QFND	Junction-to-Ambient Thermal Resistance (θ _{JA})26°C/W
	Junction-to-Case Thermal Resistance (θ _{JC}).....1°C/W		Junction-to-Case Thermal Resistance (θ _{JC}).....1°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (GPI, CDS, HIM, EQS, PWDN, OEN, I2CSEL, MS, SSEN, DRS, WS, SCK)							
High-Level Input Voltage	V _{IH1}			0.65 x V _{IOVDD}			V
Low-Level Input Voltage	V _{IL1}				0.35 x V _{IOVDD}		V
Input Current	I _{IN1}	V _{IN} = 0V to V _{IOVDD}		-10		+20	μA
SINGLE-ENDED OUTPUTS (MCLK, WS, SCK, SD, CNTL_, INTOUT)							
High-Level Output Voltage	V _{OH1}	I _{OUT} = -2mA	DCS = 0	V _{IOVDD} - 0.3			V
			DCS = 1	V _{IOVDD} - 0.2			
Low-Level Output Voltage	V _{OL1}	I _{OUT} = 2mA	DCS = 0		0.3		V
			DCS = 1		0.2		
Output Short-Circuit Current	I _{OS}	V _O = 0V, DCS = 0	V _{IOVDD} = 3.0V to 3.6V	15	25	39	mA
			V _{IOVDD} = 1.7V to 1.9V	3	7	13	
		V _O = 0V, DCS = 1	V _{IOVDD} = 3.0V to 3.6V	20	35	63	
			V _{IOVDD} = 1.7V to 1.9V	5	10	21	

DC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN INPUT/OUTPUT (GPIO0, GPIO1, RX/SDA, TX/SCL, ERR, LOCK)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 4)	RX/SDA, TX/SCL	-100		+5	μA
			LOCK, ERR, GPIO_	-80		+5	
Low-Level Output Voltage	V_{OL2}	$I_{OUT} = 3mA$	$V_{IOVDD} = 1.7V$ to $1.9V$			0.4	V
			$V_{IOVDD} = 3.0V$ to $3.6V$			0.3	
Input Capacitance	C_{IN}	Each pin (Note 5)				10	pF
OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage (V_{IN+}) - (V_{IN-})	V_{RODH}	Forward channel disabled, Figure 1	Legacy reverse control-channel mode	30		60	mV
			High-immunity mode	50		100	
Differential Low Output Peak Voltage (V_{IN+}) - (V_{IN-})	V_{RODL}	Forward channel disabled, Figure 1	Legacy reverse control-channel mode	-60		-30	mV
			High-immunity mode	-100		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled	Legacy reverse control-channel mode	30		60	mV
			High-immunity mode	50		100	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled	Legacy reverse control-channel mode	-60		-30	mV
			High-immunity mode	-100		-50	
DIFFERENTIAL INPUTS (IN+, IN-)							
Differential High Input Threshold (Peak) Voltage (V_{IN+}) - (V_{IN-})	$V_{IDH(P)}$	Figure 2	Activity detector medium threshold, (0x0B D[6:5] = 01)			60	mV
			Activity detector low threshold, (0x0B D[6:5] = 00)			47.5	
Differential Low Input Threshold (Peak) Voltage (V_{IN+}) - (V_{IN-})	$V_{IDL(P)}$	Figure 2	Activity detector medium threshold, (0x0B D[6:5] = 01)	-60			mV
			Activity detector medium threshold, (0x0B D[6:5] = 00)	-47.5			
Input Common-Mode Voltage ($(V_{IN+}) + (V_{IN-})/2$)	V_{CMR}			1	1.3	1.6	V

DC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Resistance (Internal)	R_{IN}		80	100	130	Ω
SINGLE-ENDED INPUTS (IN+, IN-)						
Single-Ended High Input Threshold (Peak) Voltage	$V_{ISH(P)}$	Activity detector medium threshold, (0x0B D[6:5] = 01)			43	mV
		Activity detector low threshold, (0x0B D[6:5] = 00)			33	
Single-Ended Low Input Threshold (Peak) Voltage	$V_{ISL(P)}$	Activity detector medium threshold, (0x0B D[6:5] = 01)	-43			mV
		Activity detector medium threshold, (0x0B D[6:5] = 00)	-33			
Input Resistance (Internal)	R_I		40	50	65	Ω
THREE-LEVEL LOGIC INPUTS (BWS, ADD_, CX/TP)						
High-Level Input Voltage	V_{IH}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}			0.3 x V_{IOVDD}		V
Mid-Level Input Current	I_{INM}	(Note 6)	-10		10	μA
Input Current	I_{IN}		-150		150	μA
LVDS OUTPUTS (TXOUT_, TXCLKOUT_ (Figure 4))						
Differential Output Voltage	V_{OD}		250		450	mV
Change in V_{OS} Between Complementary Output States	ΔV_{OD}				25	mV
Output Offset Voltage	V_{OS}		1.125		1.375	V
Cange in V_{OS} Between Complementary Output States	ΔV_{OS}				25	mV
Output Short-Circuit Current	I_{OS}	$V_{OUT} = 0$ or $3.6V$	3.5mA LVDS output	-7.5	+7.5	mA
			7mA LVDS output	-15	+15	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	3.5mA LVDS output			7.5	mA
		7mA LVDS output			15	
Output High-Impedance Current	I_{OZ}	Power-off or $PWDN = low$, $V_{OUT+} = 0$ or $3.6V$, $V_{OUT-} = 0$ or $3.6V$	-0.5		+0.5	μA

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
POWER SUPPLY								
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case Pattern, Figure 5)	I _{WCS}	BWS = low, DRS = low, f _{TXCLKOUT} = 33.33MHz	I _{AVDD} + I _{DVDD} , 2% spread enabled or disabled	162	190		mA	
			I _{IOVDD}	V _{IOVDD} = 3.6V	9	10		
				V _{IOVDD} = 1.9V	4.8	5.1		
		BWS = low, DRS = low, f _{TXCLKOUT} = 104MHz	I _{AVDD} + I _{DVDD} , 2% spread enabled or disabled		240	280		
				I _{IOVDD}	V _{IOVDD} = 3.6V	9		10
					V _{IOVDD} = 1.9V	4.8		5.1
		BWS = open, DRS = low, f _{TXCLKOUT} = 36.66MHz	I _{AVDD} + I _{DVDD} , 2% spread enabled or disabled		178	210		
				I _{IOVDD}	V _{IOVDD} = 3.6V	10		11
					V _{IOVDD} = 1.9V	5.3		5.6
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case Pattern, Figure 5)	I _{WCS}	BWS = open, DRS = low, f _{TXCLKOUT} = 104MHz	I _{AVDD} + I _{DVDD} , 2% spread enabled or disabled	258	300		mA	
			I _{IOVDD}	V _{IOVDD} = 3.6V	11.5	12.5		
				V _{IOVDD} = 1.9V	6.2	6.5		
		BWS = high, DRS = low, f _{TXCLKOUT} = 33.33MHz	I _{AVDD} + I _{DVDD} , 2% spread enabled or disabled		175	210		
				I _{IOVDD}	V _{IOVDD} = 3.6V	10.7		11.7
					V _{IOVDD} = 1.9V	5.7		6
		BWS = high, DRS = low, f _{TXCLKOUT} = 78MHz	I _{AVDD} + I _{DVDD} , 2% spread enabled or disabled		231	280		
				I _{IOVDD}	V _{IOVDD} = 3.6V	13		14.1
					V _{IOVDD} = 1.9V	7		7.4
Sleep Mode Supply Current	I _{CCS}			64	300		μA	
Power-Down Current	I _{CCZ}	PWDN = GND		27	250		μA	
ESD PROTECTION								
IN+, IN- (Note 8)	V _{ESD}	Human Body Model, R _D = 1.5kΩ, C _S = 100pF		±8			kV	
		IEC 61000-4-2, R _D = 330Ω, C _S = 150pF	Contact discharge	±10				
			Air discharge	±12				
		ISO 10605, R _D = 2kΩ, C _S = 330pF	Contact discharge	±8				
			Air discharge	±15				

DC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TXOUT_, TXCLKOUT_	V_{ESD}	Human Body Model, $R_D = 1.5k\Omega$, $C_S = 100pF$		± 8		kV
		IEC 61000-4-2, $R_D = 330\Omega$, $C_S = 150pF$	Contact discharge	± 8		
			Air discharge	± 20		
		ISO 10605, $R_D = 2k\Omega$, $C_S = 330pF$	Contact discharge	± 8		
Air discharge	± 30					
All Other Pins (Note 9)	V_{ESD}	Human Body Model, $R_D = 1.5k\Omega$, $C_S = 100pF$		± 4		kV

AC Electrical Characteristics

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS CLOCK OUTPUT (TXCLKOUT_)						
Clock Frequency	$f_{TXCLKOUT_}$	BWS = low, DRS = high	8.33		16.66	MHz
		BWS = low, DRS = low	16.66		104	
		BWS = mid, DRS = high	18.33		36.66	
		BWS = mid, DRS = low	36.66		104	
		BWS = high, DRS = high	6.25		12.5	
		BWS = high, DRS = low	12.5		78	
I²C/UART PORT TIMING						
I ² C/UART Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, $C_L = 10pF$ to $100pF$, $1k\Omega$ pullup to V_{IOVDD}	20		150	ns
Output Fall Time	t_F	70% to 30%, $C_L = 10pF$ to $100pF$, $1k\Omega$ pullup to V_{IOVDD}	20		150	ns
I²C TIMING (Figure 6)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)	> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)	> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0	μs
		Mid		0.6		
		High		0.26		

AC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low	4.7			μs
			Mid	1.3			
			High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low	4.0			μs
			Mid	0.6			
			High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low	4.7			μs
			Mid	0.6			
			High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low	0			μs
			Mid	0			
			High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low	250			μs
			Mid	100			
			High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low	4.0			μs
			Mid	0.6			
			High	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low	4.7			μs
			Mid	1.3			
			High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low		3.45		μs
			Mid		0.9		
			High		0.45		
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low		3.45		μs
			Mid		0.9		
			High		0.45		
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low		50		ns
			Mid		50		
			High		50		
Capacitive Load Each Bus Line	C_b					100	pF

AC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS							
CNTL3–CNL0, MCLK Output Rise-and-Fall Time (Figure 7)	t_R, t_F	20% to 80%, DCS = 1, $C_L = 10pF$	DCS = 1, $C_L = 10pF$	0.5		3.1	ns
			DCS = 0, $C_L = 5pF$	0.3		2.2	
		20% to 80%, DCS = 0, $C_L = 5pF$	$V_{IOVDD} = 1.7V$ to $1.9V$	0.6		3.8	
			$V_{IOVDD} = 3.0V$ to $3.6V$	0.4		2.4	
LVDS Output Rise Time	t_R	20% to 80%, $R_L = 100\Omega$			200	350	ps
LVDS Output Fall Time	t_F	80% to 20%, $R_L = 100\Omega$			200	350	ps
LVDS Output Pulse Position (Figure 8)	t_{PPOSN}	N = 0 to 6, $t_{CLK} = 1/$ $f_{TXCLKOUT_}$	$f_{TXCLKOUT_} = 6.25MHz$	$N/7 \times t_{CLK} - 400$	$N/7 \times t_{CLK}$	$N/7 \times t_{CLK} + 400$	ps
			$f_{TXCLKOUT_} = 12.5MHz$	$N/7 \times t_{CLK} - 250$	$N/7 \times t_{CLK}$	$N/7 \times t_{CLK} + 250$	
			$f_{TXCLKOUT_} = 33MHz$	$N/7 \times t_{CLK} - 200$	$N/7 \times t_{CLK}$	$N/7 \times t_{CLK} + 200$	
			$f_{TXCLKOUT_} = 78MHz$	$N/7 \times t_{CLK} - 125$	$N/7 \times t_{CLK}$	$N/7 \times t_{CLK} + 125$	
			$f_{TXCLKOUT_} = 104MHz$	$N/7 \times t_{CLK} - 100$	$N/7 \times t_{CLK}$	$N/7 \times t_{CLK} + 100$	
LVDS Output Enable Time	t_{LVEN}	From last bit of the enable UART packet to $V_{OS} = 1.25V$ (Figure 9, 10)				50	μs
LVDS Output Disable Time	t_{LVDS}	From last bit of the enable UART packet to $V_{OS} = 0V$ (Figure 9, 10)				50	μs
Deserializer Delay	t_{SD}	(Note 11) Figure 11		38		48	t_{PCLK}
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission, Figure 1		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission, Figure 1		180		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included), Figure 12				350	μs
Lock Time	t_{LOCK}	Figure 13				3.6	ms
Power-Up Time	t_{PU}	Figure 14				9.4	ms

AC Electrical Characteristics (continued)

($V_{AVDD} = V_{DVDD} = 3.0V$ to $3.6V$, $V_{IOVDD} = 1.7V$ to $3.6V$, $R_L = 100\Omega \pm 1\%$ (differential), EP connected to PCB ground (GND), $T_A = -40^\circ C$ to $+105^\circ C$, unless otherwise noted. Typical values are at $V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²S/TDM OUTPUT TIMING (Note 6)						
WS Jitter	t_{jWS}	$t_{WS} = 1/f_{WS}$, (cycle-to-cycle), rising-to-falling edge or falling-to-rising edge	$f_{WS} = 48kHz$ or $44.1kHz$	1.2e-3 x t_{WS}	1.5e-3 x t_{WS}	ns
			$f_{WS} = 96kHz$	1.6e-3 x t_{WS}	2e-3 x t_{WS}	
			$f_{WS} = 192kHz$	1.6e-3 x t_{WS}	2e-3 x t_{WS}	
SCK Jitter (2-Channel I ² S)	t_{jSCK1}	$t_{SCK} = 1/f_{SCK}$, (cycle-to-cycle), rising-to-rising edge	$n_{SCK} = 16$ bits, $f_{WS} = 48kHz$ or $44.1kHz$	13e-3 x t_{SCK}	16e-3 x t_{SCK}	ns
			$n_{SCK} = 24$ bits, $f_{WS} = 96kHz$	39e-3 x t_{SCK}	48e-3 x t_{SCK}	
			$n_{SCK} = 32$ bits, $f_{WS} = 192kHz$	0.1 x t_{SCK}	0.13 x t_{SCK}	
SCK Jitter (8-Channel TDM)	t_{jSCK2}	$t_{SCK} = 1/f_{SCK}$, (cycle-to-cycle), rising-to-rising edge	$n_{SCK} = 16$ bits, $f_{WS} = 48kHz$ or $44.1kHz$	52e-3 x t_{SCK}	64e-3 x t_{SCK}	ns
			$n_{SCK} = 24$ bits, $f_{WS} = 96kHz$	156e-3 x t_{SCK}	192e-3 x t_{SCK}	
			$n_{SCK} = 32$ bits, $f_{WS} = 192kHz$	0.4 x t_{SCK}	0.52 x t_{SCK}	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized		3 x t_{WS}	4 x t_{WS}	μs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	$C_L = 10pF$, DCS = 1	0.3	3.1	ns
			$C_L = 5pF$, DCS = 0	0.4	3.8	
SD, WS Valid Time Before SCK (2-Channel I ² S)	t_{DVB1}	$t_{SCK} = 1/f_{SCK}$, Figure 15	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (2-Channel I ² S)	t_{DVA1}	$t_{SCK} = 1/f_{SCK}$, Figure 15	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time Before SCK (8-Channel TDM)	t_{DVB2}	$t_{SCK} = 1/f_{SCK}$, Figure 15	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (8-Channel TDM)	t_{DVA2}	$t_{SCK} = 1/f_{SCK}$, Figure 15	0.20 x t_{SCK}	0.5 x t_{SCK}		ns

Note 3: Limits are 100% production tested at $T_A = +25^\circ C$. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 5: Not production tested. Guaranteed by design.

Note 6: To provide a mid level, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than $\pm 10\mu A$.

Note 7: I_{IOVDD} not production tested. HDCP not enabled (MAX9282A only). See [Table 21](#) for additional supply current when HDCP is enabled

Note 8: Specified pin to ground.

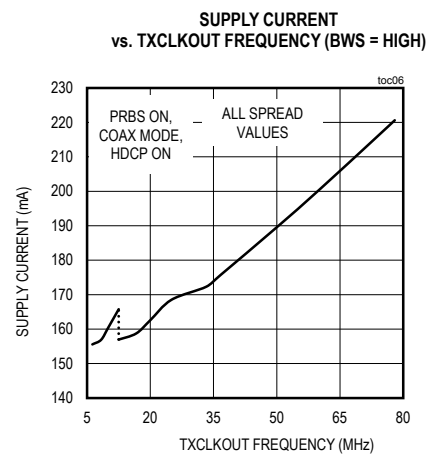
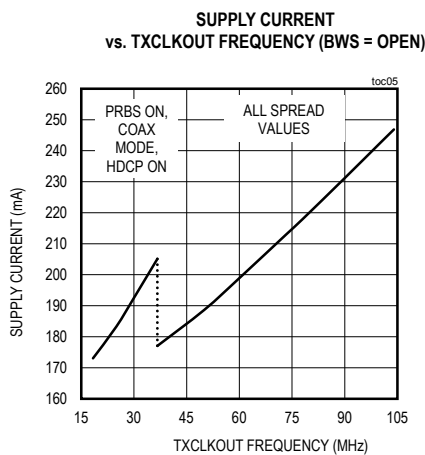
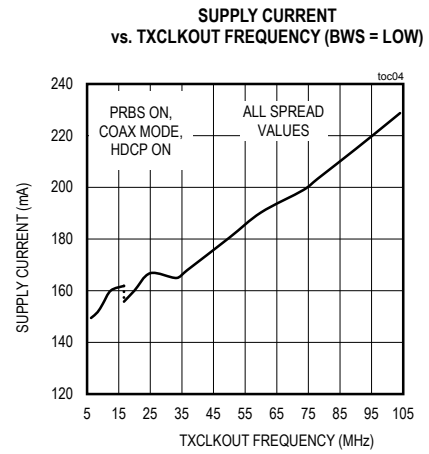
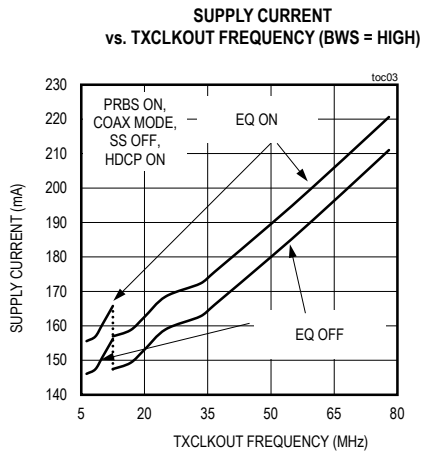
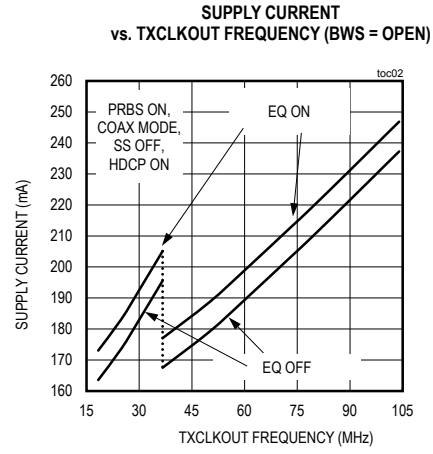
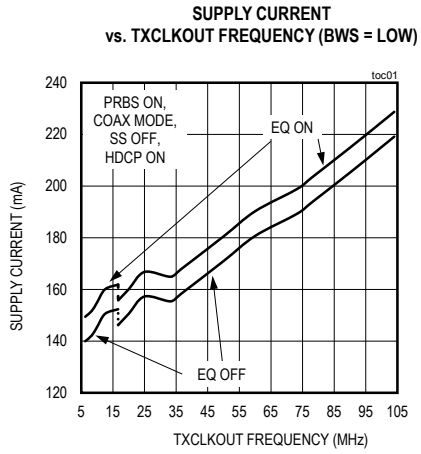
Note 9: Specified pin to all supply/ground.

Note 10: Not production tested, guaranteed by bench characterization.

Note 11: Measured in pixel clock bit times. $t_{PCLK} = 1 / x f_{TXCLKOUT_}$.

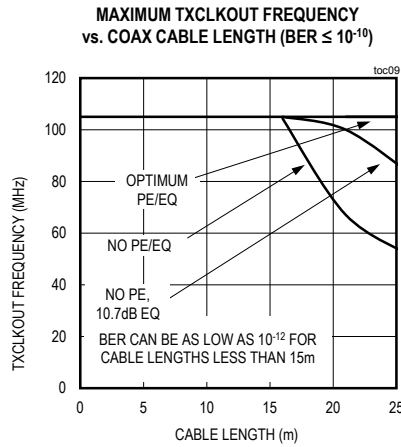
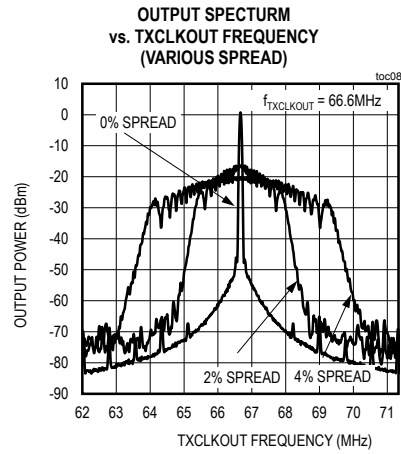
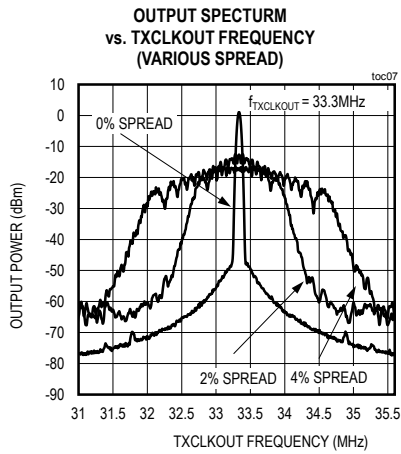
Typical Operating Characteristics

($V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

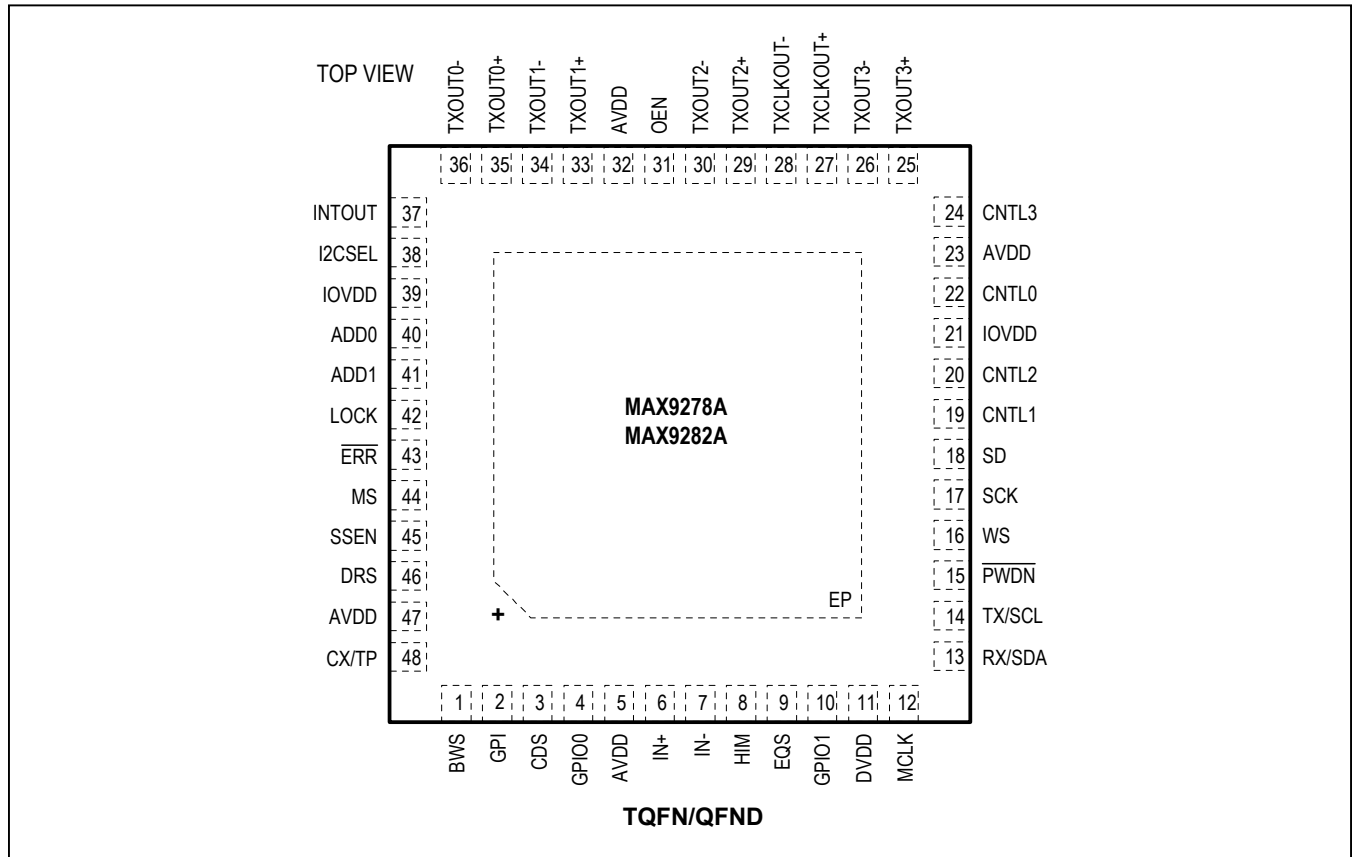


Typical Operating Characteristics (continued)

($V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low for 3-channel mode. Set BWS = high for 4-channel mode. Set BWS = open for high-bandwidth mode.
2	GPI	General-Purpose Input with Internal Pulldown to EP. The serializer GPO (or INT) output follows GPI.
3	CDS	Control Channel Direction Select Input with Internal Pulldown to EP. Set CDS = high when a control-channel master μC is connected at the deserializer. set CDS = low when a control-channel master μC is connected at the serializer.
4	GPIO0	Open-Drain, General-Purpose Input/Output with Internal 60k Ω Pullup to IOVDD
5, 23, 32, 47	AVDD	3.3V Analog Power Supply. Bypass AVDD to EP with 0.1 μF and 0.001 μF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
6	IN+	Noninverting Coax/Twisted-Pair Serial Input
7	IN-	Inverting Coax/Twisted-Pair Serial Input
8	HIM	High-Immunity Mode Input with Internal Pulldown to EP. Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\text{PWN} = \text{low}$) and is active-high. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value.

Pin Description (continued)

PIN	NAME	FUNCTION
9	EQS	Equalizer Select Input with Internal Pulldown to EP. The state of EQS is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}} = \text{low}$). EQS = low selects 10.7dB boost. EQS = high selects 5.7dB boost.
10	GPIO1	Open-Drain, General-Purpose Input/Output with Internal 60k Ω Pullup to IOVDD
11	DVDD	3.3V Digital Power Supply. Bypass DVDD to EP with 0.1 μF and 0.001 μF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
12	MCLK	Master Clock Output. See the <i>Additional MCLK Output for Audio Applications</i> section.
13	RX/SDA	UART Receive/I ² C Serial-Data Input/Output with Internal 30k Ω Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I ² C master/slave.
14	TX/SCL	UART Transmit/I ² C Serial-Clock Input/Output with Internal 30k Ω Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I ² C master/slave.
15	$\overline{\text{PWDN}}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{\text{PWDN}}$ low to enter power-down mode to reduce power consumption.
16	WS	I ² S/TDM Word-Select Input/Output. Powers up as an I ² S output (deserializer-provided clock). Set AUDIOMODE bit = 1 to change WS to an input with internal pulldown to GND and supply WS externally (system provided clock).
17	SCK	I ² S/TDM Serial-Clock Input/Output. Powers up as an I ² S output (deserializer-provided clock). Set AUDIOMODE bit = 1 to change SCK to an input with internal pulldown to GND and supply SCK externally (system provided clock).
18	SD	I ² S/TDM Serial-Data Output. Disable I ² S/TDM encoding to serial data to use SD as an additional control/data output valid on the selected edge of TXCLKOUT_. Encrypted when HDCP is enabled (MAX9282A only).
19	CNTL1	Auxiliary Control-Signal Output. CNTL1 remains high impedance in 24-bit mode (BWS = low) CNTL1 used only in 32-bit or high-bandwidth mode (BWS = high or open). CNTL1 not encrypted when HDCP is enabled (MAX9282A only)
20	CNTL2	Auxiliary Control-Signal Output. CNTL2 remains high impedance in 24-bit mode (BWS = low). CNTL2 used only in 32-bit or high-bandwidth mode (BWS = high or open). CNTL2 not encrypted when HDCP is enabled (MAX9282A only).
21, 39	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1 μF and 0.001 μF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
22	CNTL0	Auxiliary Control-Signal Output. CNTL0: Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9282A only).
24	CNTL3	Auxiliary Control-Signal Output. CNTL3: Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9282A only).

Pin Description (continued)

PIN	NAME	FUNCTION
25, 26, 29, 30, 33–36	TXOUT_+, TXOUT_-	LVDS Data Output. Output use depends on BWS pin setting (Table 3). Certain data bits encrypted when HDCP is enabled (MAX9282A only).
27, 28	TXCLKOUT+, TXCLKOUT-	LVDS Clock Output
31	OEN	CMOS Output-Enable Input with Internal Pulldown to EP. Set OEN high to enable MCLK, CNTL0, CNTL3, and INTOUT. Set OEN = low to put MCLK CNTL0, CNTL3, and INTOUT into high impedance.
37	INTOUT	A/V Status Register Interrupt Output. Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
38	I2CSEL	I ² C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I ² C-to-I ² C interface. Set I2CSEL = low to select UART-to-UART or UART-to-I ² C interface.
40	ADD0	Three-Level Address Selection Input with Internal Pulldown to EP. The state of ADD0 is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1.
41	ADD1	Three-Level Address Selection Input with Internal Pulldown to EP. The state of ADD1 is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1.
42	LOCK	Open-Drain Lock Output with Internal 30k Ω Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when $\overline{\text{PWDN}}$ = low.
43	$\overline{\text{ERR}}$	Error Output. Open-drain data error detection and/or correction indication output with internal 30k Ω pullup to IOVDD. $\overline{\text{ERR}}$ is high when $\overline{\text{PWDN}}$ is low.
44	MS	Mode Select with Internal Pulldown to EP. MS sets the control-link mode when CDS = high. Set MS = low to select base mode. Set MS = high to select bypass mode. MS sets the power-up state when CDS = low.
45	SSEN	Spread-Spectrum Enable Input with Internal Pulldown to EP (Default). The state of SSEN is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set SSEN = high for 2% spread spectrum on the LVDS and control outputs. Set SSEN = low to use the LVDS and control outputs without spread spectrum.
46	DRS	Data-Rate Select Input with Internal Pulldown to EP (Default). The state of DRS is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set DRS = high for slow TXCLKOUT_ frequencies (Table 4). Set SSEN = low for fast TXCLKOUT_ frequencies.
48	CX/TP	Three-Level Coax/Twisted-Pair Select Input. See Table 10 for function.
—	EP	Exposed Pad. EP is internally connected to device ground. MUST connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

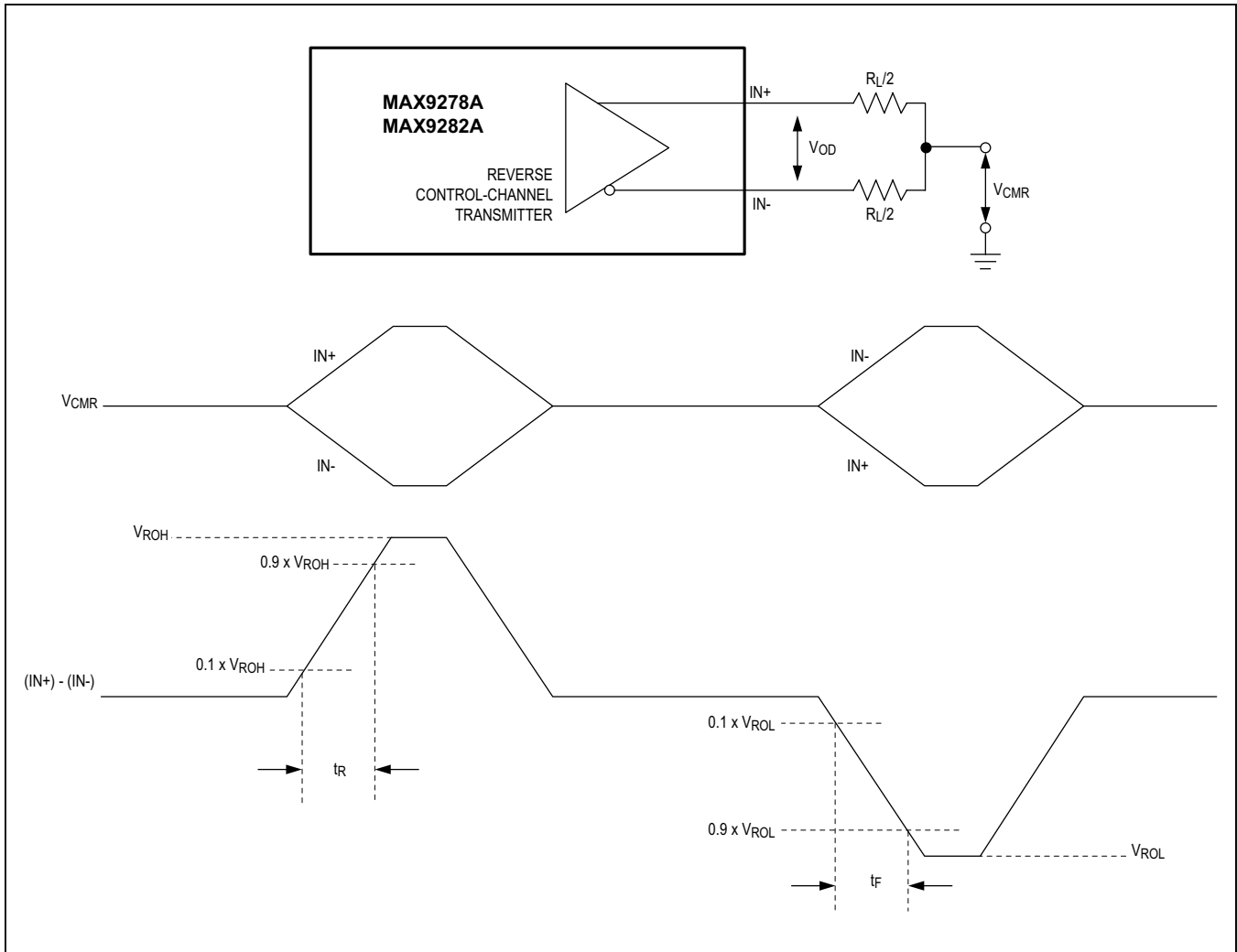


Figure 1. Reverse Control-Channel Output Parameters

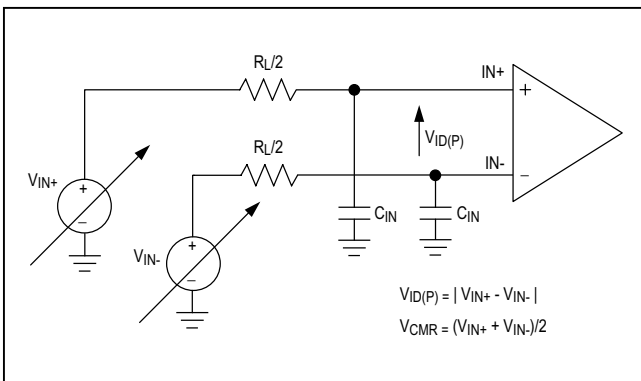


Figure 2. Test Circuit for Differential Input Measurement

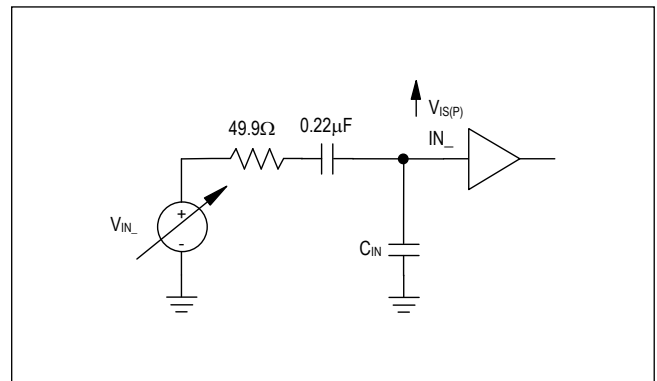


Figure 3. Test Circuit for Single-Ended Input Measurement

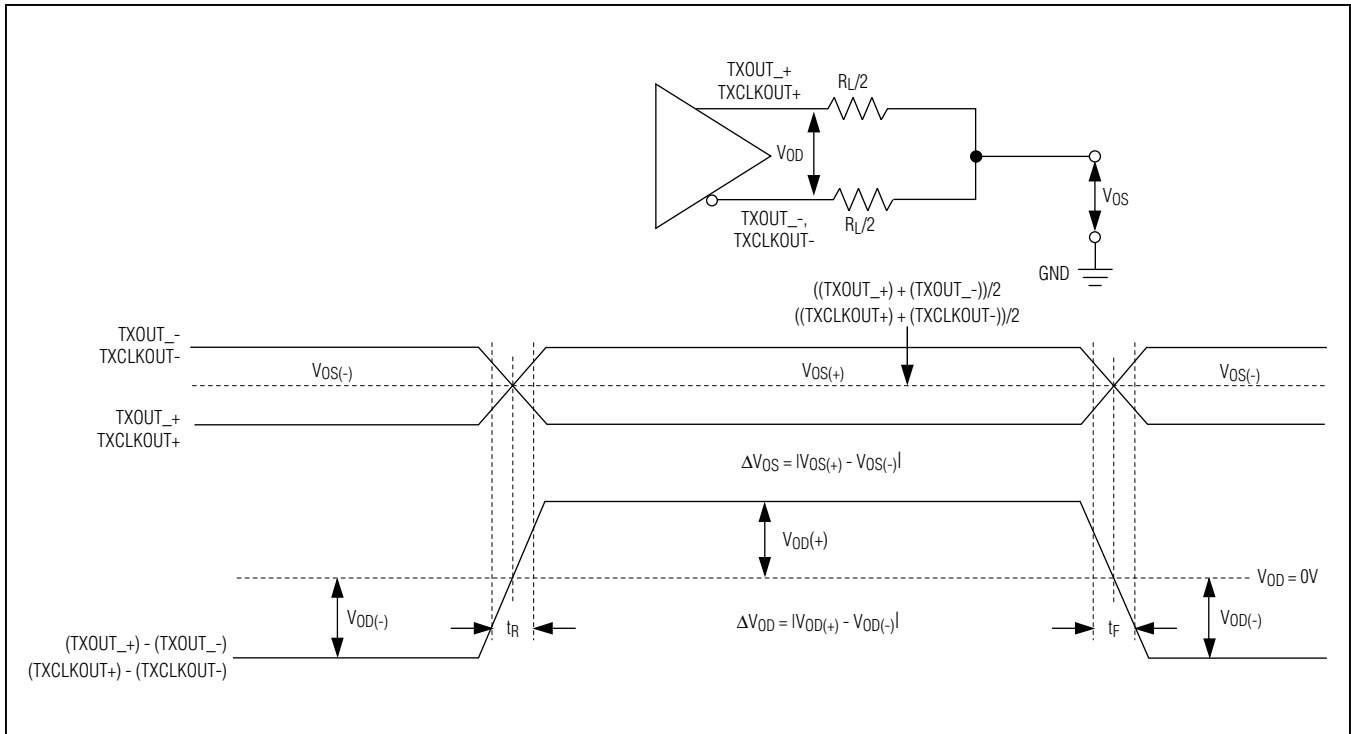


Figure 4. LVDS Output Parameters

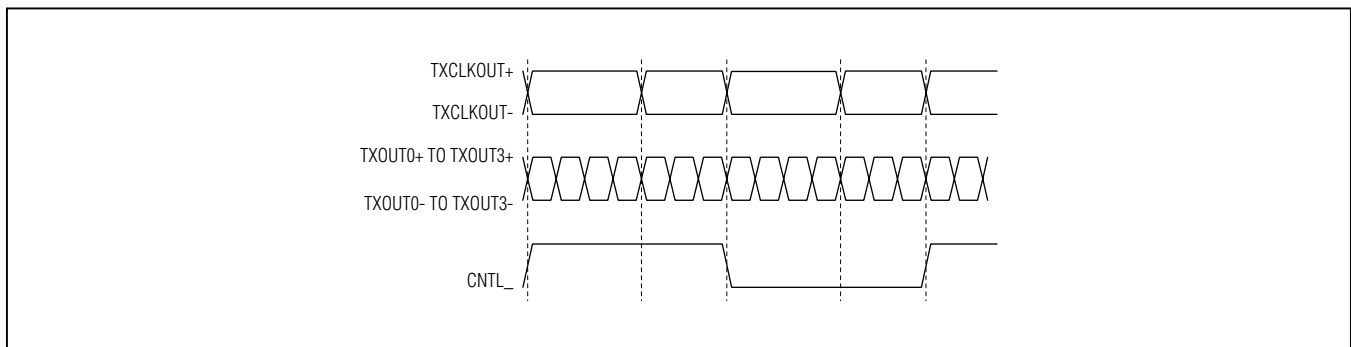


Figure 5. Worst-Case Pattern Output

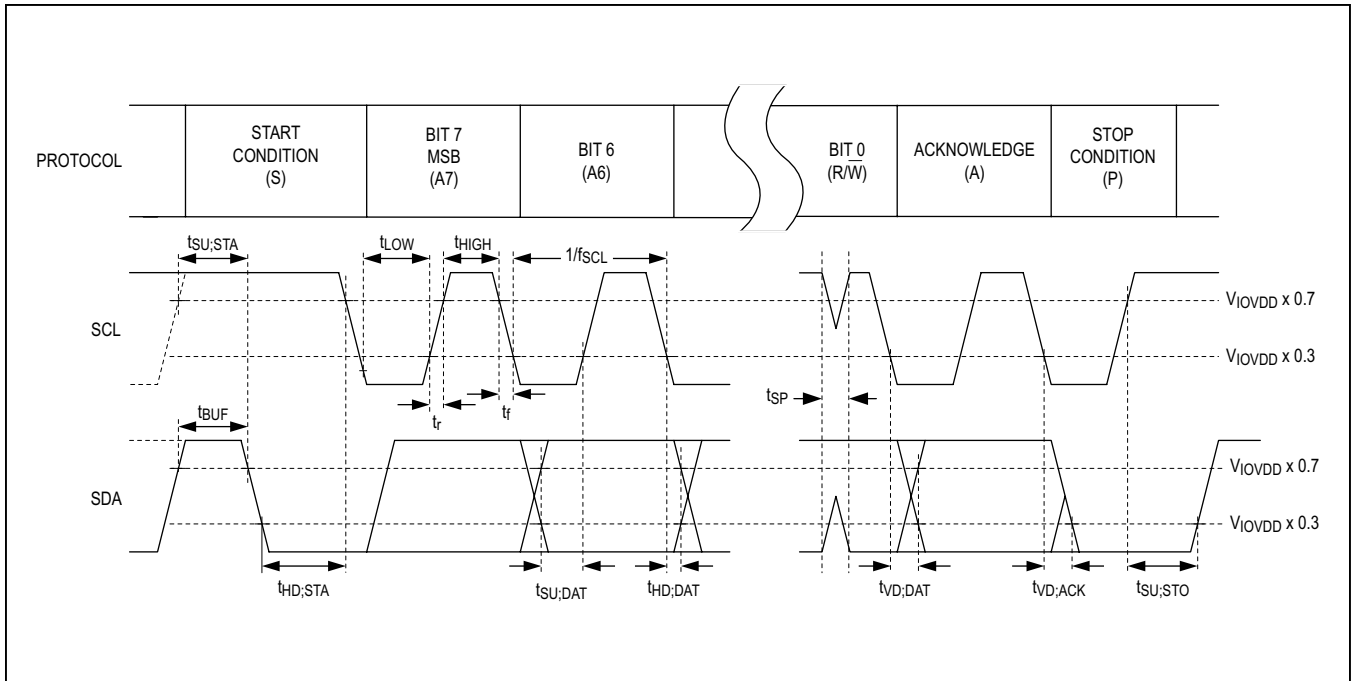


Figure 6. I²C Timing Parameters

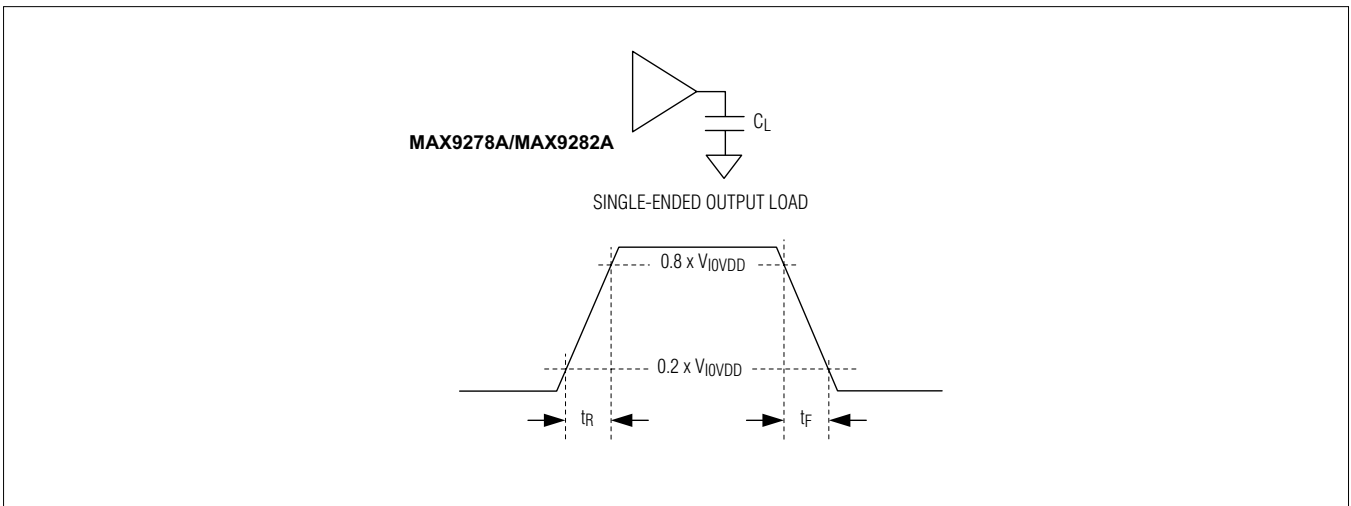


Figure 7. Parallel Clock Output Requirements

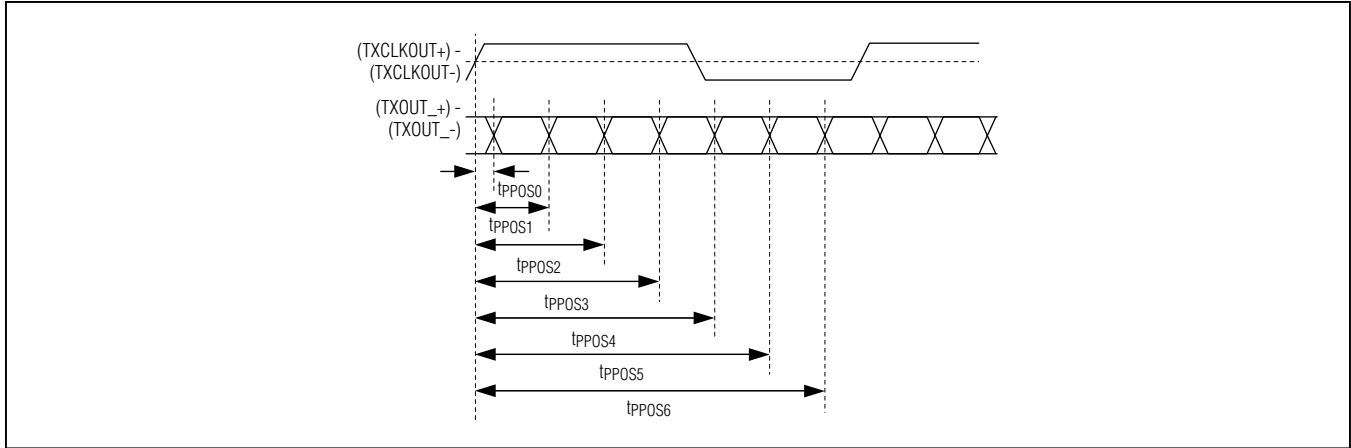


Figure 8. Output Pulse Positions

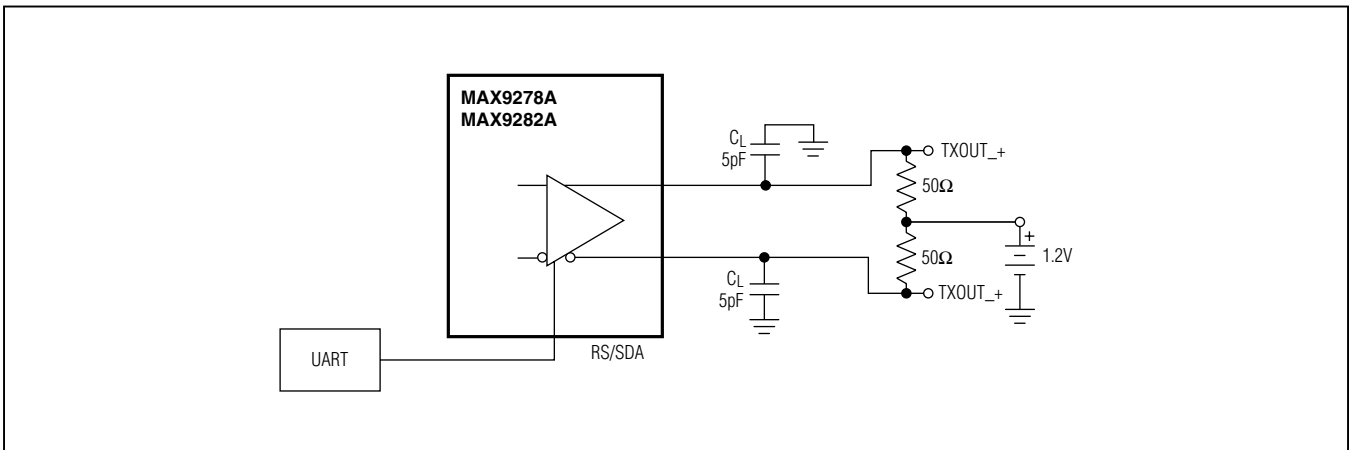


Figure 9. Enable and Disable Time Test Circuit

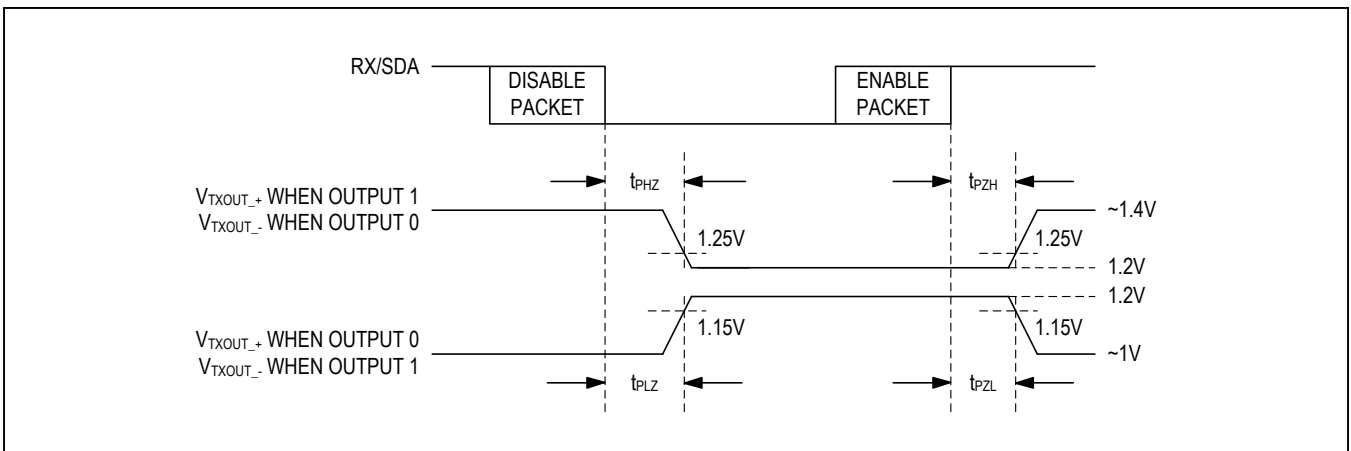


Figure 10. LVDS Enable and Disable Time

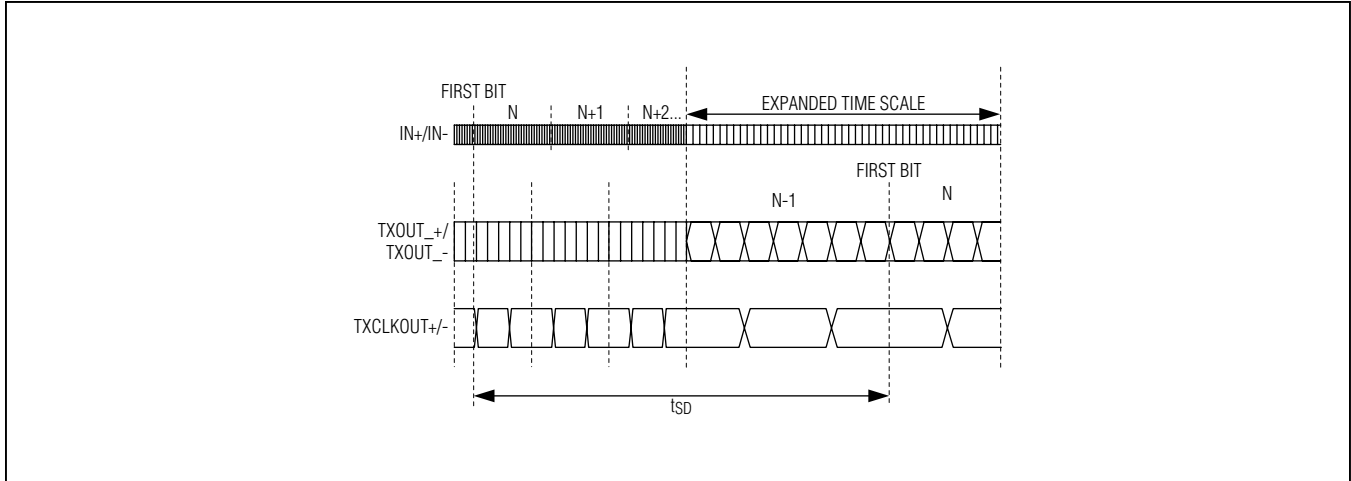


Figure 11. Deserializer Delay

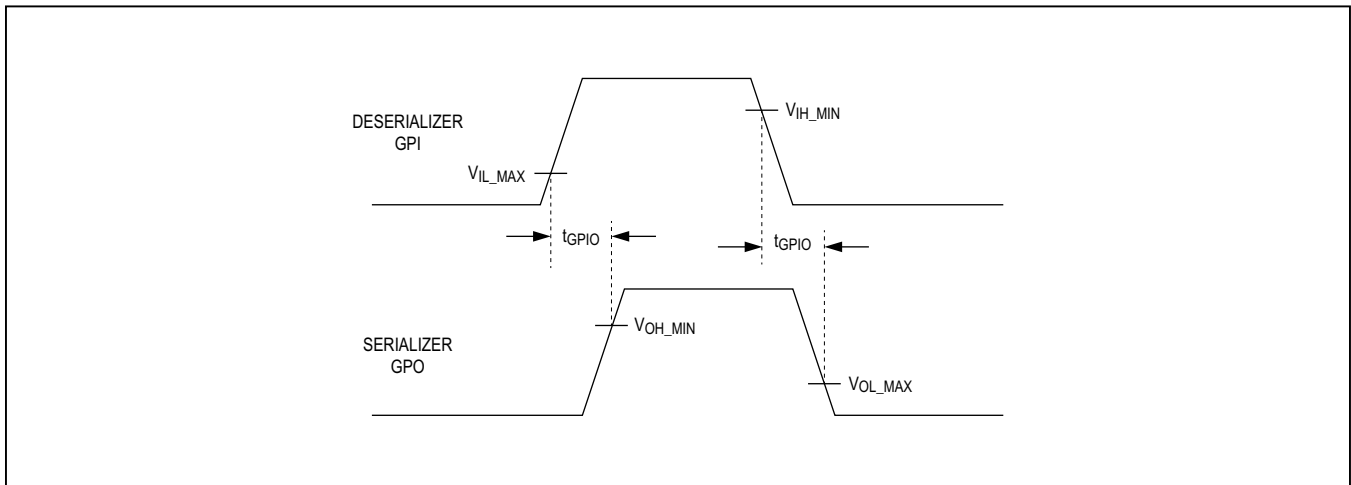


Figure 12. GPI-to-GPO Delay