Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX9275/MAX9279

3.12Gbps GMSL Serializers for Coax or STP Output Drive and Parallel Input

General Description

The MAX9275/MAX9279 are 3.12Gbps Gigabit Multimedia Serial Link (GMSL) serializers with parallel LVCMOS inputs and a CML serial output programmable for 50Ω coax or 100Ω shielded twisted pair (STP) cable drive. The MAX9279 has HDCP content protection but otherwise is the same as the MAX9275. The serializers pair with any GMSL deserializer capable of coax input. When programmed for STP output they are backward compatible with any GMSL deserializer. The output amplitude is programmable 100mV to 500mV, single-ended (coax) or 100mV to 400mV differential (STP).

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-UART and UART-I²C modes, and up to 1Mbps in I²C-I²C mode. Using the control channel, a µC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9279). A GPO output supports touch-screen controller interrupt requests from the remote end of the link.

For use with longer cables, the serializers have programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 1.7V to 1.9V and the I/O supply is 1.7V to 3.6V. The MAX9275/MAX9279 are available in a lead-free, 56-pin, 8mm x 8mm, TQFN package with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Benefits and Features

- Ideal for High-Definition Video Applications
  - Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - 104MHz High-Bandwidth Mode Supports 1920x720p/60Hz Display With 24-Bit Color
  - Serializer Pre/Deemphasis Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate And 32-Bit Sample Depth For 7.1 Channel HD Audio
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 6.25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock Stretch Capability
- Reduces EMI and Shielding Requirements
  - Serial Output Programmable for 100mV to 500mv Single-Ended or 100mV to 400mV Differential
  - Programmable Spread Spectrum Reduces EMI
  - Bypassable Input PLL for Parallel Clock Jitter Attenuation
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Generator for BER Testing of the Serial Link
  - Dedicated “Up/Down” GPO for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

***Ordering Information* appears at end of data sheet.**

19-6751; Rev 3; 12/17

maxim integrated™

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF FIGURES (continued)

LIST OF TABLES

Absolute Maximum Ratings (Note 1)

AVDD to EP .....-0.5V to +1.9V
DVDD to EP .....-0.5V to +1.9V
IOVDD to EP .....-0.5V to +3.9V
LMN_ to EP (15mA current limit).....-0.5V to +3.9V
OUT+, OUT- to EP .....-0.5V to +1.9V
All Other Pins to EP .....-0.5V to (V_{IOVDD} + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply.....Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 47.6mW/°C above +70°C).....3809.5mW
Junction Temperature.....+150°C
Storage Temperature..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....21°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, SD, SCK, WS, HIM)							
High-Level Input Voltage	V_{IH1}	(DIN_, PCLKIN, $\overline{PWDN}$, MS/CNTL0, CDS/CNTL3, HIM)		0.65 x V_{IOVDD}			V
		SD, SCK, WS		0.7 x V_{IOVDD}			
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-20		+20	µA
THREE-LEVEL LOGIC INPUTS (CONF0, CONF1, CONF2, CONF3, BWS)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUT (GPO)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA		V_{IOVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA				0.2	V
OUTPUT Short-Circuit Current	I_{OS}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN INPUT/OUTPUT (RX/SDA, TX/SCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL	-110		+5	µA
			$\overline{LFLT}$	-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 6)				10	pF
DIFFERENTIAL SERIAL OUTPUT (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Preemphasis off (Figure 1)		300	400	500	mV
		3.3dB Preemphasis setting (Figure 2)		350		610	
		3.3dB Deemphasis setting (Figure 2)		240		425	
Change in V_{OD} Between Complimentary Output States	DV_{OD}	Preemphasis off, deemphasis only				25	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V
Change in V_{OS} between Complimentary Output States	DV_{OS}					25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V				25	
Magnitude of Differential Output Short Circuit Current	I_{OSD}	V_{OD} = 0V				25	mA
Output Termination Resistance (Internal)	R_O	From OUT+, OUT- to V_{AVDD}		45	54	63	Ω
SINGLE-ENDED SERIAL OUTPUT (OUT+, OUT-)							
Single-Ended Output Voltage	V_{OUT}	Preemphasis off, high drive, Figure 3		375	500	625	mV
		3.3dB preemphasis setting, high drive, (Figure 2)		435		765	
		3.3dB deemphasis setting, high drive, (Figure 2)		300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V		-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V				32	
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}		45	54	63	Ω
REVERSE CONTROL CHANNEL RECEIVER (OUT+, OUT-)							
High Switching Threshold	V_{CHR}	Normal-immunity mode				27	mV
		High-immunity mode				40	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low Switching Threshold	V_{CLR}	Normal-immunity mode		-27			mV
		High-immunity mode		-40			
LINE FAULT DETECTION INPUT (LMN_)							
Short-to-GND Threshold	V_{TG}	Figure 4				0.3	V
Normal Threshold	V_{TN}	Figure 4		0.57		1.07	V
Open Threshold	V_{TO}	Figure 4		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	Figure 4		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	Figure 4		2.47			V
POWER SUPPLY							
Worst-Case Supply Current (Figure 5, Note 7)	I_{WCS}	BWS = low	$f_{PCLKIN\_}$ = 16.6MHz		96	120	mA
			$f_{PCLKIN\_}$ = 33.3MHz		99	125	
			$f_{PCLKIN\_}$ = 66.6MHz		111	140	
			$f_{PCLKIN\_}$ = 104MHz		134	160	
		BWS = mid	$f_{PCLKIN\_}$ = 36.6MHz		102	130	
			$f_{PCLKIN\_}$ = 104MHz		133	165	
Sleep Mode Supply Current	I_{CCS}	Single wake-up receiver enabled			40	170	µA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = GND			5	120	µA
ESD PROTECTION							
OUT+, OUT- (Note 8)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±10			
			Air discharge	±12			
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±10			
			Air discharge	±20			
All Other Pins (Note 9)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF		±4			kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
PARALLEL CLOCK INPUT (PCLKIN)								
Clock Frequency	$f_{PCLKIN\_}$	BWS = low, DRS = '1'			8.33		16.66	MHz
		BWS = low, DRS = '0'			16.66		104	
		BWS = mid, DRS = '1'			18.33		52	
		BWS = mid, DRS = '0'			36.66		104	
		BWS = high, DRS = '1'			6.25		12.5	
		BWS = high, DRS = '0'			12.5		78	
Clock Duty Cycle	DC_	t_{high}/t_T or t_{low}/t_T (Figure 6), (Note 10)			35	50	65	%
Clock Transition Time	t_R, t_F_	(Figure 6), (Note 10)					4	ns
Clock Jitter	t_J	3.12Gbps bit rate, 300kHz sinusoidal jitter					800	ps_{P-P}
I²C/UART PORT TIMING								
I²C/UART Bit Rate					9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD			20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD			20		150	ns
I²C TIMING (Figure 7)								
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range (I2CMSTBT = 010, I2CSLVSH = 10)			9.6		100	kHz
		Mid f_{SCL} range (I2CMSTBT 101, I2CSLVSH = 01)			> 100		400	kHz
		High f_{SCL} range (I2CMSTBT = 111, I2CSLVSH = 00)			> 400		1000	kHz
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High	V_{IOVDD} = 1.7V to < 3V (Note 11)	0.6			
				V_{IOVDD} = 3.0V to 3.6V	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7			µs
			Mid		0.6			
			High		0.26			

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range (Note 10)	Low		0			µs
			Mid		0			
			High		0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low		250			ns
			Mid		100			
			High		50			
Setup Time for Stop Condition	$t_{SU:STO}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High		0.5			
Data Valid Time (Note 12)	$t_{VD:DAT}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 13)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Data Valid Acknowledge Time (Note 12)	$t_{VD:ACK}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 14)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low				50	ns
			Mid				50	
			High				50	
Capacitive Load Each Bus Line	C_B	(Note 6)					100	pF
SWITCHING CHARACTERISTICS (Note 10)								
Differential Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps				90	150	ps
Total Serial Output Jitter (Differential Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled, Figure 8				0.25		UI

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.7V to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C.) (Note 3)

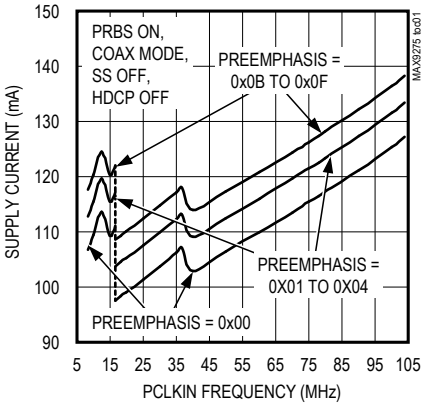
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deterministic Serial Output Jitter (Differential Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 8)			0.15		UI
Total Serial Output Jitter (Single-ended Output)	t_{TSOJ1}	3.12Gbps PRBS signal, measured at V_O/2, preemphasis disabled (Figure 3)			0.25		UI
Deterministic Serial Output Jitter (Single-Ended Output)	t_{DSOJ2}	3.12Gbps PRBS signal, measured at V_O/2, preemphasis disabled (Figure 3)			0.15		UI
Parallel Data Input Setup Time	t_{SET}	(Figure 9)		2			ns
Parallel Data Input Hold Time	t_{HOLD}	(Figure 9)		1			ns
GPI to GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO, (Figure 10)				350	µs
Serializer Delay (Note 15)	t_{SD}	(Figure 11)	Spread spectrum enabled			5440	Bits
			Spread spectrum disabled			1920	
Link Start Time	t_{LOCK}	(Figure 12)				3.5	ms
Power-Up Time	t_{PU}	(Figure 13)				8	ms
I²S/TDM INPUT TIMING							
WS Frequency	f_{WS}	(See Table 3)		8		192	kHz
Sample Word Length	n_{WS}	(See Table 3)		8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$		(8 x 8) x 2		(192 x 32) x 8	kHz
SCK Clock High Time	t_{HC}	V_{SCK} RV_{IH}, $t_{SCK} = 1/f_{SCK}$ (Note 6)		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	V_{SCK} RV_{IL}, $t_{SCK} = 1/f_{SCK}$ (Note 6)		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}	(Note 6) (Figure 14)		2			ns
SD, WS Hold Time	t_{HOLD}	(Note 6) (Figure 14)		2			ns

Note 3: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range and are guaranteed by design and characterization, unless otherwise noted.
Note 4: To provide a midlevel, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.
Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.
Note 6: Not production tested. Guaranteed by design
Note 7: HDCP not enabled (MAX9279 only). See Table 21 for additional supply current when HDCP is enabled.
Note 8: Specified pin to ground.
Note 9: Specified pin to all supply/ground.
Note 10: Not production tested. Guaranteed by design and characterization.
Note 11: The I²C bus standard t_{LOW} min = 0.5µs.
Note 12: I²C valid times apply only when the device is operating as a local-side device.
Note 13: The I²C bus standard $t_{VD:DAT}$ max = 0.45µs.
Note 14: The I²C bus standard $t_{VD:ACK}$ max = 0.45µs.
Note 15: Measured in serial link bit times. Bit time = 1/ (30 x f_{PCLKIN}) for BWS = '0' or open. Bit time = 1/ (40 x f_{PCLKIN}) for BWS = '1'.

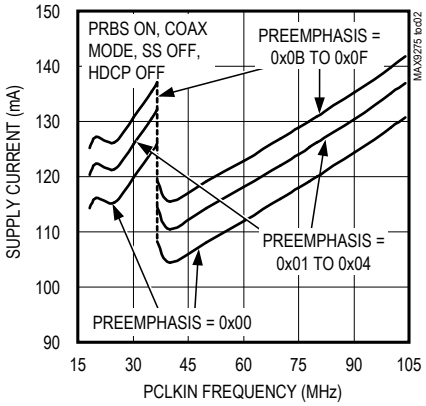
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

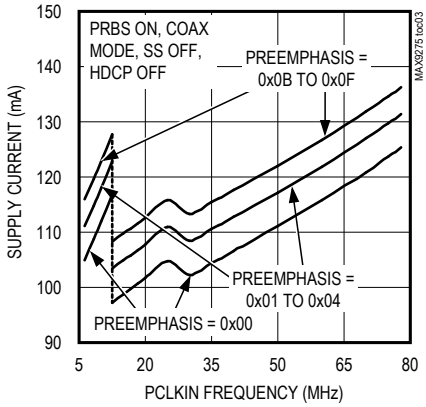
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = LOW)



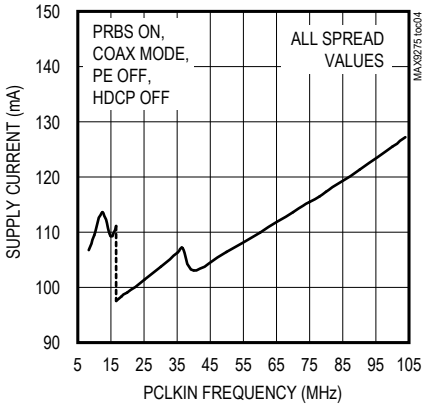
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = OPEN)



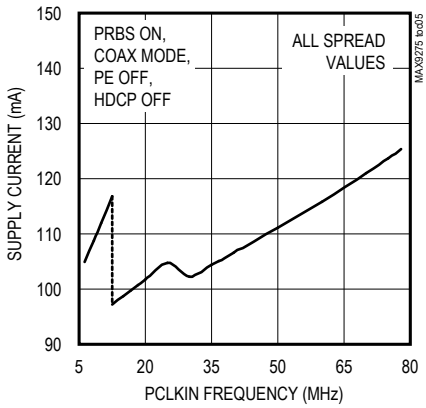
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = HIGH)



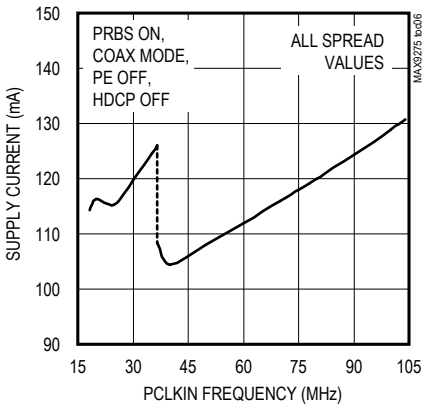
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = LOW)



SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = HIGH)



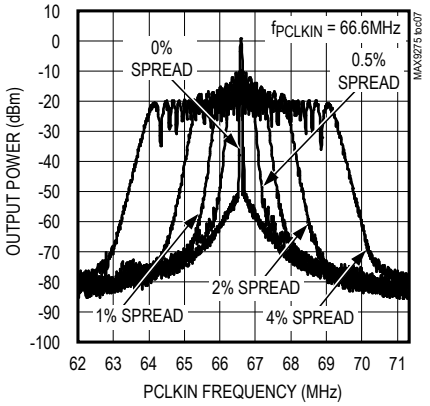
SUPPLY CURRENT vs. PCLKIN FREQUENCY (BWS = OPEN)



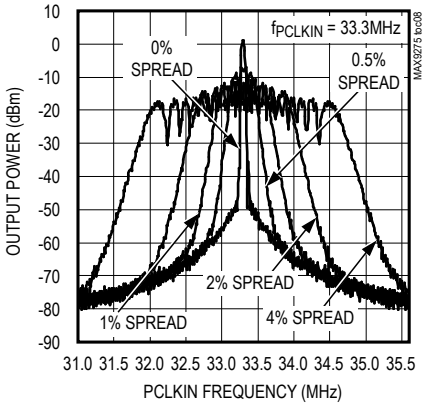
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

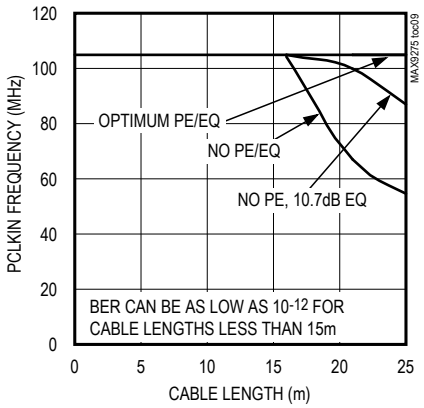
OUTPUT SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)



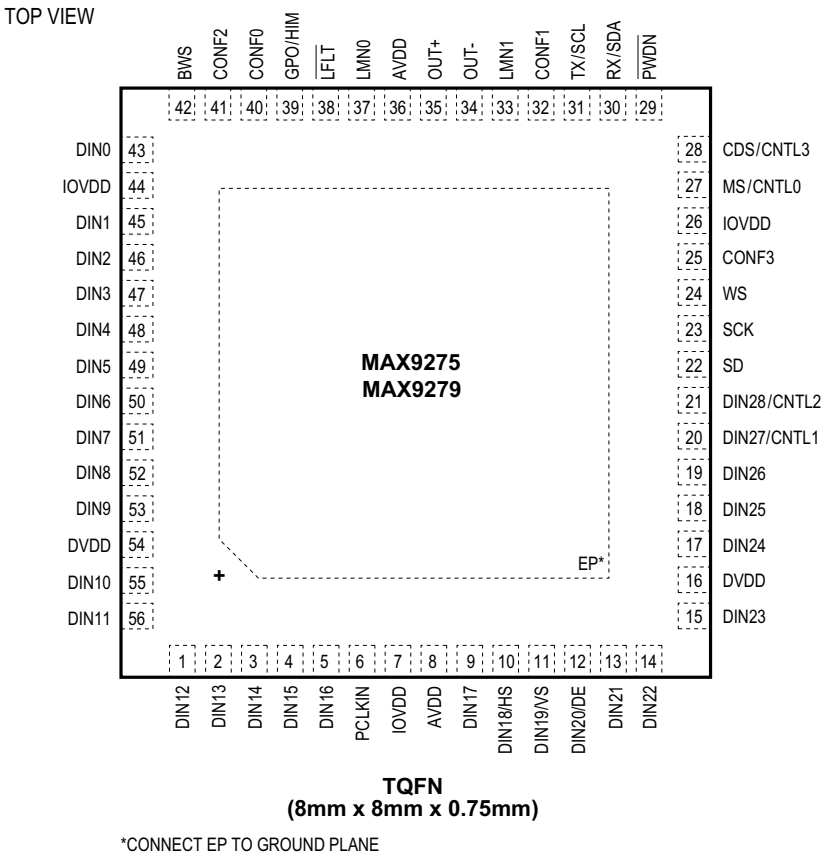
OUTPUT SPECTRUM vs. PCLKIN FREQUENCY (VARIOUS SPREAD)



MAXIMUM PCLKIN FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



TQFN
(8mm x 8mm x 0.75mm)

*CONNECT EP TO GROUND PLANE

Pin Description

PIN	NAME	FUNCTION
1–5, 9, 43, 45–53, 55, 56	DIN[17:0]	Parallel Data Inputs with Internal Pulldown to EP. Encrypted when HDCP is enabled (MAX9279 only).
6	PCLKIN	Parallel Clock Input with Internal Pulldown to EP. Latches parallel data inputs and provides the PLL reference clock.
7, 26, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
8, 36	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
10	DIN18/HS	Parallel Data Input/Horizontal Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Horizontal sync input when HDCP is enabled (MAX9279 only) or when in high-bandwidth mode (BWS = open).

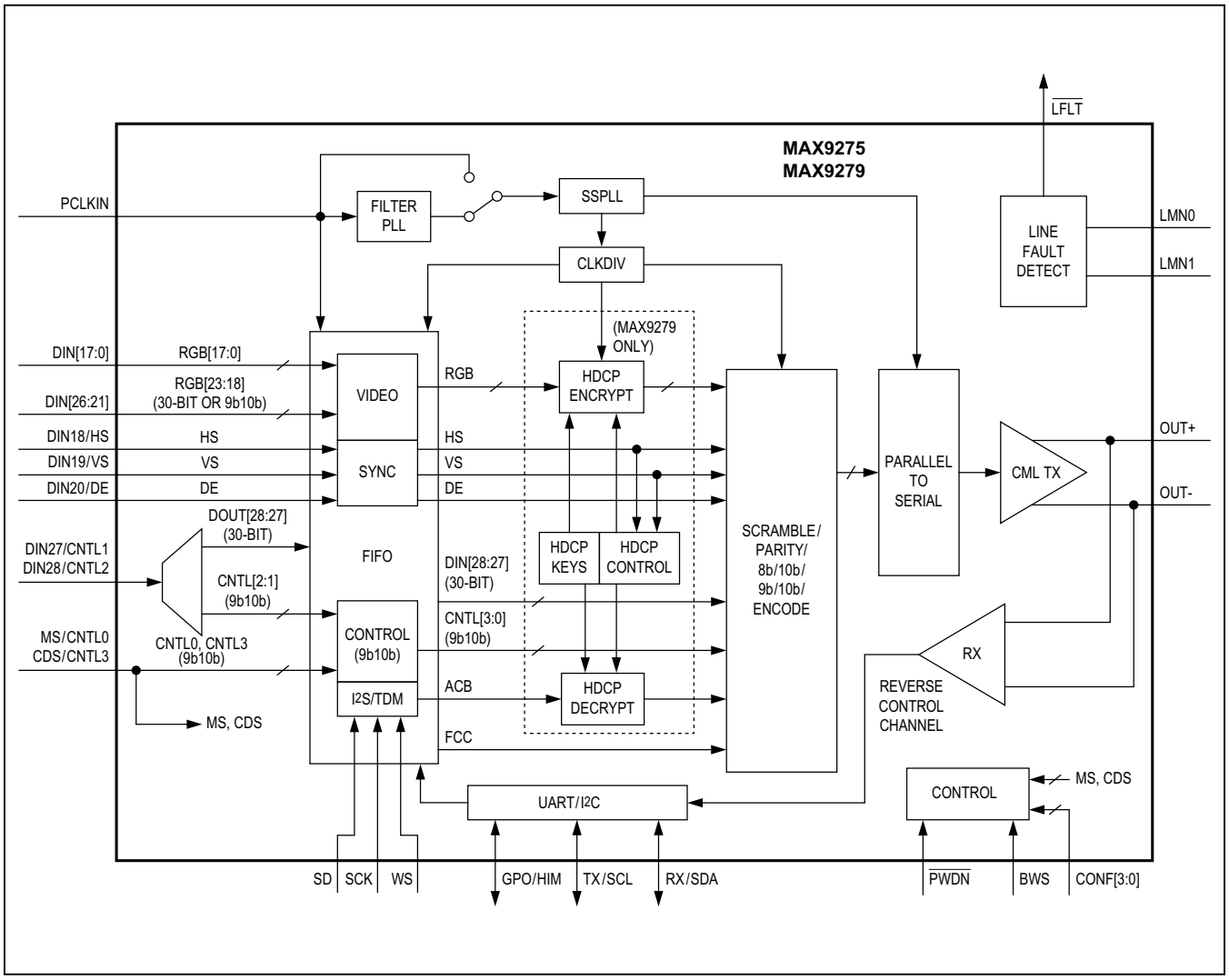
Pin Description (continued)

PIN	NAME	FUNCTION
11	DIN19/VS	Parallel Data Input/Vertical Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Vertical sync input when HDCP is enabled (MAX9279 only) or when in high-bandwidth mode (BWS = open).
12	DIN20/DE	Parallel Data Input/Device Enable with Internal Pulldown to EP. Defaults to parallel data input on power-up. Device enable input when HDCP is enabled (MAX9279 only) or when in high-bandwidth mode (BWS = open).
13–15, 17–19	DIN[26:21]	Parallel Data Inputs with Internal Pulldown to EP. Encrypted when HDCP is enabled (MAX9279 only). DIN[26:21] used only in 32-bit and high-bandwidth modes (BWS = high or open).
16, 54	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
20	DIN27/CNTL1	Parallel Data/Auxiliary Control Signal Input with Internal Pulldown to EP. DIN27 used only in 32-bit mode (BWS = high). DIN27 not encrypted when HDCP is enabled (MAX9279 only). CNTL1 used only in high-bandwidth mode (BWS = open). CNTL1 not encrypted when HDCP is enabled (MAX9279 only).
21	DIN28/CNTL2	Parallel Data/Auxiliary Control Signal Input with Internal Pulldown to EP. DIN28 used only in 32-bit mode (BWS = high). DIN28 not encrypted when HDCP is enabled (MAX9279 only). CNTL2 used only in high-bandwidth mode (BWS = open). CNTL2 not encrypted when HDCP is enabled (MAX9279 only).
22	SD	I^2S/TDM Serial-Data Input with Internal Pulldown to EP. Disable I^2S/TDM encoding to use SD as an additional control/data input latched on the selected edge of PCLKIN. Encrypted when HDCP is enabled.
23	SCK	I^2S/TDM Serial-Clock Input with Internal Pulldown to EP
24	WS	I^2S/TDM Word-Select Input with Internal Pulldown to EP
25	CONF3	Three-Level Configuration Input. See Table 11 for details. Use 6kΩ (max) for pullup to IOVDD/pulldown to GND.
27	MS/CNTL0	Mode Select/Auxiliary Control Signal Input with Internal Pulldown to EP. Function is determined by the MSCNTL0 register bit and defaults to MS on power-up. MS (MSCNTL0 = 0): Set MS = low, to select base mode. Set MS = high to select the bypass mode. CNTL0 (MSCNTL0 = 1): Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9279 only).
28	CDS/CNTL3	Control Direction Selection/Auxiliary Control Signal Input with Internal Pulldown to EP. Function is determined by the CDSCNTL3 register bit and defaults to CDS on power-up. CDS (CDSCNTL3 = 0): Control link direct selection input with internal pulldown to EP. Set CDS = low when the control channel master µC is connected at the serializer. Set CDS = high when the control channel master µC is connected at the deserializer. CNTL3 (CDSCNTL3 = 1): Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9279 only).

Pin Description (continued)

PIN	NAME	FUNCTION
29	$\overline{\text{PWDN}}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{\text{PWDN}}$ low to enter power-down mode to reduce power consumption.
30	RX/SDA	UART Receive/I²C Serial Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 10). RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I²C master/slave.
31	TX/SCL	UART Transmit/I²C Serial Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of CONF[1:0] at power-up (Table 10). TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I²C master/slave.
32	CONF1	Three-Level Configuration Input. See Table 10 for details. Use 6kΩ (max) for pullup to IOVDD/pulldown to GND.
33	LMN1	Line-Fault Monitor Input 1 (see Figure 4)
34	OUT-	Inverting CML Coax/Twisted-Pair Serial Output
35	OUT+	Noninverting CML Coax/Twisted-Pair Serial Output
37	LMN0	Line-Fault Monitor Input 0 (see Figure 4)
38	$\overline{\text{LFLT}}$	Active-Low Open-Drain Line-Fault Output. $\overline{\text{LFLT}}$ has a 60kΩ internal pullup to IOVDD. $\overline{\text{LFLT}}$ = low indicates a line fault. $\overline{\text{LFLT}}$ is output high when $\overline{\text{PWDN}}$ = low.
39	GPO/HIM	General-Purpose Output/High-Immunity Mode Input. Functions as HIM input with internal pulldown to EP at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to GPO output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low) and is active high. Connect HIM to IOVDD with a 30kΩ or less pullup resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO: Output follows the state of the GPI (or INT) input on the deserializer. GPO is low after power-up or when $\overline{\text{PWDN}}$ is low.
40	CONF0	Three-Level Configuration Input. The state of CONF0 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 10 for details. Use 6kΩ (max) for pullup to IOVDD/pulldown to GND.
41	CONF2	Three-Level Configuration Input. The state of CONF2 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 11 for details. Use 6kΩ (max) for pullup to IOVDD/pulldown to GND.
42	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low with 6kΩ (max) pulldown for 24 bit mode. Set BWS = 6kΩ (max) pullup to IOVDD high for 32-bit mode. Set BWS = open for high-bandwidth mode.
—	EP	Exposed Pad. EP is internally connected to device ground. **must** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



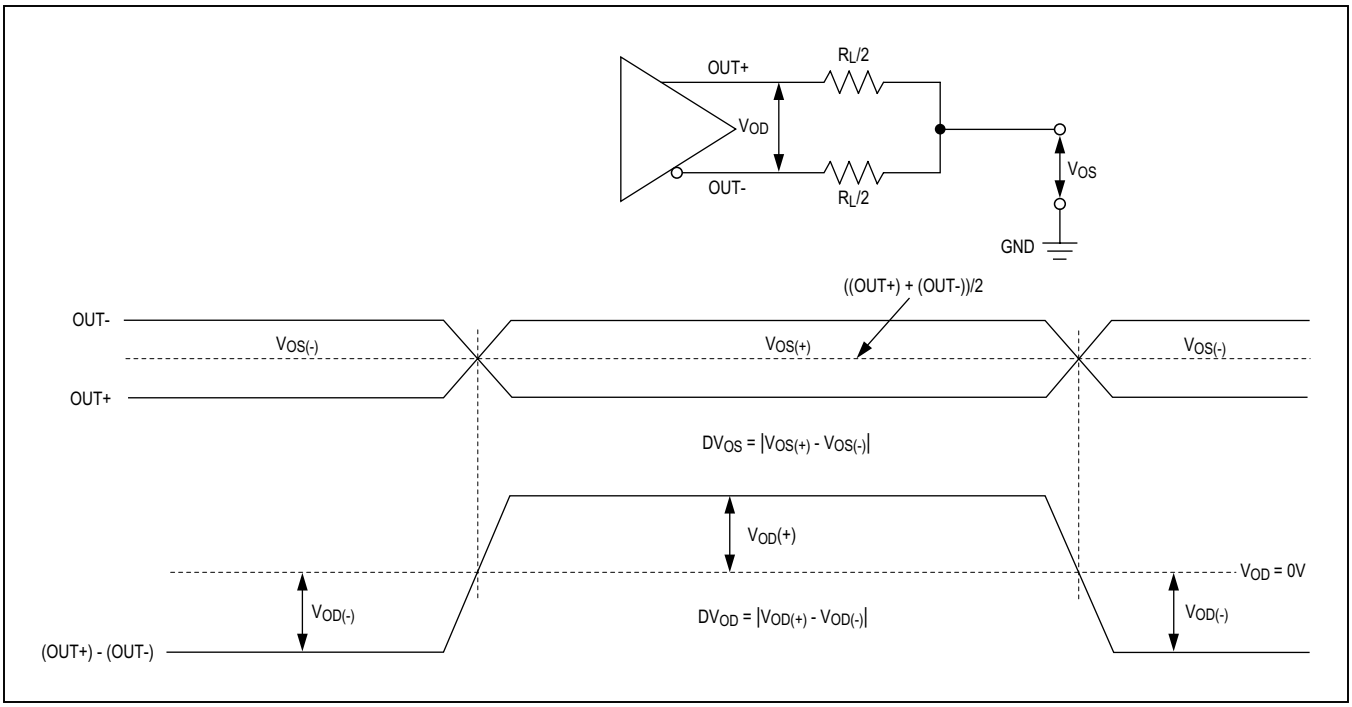


Figure 1. Serial-Output Parameters

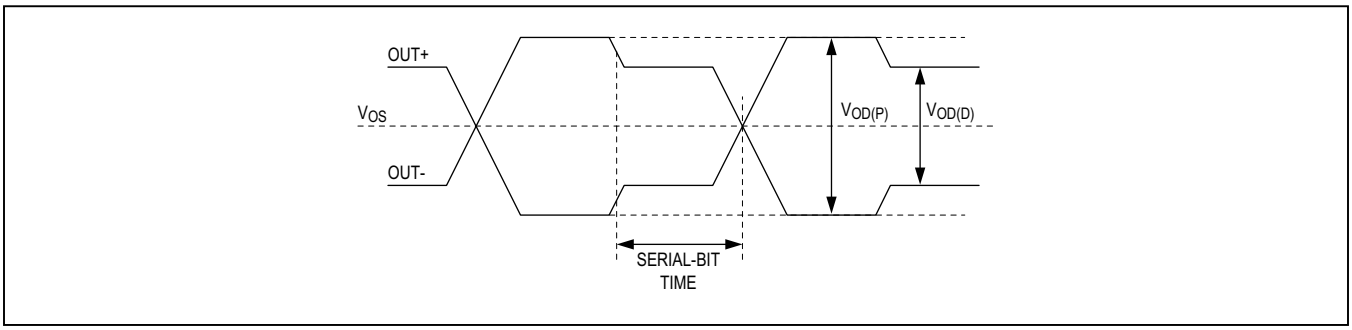


Figure 2. Output Waveforms at OUT+, OUT-

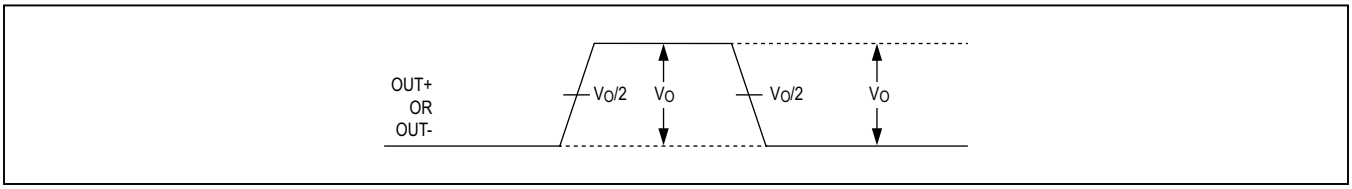


Figure 3. Single-Ended Output Template

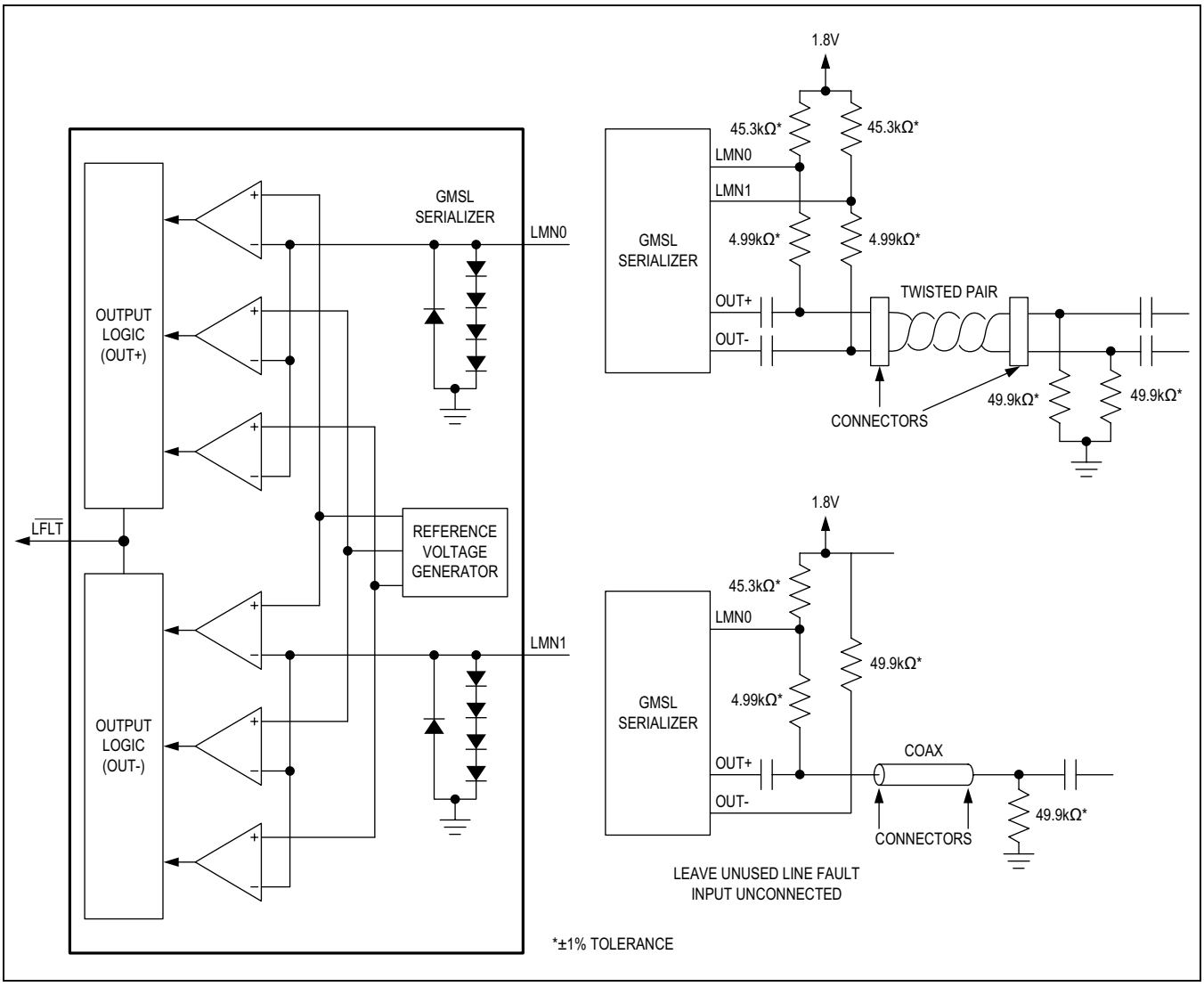


Figure 4. Line Fault Detector Circuit

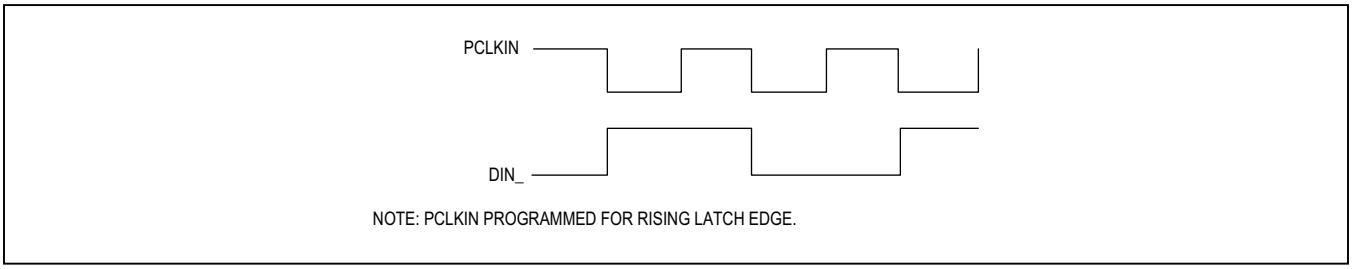


Figure 5. Worst-Case Pattern Input

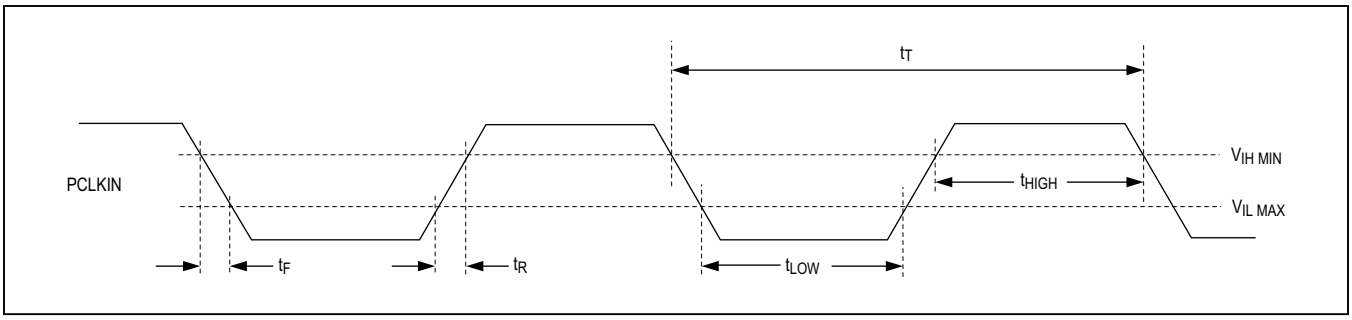


Figure 6. Parallel Clock Input Requirements

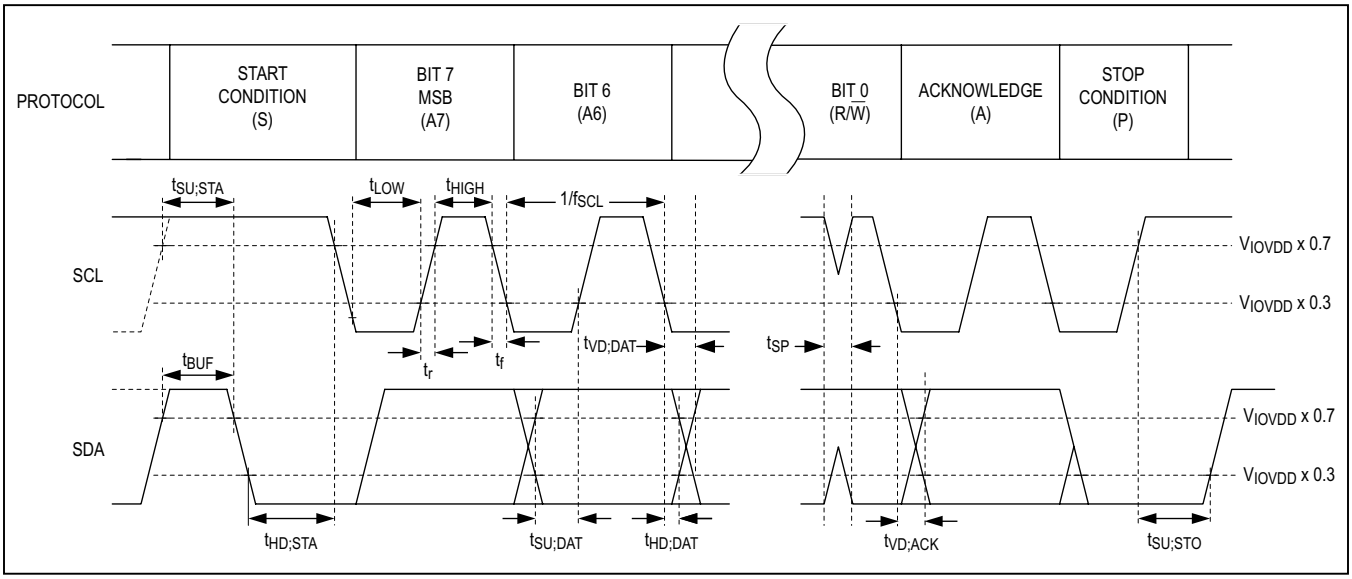


Figure 7. I²C Timing Parameters

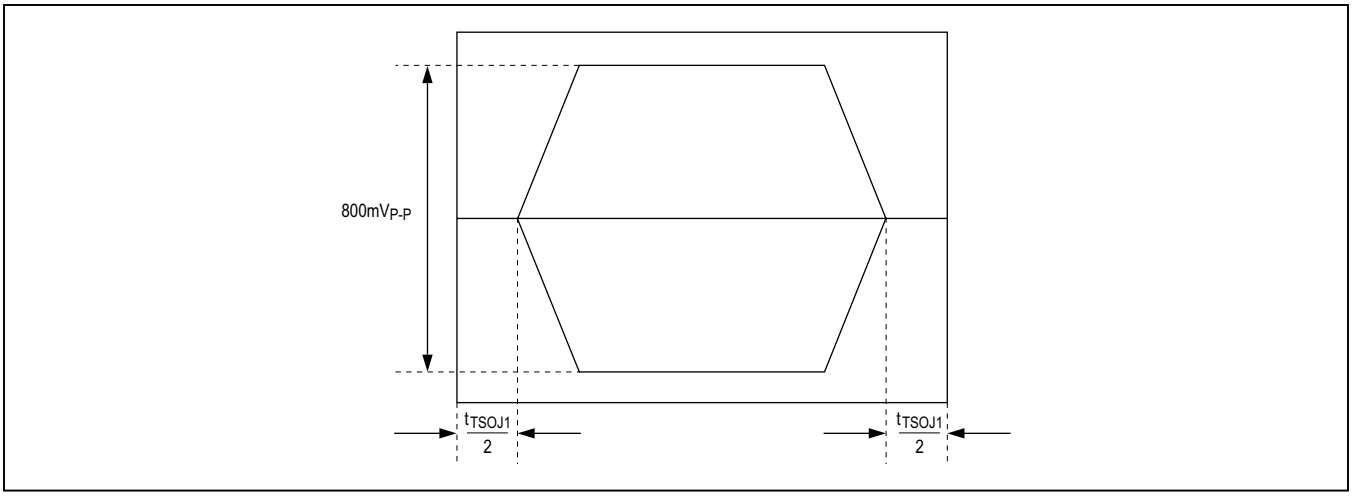


Figure 8. Differential Output Template

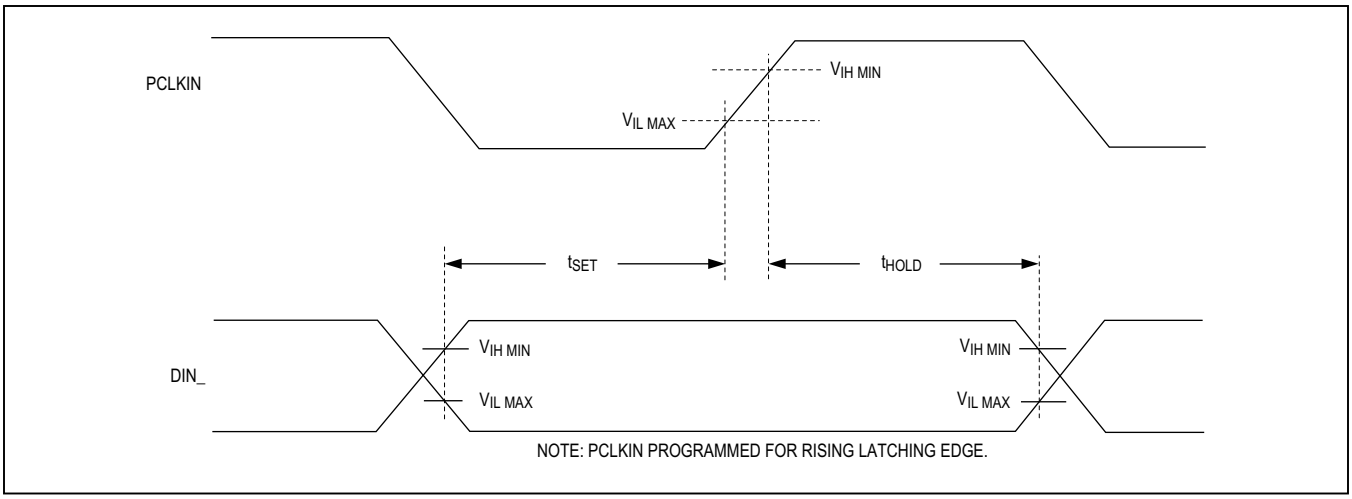


Figure 9. Input Setup and Hold Times

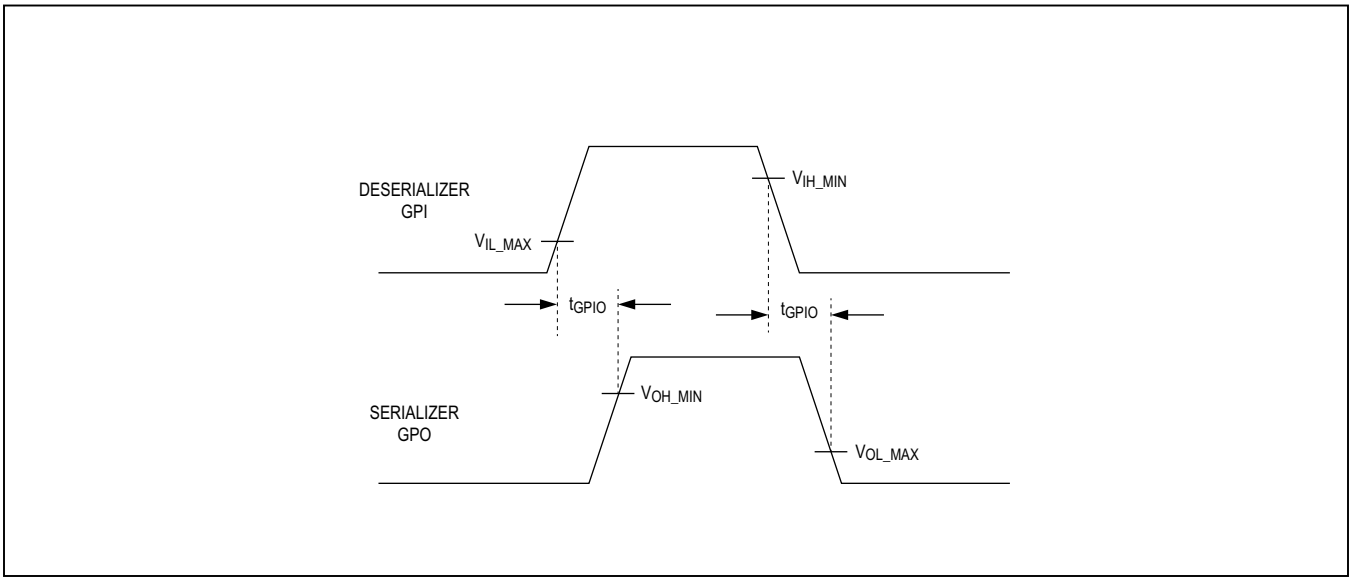


Figure 10. GPI-to-GPO Delay

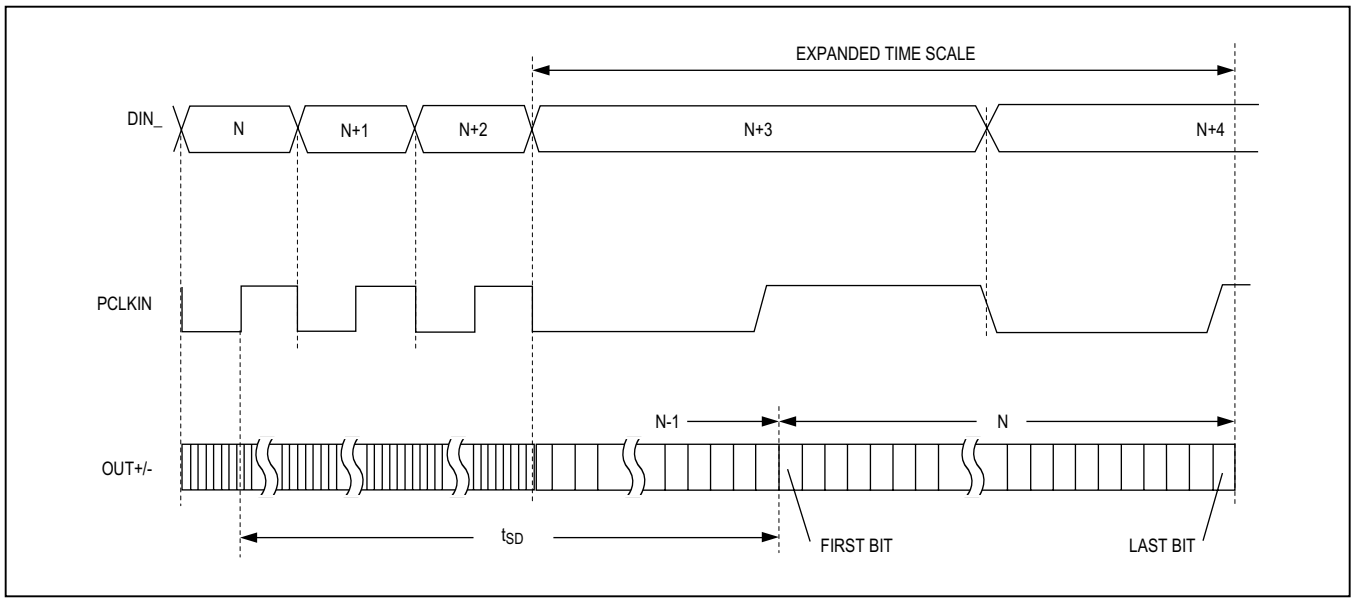


Figure 11. Serializer Delay

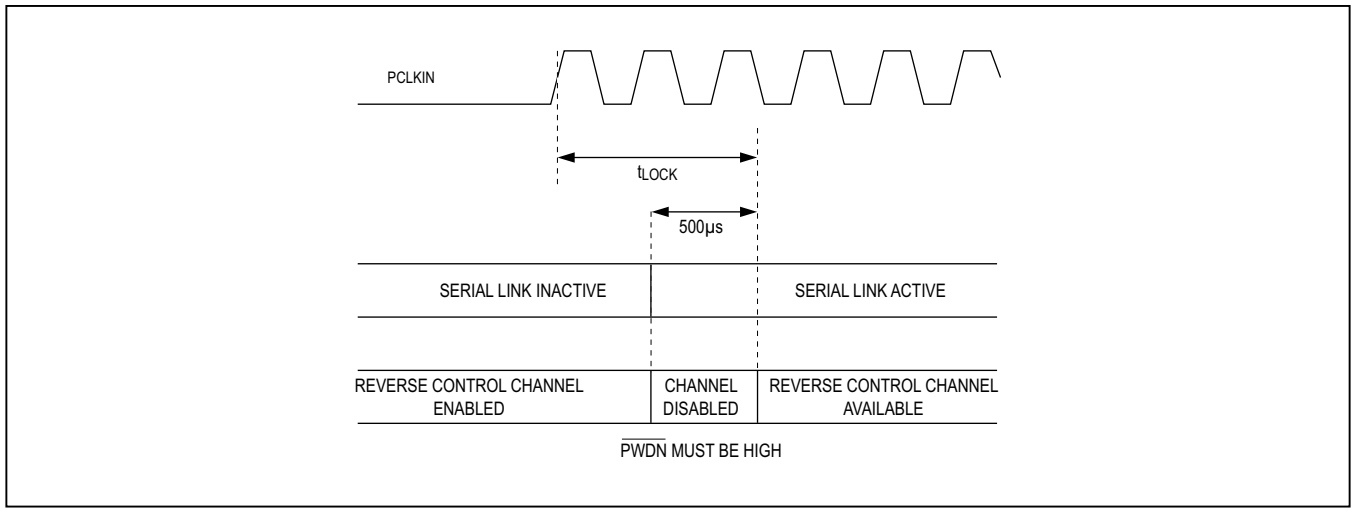


Figure 12. Link Startup Time

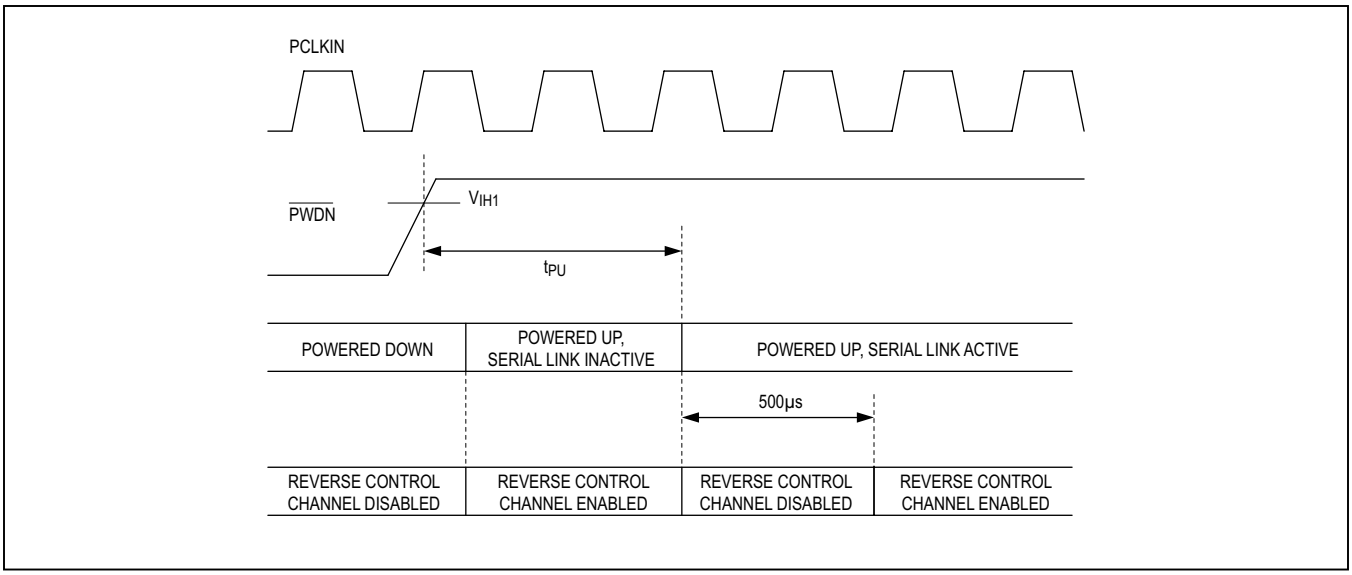


Figure 13. Power-Up Delay

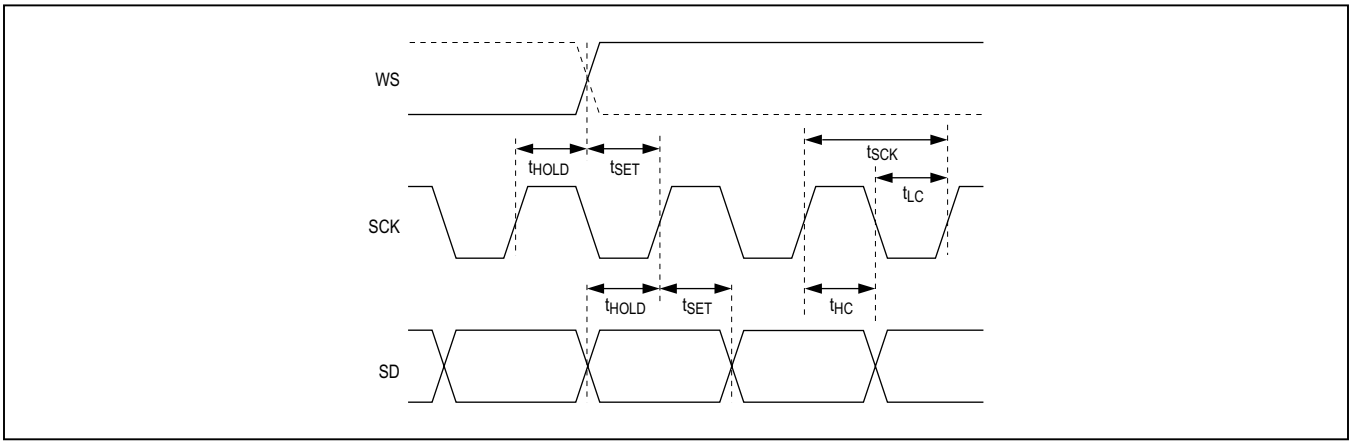


Figure 14. Input I²S Timing Parameters

Detailed Description

The MAX9275/MAX9279 serializers, when paired with the MAX9276/MAX9280 deserializers, provides the full set of operating features, but is backward compatible with the MAX9249–MAX9270 family of Gigabit Multimedia Serial Link (GMSL) devices, and have basic functionality when paired with any GMSL device. The MAX9279 has High-Bandwidth Digital Content Protection (HDCP) while the MAX9275 does not.

The serializer has a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operates up to a maximum output clock of 104MHz in 24-bit mode and 27-bit high-bandwidth mode, or 78MHz in 32-bit mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Output pre/deemphasis, combined with GMSL deserializer equalization, extends the cable length and enhances link reliability.

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9279 only). The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I²C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the serial output. The serial output complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the serializers and are programmed using the control channel in base mode. The MAX9275/MAX9279 holds its own device address and the device address of the deserializer it is paired with. Similarly, the deserializer holds its own device address and the address of the MAX9275/MAX9279. Whenever a device address is changed, be sure to write the new address to both devices. The default device address of the serializer is 0x80. Registers 0x00 and 0x01 in both devices hold the device addresses.

Table 1. Input Map

SIGNAL	INPUT PIN	MODE		
		24-BIT MODE (BWS = LOW)	HIGH-BANDWIDTH MODE (BWS = MID)	32-BIT MODE (BWS = HIGH)
R[5:0]	DIN[5:0]	Used	Used	Used
G[5:0]	DIN[11:6]	Used	Used	Used
B[5:0]	DIN[17:12]	Used	Used	Used
HS, VS, DE	DIN18/HS, DIN19/VS, DIN20/DE	Used**	Used**	Used**
R[7:6]	DIN[22:21]	Not used	Used	Used
G[7:6]	DIN[24:23]	Not used	Used	Used
B[7:6]	DIN[26:25]	Not used	Used	Used
CNTL[2:1]	DIN[28:27]/CNTL[2:1]	Not used	Used*,**	Used**
CNTL3, CNTL0	CDS/CNTL3, MS/CNTL0	Not used	Used*,**	Not used
I²S/TDM	WS, SCK, SD	Used	Used	Used
AUX SIGNAL		Used	Used	Used

**See the High-Bandwidth Mode section for details on timing requirements.*

***Not encrypted when HDCP is enabled (MAX9279 only).*