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MAX9276/MAX9280

3.12Gbps GMSL Deserializers for Coax or STP Input and Parallel Output

General Description

The MAX9276/MAX9280 gigabit multimedia serial link (GMSL) deserializers receive data from a GMSL serializer over 50Ω coax or 100Ω shielded twisted pair (STP) cable and output deserialized data on the LVCMOS outputs.

The MAX9280 has HDCP content protection but otherwise is the same as the MAX9276. The deserializers pair with any GMSL serializer capable of coax output including the MAX9293 HDMI/MHL serializer. When programmed for STP input they are backward compatible with any GMSL serializer.

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

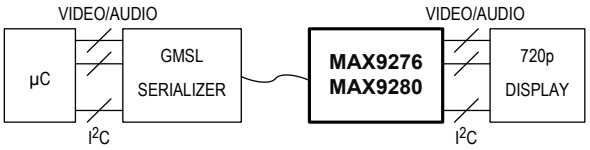
The embedded control channel operates at 9.6kbps to 1Mbps in UART-UART and UART-I²C modes, and up to 1Mbps in I²C-I²C mode. Using the control channel, a µC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9280). Two GPIO ports are included, allowing display power-up and switching of the backlight among other uses. A continuously-sampled GPI input supports touch-screen controller interrupt requests in display applications.

For use with longer cables, the deserializers have a programmable cable equalizer. Programmable spread spectrum is available on the parallel output. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 3.0V to 3.6V and the I/O supply is 1.7V to 3.6V.

The devices are in lead-free, 56-lead, 8mm x 8mm TQFN and QFND packages with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems



Benefits and Features

- Ideal for High-Definition Video Applications
  - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - 104MHz High-Bandwidth Mode Supports 1920x720p/60Hz Display With 24-Bit Color
  - Equalization Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate And 32-Bit Sample Depth For 7.1 Channel HD Audio
  - Audio Clock from Audio Source or Audio Sink
  - Color Lookup-Table for Gamma Correction
  - CNTL[3:0] Control Outputs
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 6.25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock Stretch Capability
- Reduces EMI and Shielding Requirements
  - Programmable Spread Spectrum Reduces EMI
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Tester for BER Testing of the Serial Link
  - Programmable Choice of 8 Default Device Addresses
  - Two Dedicated GPIO Ports
  - Dedicated “Up/Down” GPI for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

Ordering Information ***appears at end of data sheet.***

19-6623; Rev 1; 11/15

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Absolute Maximum Ratings (Note 1)

AVDD to EP ..... -0.5V to +3.9V
DVDD to EP ..... -0.5V to +3.9V
IOVDD to EP ..... -0.5V to +3.9V
IN+, IN- to EP ..... -0.5V to +1.9V
All Other Pins to EP ..... -0.5V to (V_{IOVDD} + 0.5V)
IN+, IN- Short Circuit to Ground or Supply ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
QFND (derate 42.7mW/°C above +70°C) 3418mW
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 21°C/W

QFND
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.6°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 23.4°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (ADD_, HIM, I2CSEL, GPI, $\overline{PWDN}$, MS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-10		+20	µA
THREE-LEVEL LOGIC INPUTS (BWS, CX/TP)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		10	µA
Input Current	I_{IN}			-150		150	µA
SINGLE-ENDED OUTPUTS (WS, SCK, SD, DOUT_, CNTL_, INTOUT, PCLKOUT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = '0'	V_{IOVDD} - 0.3			V
			DCS = '1'	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = '0'			0.3	V
			DCS = '1'			0.2	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
OUTPUT Short-Circuit Current	I_{OS}	DOUT_	V_O = 0V, DCS = '0'	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
				V_{IOVDD} = 1.7V to 1.9V	3	7	13	
			V_O = 0V, DCS = '1'	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
				V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT	V_O = 0V, DCS = '0'	V_{IOVDD} = 3.0V to 3.6V	15	33	50	
				V_{IOVDD} = 1.7V to 1.9V	5	10	17	
			V_O = 0V, DCS = '1'	V_{IOVDD} = 3.0V to 3.6V	30	54	97	
				V_{IOVDD} = 1.7V to 1.9V	9	16	32	
OPEN-DRAIN INPUT/OUTPUT (GPIO0, GPIO1, RX/SDA, TX/SCL, $\overline{ERR}$, LOCK)								
High-Level Input Voltage	V_{IH2}				0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}						0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL		-100		+5	µA
			LOCK, $\overline{ERR}$, GPIO_		-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V				0.4	V
			V_{IOVDD} = 3.0V to 3.6V				0.3	
Input Capacitance	C_{IN}	Each pin (Note 6)					10	pF
OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)								
Differential High Output Peak Voltage (V_{IN}+) - (V_{IN}-)	V_{RODH}	Forward channel disabled, Figure 1	Legacy reverse control channel mode		30		60	mV
			High immunity mode		50		100	
Differential Low Output Peak Voltage (V_{IN}+) - (V_{IN}-)	V_{RODL}	Forward channel disabled, Figure 1	Legacy reverse control channel mode		-60		-30	mV
			High immunity mode		-100		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled	Legacy reverse control channel mode		30		60	mV
			High immunity mode		50		100	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled	Legacy reverse control channel mode		-60		-30	mV
			High immunity mode		-100		-50	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (IN+, IN-)								
Differential High Input Threshold (Peak) Voltage (V_{IN}+) - (V_{IN}-)	$V_{IDH(P)}$	Figure 2	Activity detector medium Threshold, (0x0B D[6:5] = 01)				60	mV
			Activity detector low Threshold, (0x0B D[6:5] = 00)				47.5	
Differential Low Input Threshold (Peak) Voltage (V_{IN}+) - (V_{IN}-)	$V_{IDL(P)}$	Figure 2	Activity detector medium Threshold, (0x0B D[6:5] = 01)		-60			mV
			Activity detector medium Threshold, (0x0B D[6:5] = 00)		-47.5			
Input Common-Mode Voltage ((V_{IN}+) + (V_{IN}-))/2	V_{CMR}				1	1.3	1.6	V
Differential Input Resistance (Internal)	R_{IN}				80	100	130	Ω
SINGLE-ENDED INPUTS (IN+, IN-)								
Single-Ended High Input Threshold (Peak) Voltage	$V_{ISH(P)}$	Figure 2a	Activity detector medium threshold, (0x0B D[6:5] = 01)				43	mV
			Activity detector low threshold, (0x0B D[6:5] = 00)				33	
Single-Ended Low Input Threshold (Peak) Voltage	$V_{ISL(P)}$	Figure 2a	Activity detector medium threshold, (0x0B D[6:5] = 01)		-43			mV
			Activity detector medium threshold, (0x0B D[6:5] = 00)		-33			
Input Resistance (Internal)	R_I				40	50	65	Ω
POWER SUPPLY								
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 3)	I_{WCS}	BWS = low, $f_{PCLKOUT}$ = 16.6MHz	2% spread active	C_L = 5pF		131	164	mA
				C_L = 10pF		136	169	
			Spread spectrum disabled	C_L = 5pF		122	153	
				C_L = 10pF		127	158	
		BWS = low, $f_{PCLKOUT}$ = 33.3MHz	2% spread active	C_L = 5pF		144	179	
				C_L = 10pF		153	189	
			Spread spectrum disabled	C_L = 5pF		133	167	
				C_L = 10pF		142	177	
		BWS = low, $f_{PCLKOUT}$ = 66.6MHz	2% spread active	C_L = 5pF		175	216	
				C_L = 10pF		190	233	
			Spread spectrum disabled	C_L = 5pF		159	197	
				C_L = 10pF		174	214	

DC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Total Supply Current (AVDD + DVDD + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 3)	I_{WCS}	BWS = low, $f_{PCLKOUT}$ = 104MHz	2% spread active	C_L = 5pF		212	255	mA
				C_L = 10pF		234	278	
			Spread spectrum disabled	C_L = 5pF		190	228	
				C_L = 10pF		212	251	
		BWS = mid, $f_{PCLKOUT}$ = 36.6MHz	2% spread active	C_L = 5pF		154	191	
				C_L = 10pF		164	203	
			Spread spectrum disabled	C_L = 5pF		143	177	
				C_L = 10pF		154	189	
		BWS = mid, $f_{PCLKOUT}$ = 104MHz	2% spread active	C_L = 5pF		231	277	
				C_L = 10pF		257	305	
			Spread spectrum disabled	C_L = 5pF		209	249	
				C_L = 10pF		234	277	
Sleep Mode Supply Current	I_{CCS}					70	265	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = GND				20	195	µA
ESD PROTECTION								
IN+, IN- (Note 8)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF				±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge			±10		
			Air discharge			±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge			±10		
			Air discharge			±20		
All Other Pins (Note 9)	V_{ESD}	Human body model, R_D = 1.5kΩ, C_S = 100pF				±4		kV

AC Electrical Characteristics

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)								
Clock Frequency	$f_{PCLKOUT}$	BWS = low, DRS = '1'			8.33		16.66	MHz
		BWS = low, DRS = '0'			16.66		104	
		BWS = mid, DRS = '1'			18.33		36.66	
		BWS = mid, DRS = '0'			36.66		104	
		BWS = high, DRS = '1'			6.25		12.5	
		BWS = high, DRS = '0'			12.5		78	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Note 6)			40	50	60	%
Clock Jitter	t_J	Period jitter, peak-to-peak, spread off, 3.12Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$ (Note 6)				0.05		UI
I^2C/UART PORT TIMING								
I^2C/UART Bit Rate					9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}			20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}			20		150	ns
I^2C TIMING (Figure 4)								
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)			9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)			> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)			> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High	V_{IOVDD} = 1.7V to < 3V (Note 11)	0.6			
				V_{IOVDD} = 3.0V to 3.6V	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low		4.7			µs
			Mid		0.6			
			High		0.26			

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low		0			µs
			Mid		0			
			High		0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low		250			µs
			Mid		100			
			High		50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low		4.0			µs
			Mid		0.6			
			High		0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low		4.7			µs
			Mid		1.3			
			High		0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 12)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low				3.45	µs
			Mid				0.9	
			High	V_{IOVDD} = 1.7V to < 3V (Note 13)			0.55	
				V_{IOVDD} = 3.0V to 3.6V			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low				50	ns
			Mid				50	
			High				50	
Capacitive Load Each Bus Line	C_b						100	pF
SWITCHING CHARACTERISTICS								
PCLKOUT Rise-and-Fall Time, Figure 5	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V (Note 6)	DCS = '1', C_L = 10pF		0.4		2.2	ns
			DCS = '0', C_L = 5pF		0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V (Note 1)	DCS = '1', C_L = 10pF		0.25		1.8	
			DCS = '0', C_L = 5pF		0.3		2.0	
Parallel Data Rise-and-Fall Time, Figure 6	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V (Note 1)	DCS = '1', C_L = 10pF		0.5		3.1	ns
			DCS = '0', C_L = 5pF		0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V (Note 6)	DCS = '1', C_L = 10pF		0.3		2.2	
			DCS = '0', C_L = 5pF		0.4		2.4	

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Deserializer Delay	t_{SD}	(Note 14) Figure 7	Spread spectrum enabled			6960	Bits
			Spread spectrum disabled			2160	
Reverse Control Channel Output Rise Time	t_R	No forward channel data transmission, Figure 1		180		400	ns
Reverse Control Channel Output Fall Time	t_F	No forward channel data transmission, Figure 1		180		400	ns
GPI to GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included), Figure 8				350	µs
Lock Time	t_{LOCK}	Figure 9	Spread spectrum enabled			3	ms
			Spread spectrum disabled			2	
Power-Up Time	t_{PU}	Figure 10				8	ms
I^2S/TDM OUTPUT TIMING (Note 6)							
WS Jitter	tj_{WS}	t_{WS} = 1/f_{WS}, (cycle-to-cycle), rising-to-falling edge or falling-to-rising edge	f_{WS} = 48kHz or 44.1kHz		1.2e-3 x t_{WS}	1.5e-3 x t_{WS}	ns
			f_{WS} = 96kHz		1.6e-3 x t_{WS}	2e-3 x t_{WS}	
			f_{WS} = 192kHz		1.6e-3 x t_{WS}	2e-3 x t_{WS}	
SCK Jitter (2-Channel I^2S)	tj_{SCK1}	t_{SCK} = 1/f_{SCK}, (cycle-to-cycle), rising-to-rising edge	n_{SCK} = 16 bits, f_{SCK} = 48kHz or 44.1kHz		13e-3 x t_{SCK}	16e-3 x t_{SCK}	ns
			n_{SCK} = 24 bits, f_{WS} = 96kHz		39e-3 x t_{SCK}	48e-3 x t_{SCK}	
			n_{SCK} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
SCK Jitter (8-Channel TDM)	tj_{SCK2}	t_{SCK} = 1/f_{SCK}, (cycle-to-cycle), rising-to-rising edge	n_{SCK} = 16 bits, f_{WS} = 48kHz or 44.1kHz		52e-3 x t_{SCK}	64e-3 x t_{SCK}	ns
			n_{SCK} = 24 bits, f_{WS} = 96kHz		156e-3 x t_{SCK}	192e-3 x t_{SCK}	
			n_{SCK} = 32 bits, f_{WS} = 192kHz		0.4 x t_{SCK}	0.52 x t_{SCK}	
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	C_L = 10pF, DCS = 1	0.3		3.1	ns
			C_L = 5pF, DCS = 0	0.4		3.8	

AC Electrical Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C.) (Note 10)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SD, WS Valid Time Before SCK (2-Channel I²S)	t_{DVB1}	t_{SCK} = 1/f_{SCK}, Figure 11	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (2-Channel I²S)	t_{DVA1}	t_{SCK} = 1/f_{SCK}, Figure 11	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time Before SCK (8-Channel TDM)	t_{DVB2}	t_{SCK} = 1/f_{SCK}, Figure 11	0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (8-Channel TDM)	t_{DVA2}	t_{SCK} = 1/f_{SCK}, Figure 11	0.20 x t_{SCK}	0.5 x t_{SCK}		ns

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a mid level, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 5: I_{IN} MIN due to voltage drop across the internal pullup resistor.

Note 6: Not production tested. Guaranteed by design.

Note 7: HDCP not enabled (MAX9280 only). IOVDD current is not production tested. See Table 23 for additional supply current when HDCP is enabled

Note 8: Specified pin to ground.

Note 9: Specified pin to all supply/ground.

Note 10: Not production tested, guaranteed by bench characterization.

Note 11: The I²C bus standard t_{LOW} (min) = 0.5µs.

Note 12: The I²C bus standard $t_{VD:DAT}$ (max) = 0.45µs.

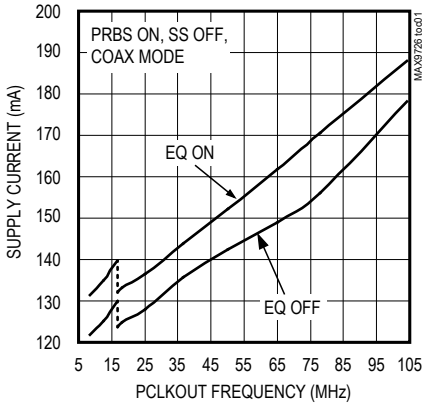
Note 13: The I²C bus standard $t_{VD:ACK}$ (max) = 0.45µs.

Note 14: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = '0' or open. Bit time = 1/(40 x f_{PCLKIN}) for BWS = '1'.

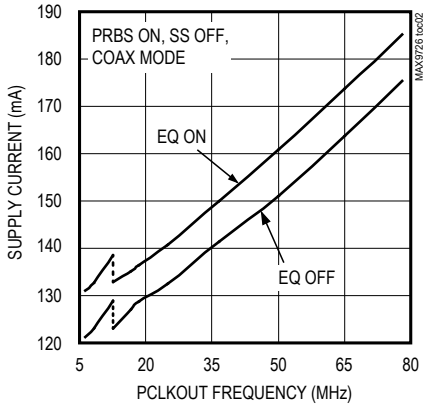
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

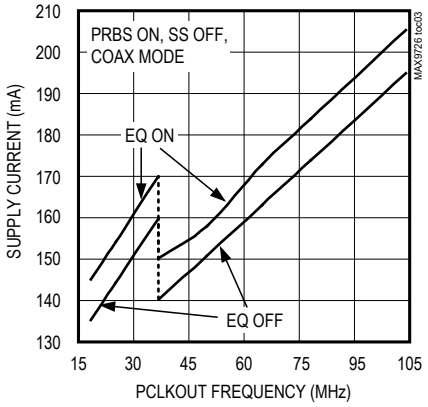
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



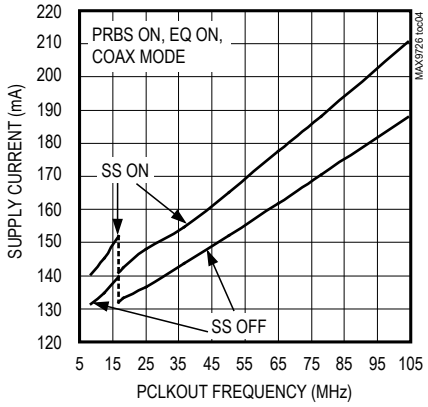
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



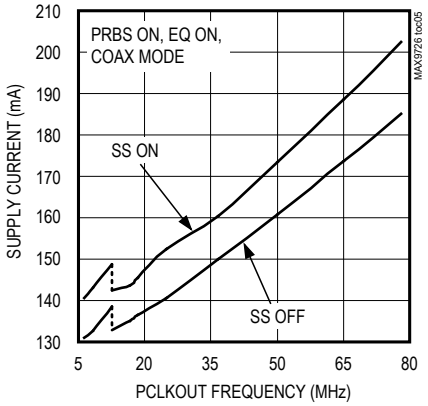
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = OPEN)



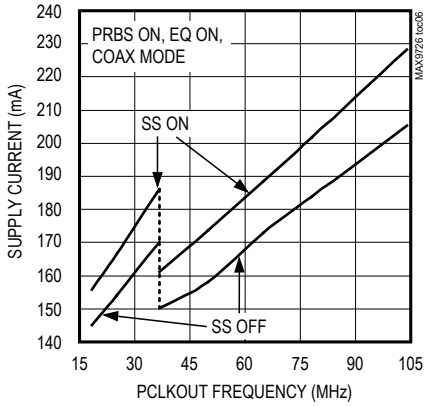
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 0)



SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = 1)



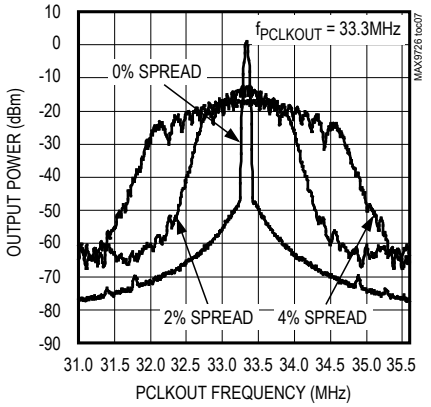
SUPPLY CURRENT vs. PCLKOUT FREQUENCY (BWS = OPEN)



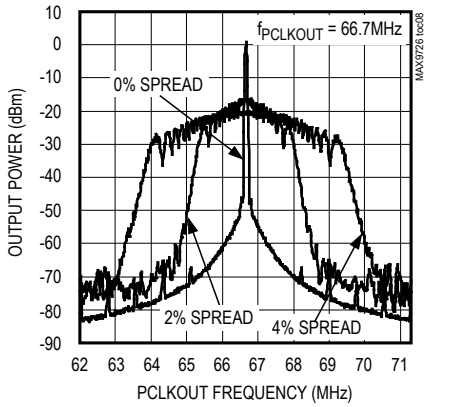
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

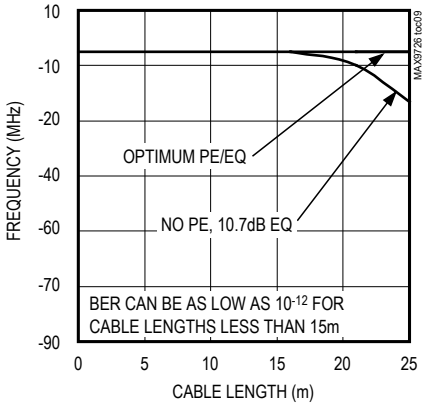
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



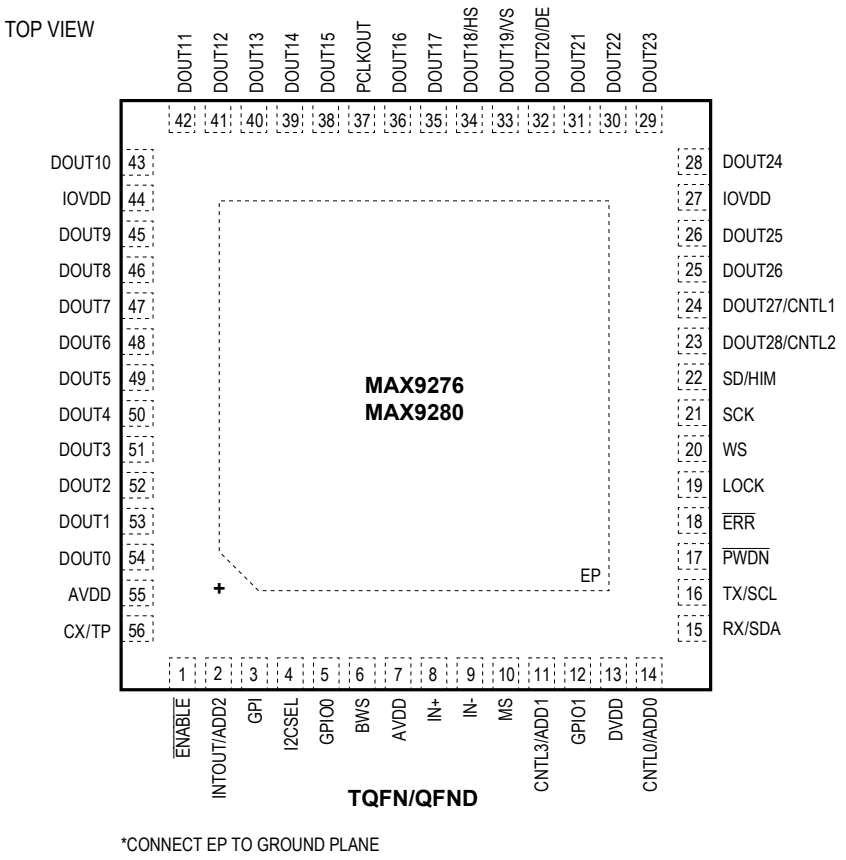
OUTPUT POWER SPECTRUM vs. PCLKOUT FREQUENCY (VARIOUS SPREAD)



MAXIMUM PCLKOUT FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{ENABLE}}$	Active-Low Parallel Output-Enable Input With Internal Pulldown to EP. Set $\overline{\text{ENABLE}}$ = low to enable PCLKOUT DOUT_ and CNTL_ outputs. Set $\overline{\text{ENABLE}}$ = high to put PCLKOUT, DOUT_ and CNTL_ into high impedance.
2	INTOUT/ADD2	A/V Status Register Interrupt Output/Address Selection Input With Internal Pulldown to EP. Functions as ADD2 input at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low), and switches to INTOUT output automatically after power-up. ADD2: Bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1. Connect INTOUT/ADD2 to IOVDD with a 30kΩ resistor to set high or leave open to set low. INTOUT: Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
3	GPI	General-Purpose Input With Internal Pulldown to EP. The serializer GPO (or INT) output follows GPI.
4	I2CSEL	I^2C Select. Control channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I^2C interface. Set I2CSEL = low to select UART interface.
5	GPIO0	Open-Drain, General-Purpose Input/Output with Internal 60kΩ Pullup to IOVDD

Pin Description (continued)

PIN	NAME	FUNCTION
6	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low for 24 bit mode. Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode.
7, 55	AVDD	3.3V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
8	IN+	Noninverting Coax/Twisted-Pair Serial Input
9	IN-	Inverting Coax/Twisted-Pair Serial Input
10	MS	Mode Select with Internal Pulldown to EP. Set MS = low, to select base mode. Set MS = high to select the bypass mode.
11	CNTL3/ADD1	Auxiliary Control Signal Output/Address Selection Input With Internal Pulldown to EP. Functions as ADD1 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL3 output automatically after power-up. ADD1: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect CNTL3/ADD1 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL3: Used only in high-bandwidth mode (BWS = open). CNTL3 not encrypted when HDCP is enabled (MAX9280 only).
12	GPIO1	Open-Drain, General-Purpose Input/Output With Internal 60kΩ Pullup to IOVDD
13	DVDD	3.3V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
14	CNTL0/ADD0	Auxiliary Control Signal Output/Address Selection Input With Internal Pulldown to EP. Functions as ADD0 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL0 output automatically after power-up. ADD0: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect CNTL0/ADD0 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL0: Used only in high-bandwidth mode (BWS = open). CNTL0 not encrypted when HDCP is enabled (MAX9280 only).
15	RX/SDA	UART Receive/I^2C Serial Data Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I^2C Master/Slave.
16	TX/SCL	UART Transmit/I^2C Serial Clock Input/Output with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I^2C Master/Slave.
17	$\overline{PWDN}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
18	$\overline{ERR}$	Error Output. Open-drain data error detection and/or correction indication output with internal 30kΩ pullup to IOVDD. $\overline{ERR}$ is high when $\overline{PWDN}$ is low
19	LOCK	Open-Drain Lock Output with Internal 30kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when $\overline{PWDN}$ = low.

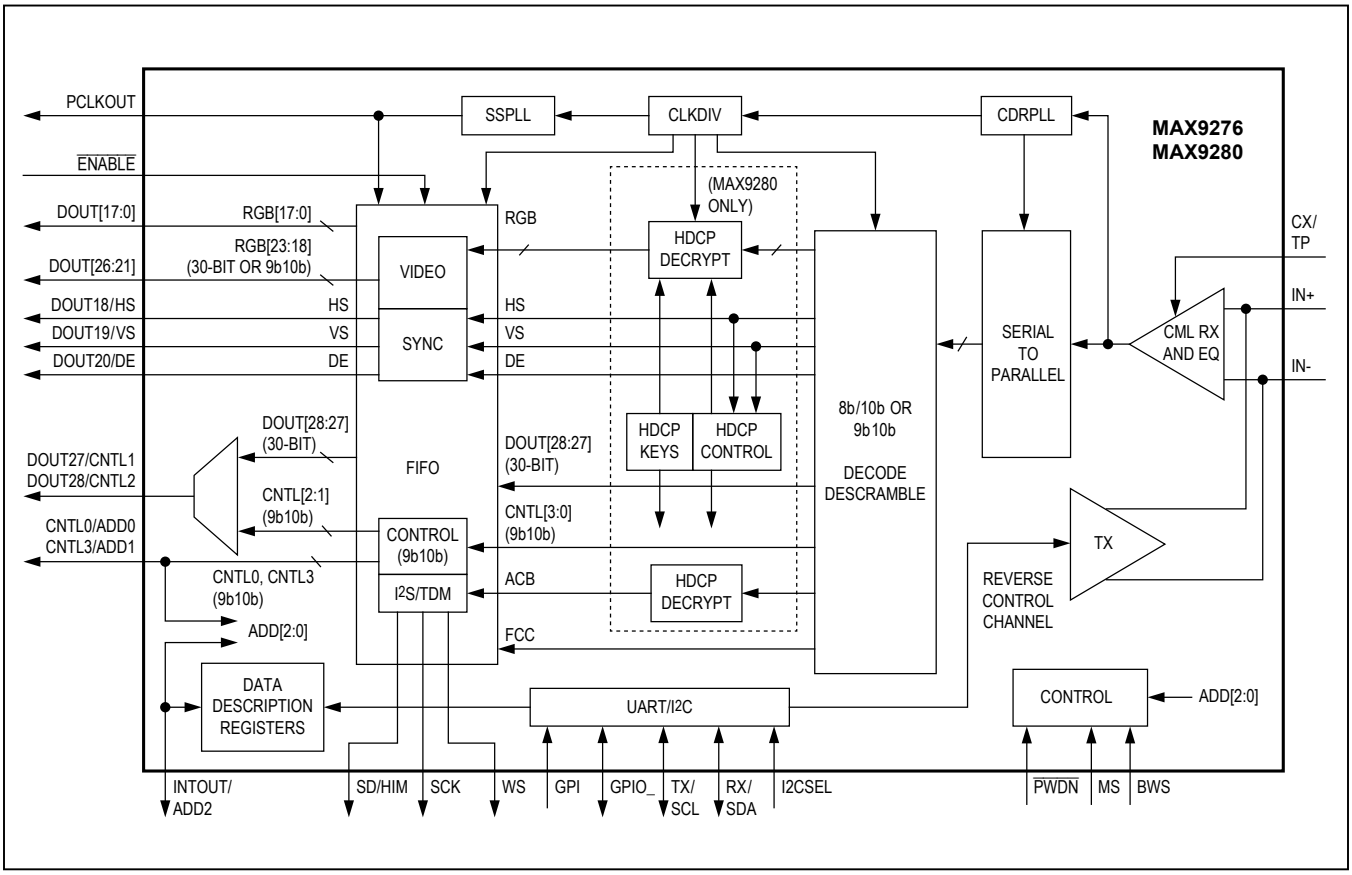
Pin Description (continued)

PIN	NAME	FUNCTION
20	WS	I²S/TDM Word-Select Input/Output. Powers up as an I²S output (deserializer provided clock). Set AUDIOMODE bit = '1' to change WS to an input with internal pulldown to GND and supply WS externally (system provided clock).
21	SCK	I²S/TDM Serial-Clock Input/Output. Powers up as an I²S output (deserializer provided clock). Set AUDIOMODE bit = '1' to change SCK to an input with internal pulldown to GND and supply WS externally (system provided clock).
22	SD/HIM	I²S/TDM Serial-Data Output/High-Immunity Mode Input. Functions as HIM input with internal pulldown to EP at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to SD output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low) and is active-high. Connect SD/HIM to IOVDD with a 30kΩ resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. SD: Disable I²S/TDM encoding to serial data to use SD as an additional control/data output valid on the selected edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280 only).
23	DOUT28/CNTL2	Parallel Data/Auxiliary Control Signal Output Valid on the Selected Edge of PCLKOUT. DOUT28/CNTL2 remains high impedance in 24-bit mode (BWS = low) DOUT28 used only in 32-bit mode (BWS = high). DOUT28 not encrypted when HDCP is enabled (MAX9280 only). CNTL2 used only in high-bandwidth mode (BWS = open). CNTL2 not encrypted when HDCP is enabled (MAX9280 only).
24	DOUT27/CNTL1	Parallel Data/Auxiliary Control Signal Output Valid on the Selected Edge of PCLKOUT. DOUT27/CNTL1 remains high impedance in 24-bit mode (BWS = low) DOUT27 used only in 32-bit mode (BWS = high). DOUT27 not encrypted when HDCP is enabled (MAX9280 only). CNTL1 used only in high-bandwidth mode (BWS = open). CNTL1 not encrypted when HDCP is enabled (MAX9280 only)
25, 26, 28–31	DOUT[26:21]	Parallel Data Outputs Valid on the Selected Edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280 only). DOUT[26:21] used only in 32-bit and high-bandwidth modes (BWS = high or open). DOUT[26:21] remains high-impedance in 24-bit mode.
27, 44	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
32	DOUT20/DE	Parallel Data/Device Enable Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Device enable output when HDCP is enabled (MAX9280 only) or when in high-bandwidth mode (BWS = open).
33	DOUT19/VS	Parallel Data/Vertical Sync Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Vertical sync output when HDCP is enabled (MAX9280 only) or when in high-bandwidth mode (BWS = open).
34	DOUT18/HS	Parallel Data/Horizontal Sync Output Valid on the Selected Edge of PCLKOUT. Defaults to parallel data output on power-up. Horizontal sync output when HDCP is enabled (MAX9280 only) or when in high-bandwidth mode (BWS = open).

Pin Description (continued)

PIN	NAME	FUNCTION
35, 36, 38–43, 45–54	DOUT[17:0]	Parallel Data Outputs Valid on the Selected Edge of PCLKOUT. Encrypted when HDCP is enabled (MAX9280 only)
37	PCLKOUT	Parallel Clock Output Used for DOUT[28:0]. Latches parallel data into the input of another device.
56	CX/TP	Three-Level Coax/Twisted Pair Select Input. See Table 10 for function.
—	EP	Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



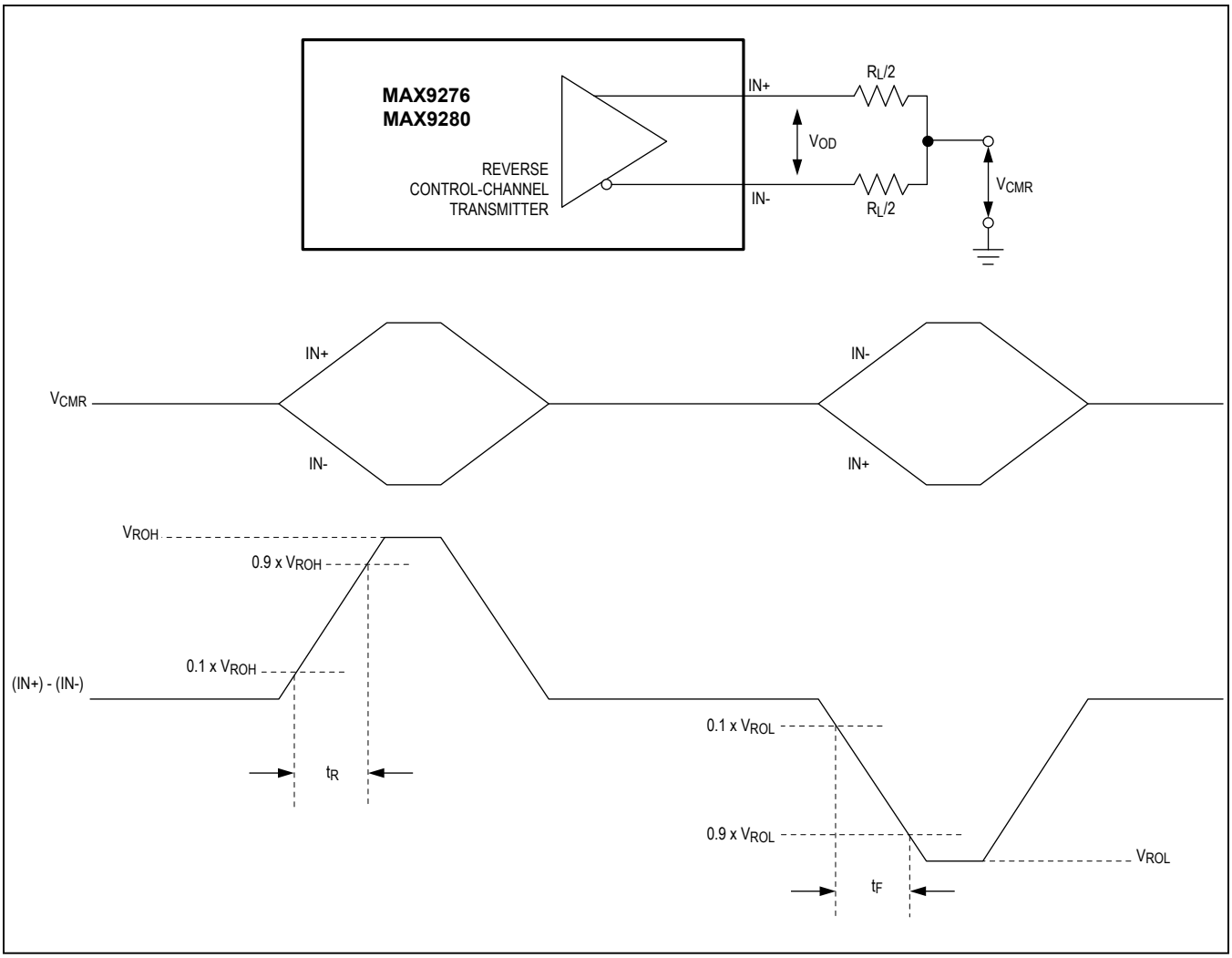


Figure 1. Reverse Control Channel Output Parameters

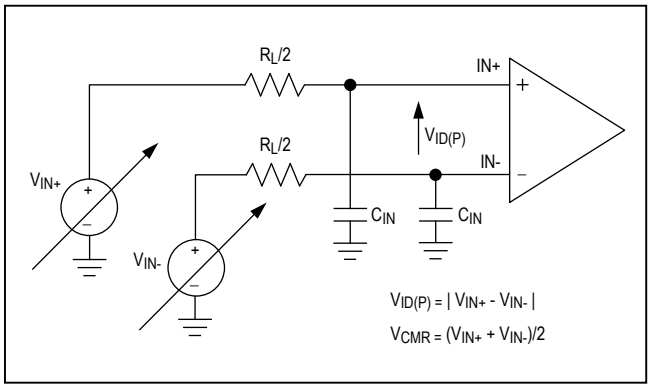


Figure 2. Test Circuit for Differential Input Measurement

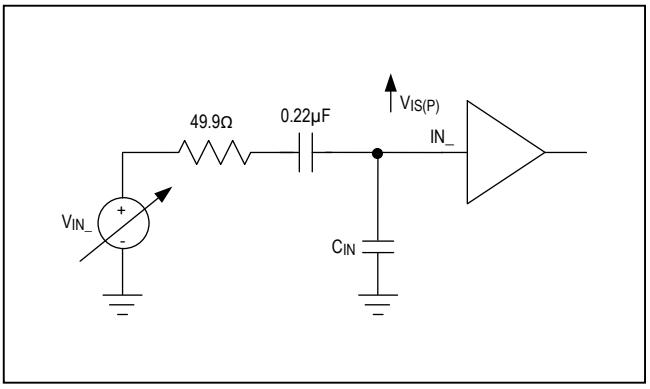


Figure 2a. Test Circuit for Single-Ended Input Measurement

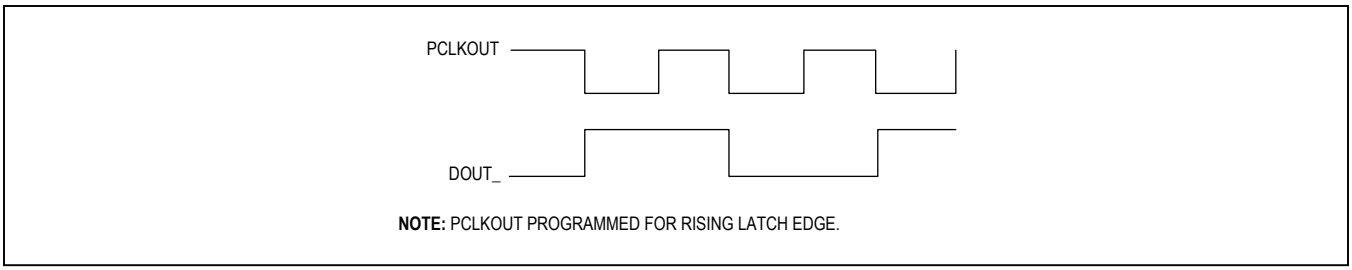


Figure 3. Worst-Case Pattern Output

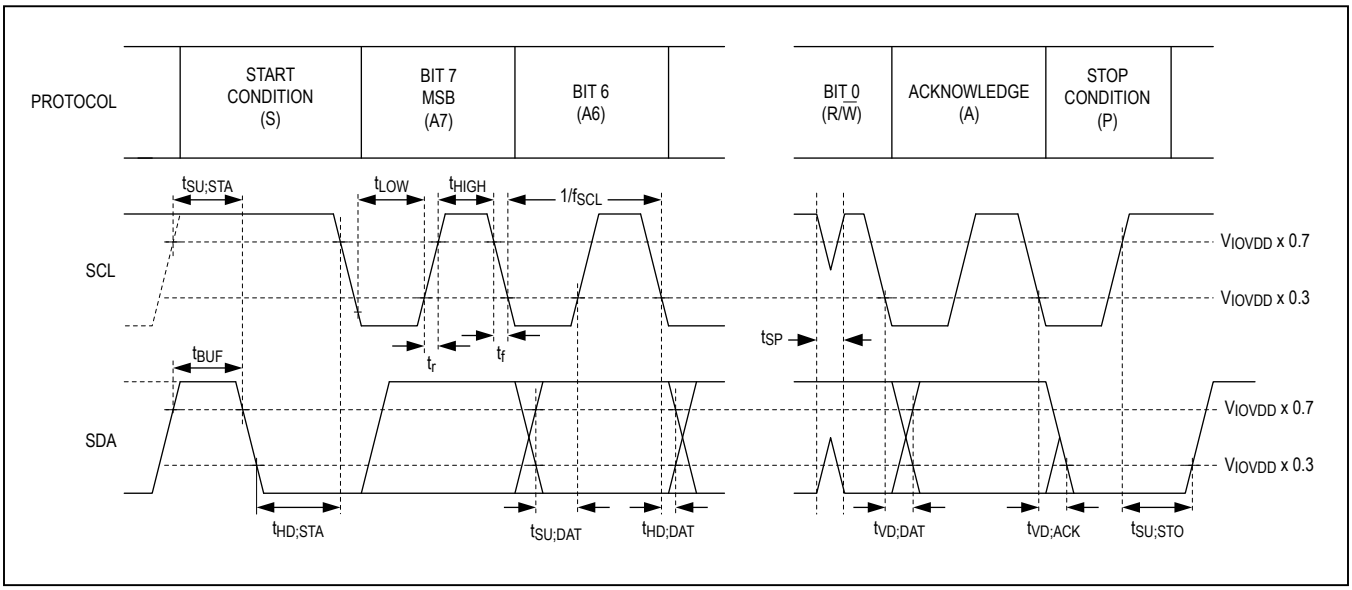


Figure 4. I²C Timing Parameters

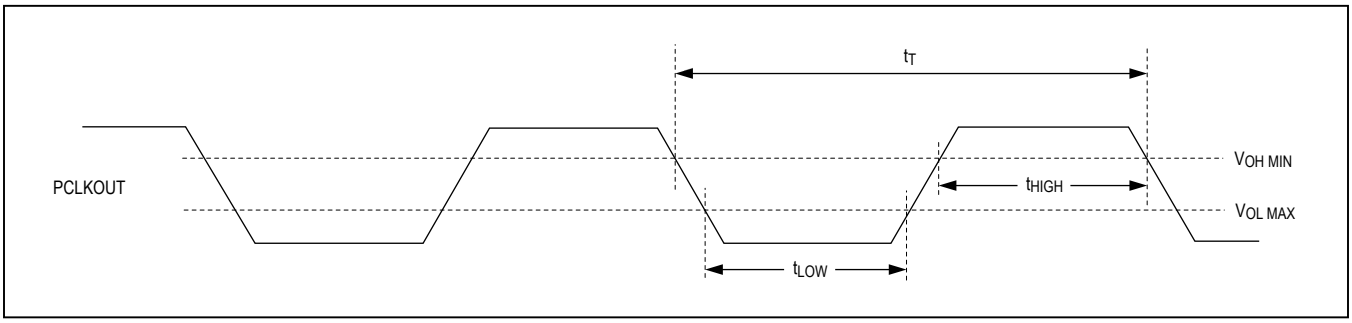


Figure 5. Parallel Clock Output Requirements

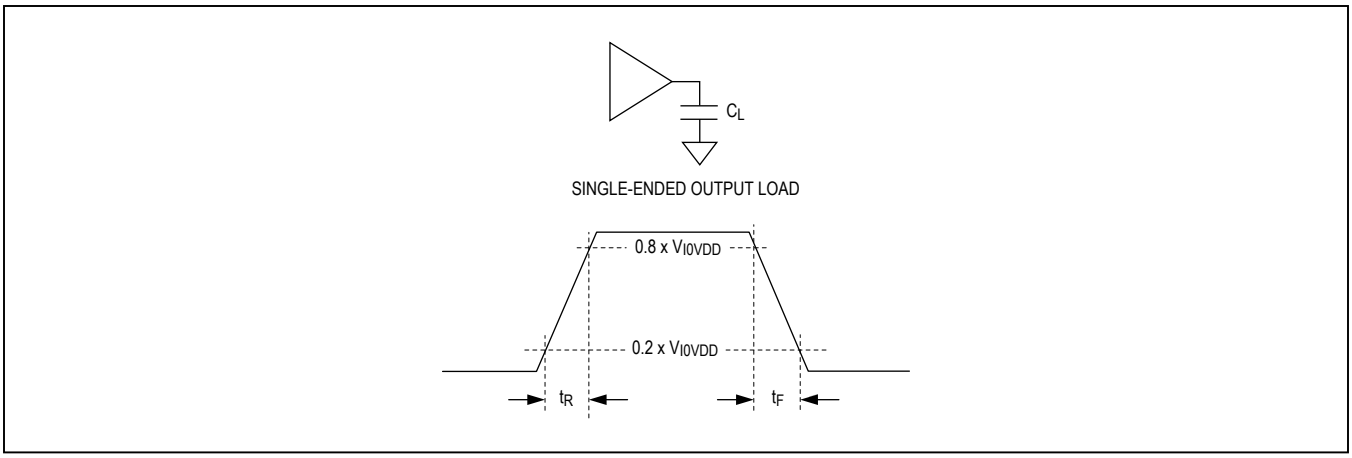


Figure 6. Output Rise-and-Fall Times

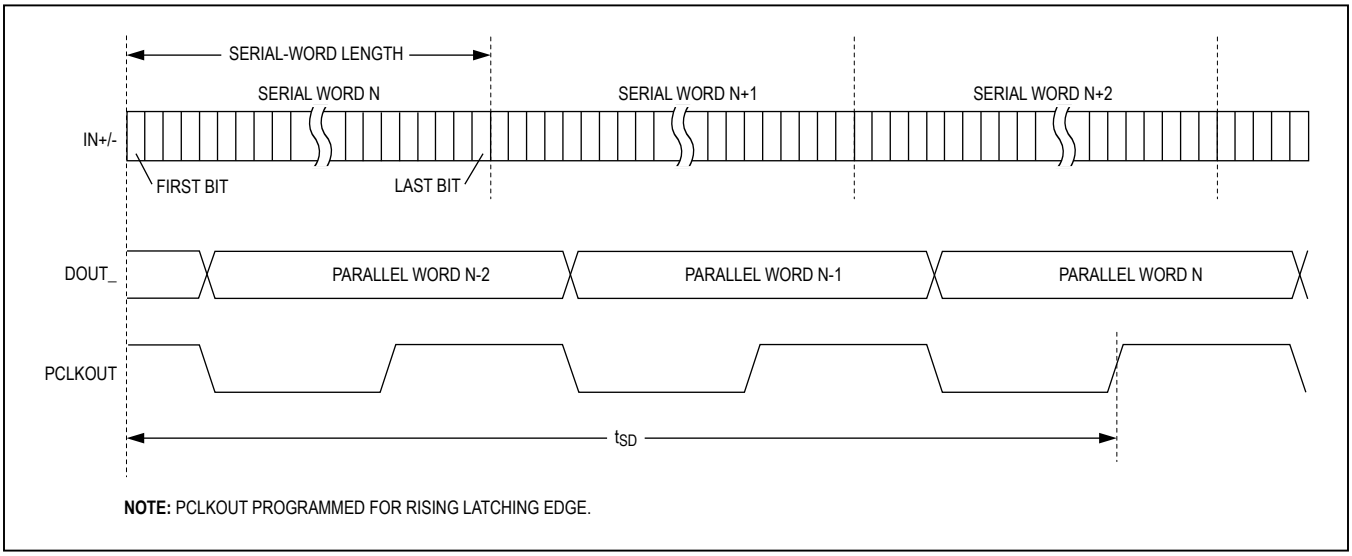


Figure 7. Deserializer Delay

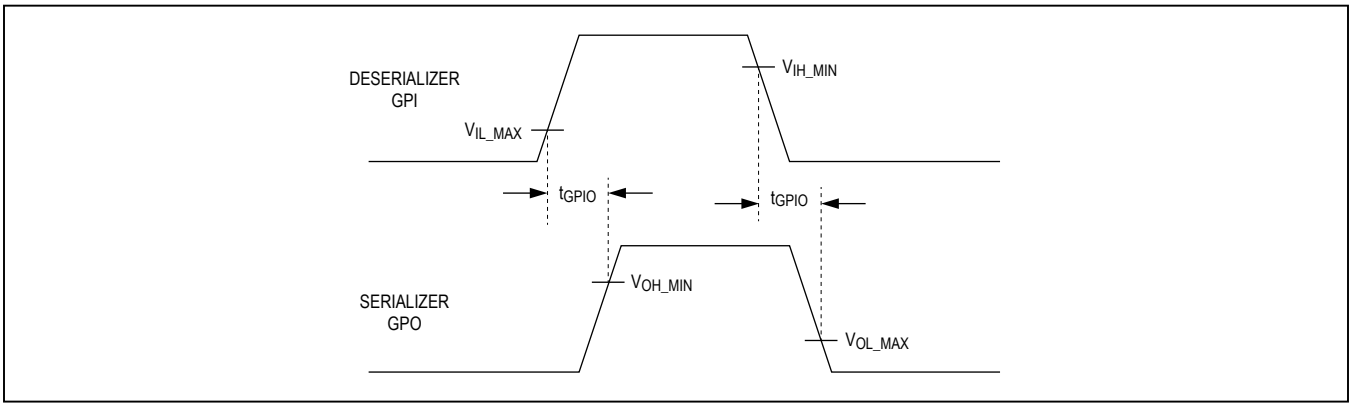


Figure 8. GPI-to-GPO Delay

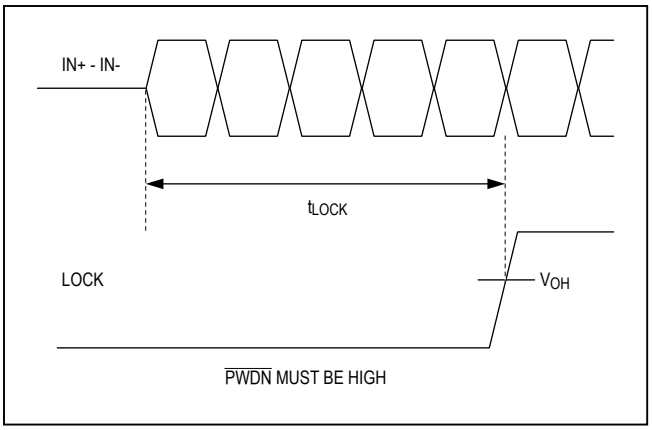


Figure 9. Lock Time

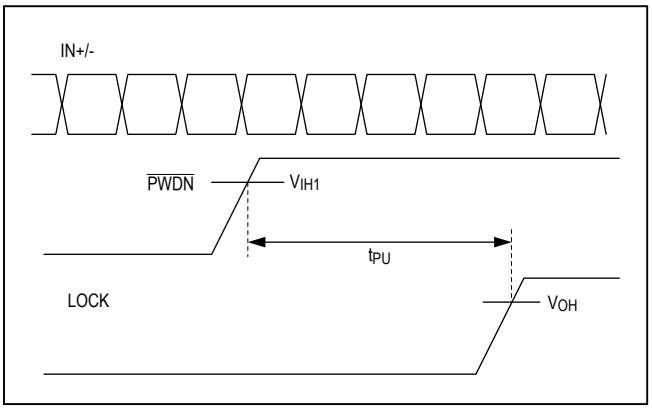


Figure 10. Power-Up Delay

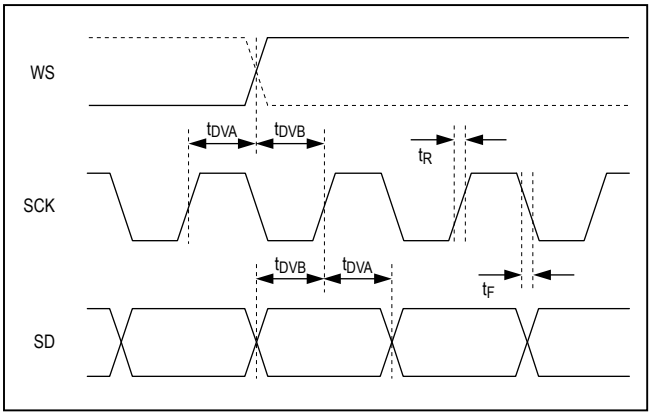


Figure 11. Output I²S Timing Parameters

Detailed Description

The MAX9276/MAX9280 deserializers, when paired with the MAX9275/MAX9277/MAX9279/MAX9281 serializers, provides the full set of operating features, but is backward-compatible with the MAX9249–MAX9270 family of gigabit multimedia serial link (GMSL) devices, and have basic functionality when paired with any GMSL device. The MAX9280 has high-bandwidth digital content protection (HDCP) while the MAX9276 does not.

The deserializer has a maximum serial-bit rate of 3.12Gbps for up to 15m of cable and operates up to a maximum output clock of 104MHz in 24-bit mode and 27-bit high-bandwidth mode, or 78MHz in 32-bit mode. This bit rate and output flexibility support a wide range of displays, from QVGA (320 x 240) to 1920 x 720 and higher with 24-bit color, as well as megapixel image sensors. An encoded audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth from 8 to 32 bits. Input equalization, combined with GMSL serializer pre/deemphasis, extends the cable length and enhances link reliability

The control channel enables a µC to program the serializer and deserializer registers and program registers on peripherals. The control channel is also used to perform HDCP functions (MAX9280 only). The µC can be located at either end of the link, or when using two µCs, at both ends. Two modes of control-channel operation are available. Base mode uses either I²C or GMSL UART protocol, while bypass mode uses a user-defined UART protocol. UART protocol allows full-duplex communication, while I²C allows half-duplex communication.

Spread spectrum is available to reduce EMI on the parallel output. The serial input complies with ISO 10605 and IEC 61000-4-2 ESD protection standards.

Register Mapping

Registers set the operating conditions of the deserializers and are programmed using the control channel in base mode. The MAX9276/MAX9280 holds its own device address and the device address of the serializer it is paired with. Similarly, the serializer holds its own device address and the address of the MAX9276/MAX9280. Whenever a device address is changed be sure to write the new address to both devices. The default device address of the deserializer is set by the ADD[2:0] and CX/TP inputs (see Table 1). Registers 0x00 and 0x01 in both devices hold the device addresses.

Table 1. Device Address Defaults (Register 0x00, 0x01)

PIN				DEVICE ADDRESS (BIN)								SERIALIZER DEVICE ADDRESS (hex)	DESERIALIZER DEVICE ADDRESS (hex)
CX/TP**	ADD2	ADD1	ADD0	D7	D6	D5	D4	D3	D2	D1	D0		
High/Low	Low	Low	Low	1	0	0	X*	0	0	0	RW	80	90
High/Low	Low	Low	High	1	0	0	X*	0	1	0	R//W	84	94
High/Low	Low	High	Low	1	0	0	X*	1	0	0	R//W	88	98
High/Low	Low	High	High	0	1	0	X*	0	1	0	R//W	44	54
High/Low	High	Low	Low	1	1	0	X*	0	0	0	R//W	C0	D0
High/Low	High	Low	High	1	1	0	X*	0	1	0	R//W	C4	D4
High/Low	High	High	Low	1	1	0	X*	1	0	0	R//W	C8	D8
High/Low	High	High	High	0	1	0	X*	1	0	0	R//W	48	58
Open	Low	Low	Low	1	0	0	X*	0	0	X*	R//W	80	92
Open	Low	Low	High	1	0	0	X*	0	1	X*	R//W	84	96
Open	Low	High	Low	1	0	0	X*	1	0	X*	R//W	88	9A
Open	Low	High	High	0	1	0	X*	0	1	X*	R//W	44	56
Open	High	Low	Low	1	1	0	X*	0	0	X*	R//W	C0	D2
Open	High	Low	High	1	1	0	X*	0	1	X*	R//W	C4	D6
Open	High	High	Low	1	1	0	X*	1	0	X*	R//W	C8	DA
Open	High	High	High	0	1	0	X*	1	0	X*	R//W	48	5A

**X = 0 for the serializer address, X = 1 for the deserializer address*

***CX/TP determine the serial cable type CX/TP = open addresses only for coax mode.*

Output Bit Map

The output bit width depends on settings of the bus width (BWS) pin. Table 2 lists the bit map. Unused output bits are pulled low.

Serial Link Signaling and Data Format

The serializer uses differential CML signaling to drive twisted-pair cable and single-ended CML to drive coaxial cable with programmable pre/deemphasis and AC-coupling. The deserializer uses AC-coupling and programmable channel equalization.

Input data is scrambled and then 8b/10b coded (9b10b in high-bandwidth mode). The deserializer recovers the embedded serial clock, then samples, decodes, and descrambles the data. In 24-bit mode, the first 21 bits contain video data. In 32-bit mode, the first 29 bits contain video data. In high-bandwidth mode, the first 24 bits contain video data, or special control signal packets. The last 3 bits contain the embedded audio channel, the embedded forward control channel, the parity bit of the serial word (Figure 12, Figure 13).