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MAX9288/MAX9290

3.12Gbps GMSL Deserializers for Coax or STP Input and MIPI CSI-2 Output

General Description

The MAX9288/MAX9290 gigabit multimedia serial link (GMSL) deserializers receive data from a GMSL serializer over 50Ω coax or 100Ω shielded twisted-pair (STP) cable and output deserialized data on the CSI-2 outputs.

The MAX9290 has HDCP content protection but otherwise is the same as the MAX9288. The deserializers pair with any GMSL serializer capable of coax output. When programmed for STP input, they are backward compatible with any GMSL serializer.

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-to-UART and UART-to-I²C modes, and up to 1Mbps in I²C-to-I²C mode. Using the control channel, a µC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing, and manage HDCP operation (MAX9290). Two GPIO ports are included, allowing display power-up and switching of the backlight, among other uses. A continuously sampled GPI input supports touch-screen controller interrupt requests in display applications.

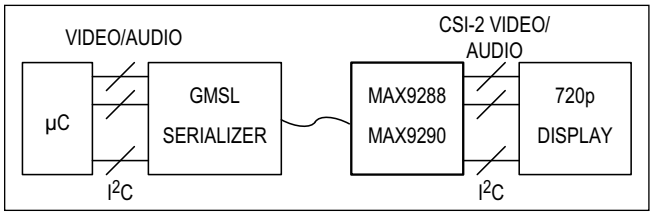
For use with longer cables, the deserializers have a programmable cable equalizer. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The GMSL supply is 3.0V to 3.6V, the MIPI CSI-2 supply is 1.7V to 1.9V, and the I/O supply is 1.7V to 3.6V.

The devices are available in lead(Pb)-free, 48-pin, 7mm x 7mm TQFN and SWTQFN packages with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Simplified Diagram



Benefits and Features

- Ideal for High-Definition Video Applications
  - 4-Lane CSI-2 Output with Up to 1Gbps Per Lane
  - Works with Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP
  - 104MHz High-Bandwidth Mode Supports 1920 x 720p/60Hz Display with 24-Bit Color
  - Equalization Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate and 32-Bit Sample Depth For 7.1 Channel HD Audio
  - Audio Clock from Audio Source or Audio Sink
  - Color Lookup Table for Gamma Correction
  - CNTL0–CNTL3 Control Outputs for HDMI/MHL
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 6.25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock-Stretch Capability
- Reduces EMI and Shielding Requirements
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Tester for BER Testing of the Serial Link
  - Programmable Choice of 8 Default Device Addresses
  - Two Dedicated GPIO Ports
  - Dedicated “Up/Down” GPI for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±8kV Contact and ±12kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

***Ordering Information* appears at end of data sheet.**

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Absolute Maximum Ratings (Note 1)

AVDD3 to EP ..... -0.5V to +3.9V
AVDD18, DVDD18 to EP ..... -0.5V to +1.9V
IOVDD to EP ..... -0.5V to +3.9V
IN+, IN- to EP ..... -0.5V to +1.9V
LMN_ to EP (15mA current limit) ..... -0.5V to +3.9V
CLK_, DOUT_ to EP ..... -0.5V to +1.9V
All Other Pins to EP ..... -0.5V to (V_{IOVDD} + 0.5V)
IN+, IN- Short Circuit to Ground or Supply ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN/SWTQFN (derate 40mW/°C above +70°C) 3200mW
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN/SWTQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 25°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (ADD_, I2CSEL, $\overline{PWDN}$, MS, GPI, DRS, EQS, CDS, HIM, SCK, WS)							
High-Level Input Voltage	V_{IH1}			0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}					0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0V to V_{IOVDD}		-20		+20	µA
THREE-LEVEL LOGIC INPUTS (BWS, CX/TP)							
High-Level Input Voltage	V_{IH}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL}					0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 4)		-10		+10	µA
Input Current	I_{IN}			-150		+150	µA
SINGLE-ENDED OUTPUTS (WS, SCK, SD, CNTL_, INTOUT)							
High-Level Output Voltage	V_{OH1}	I_{OUT} = -2mA	DCS = 0	V_{IOVDD} - 0.3			V
			DCS = 1	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OUT} = 2mA	DCS = 0			0.3	V
			DCS = 1			0.2	

DC Electrical Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = V_{IOVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Short-Circuit Current	I_{OS}	V_O = 0V, DCS = 0	V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
			V_{IOVDD} = 1.7V to 1.9V	3	7	15	
		V_O = 0V, DCS = 1	V_{IOVDD} = 3.0V to 3.6V	20	35	63	
			V_{IOVDD} = 1.7V to 1.9V	5	10	21	
MIPI HIGH-SPEED DIFFERENTIAL OUTPUT PORTS (DOUT0–DOUT3_, CLK_) (Note 3)							
Transmit Static Common-Mode Voltage	V_{CMTX}			150	200	250	mV
V_{CMTX} Mismatch When Output is Differential 1 or 0	$\lvert\Delta V_{CMT(1,0)}\rvert$					5	mV
Transmit Differential Voltage	$\lvert V_{OD}\rvert$			140	200	270	mV
V_{OD} Mismatch When Output is Differential 1 or 0	$\lvert\Delta V_{OD}\rvert$					14	mV
Output High Voltage	V_{OHHS}					360	mV
Single-Ended Output Impedance	Z_{OS}			40	50	62.5	Ω
Single-Ended Output Impedance Mismatch	ΔZ_{OS}	Mismatch of the single-ended output impedance at both DOUT_+ and DOUT_- pins for both differential 1 and 0				10	%
MIPI LOW-SPEED SINGLE-ENDED OUTPUT PORTS (DOUT0–DOUT3_, CLK_)							
Thevenin Output High Level	V_{OH}			1.05	1.2	1.3	V
Thevenin Output Low Level	V_{OL}			-50		+50	mV
Output Impedance of Low Power Transmitter	Z_{OLP}			110			Ω
OPEN-DRAIN INPUT/OUTPUT (GPIO0, GPIO1, RX/SDA, TX/SCL, $\overline{ERR}$, LOCK, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH2}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}					0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	(Note 5)	RX/SDA, TX/SCL	-100		+5	µA
			LOCK, $\overline{ERR}$, GPIO_, $\overline{LFLT}$	-80		+5	
Low-Level Output Voltage	V_{OL2}	I_{OUT} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 6)				10	pF
LINE-FAULT DETECTION INPUT (LMN0, LMN1)							
Short-to-GND Threshold	V_{TG}	Figure 1				0.3	V
Normal Threshold	V_{TN}	Figure 1		0.57		1.07	V
Open Threshold	V_{TO}	Figure 1		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}	Figure 1		1.49		1.75	V

DC Electrical Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Short-to-Battery Threshold	V_{TB}	Figure 1		2.47			V
OUTPUT FOR REVERSE CONTROL CHANNEL (IN+, IN-)							
Differential High Output Peak Voltage (V_{IN+}) - (V_{IN-})	V_{RODH}	Forward channel disabled, Figure 2	Legacy reverse control-channel mode	30		60	mV
			High-immunity mode	50		100	
Differential Low Output Peak Voltage (V_{IN+}) - (V_{IN-})	V_{RODL}	Forward channel disabled, Figure 2	Legacy reverse control-channel mode	-60		-30	mV
			High-immunity mode	-100		-50	
Single-Ended High Output Peak Voltage	V_{ROSH}	Forward channel disabled	Legacy reverse control-channel mode	30		60	mV
			High-immunity mode	50		100	
Single-Ended Low Output Peak Voltage	V_{ROSL}	Forward channel disabled	Legacy reverse control-channel mode	-60		-30	mV
			High-immunity mode	-100		-50	
DIFFERENTIAL INPUTS (IN+, IN-)							
Differential High Input Threshold (Peak) Voltage (V_{IN+}) - (V_{IN-})	$V_{IDH(P)}$	Figure 3	Activity detector medium threshold, (0x0B D[6:5] = 01)			60	mV
			Activity detector low threshold, (0x0B D[6:5] = 00)			52	
Differential Low Input Threshold (Peak) Voltage (V_{IN+}) - (V_{IN-})	$V_{IDL(P)}$	Figure 3	Activity detector medium threshold, (0x0B D[6:5] = 01)	-60			mV
			Activity detector low threshold, (0x0B D[6:5] = 00)	-52			
Input Common-Mode Voltage ((V_{IN+}) + (V_{IN-}))/2	V_{CMR}			1	1.3	1.6	V
Differential Input Resistance (Internal)	R_{IN}			80	100	130	Ω
SINGLE-ENDED INPUTS (IN+, IN-)							
Single-Ended High Input Threshold (Peak) Voltage	$V_{ISH(P)}$	Figure 4	Activity detector medium threshold, (0x0B D[6:5] = 01)			43	mV
			Activity detector low threshold, (0x0B D[6:5] = 00)			36	
Single-Ended Low Input Threshold (Peak) Voltage	$V_{ISL(P)}$	Figure 4	Activity detector medium threshold, (0x0B D[6:5] = 01)	-43			mV
			Activity detector low threshold, (0x0B D[6:5] = 00)	-36			
Input Resistance (Internal)	R_I			40	50	65	Ω

DC Electrical Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Total Supply Current (AVDD_ + DVDD_ + IOVDD) (Note 7) (Worst-Case-Pattern, Figure 5)	I_{WCS}	BWS = low, $f_{PCLKOUT}$ = 16.6MHz, 1 MIPI lane, RGB666	AVDD3		97	131	mA
			DVDD18		28	38	
			IOVDD		0.3	2	
			AVDD18		21	33	
			Total		146	197	
		BWS = low, $f_{PCLKOUT}$ = 33.3MHz, 1 MIPI lanes, RGB666	AVDD3		99	134	
			DVDD18		45	62	
			IOVDD		0.3	2	
			AVDD18		25	34	
			Total		170	227	
		BWS = low, $f_{PCLKOUT}$ = 66.6MHz, 2 MIPI lanes, RGB666	AVDD3		103	140	
			DVDD18		69	94	
			IOVDD		0.3	2	
			AVDD18		29	39	
			Total		201	270	
		BWS = low, $f_{PCLKOUT}$ = 104MHz, 2 MIPI lanes, RGB666	AVDD3		112	152	
			DVDD18		100	139	
			IOVDD		0.3	2	
			AVDD18		46	63	
			Total		259	351	
		BWS = mid, $f_{PCLKOUT}$ = 36.6MHz, 1 MIPI lanes, RGB888	AVDD3		100	136	
			DVDD18		51	70	
			IOVDD		0.3	2	
			AVDD18		27	36	
			Total		178	236	
		BWS = mid, $f_{PCLKOUT}$ = 104MHz, 2 MIPI lanes, RGB888	AVDD3		112	153	
			DVDD18		123	169	
			IOVDD		0.3	2	
			AVDD18		55	75	
			Total		290	394	
Sleep-Mode Supply Current	I_{CCS}				44	120	µA
Power-Down Current	I_{CCZ}	$\overline{PWDN}$ = GND			12	75	µA
ESD PROTECTION							
IN+, IN- (Note 8)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8			kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge	±8			
			Air discharge	±12			
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge	±8			
			Air discharge	±20			
All Other Pins (Note 9)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±2.5			kV

AC Electrical Characteristics

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
I²C/UART PORT TIMING							
I²C/UART Bit Rate				9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
I²C TIMING (Figure 6)							
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)		9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)		> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)		> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low	4.7			µs
			Mid	0.6			
			High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low	0			µs
			Mid	0			
			High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low	250			ns
			Mid	100			
			High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	

AC Electrical Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low			50	ns
			Mid			50	
			High			50	
Capacitive Load Each Bus Line	C_b	(Note 8)				100	pF
SWITCHING CHARACTERISTICS (Note 10)							
Deserializer Delay	t_{SD}	(Note 11) Figure 8			1388	1500	Bits
Reverse Control-Channel Output Rise Time	t_R	No forward channel data transmission, Figure 2		180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward channel data transmission, Figure 2		180		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (cable delay not included), Figure 9				350	µs
Lock Time	t_{LOCK}	Figure 10 (Note 12)				4	ms
Power-Up Time	t_{PU}	Figure 11				8.5	ms
I^2S/TDM OUTPUT TIMING (Note 10)							
WS Jitter	tj_{WS}	t_{WS} = 1/f_{WS}, (cycle-to-cycle), rising-to-falling edge or falling-to-rising edge	f_{WS} = 48kHz or 44.1kHz		1.2^{e-3} x t_{WS}	1.5^{e-3} x t_{WS}	ns
			f_{WS} = 96kHz		1.6^{e-3} x t_{WS}	2^{e-3} x t_{WS}	
			f_{WS} = 192kHz		1.6^{e-3} x t_{WS}	2e-3 x t_{WS}	
SCK Jitter (2-Channel I^2S)	tj_{SCK1}	t_{SCK} = 1/f_{SCK}, (cycle-to-cycle), rising-to-rising edge	n_{SCK} = 16 bits, f_{WS} = 48kHz or 44.1kHz		13^{e-3} x t_{SCK}	16^{e-3} x t_{SCK}	ns
			n_{SCK} = 24 bits, f_{WS} = 96kHz		39^{e-3} x t_{SCK}	48^{e-3} x t_{SCK}	
			n_{SCK} = 32 bits, f_{WS} = 192kHz		0.1 x t_{SCK}	0.13 x t_{SCK}	
SCK Jitter (8-Channel TDM)	tj_{SCK2}	t_{SCK} = 1/f_{SCK}, (cycle-to-cycle), rising-to-rising edge	n_{SCK} = 16 bits, f_{WS} = 48kHz or 44.1kHz		52^{e-3} x t_{SCK}	64^{e-3} x t_{SCK}	ns
			n_{SCK} = 24 bits, f_{WS} = 96kHz		156^{e-3} x t_{SCK}	192^{e-3} x t_{SCK}	
			n_{SCK} = 32 bits, f_{WS} = 192kHz		0.4 x t_{SCK}	0.52 x t_{SCK}	

AC Electrical Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Audio Skew Relative to Video	t_{ASK}	Video and audio synchronized			3 x t_{WS}	4 x t_{WS}	µs
SCK, SD, WS Rise-and-Fall Time	t_R, t_F	20% to 80%	C_L = 10pF, DCS = 1	0.3		3.1	ns
			C_L = 5pF, DCS = 0	0.4		3.8	
SD, WS Valid Time Before SCK (2-Channel I²S)	t_{DVB1}	t_{SCK} = 1/f_{SCK}, Figure 12		0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (2-Channel I²S)	t_{DVA1}	t_{SCK} = 1/f_{SCK}, Figure 12		0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time Before SCK (8-Channel TDM)	t_{DVB2}	t_{SCK} = 1/f_{SCK}, Figure 12		0.20 x t_{SCK}	0.5 x t_{SCK}		ns
SD, WS Valid Time After SCK (8-Channel TDM)	t_{DVA2}	t_{SCK} = 1/f_{SCK}, Figure 12		0.20 x t_{SCK}	0.5 x t_{SCK}		ns
HIGH-SPEED DIFFERENTAIL OUTPUT PORTS (DOUT0_–DOUT3_, CLK_) (Note 10)							
20% to 80% Rise Time and Fall Time	t_R, t_F	Bit rate ≤ 1Gbps				0.3	UI
				100			ps
Data-to-Clock Skew	t_{SKW}			-0.15		+0.15	UI
UI Instantaneous	UI_{INS}			1		12.5	ns
Common-Level Variation Above 450MHz	ΔV_{CM}					15	mV_{RMS}
Common-Level Variation Between 50MHz to 450MHz						25	mV_{PEAK}
LOW-SPEED DIFFERENTIAL OUTPUT PORTS (DOUT0_–DOUT3_, CLK_) (Note 10)							
15% to 85% Rise Time and Fall Time	t_{RLP}/t_{FLP}					25	ns
30% to 85% Rise Time and Fall Time Transition from HS to LP	t_{REOP}					35	ns
GENERAL CSI-2 TIMING SPECIFICATIONS (Note 10, Figure 13)							
Start of Transmission: Clock Prepare Time	$t_{CLK-PREPARE}$	Time that the transmitter drives the clock lane LP-00 line state immediately before HS-0 line state starting the HS transition		38		95	ns
End of Transmission: Clock Trail Time	$t_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst		60			ns
Clock Start of Transmission Time	$t_{CLK-PREPARE}$ + $t_{CLK-ZERO}$	$t_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the clock		300			ns

AC Electrical Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = 1.7V to 1.9V, V_{AVDD3} = 3.0V to 3.6V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground (GND), T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock End of Transmission Time	t_{EOT}	Transmitted time interval from the start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ to start of the LP-11 state following a HS burst			105ns + 12 x UI	ns
HS Exit Time	$t_{HS-EXIT}$	Time that the transmitter drivesLP-11 following a HS burst	100			ns
Start of Transmission: Data Prepare Time	$t_{HS-PREPARE}$	Time that the transmitter drives the data lane LP-00 line state immediately before the HS-0 line state starting the HS transmission	40ns + 4 x UI		85ns + 6 x UI	ns
Start of Transition Time	$t_{HS-PREPARE}$ + $t_{HS-ZERO}$	$t_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the sync sequence	145ns + 10 x UI			ns
End of Transmission: Data Trail Time	$t_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	Max(8 x UI, 60ns + 4 x UI)			ns
LP Transmit Time	t_{LPTX}	Transmitted length of any low-power state period	50			ns

Note 3: Limits are 100% production tested at T_A = +105°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 4: To provide a mid level, leave the input open, or, if driven, put driver in high impedance. High-impedance leakage current must be less than ±10µA.

Note 5: I_{IN} min due to voltage drop across the internal pullup resistor.

Note 6: Not production tested. Guaranteed by design.

Note 7: HDCP enabled (MAX9290 only). IOVDD current is not production tested. For the MAX9288 (or when HDCP is disabled on the MAX9290), subtract the HDCP supply current, as shown in Table 25.

Note 8: Specified pin to ground.

Note 9: Specified pin to all supply/ground.

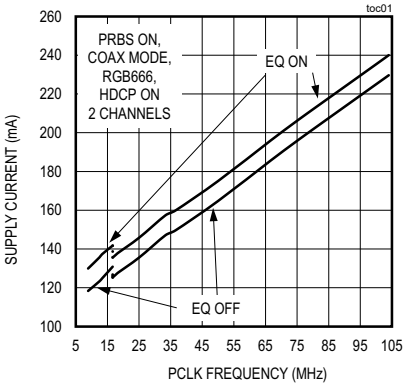
Note 10: Not production tested, guaranteed by characterization.

Note 11: Measured in serial link bit times. Bit time = 1/(30 x f_{PIXEL}) for BWS = 0 or open. Bit time = 1/(40 x f_{PIXEL}) for BWS = 1.

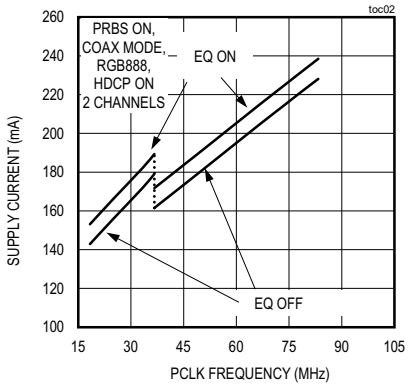
Typical Operating Characteristics

(V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C, unless otherwise noted.)

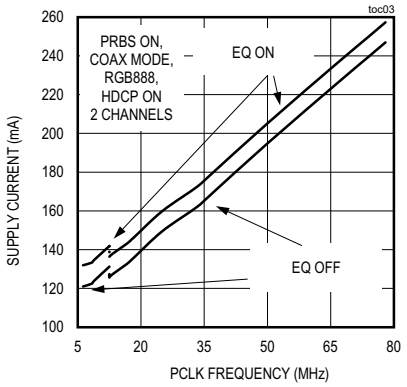
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = LOW)



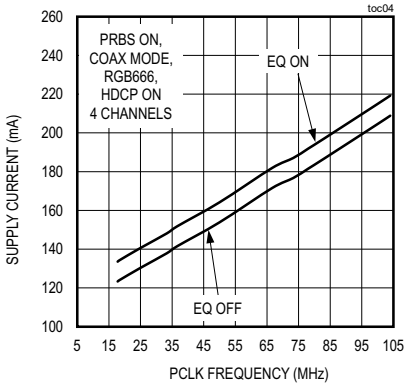
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = OPEN)



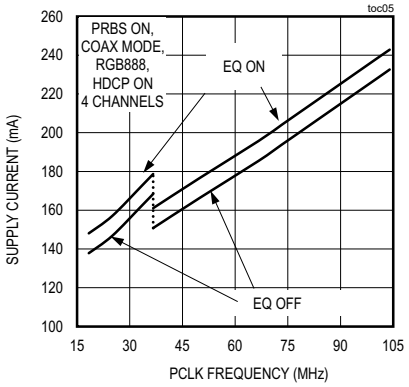
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = HIGH)



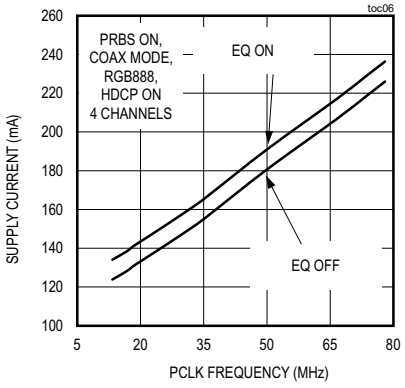
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = LOW)



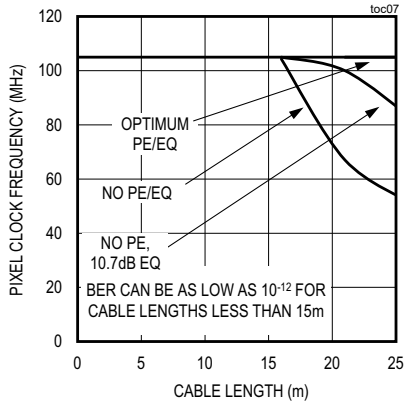
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = OPEN)



SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = HIGH)



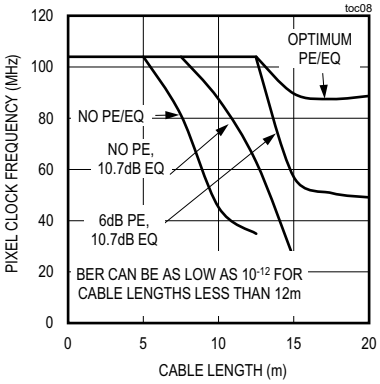
MAXIMUM PIXEL CLOCK FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



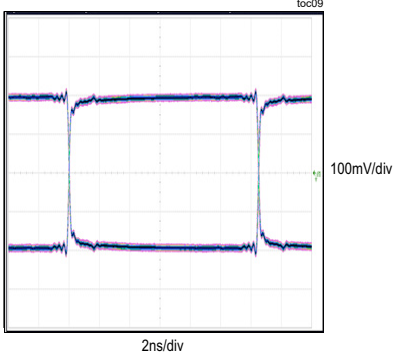
Typical Operating Characteristics (continued)

(V_{AVDD18} = V_{DVDD18} = V_{IOVDD} = 1.8V, V_{AVDD3} = 3.3V, T_A = +25°C, unless otherwise noted.)

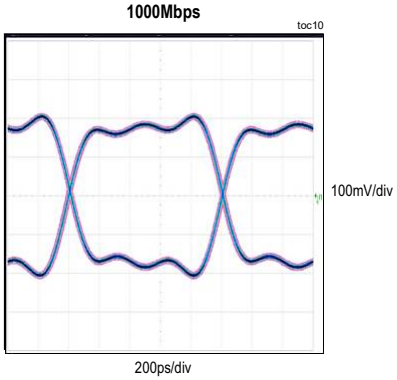
MAXIMUM PIXEL CLOCK FREQUENCY vs. STP CABLE LENGTH (BER ≤ 10^{-9})



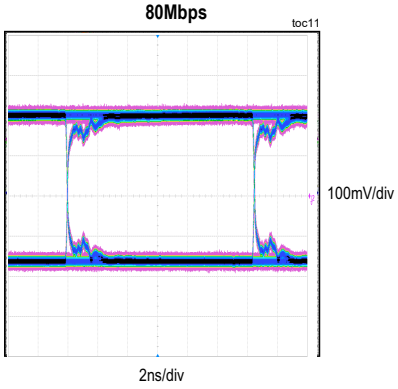
MIPI CLOCK EYE PATTERN 80Mbps



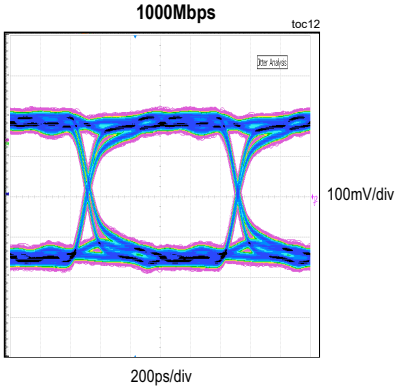
MIPI CLOCK EYE PATTERN 1000Mbps



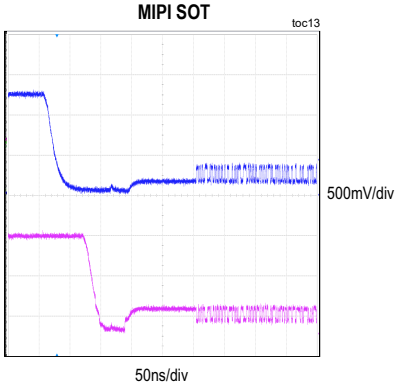
MIPI DATA EYE PATTERN 80Mbps



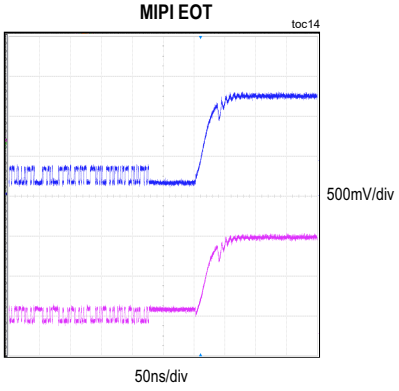
MIPI DATA EYE PATTERN 1000Mbps



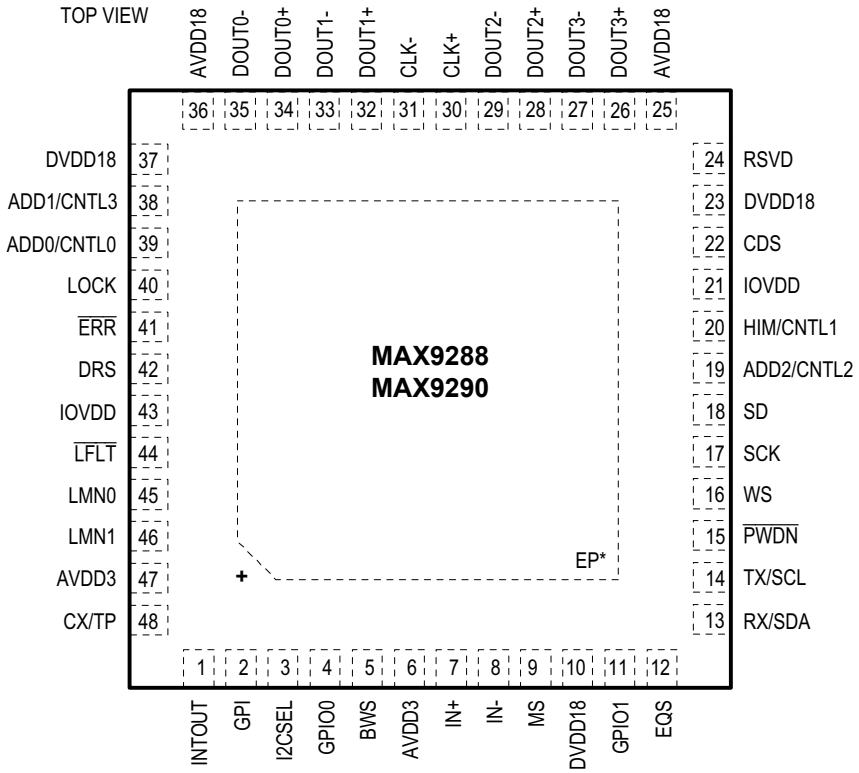
MIPI SOT



MIPI EOT



Pin Configuration



TQFN/SWTQFN
(7mm x 7mm x 0.75mm)

CONNECT EP TO GROUND PLANE

Pin Description

PIN	NAME	FUNCTION
1	INTOUT	A/V Status Register Interrupt Output. Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
2	GPI	General-Purpose Input with Internal Pulldown to EP. The serializer GPO (or INT) output follows GPI.
3	I2CSEL	I²C Select. Control channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I²C interface. Set I2CSEL = low to select UART interface.
4	GPIO0	Open-Drain, General-Purpose Input/Output, with Internal 60kΩ Pullup to IOVDD
5	BWS	Three-Level Bus Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = low, with 6kΩ (max) pulldown for 24-bit mode. Set BWS = high, with 6kΩ (max) pullup to IOVDD for 32-bit mode. Set BWS = open for high-bandwidth mode.
6, 47	AVDD3	3.3V Analog Power Supply. Bypass AVDD3 to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD3.
7	IN+	Noninverting Coax/Twisted-Pair Serial Input
8	IN-	Inverting Coax/Twisted-Pair Serial Input

Pin Description (continued)

PIN	NAME	FUNCTION
9	MS	Mode Select with Internal Pulldown to EP. MS sets the control-link mode when CDS = high. Set MS = low, to select base mode. Set MS = high to select the bypass mode. MS sets autostart mode when CDS = low.
10, 23, 37	DVDD18	1.8V Digital Power Supply. Bypass DVDD18 to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD18.
11	GPIO1	Open-Drain, General-Purpose Input/Output, with Internal 60kΩ Pullup to IOVDD
12	EQS	Equalizer Select Input, with Internal Pulldown to EP. The state of EQS latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Leave EQS open for 10.7dB equalizer boost (EQTUNE = 1001). Connect EQS to IOVDD with a 30kΩ resistor for 5.2dB equalizer boost (EQTUNE = 0100).
13	RX/SDA	UART Receive/I^2C Serial Data Input/Output, with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the deserializer's UART. SDA: Data input/output of the deserializer's I^2C Master/Slave.
14	TX/SCL	UART Transmit/I^2C Serial Clock Input/Output, with Internal 30kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the deserializer's UART. SCL: Clock input/output of the deserializer's I^2C Master/Slave.
15	$\overline{PWDN}$	Active-Low, Power-Down Input, with Internal Pulldown to EP. Set $\overline{PWDN}$ low to enter power-down mode to reduce power consumption.
16	WS	I^2S/TDM Word-Select Input/Output. Powers up as an I^2S output (deserializer provided clock). Set AUDIOMODE bit = '1' to change WS to an input with internal pulldown to GND and supply WS externally (system provided clock).
17	SCK	I^2S/TDM Serial-Clock Input/Output. Powers up as an I^2S output (deserializer provided clock). Set AUDIOMODE bit = '1' to change SCK to an input with internal pulldown to GND and supply SCK externally (system provided clock).
18	SD	I^2S/TDM Serial-Data Output. Disable I^2S/TDM encoding to serial data to use SD as an additional control/data output. Encrypted when HDCP is enabled.
19	ADD2/CNTL2	Address Selection Input/Auxiliary Control Signal Output, with Internal Pulldown to EP. Functions as ADD2 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL2 output automatically after power-up. ADD2: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect ADD2/CNTL2 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL2: Used only in 32-bit and high-bandwidth mode (BWS = high, open). CNTL2 is mapped from the GMSL serializer's CNTL2 or DIN28 input.

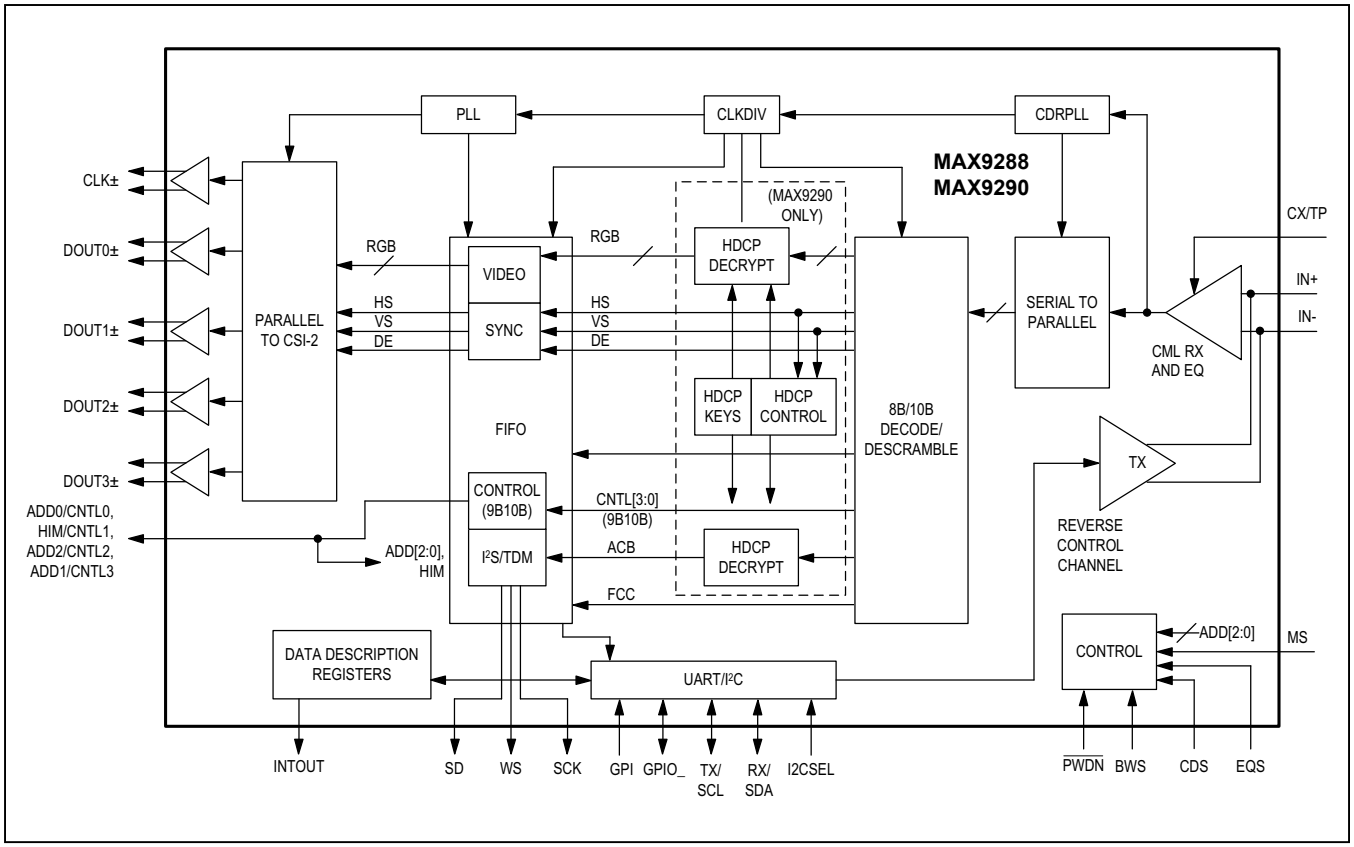
Pin Description (continued)

PIN	NAME	FUNCTION
20	HIM/CNTL1	High-Immunity Mode Input/Auxiliary Control Signal Output With Internal Pulldown to EP. Functions as HIM input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL2 output automatically after power-up. HIM: Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low) and is active-high. Connect HIM/CNTL1 to IOVDD with a 30kΩ resistor to set high or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the serializer must be set to the same value. CNTL1: Used only in 32-bit and high-bandwidth mode (BWS = high, open). CNTL1 is mapped from the GMSL serializer's CNTL1, DIN27, or RES input.
21, 43	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
22	CDS	Control Direction Selection Input, with Internal Pulldown to EP. Control link direct selection input with internal pulldown to EP. Set CDS = low when the control channel master µC is connected at the serializer. Set CDS = high when the control channel master µC is connected at the deserializer.
24	RES	Reserved. Leave unconnected
25, 36	AVDD18	1.8V Analog Power Supply. Bypass AVDD18 to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD18.
26–29, 32–35	DOUT_+, DOUT_-	CSI-2 Data Outputs
30, 31	CLK+, CLK-	CSI-2 Clock Output
38	ADD1/CNTL3	Auxiliary Control Signal Output/Address Selection Input, with Internal Pulldown to EP. Functions as ADD1 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL3 output automatically after power-up. ADD1: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect ADD1/CNTL3 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL3: Used only in high-bandwidth mode (BWS = open.
39	ADD0/CNTL0	Auxiliary Control Signal Output/Address Selection Input, with Internal Pulldown to EP. Functions as ADD0 input at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low), and switches to CNTL0 output automatically after power-up. ADD0: Bit value is latched at power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). See Table 1. Connect ADD0/CNTL0 to IOVDD with a 30kΩ resistor to set high or leave open to set low. CNTL0: Used only in high-bandwidth mode (BWS = open).
40	LOCK	Open-Drain Lock Output, with Internal 60kΩ Pullup to IOVDD. LOCK = high indicates that PLLs are locked with correct serial-word-boundary alignment. LOCK = low indicates that PLLs are not locked or an incorrect serial-word-boundary alignment. LOCK is high when $\overline{PWDN}$ = low.
41	$\overline{ERR}$	Error Output. Open-drain data error detection and/or correction indication output with internal 60kΩ pullup to IOVDD. $\overline{ERR}$ is high when $\overline{PWDN}$ is low.

Pin Description (continued)

PIN	NAME	FUNCTION
42	DRS	Data-Rate Select Input. DRS is latched upon power-up or when $\overline{PWDN}$ transitions low-to-high. Set DRS high for pixel clock rates below 16.66MHz (BWS = low), 12.5MHz (BWS = high), or 36.66MHz (BWS = open). Set DRS = low for faster pixel clock rates.
44	$\overline{LFLT}$	Active-Low Open-Drain Line-Fault Output. $\overline{LFLT}$ has a 60kΩ internal pullup to IOVDD. $\overline{LFLT}$ = low indicates a line fault. $\overline{LFLT}$ is high when $\overline{PWDN}$ = low.
45	LMN0	Line Fault Monitor Input 0 (See Figure 1)
46	LMN1	Line Fault Monitor Input 1 (See Figure 1)
48	CX/TP	Three-Level Coax/Twisted Pair Select Input. Use 6kΩ (max) pullup to IOVDD or pulldown resistor for setting CX/TP = high or low. See Table 12 for function.
—	EP	Exposed Pad. EP is internally connected to device ground. **MUST** connect EP to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



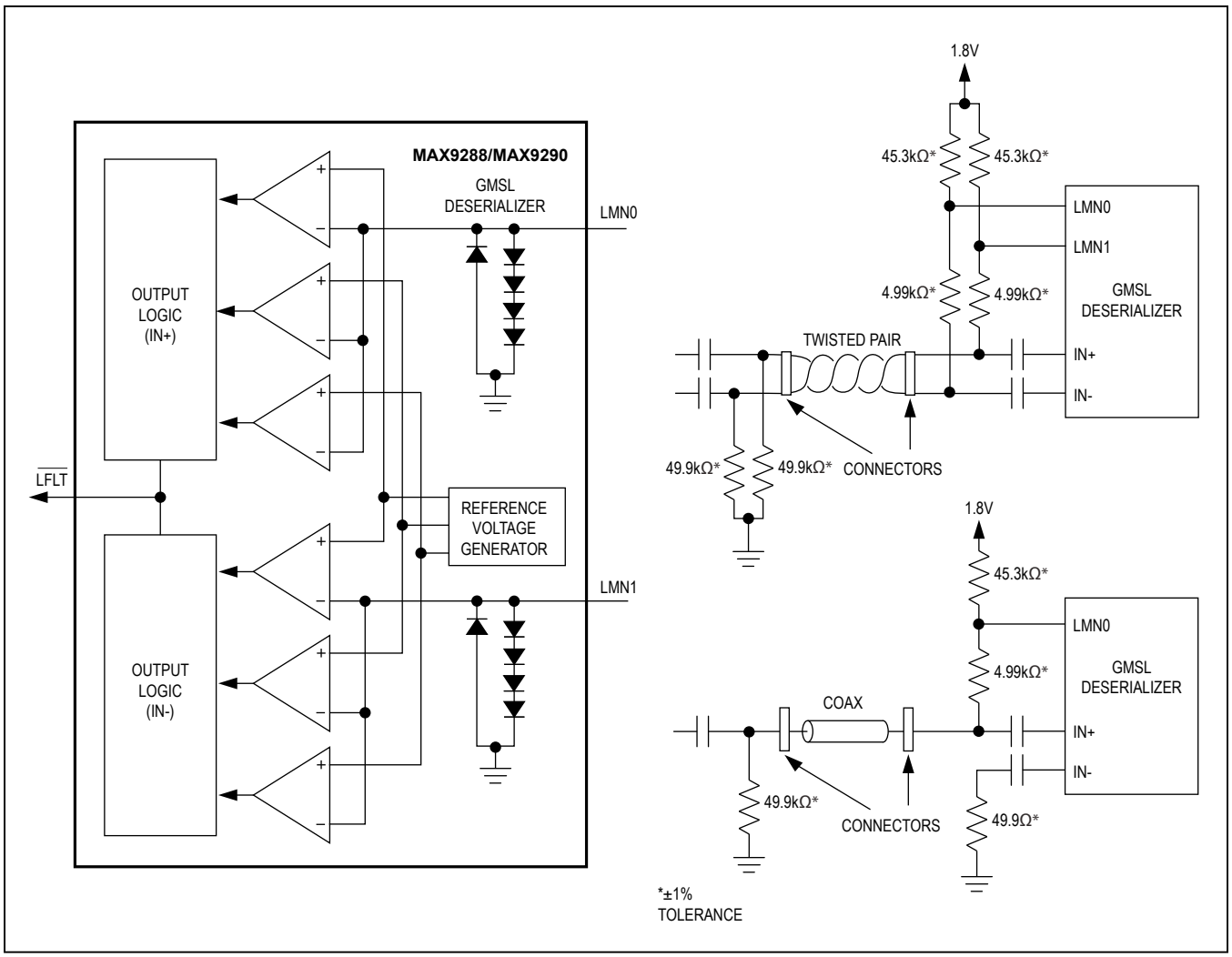


Figure 1. Line Fault

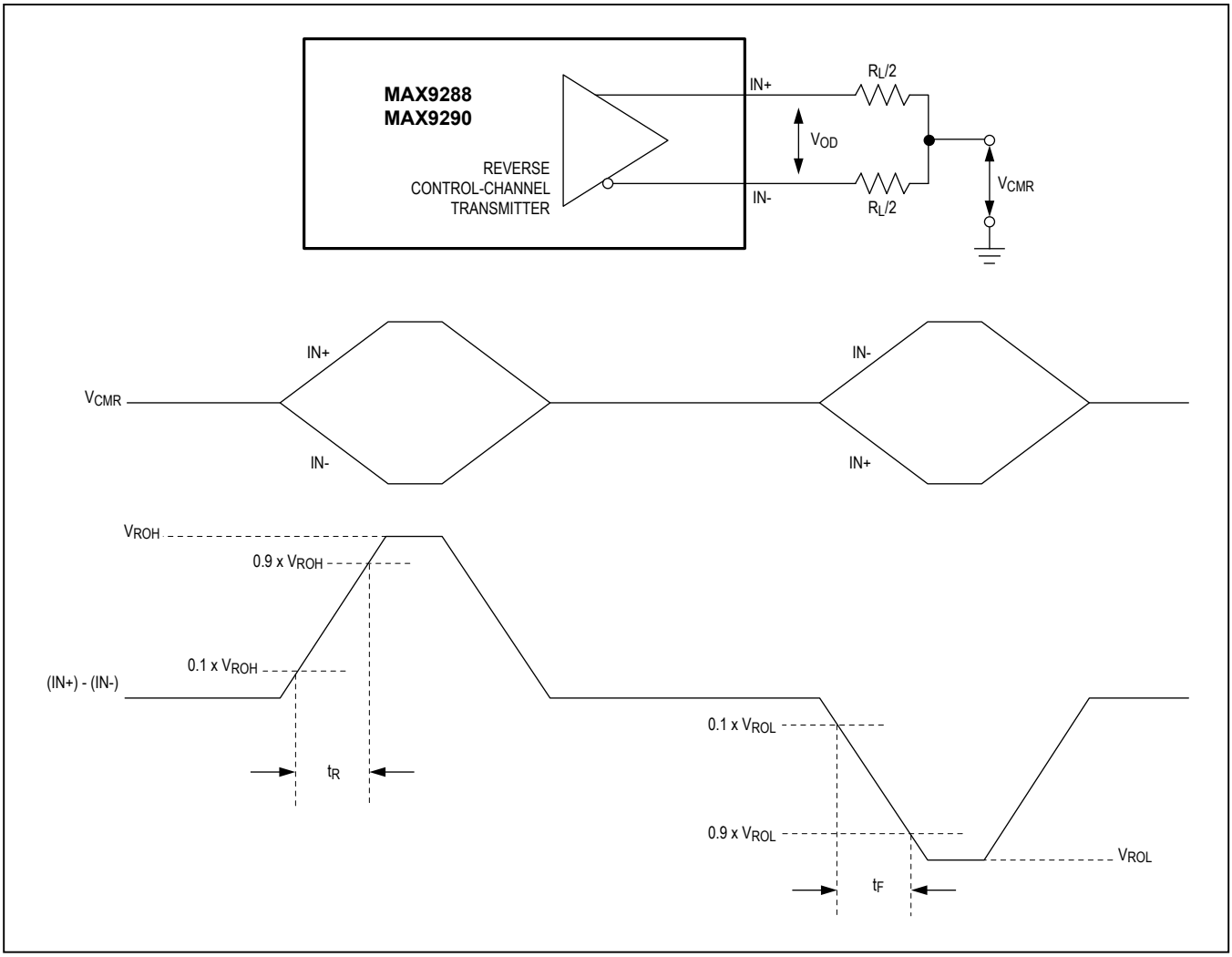


Figure 2. Reverse Control-Channel Output Parameters

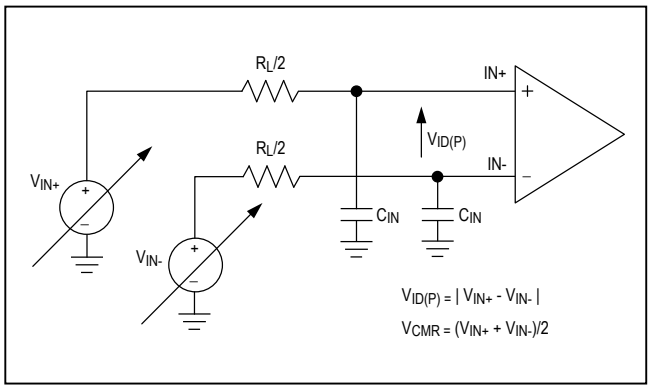


Figure 3. Test Circuit for Differential Input Measurement

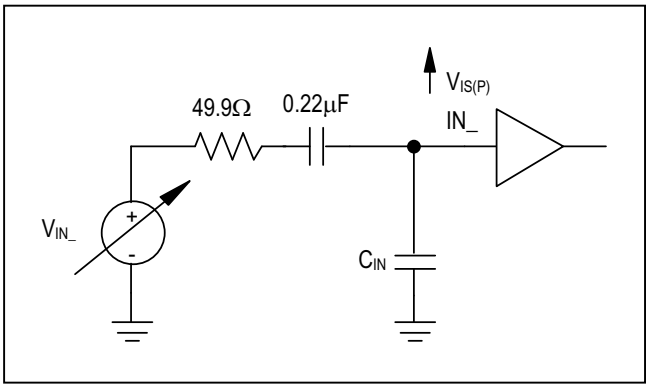


Figure 4. Test Circuit for Single-Ended Input Measurement

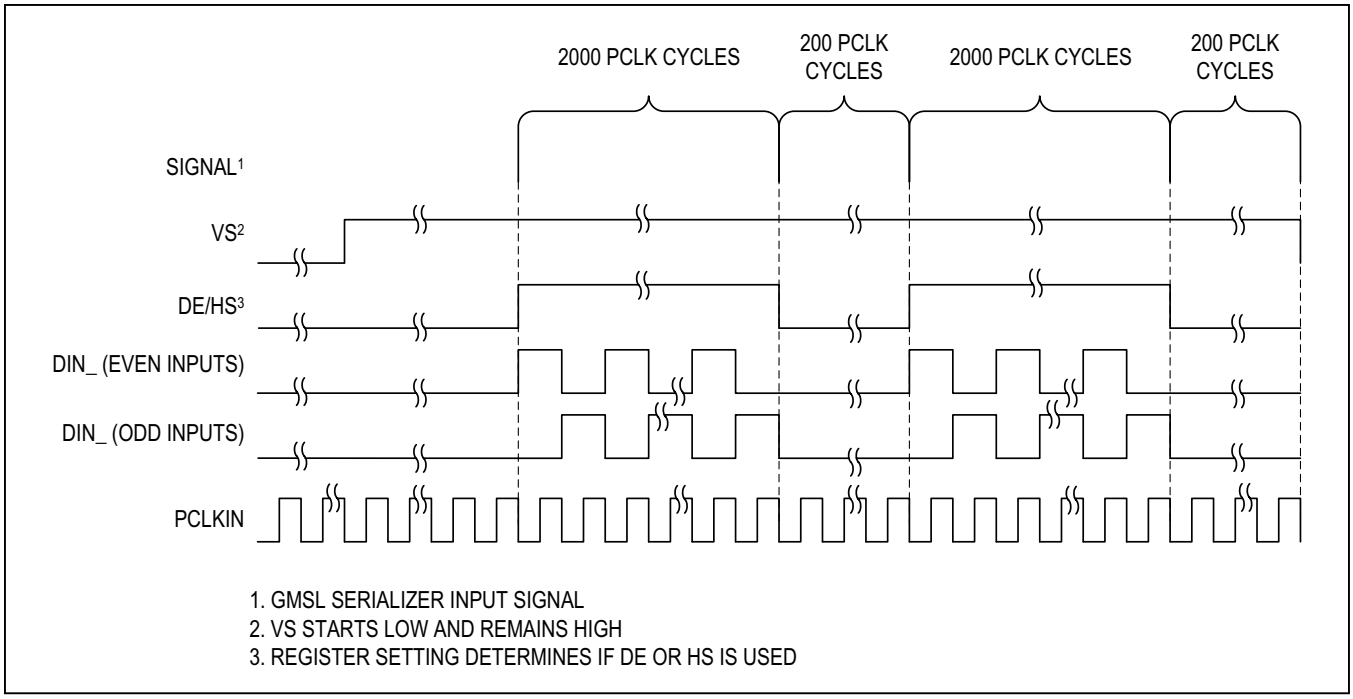


Figure 5. Worst-Case Pattern Output

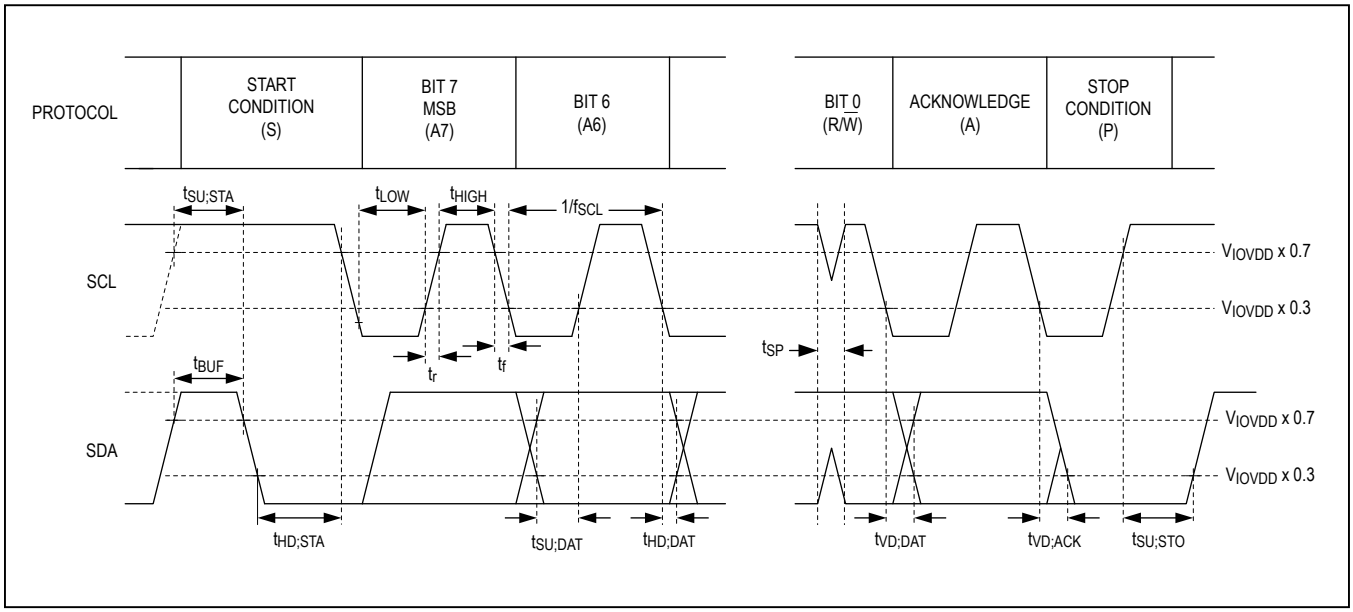


Figure 6. I²C Timing Parameters

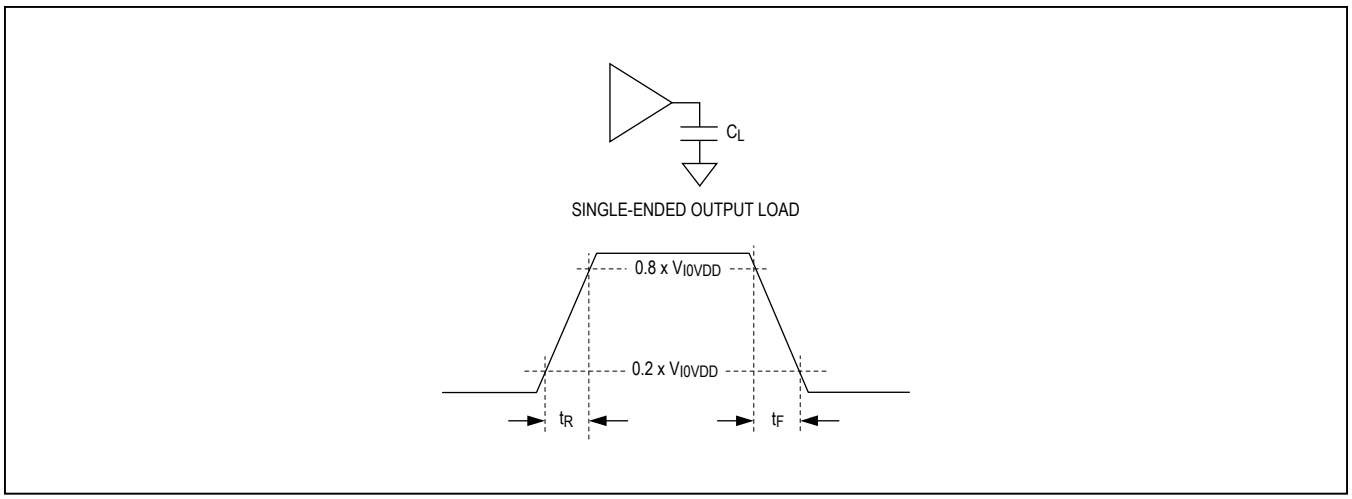


Figure 7. Output Rise-and-Fall Times

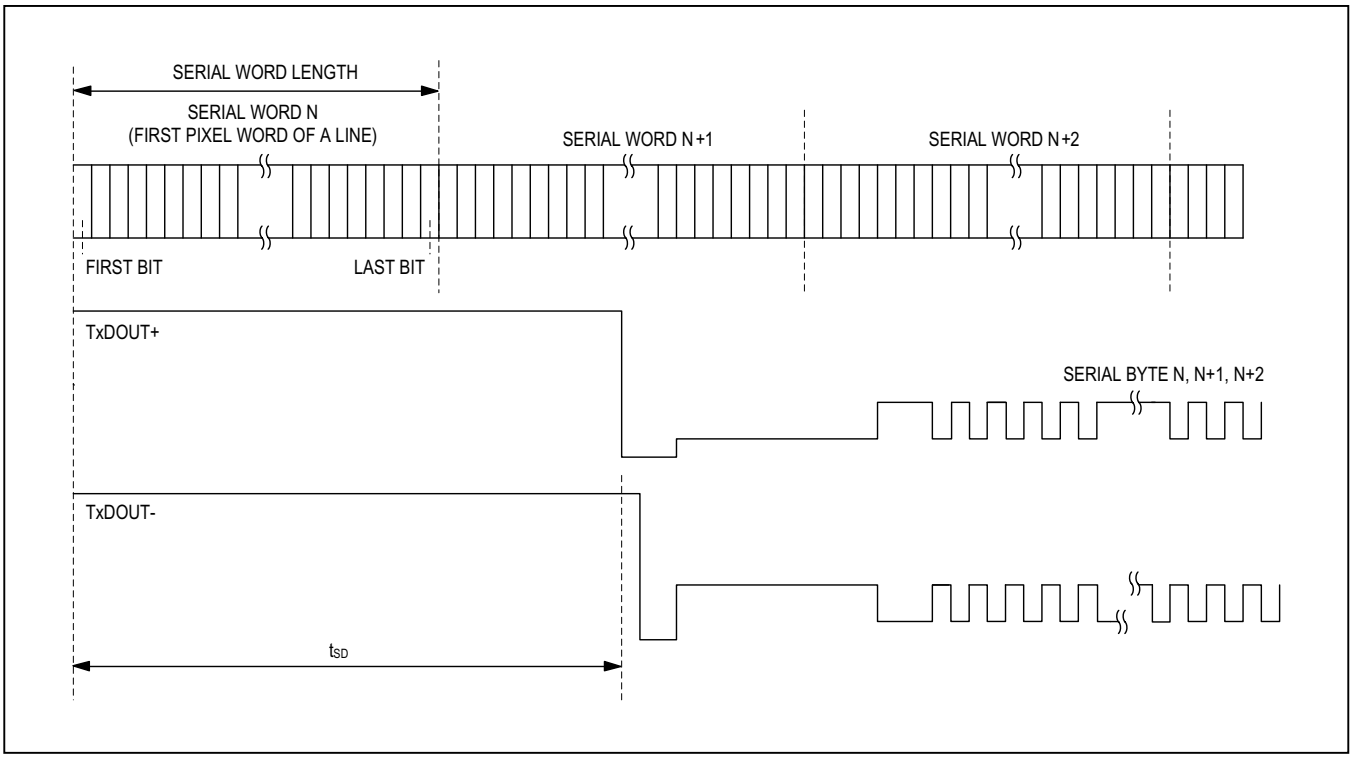


Figure 8. Deserializer Delay