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MAX9291/MAX9293

3.12Gbps GMSL Serializers for Coax or STP Output and HDMI Input

General Description

The MAX9291/MAX9293 GMSL serializers convert an HDMI input to a gigabit multimedia serial link (GMSL) output for transmission of video, audio, and control signals over 15m or more of 50Ω coax or 100Ω shielded twisted-pair (STP) cable. The MAX9293 has HDCP content protection, but is otherwise the same as the MAX9291. The serializers pair with any GMSL deserializer capable of coax input. When programmed for STP output, the serializers are backward compatible with any GMSL deserializer. The output amplitude is programmable 100mV to 500mV single-ended (coax) or 100mV to 400mV differential (STP).

The audio channel supports L-PCM I²S stereo and up to eight channels of L-PCM in TDM mode. Sample rates of 32kHz to 192kHz are supported with sample depth up to 32 bits.

The embedded control channel operates at 9.6kbps to 1Mbps in UART-to-UART and UART-to-I²C modes, and up to 1Mbps in I²C-to-I²C mode. Using the control channel, a µC can program serializer, deserializer, and peripheral device registers at any time, independent of video timing and manage HDCP operation (MAX9293). A GPO output supports touch-screen controller interrupt requests from the remote end of the link.

For use with longer cables, the serializers have programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply is 1.8V and 3.3V and the I/O supply is 1.7V to 3.6V. The package is a lead(Pb)-free, 56-pin, 8mm x 8mm TQFN with exposed pad and 0.5mm lead pitch.

Applications

- High-Resolution Automotive Navigation
- Rear-Seat Infotainment
- Megapixel Camera Systems

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Ideal for High-Definition Video Applications
  - HDMI 1.4a Input with Integrated Input Equalizer, DDC, and Input Termination
  - Drives Low-Cost 50Ω Coax Cable and FAKRA Connectors or 100Ω STP Cable
  - 104MHz High-Bandwidth Mode Supports 1920 x 720p/60Hz Display with 24-Bit Color
  - Serializer Pre/Deemphasis Allows 15m Cable at Full Speed
  - Up to 192kHz Sample Rate and 32-Bit Sample Depth for 7.1 Channel HD Audio
- Multiple Data Rates for System Flexibility
  - Up to 3.12Gbps Serial-Bit Rate
  - 25MHz to 104MHz Pixel Clock
  - 9.6kbps to 1Mbps Control Channel in UART, Mixed UART/I²C, or I²C Mode with Clock-Stretch Capability
- Reduces EMI and Shielding Requirements
  - Serial Output Programmable for 100mV to 500mV Single-Ended or 100mV to 400mV Differential
  - Programmable Spread Spectrum Reduces EMI
  - Tracks Spread Spectrum on Input
  - High-Immunity Mode for Maximum Control-Channel Noise Rejection
- Peripheral Features for System Power-Up and Verification
  - Built-In PRBS Generator for BER Testing of the Serial Link
  - Programmable Choice of 9 Default Device Addresses
  - Dedicated “Up/Down” GPO for Touch-Screen Interrupt and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets Rigorous Automotive and Industrial Requirements
  - -40°C to +105°C Operating Temperature
  - ±8kV Contact and ±15kV Air ISO 10605 and IEC 61000-4-2 ESD Protection

19-7544; Rev 1; 9/15

maxim integrated™

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Absolute Maximum Ratings (Note 1)

AVDD to EP .....-0.5V to +1.9V
DVDD to EP .....-0.5V to +1.9V
RVDD to EP .....-0.5V to +1.9V
IOVDD to EP .....-0.5V to +3.9V
HVDD to EP .....-0.5V to +3.9V
PLLVDD to EP .....-0.5V to +3.9V
XVDD to EP .....-0.5V to +3.9V
RX_, RXC_ to EP .....-0.5V to +3.9V
LMN_ to EP (15mA current limit) .....-0.5V to +3.9V
OUT+, OUT- to EP .....-0.5V to +1.9V
All Other Pins to EP ..... -0.5V to + (V_{IOVDD} + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply .....Continuous
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 47.6mW/°C above +70°C) 3809.5mW
Junction Temperature .....+150°C
Storage Temperature Range .....-65ºC to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: EP connected to PCB ground.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....1°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TWO-LEVEL INPUTS (HSPD, I2CSEL, $\overline{PWDN}$, CDS, MS, $\overline{AUTOS}$, CX/TP, SD, SCK, WS, CNTL1, CNTL2, SSEN, DRS, HIM)						
High-Level Input Voltage	V_{IH1}		0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}				0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}	-20		+20	µA
THREE-LEVEL INPUTS (ADD0, ADD1, BWS)						
High-Level Input Voltage	V_{IH2}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}				0.3 x V_{IOVDD}	V
Mid-Level Input Current	I_{INM}	(Note 3)	-10		+10	µA
Input Current	I_{IN2}		-150		+150	µA

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HOT-PLUG DETECT OUTPUT (HPD)							
High-Level Output Voltage	V_{OH1}	I_{OH} = -2mA		V_{HVDD} - 0.2			V
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS1}	V_O = 0V		16	35	64	mA
SINGLE-ENDED OUTPUTS (GPO, SD, SCK, WS, INTOUT)							
High-Level Output Voltage	V_{OH2}	I_{OH} = -2mA		V_{IOVDD} – 0.2			V
Low-Level Output Voltage	V_{OL2}	I_{OL} = 2mA				0.2	V
Output Short-Circuit Current	I_{OS2}	V_O = 0V	V_{IOVDD} = 3.0V to 3.6V	16	35	64	mA
			V_{IOVDD} = 1.7V to 1.9V	3	12	21	
OPEN-DRAIN INPUT/OUTPUTS (RX/SDA, TX/SCL, DDCSDA, DDCSCL, $\overline{LFLT}$)							
High-Level Input Voltage	V_{IH3}			0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL3}					0.3 x V_{IOVDD}	V
Input Current	I_{IN3}	(Note 4)	RX/SDA, TX/SCL, DDCSDA, DDCSCL	-110		5	µA
			$\overline{LFLT}$	-80		5	
Low-Level Output Voltage	V_{OL3}	I_{OL} = 3mA	V_{IOVDD} = 1.7V to 1.9V			0.4	V
			V_{IOVDD} = 3.0V to 3.6V			0.3	
Capacitance	C_i	Each pin (Note 5)				10	pF
GMSL DIFFERENTIAL OUTPUTS (OUT+, OUT-)							
Differential Output Voltage	V_{OD}	Pre/deemphasis off		300	400	500	mV
		3.3dB preemphasis (Note 5)		350		610	
		3.3dB deemphasis		240		425	
Change in V_{OD} Between Complimentary Output States	ΔV_{OD}	Preemphasis off and deemphasis only				25	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off		1.1	1.4	1.56	V

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Change in V_{OS} Between Complimentary Output States	ΔV_{OS}				25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-62			mA
		V_{OUT+} or V_{OUT-} = 1.9V			25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			25	mA
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}	45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER (Internally Connected to OUT+, OUT-)						
High Switching Threshold	V_{CHR}	Legacy			27	mV
		High-immunity			40	
Low Switching Threshold	V_{CLR}	Legacy	-27			mV
		High-immunity	-40			
GMSL SINGLE-ENDED OUTPUTS (OUT+, OUT-)						
Single-Ended Output Voltage	V_{OUT}	Pre/deemphasis off	375	500	625	mV
		3.3dB preemphasis (Note 5)	435		765	
		3.3dB deemphasis	300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V			32	
Output Termination Resistance (Internal)	R_O	From OUT+ or OUT- to V_{AVDD}	45	54	63	Ω
LINE-FAULT DETECTION INPUTS (LMN0, LMN1)						
Short-to-GND Threshold	V_{TG}				0.3	V
Normal Thresholds	V_{TN}		0.57		1.07	V
Open Thresholds	V_{TO}		1.45		V_{IO} + 0.06	V
Open Input Voltage	V_{IO}		1.47		1.75	V
Short-to-Battery Threshold	V_{TE}		2.47			V
HDMI DIFFERENTIAL INPUTS (RX_, RXC_)						
Input Differential Voltage Level	V_{IDIFF1}	(Note 5)	150		1200	mV_{P-P}

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Voltage Level	V_{DIFFD}	Source disabled or disconnected		-10		10	mV
Input Common-Mode Voltage	V_{ICM}	DC-coupled (Note 5)		V_{HVDD} - 300		V_{HVDD} - 37.5	mV
		AC-coupled (Note 5)		V_{HVDD} - 10		V_{HVDD} + 10	
Termination Resistance	R_T	Each pin to V_{HVDD} (Note 5)	TERM_CNTL = '010' (default)	49	55	61	Ω
			TERM_CNTL = '011'	44	50	56	
CRYSTAL OSCILLATOR (X1, X2)							
Frequency		Fundamental mode only; includes crystal tolerance			27		MHz
Input Capacitance	C_{X1}, C_{X2}	Each pin			4		pF
Load Capacitance	C_{L1}, C_{L2}	XTAL property			18		pF
OSCILLATOR INPUT (X1)							
High-Level Input Voltage	V_{IHX}	X1 as frequency Input		0.70 x V_{XVDD}			V
Low-Level Input Voltage	V_{ILX}	X1 as frequency Input				0.30 x V_{XVDD}	V
Input Current	I_{INX}	V_{IN} = 0 to V_{XVDD}		-5		+5	µA
Input Frequency Range		X1 as frequency Input (Note 5)		26		28.5	MHz

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Worst-Case Pattern Supply Current, DRS = low) (Notes 6, 7)	I_{WCS2}	$f_{RXC\_}$ = 25MHz BWS = high	HVDD		46	61	mA
			RVDD + AVDD + DVDD		172	237	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	
		$f_{RXC\_}$ = 78MHz BWS = high	HVDD		46	61	
			RVDD + AVDD + DVDD		297	425	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	
		$f_{RXC\_}$ = 36.66MHz BWS = open	HVDD		46	61	
			RVDD + AVDD + DVDD		195	275	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	
		$f_{RXC\_}$ = 104MHz BWS = open	HVDD		46	61	
			RVDD + AVDD + DVDD		347	500	
			PLLVDD + XVDD		11	16	
			IOVDD (3.0V to 3.6V)		2	2	
			IOVDD (1.7V to 1.9)		0.5	0.6	

DC Electrical Characteristics (continued)

(V_{RVDD} = V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ± 1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Sleep-Mode Supply Current	I_{CCS}	Single wake-up receiver enabled				2	mA
Power-Down Supply Current	I_{CCZ}	$\overline{PWDN}$ = EP				2	mA
ESD PROTECTION							
OUT+, OUT- (Pin to EP)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF	Contact discharge		±8		
			Air discharge		±12		
		ISO 10605, R_D = 2kΩ, C_S = 330pF	Contact discharge		±10		
			Air discharge		±25		
All Other Pins (to EP or Supply)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±4		kV
		Machine Model			±250		V
All Other Pins (to All Other Pins)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF			±2.5		kV

AC Electrical Characteristics

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPEN-DRAIN OUTPUTS (RX/SDA, TX/SCL)							
Output Rise Time	t_R	0.3 x V_{IOVDD} to 0.7 x V_{IOVDD}, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
Output Fall Time	t_F	0.7 x V_{IOVDD} to 0.3 x V_{IOVDD}, C_L = 10pF to 100pF, 1kΩ pullup to V_{IOVDD}		20		150	ns
I^2C (SDA, SCL, DDCSDA, DDCSCL) (see Figure 6) (Note 8)							
SCL Clock Frequency	f_{SCL}		Low range	9.6		100	kHz
			Mid range	> 100		400	
			High range	> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			

AC Electrical Characteristics (continued)

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low Period of SCL Clock	t_{LOW}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range	Low	4.7			µs
			Mid	0.6			
			High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range	Low	0			µs
			Mid	0			
			High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range	Low	250			ns
			Mid	100			
			High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range	Low	4.0			µs
			Mid	0.6			
			High	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range	Low	4.7			µs
			Mid	1.3			
			High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range	Low			3.45	µs
			Mid			0.9	
			High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range	Low			50	ns
			Mid			50	
			High			50	
Capacitive Load Each Bus Line	C_B					100	pF
SINGLE-ENDED OUTPUTS (GPO, SD, SCK, WS, INTOUT)							
Rise-and-Fall Time	t_R, t_F	20% to 80%, C_L = 10pF (Note 5)	V_{IOVDD} = 1.7V to 1.9V	0.5		3.6	ns
			V_{IOVDD} = 3.0 to 3.6V	0.3		2.2	

AC Electrical Characteristics (continued)

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GMSL DIFFERENTIAL OUTPUTS (OUT+, OUT-)							
Rise-and-Fall Time	t_R, t_F	20% to 80%, V_{OD} ≥ 400mV, R_L = 100Ω, serial bit rate = 3.12Gbps (Note 5)			90	160	ps
Total Serial Output Jitter	t_{TSOJ1}	3.12Gbps PRBS, measured at V_{OD} = 0V, pre/deemphasis disabled			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.12Gbps PRBS, measured at V_{OD} = 0V, pre/deemphasis disabled			0.15		UI
GMSL SINGLE-ENDED OUTPUT (OUT+ or OUT-)							
Rise-and-Fall Time	t_R, t_F	20% to 80%, V_O ≥ 500mV, R_L = 50Ω, serial bit rate = 3.12Gbps (Note 5)			90	160	ps
Total Serial Output Jitter	t_{TSOJ1}	3.12Gbps PRBS, measured at V_O/2, pre/deemphasis disabled			0.25		UI
Deterministic Serial Output Jitter	t_{DSOJ2}	3.12Gbps PRBS, measured at V_O/2, pre/deemphasis disabled			0.15		UI
HDMI DIFFERENTIAL INPUTS (RX_ _, RXC_) (Note 5)							
Input Differential Voltage Level	V_{IDIFF2}	.		150		1560	mV_{P-P}
Intra-Pair Skew	t_{SKEW1}					0.4 x t_{BIT}	ns
Inter-Pair Skew	t_{SKEW2}					0.2 x t_{CHAR} + 1.78	ns
Clock Frequency	f_{RxC}	BWS = high, DRS = low		25		78	MHz
		BWS = open, DRS = low		36.6		104	
		BWS = open, DRS bit = high		25		52	
TMDS Clock-Jitter Tolerance	t_{JTMDS}	Relative to ideal recovery clock				0.3 x t_{BIT}	ns
Termination Impedance	Z_{TERM}	TDR rise time ≤ 200ps, 10% to 90%	V_{ICM} within V_{ICM2} range, AC-coupled, V_{HVDD} ±10mV (Note 9)	65	100	135	Ω
GENERAL TIMING							
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to MAX9291/MAX9293 GPO				350	µs

AC Electrical Characteristics (continued)

(V_{RVDD} =V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, V_{HVDD} = 3.135V to 3.465V, V_{IOVDD} = 1.7V to 3.6V, V_{PLLVDD} = V_{XVDD} = 3.0V to 3.6V, R_L = 100Ω ±1% (differential), R_L = 50Ω ±1% (single-ended), EP connected to PCV PCB ground, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C.)

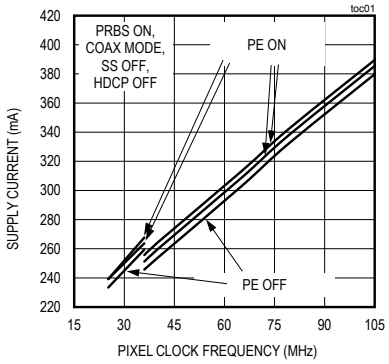
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Device Delay	t_{SD}	(Notes 5, 10)	Spread spectrum enabled	83		174	Bits
			Spread spectrum disabled	99		126	
Link Start Time	t_{LOCK}	PLLs locked				3.5	ms
Power-Up Time	t_{PU}					8	ms
I^2S/TDM							
WS Frequency	f_{WS}			8		192	kHz
Sample Word Length	n_{WS}			8		32	Bits
SCK Frequency	f_{SCK}	$f_{SCK} = f_{WS} \times n_{WS} \times (2 \text{ or } 8)$		(8 x 8) x 2		(192 x 32) x 8	kHz
SCK Clock High Time	t_{HC}	$V_{SCK} \geq V_{IH}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SCK Clock Low Time	t_{LC}	$V_{SCK} \leq V_{IL}$, $t_{SCK} = 1/f_{SCK}$		0.35 x t_{SCK}			ns
SD, WS Setup Time	t_{SET}			2			ns
SD, WS Hold Time	t_{HOLD}			2			ns

Note 3: For mid-level, leave the input open. If driven, put driver in high impedance with high-impedance leakage current ±10µA (max).
Note 4: IIN MIN due to voltage drop across the internal pullup resistor.
Note 5: Not production tested. Guaranteed by design.
Note 6: Typical values measured at V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, V_{RVDD} = V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V.
Note 7: HDCP not enabled (MAX9293 only).
Note 8: DDCSDA and DDCSCL specified for operation in 100kHz (low range) only. Characterized at 100kHz and 400kHz..
Note 9: A single excursion is permitted to 100Ω ±25% with duration less than 250ps.
Note 10: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = open. Bit time = 1/(40 x f_{PCLKIN}) for BWS = high.

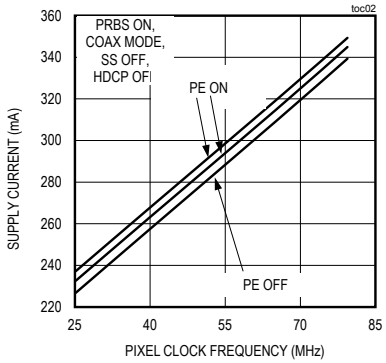
Typical Operating Characteristics

(V_{RVDD} = V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, V_{HVDD} = V_{PLLVDD} = V_{XVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)

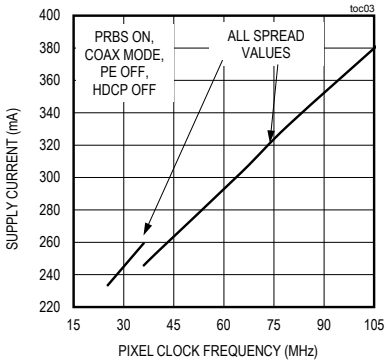
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = OPEN)



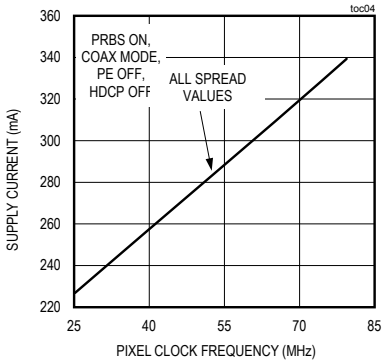
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = HIGH)



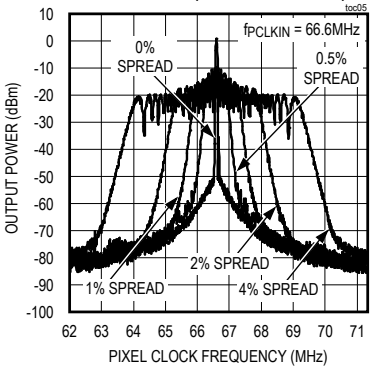
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = OPEN)



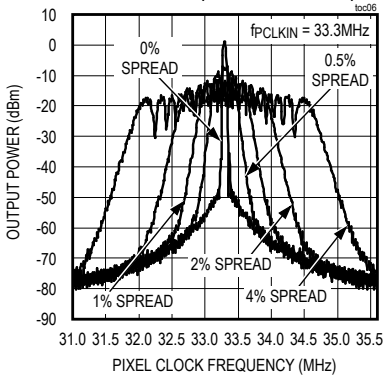
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = HIGH)



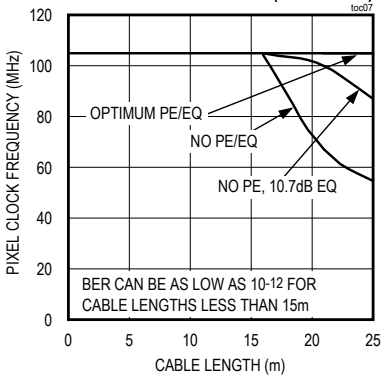
OUTPUT SPECTRUM vs. PIXEL CLOCK FREQUENCY (VARIOUS SPREAD)



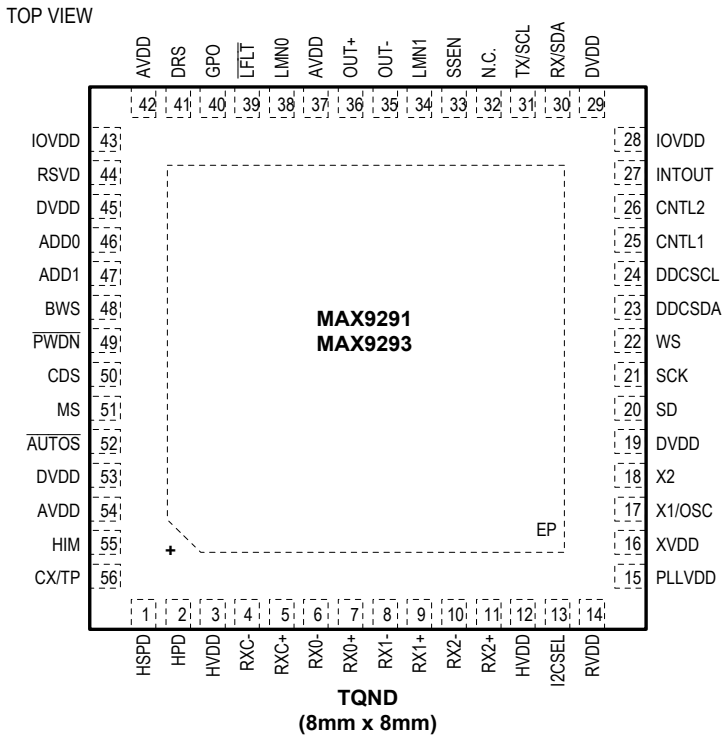
OUTPUT SPECTRUM vs. PIXEL CLOCK FREQUENCY (VARIOUS SPREAD)



MAXIMUM PIXEL CLOCK FREQUENCY vs. COAX CABLE LENGTH (BER ≤ 10^{-10})



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	HSPD	HDMI Source Power-Detect Input. Internal pulldown to EP Connect a voltage-divider to divide the 5V HDMI voltage down to V_{IOVDD}.
2	HPD	HDMI Hot-Plug Detect Output
3, 12	HVDD	3.135 to 3.465V HDMI Input Termination Power Supply. Bypass HVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to HVDD.
4, 5	RXC-, RXC+	HDMI Clock Inputs with Internal 50Ω Termination to HVDD
6–11	RX_-, RX_+	HDMI Data Inputs with Internal 50Ω Termination to HVDD
13	I2CSEL	I^2C Select. Control-channel interface protocol select input with internal pulldown to EP. Set I2CSEL = high to select I^2C-to-I^2C interface. Set I2CSEL = low to select UART-to-UART or UART-to-I^2C interface.
14	RVDD	1.8V HDMI Receiver Input Power Supply. Bypass RVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to RVDD.
15	PLLVDD	3.3V PLL Power Supply. Bypass PLLVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to PLLVDD.
16	XVDD	3.3V Crystal Oscillator Power Supply. Bypass XVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to XVDD.
17	X1/OSC	Crystal/Oscillator Input. If crystal used, connect to one terminal of a 27MHz crystal..

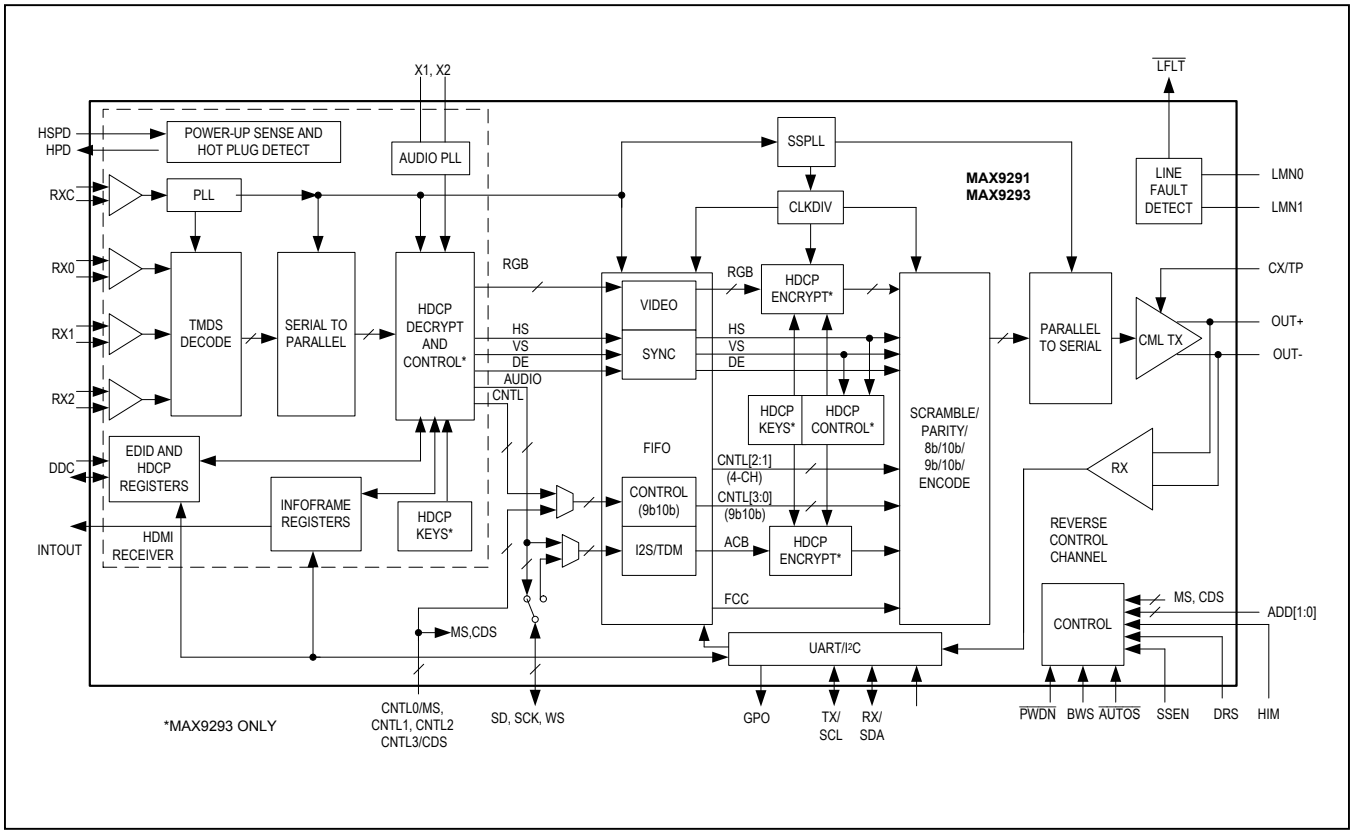
Pin Description (continued)

PIN	NAME	FUNCTION
18	X2	Crystal Input. Connect to one terminal of a 27MHz crystal.
19, 29, 45, 53	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.
20	SD	I^2S/TDM Serial-Data Input/Output with Internal Pulldown to EP. Outputs HDMI audio data or accepts external audio data (encrypted when HDCP is enabled). Disable I^2S/TDM encoding to use SD as an additional control/data input valid on the selected edge of the pixel clock.
21	SCK	I^2S/TDM Serial-Clock Input/Output with Internal Pulldown to EP. Outputs HDMI audio bit clock data or accepts external audio bit clock.
22	WS	I^2S/TDM Word-Select Input/Output with Internal Pulldown to EP. Outputs HDMI audio word select clock or accepts external audio word select clock.
23	DDCSDA	DDC I^2C Serial-Data Input/Output with Internal 40kΩ Pullup to IOVDD. Used by the HDMI source to read the EDID.
24	DDCSCL	DDC I^2C Serial-Clock Input/Output with Internal 40kΩ Pullup to IOVDD. Used by the HDMI source to read the EDID.
25	CNTL1	Control Input with Internal Pulldown to EP. Input data is latched every PCLK cycle (Figure 15). CNTL1 or the HDMI control signal is mapped to internal bit DIN27/CNTL1. CNTL1 not encrypted when HDCP is on (MAX9293 only).
26	CNTL2	Control Input with Internal Pulldown to EP. Input data is latched every PCLK cycle (Figure 15). CNTL1 or the HDMI control signal is mapped to internal bit DIN28/CNTL2. CNTL2 not encrypted when HDCP is on (MAX9293 only).
27	INTOUT	A/V Status Register Interrupt Output. Indicates new data in the A/V status registers. INTOUT is reset when the A/V status registers are read.
28, 43	IOVDD	I/O Supply Voltage. 1.8V to 3.3V Logic I/O Power Supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smallest value capacitor closest to IOVDD.
30	RX/SDA	UART Receive/I^2C Serial Data Input/Output with Internal 40kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. RX/SDA has an open-drain driver and requires a pullup resistor. RX: Input of the serializer's UART. SDA: Data input/output of the serializer's I^2C master/slave.
31	TX/SCL	UART Transmit/I^2C Serial-Clock Input/Output with Internal 40kΩ Pullup to IOVDD. Function is determined by the state of I2CSEL at power-up. TX/SCL has an open-drain driver and requires a pullup resistor. TX: Output of the serializer's UART. SCL: Clock input/output of the serializer's I^2C master/slave.
32	N.C.	Not Connected. Not internally connected.
33	SSEN	Spread-Spectrum Enable Input with Internal Pulldown to EP. The state of SSEN latches upon power-up or when resuming from power-down mode ($\overline{PWDN}$ = low). Set SSEN = high for ±0.5% spread spectrum on the serial link. Set SSEN = low to use the serial link without spread spectrum.
34	LMN1	Line-Fault Monitor Input 1 (see Figure 4 for details)
35	OUT-	Inverting Coax/Twisted-Pair Serial-Data Output
36	OUT+	Non-inverting Coax/Twisted-Pair Serial-Data Output

Pin Description (continued)

PIN	NAME	FUNCTION
37, 42, 54	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller capacitor closest to AVDD.
38	LMN0	Line-Fault Monitor Input 0 (see Figure 4 for details)
39	$\overline{\text{LFLT}}$	Active-Low Open-Drain Line-Fault Output. $\overline{\text{LFLT}}$ has a 60kΩ internal pullup to IOVDD. $\overline{\text{LFLT}}$ = low indicates a line fault. $\overline{\text{LFLT}}$ is output high when $\overline{\text{PWDN}}$ = low.
40	GPO	General-Purpose Output. GPO is low after power-up or when $\overline{\text{PWDN}}$ is low. GPO follows the state of the GPI (or INT) input on the deserializer.
41	DRS	Data-Rate Select Input with Internal Pulldown to EP. Set DRS = low, to select high data-rate mode. Set DRS = high, to select low data-rate mode.
44	RSVD	Reserved. Connect to IOVDD.
46	ADD0	Three-Level Address Selection Input. The state of ADD0 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1 for details.
47	ADD1	Three-Level Address Selection Input. The state of ADD1 latches at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). See Table 1 for details.
48	BWS	Three-Level Bus-Width Select Input. Set BWS to the same level on both sides of the serial link. Set BWS = high for 32-bit mode. Set BWS = open for high-bandwidth mode. Do not set BWS = low.
49	$\overline{\text{PWDN}}$	Active-Low, Power-Down Input with Internal Pulldown to EP. Set $\overline{\text{PWDN}}$ low to enter power-down mode to reduce power consumption.
50	CDS	Control Direction Selection with Internal Pulldown to EP. Set CDS = low when the control-channel master µC is connected to the MAX9291/MAX9293. Set CDS = high when the control-channel master µC is connected to the deserializer.
51	MS	Mode Select input with Internal Pulldown to EP. Set MS = low, to select base mode. MS sets the control-link (see the *Control Channel and Register Programming* section).
52	$\overline{\text{AUTOS}}$	Active-Low Auto-Start Input With Internal Pulldown to GND. Set $\overline{\text{AUTOS}}$ = high, to disable serialization at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low). Set $\overline{\text{AUTOS}}$ = low, to enable serialization and automatic PLL range selection power-up or when resuming from power-down mode.
55	HIM	High-Immunity Mode Input. Default HIGHIMM bit value is latched at power-up or when resuming from power-down mode ($\overline{\text{PWDN}}$ = low) and is active-high. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value.
56	CX/TP	Coax/Twisted-Pair Input with Internal Pulldown to GND. Set CX/TP low for twisted-pair cable drive (differential output). Set CX/TP high for coax cable drive (single-ended output).
—	EP	Exposed Pad. EP is internally connected to device ground. EP **must** be connected to the PCB ground plane through an array of vias for proper thermal and electrical performance.

Functional Diagram



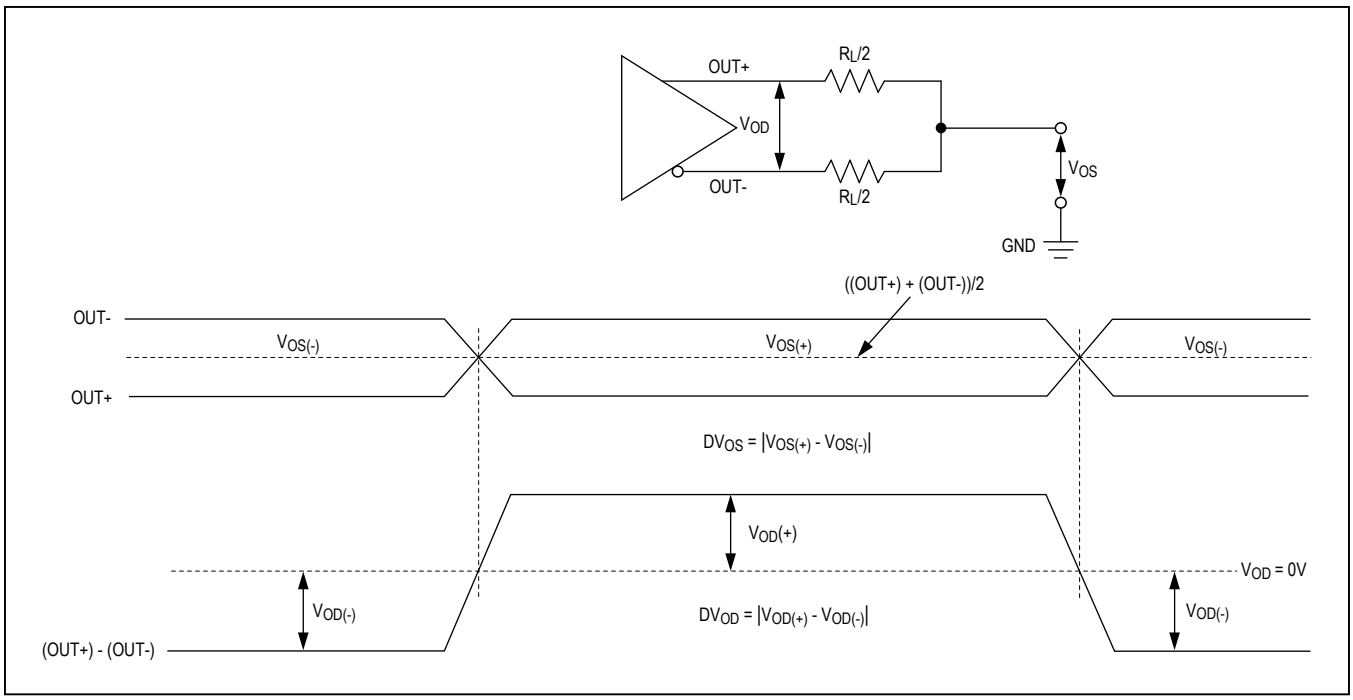


Figure 1. Serial Output Parameters

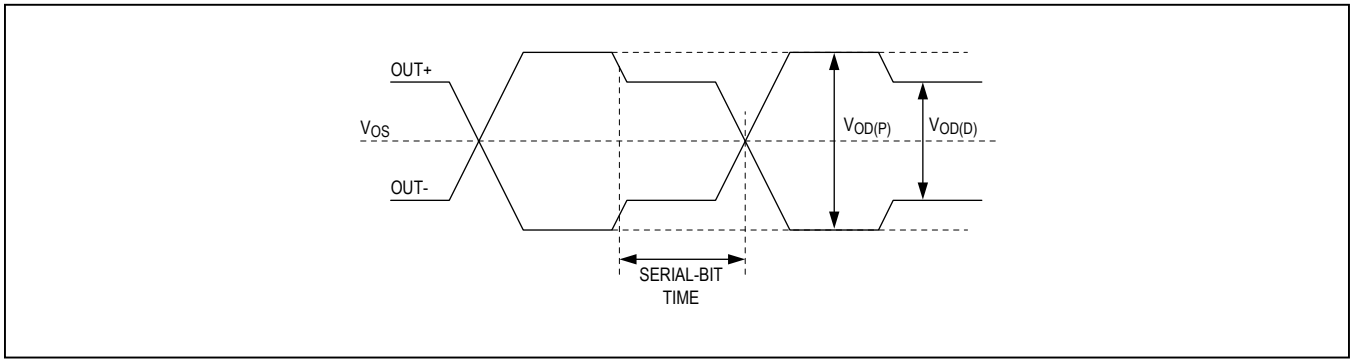


Figure 2. Output Waveforms at OUT+, OUT-

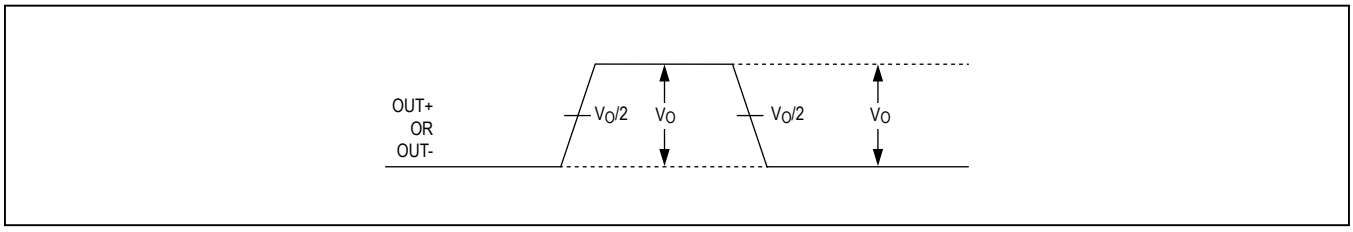


Figure 3. Single-Ended Output Template

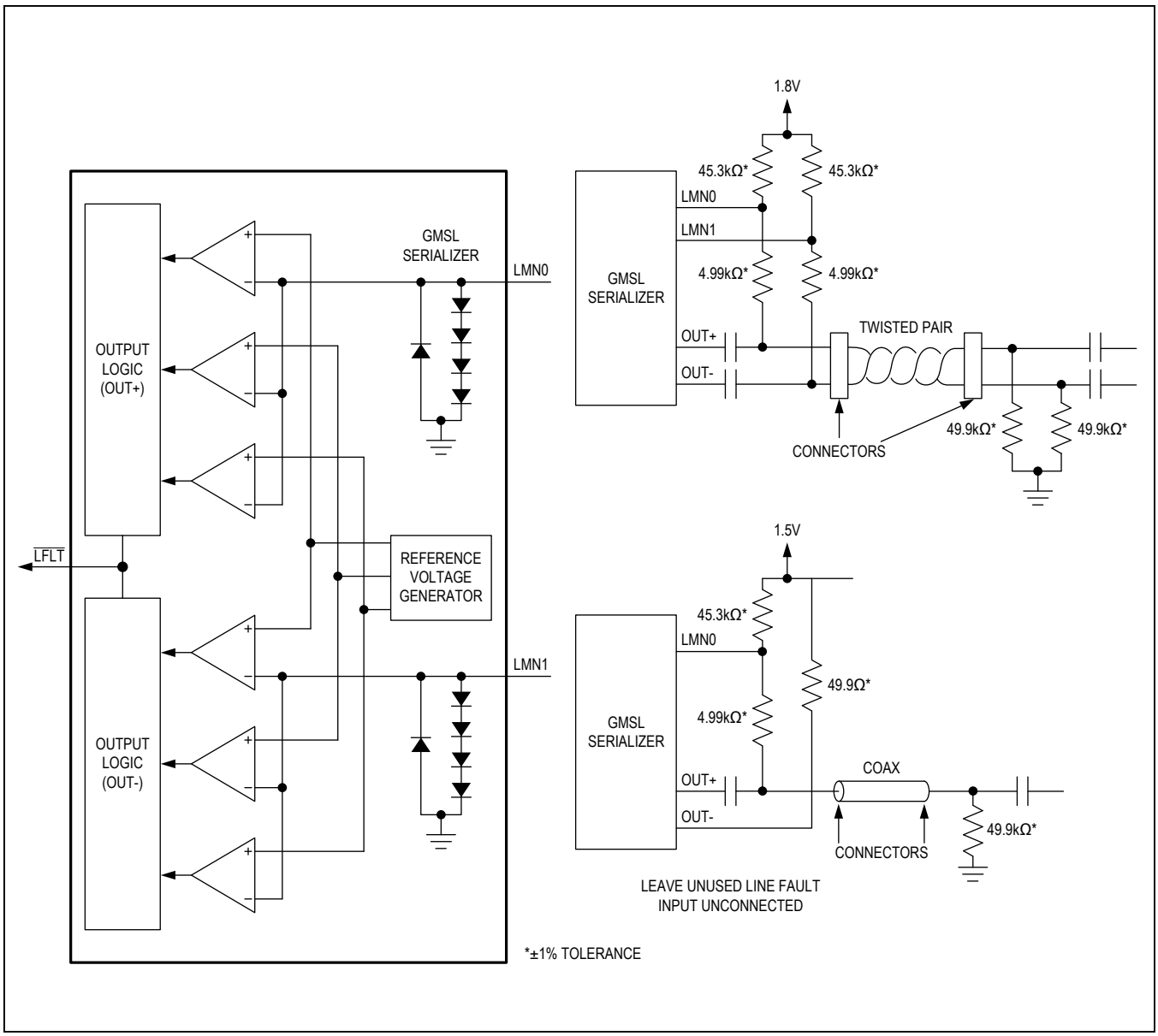


Figure 4. Line-Fault Detector Circuit

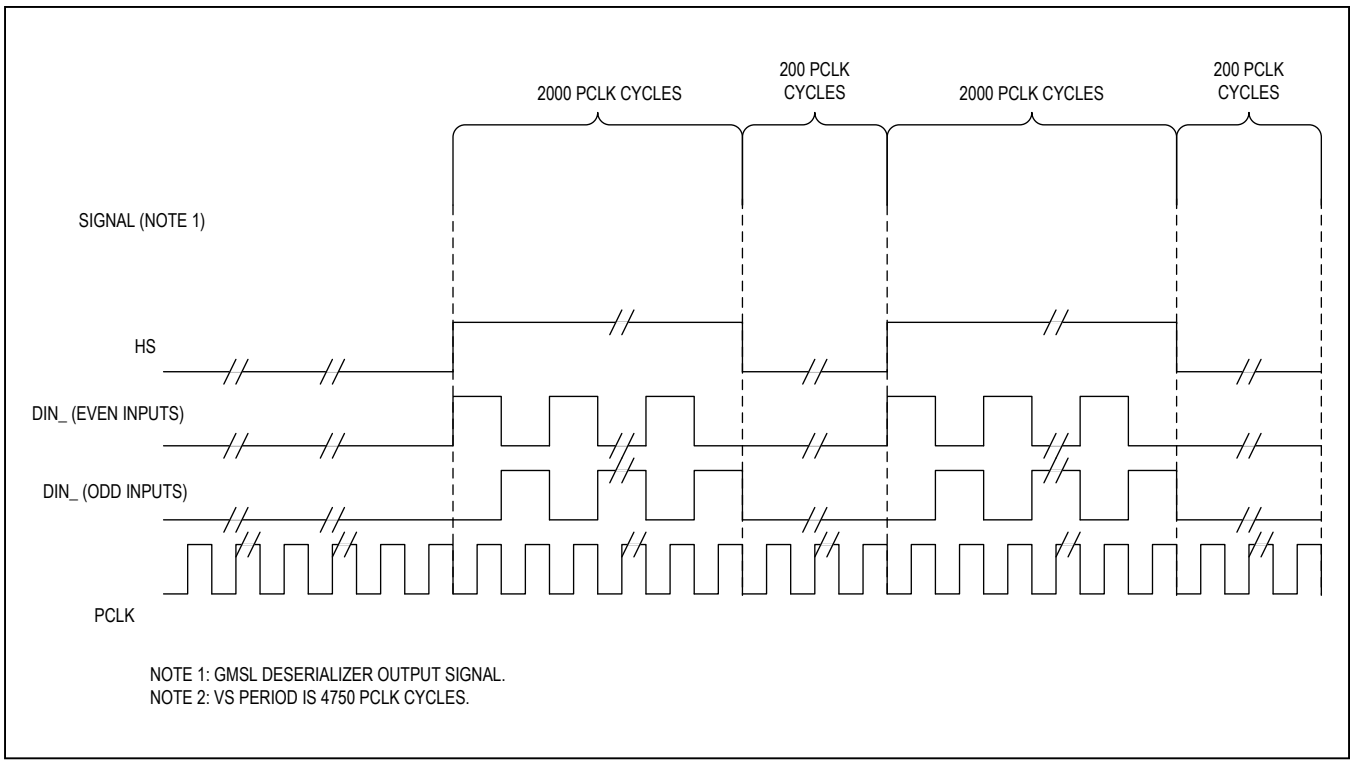


Figure 5. Worst-Case Pattern Input

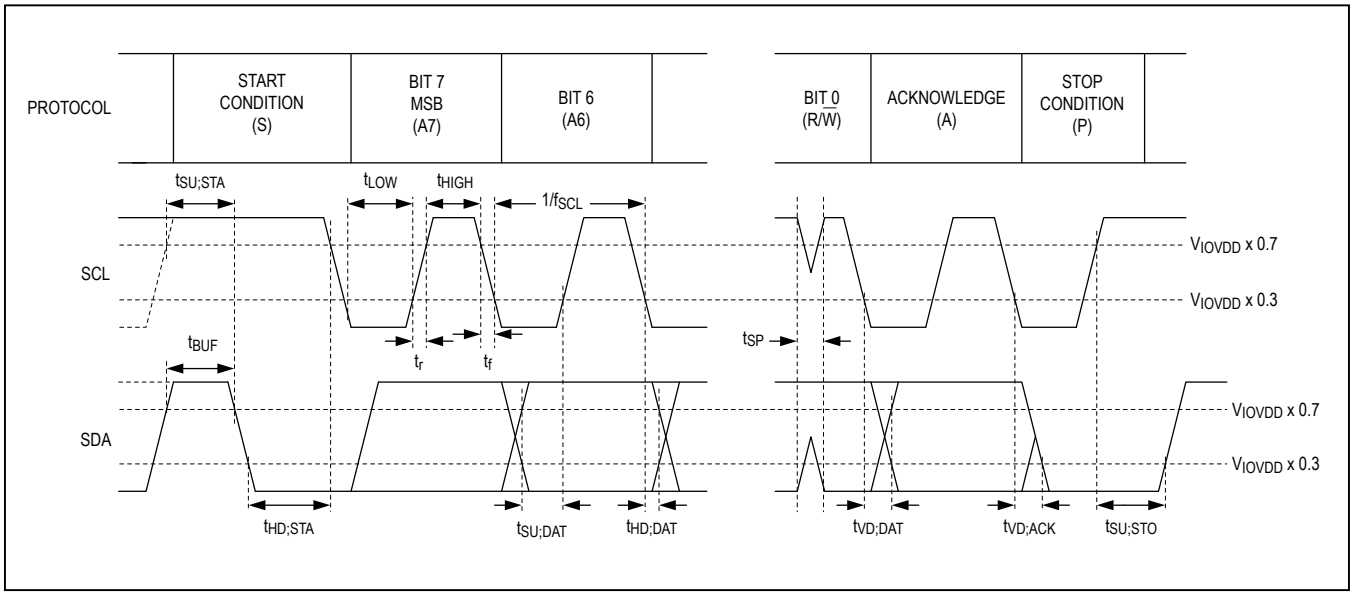


Figure 6. I^2C Timing Parameters

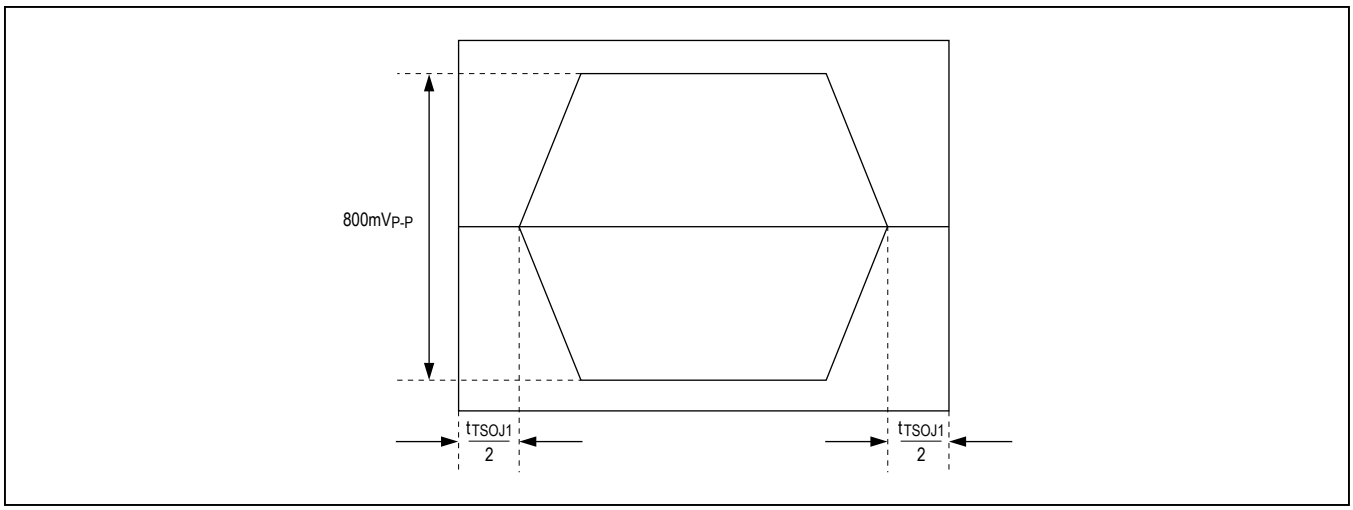


Figure 7. Differential Output Template

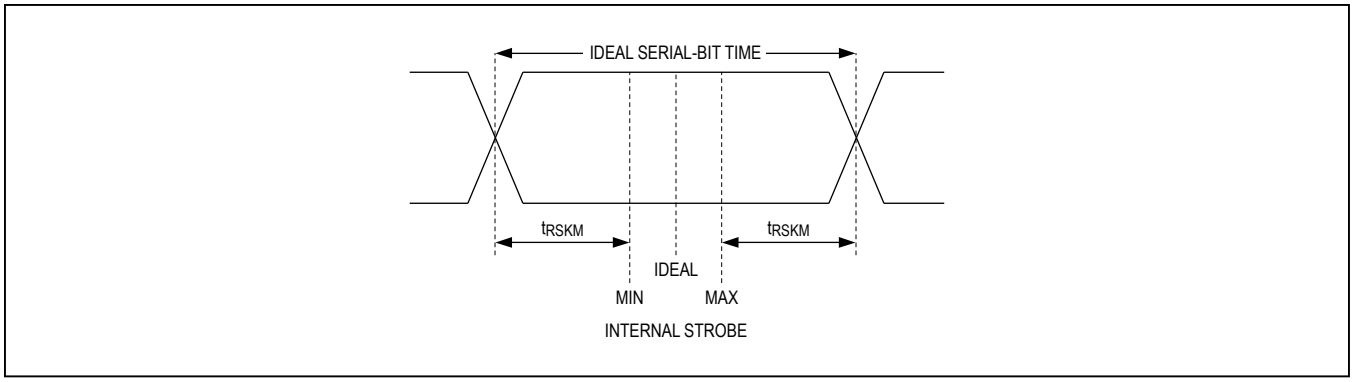


Figure 8. HDMI Receiver Input Skew Margin

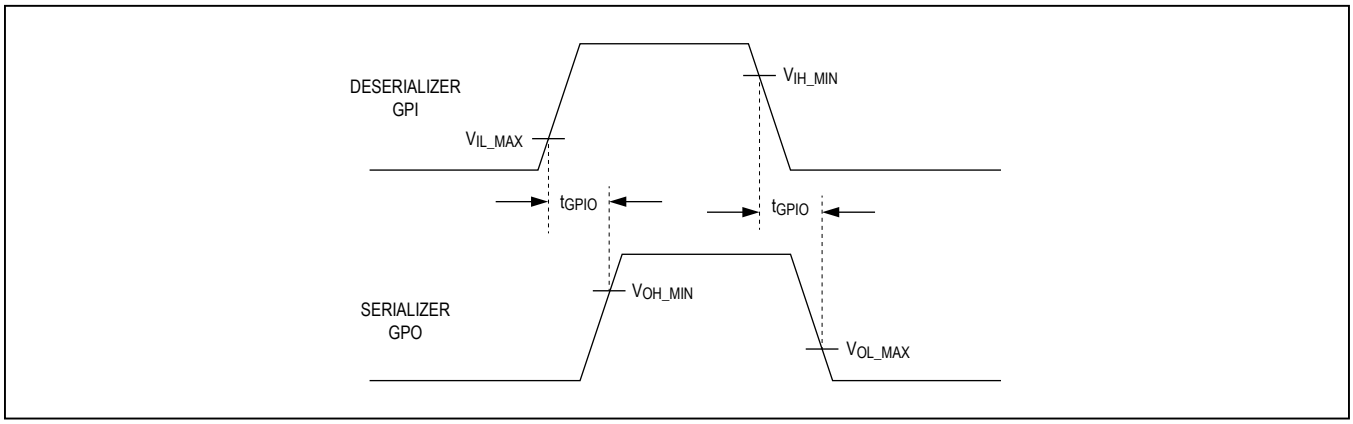


Figure 9. GPI-to-GPO Delay

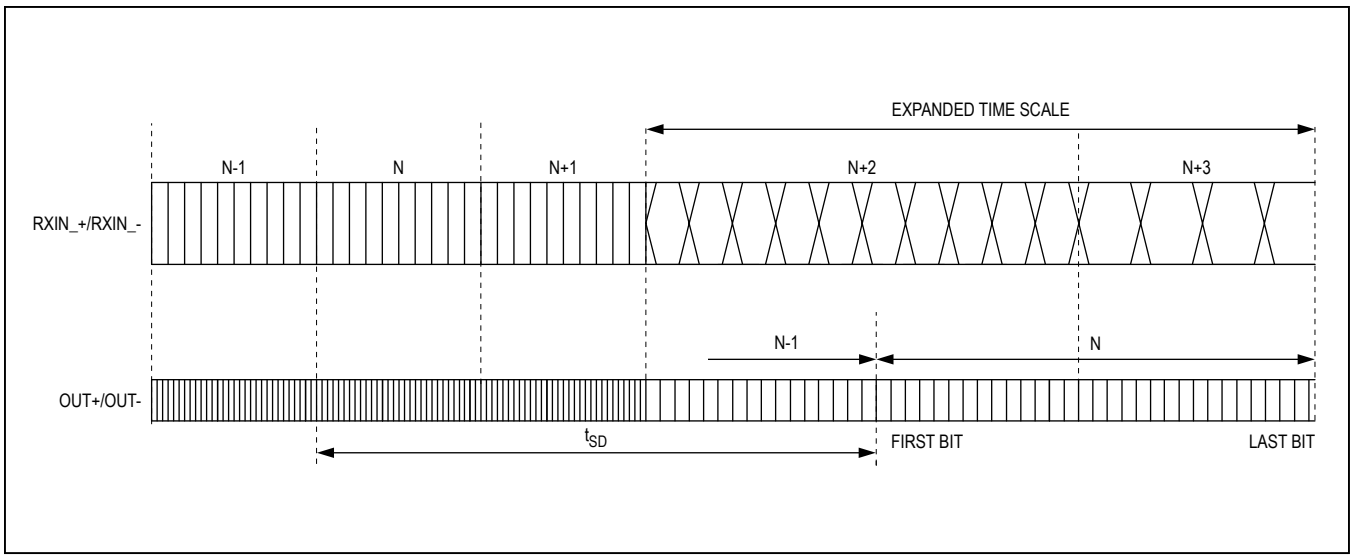


Figure 10. Serializer Delay

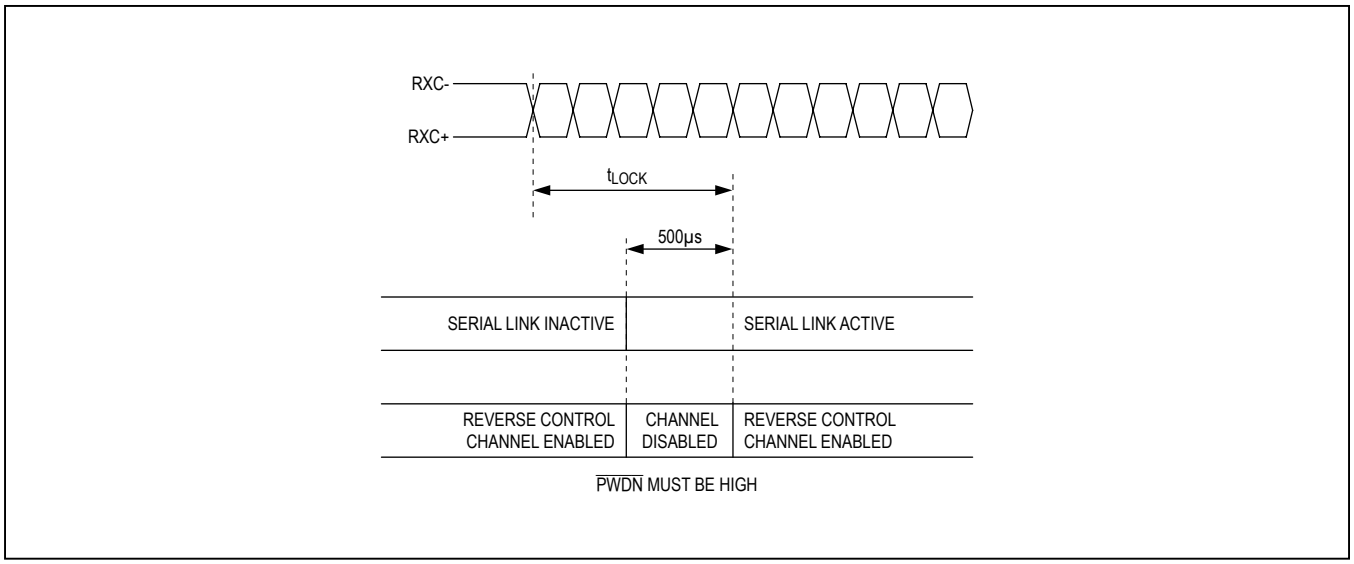


Figure 11. Link Startup Time