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19-2809; Rev 1; 10/09

LVDS/Anything-to-LVPECL/LVDS Dual Translator

General Description

The MAX9376 is a fully differential, high-speed, LVDS/anything-to-LVPECL/LVDS dual translator designed for signal rates up to 2GHz. One channel is LVDS/anything-to-LVPECL translator and the other channel is LVDS/anything-to-LVDS translator. The MAX9376's extremely low propagation delay and high speed make it ideal for various high-speed network routing and backplane applications.

The MAX9376 accepts any differential input signal within the supply rails and with minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. LVPECL outputs have sufficient current to drive 50Ω transmission lines. LVDS outputs conform to the ANSI EIA/TIA-644 LVDS standard.

The MAX9376 is available in a 10-pin µMAX® package and operates from a single +3.3V supply over the -40°C to +85°C temperature range.

Applications

Backplane Logic Standard Translation

LVDS-to-LVPECL, LVPECL-to-LVDS Up/Downconverters

LANs

WANs

DSLAMs

DLCs

Features

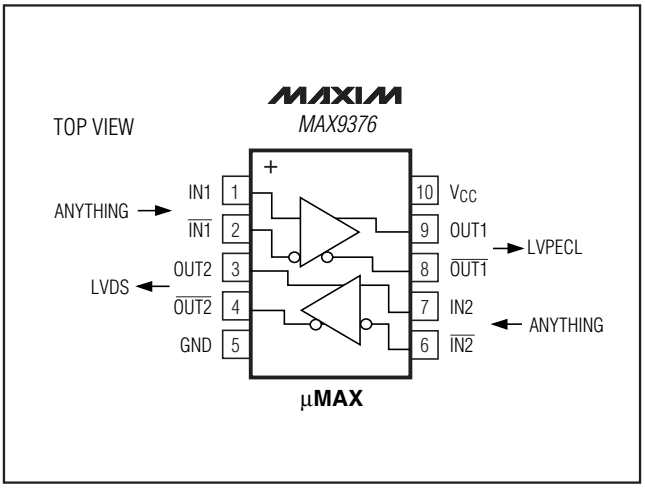
- **Guaranteed 2GHz Switching Frequency**
- **Accepts LVDS/LVPECL/Anything Inputs**
- **421ps (typ) Propagation Delays**
- **30ps (max) Pulse Skew**
- **2ps$_{RMS}$ (max) Random Jitter**
- **Minimum 100mV Differential Input to Guarantee AC Specifications**
- **Temperature-Compensated LVPECL Output**
- **+3.0V to +3.6V Power-Supply Operating Range**
- **>2kV ESD Protection (Human Body Model)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9376EUB+	-40°C to +85°C	10 µMAX

+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration



Functional Diagram appears at end of data sheet.

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LVDS/Anything-to-LVPECL/LVDS Dual Translator

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +4.1V
Inputs (IN_, $\overline{IN\_}$) .....-0.3V to (V_{CC} + 0.3V)
IN to $\overline{IN}$ .....±3.0V
Continuous Output Current 50mA
Surge Output Current 100mA
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
θ_{JA} in Still Air (Note 1) .....+180°C/W
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (IN_, $\overline{IN\_}$, OUT_, $\overline{OUT\_}$) .....≥2kV
Soldering Temperature (10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 3.0V, input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V), LVDS outputs terminated with 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUTS (IN_, $\overline{IN\_}$)												
Differential Input Threshold	V_{THD}		-100		+100	-100		+100	-100		+100	mV
Input Current	I_{IN}, $I_{\overline{IN}}$	V_{IN}, $V_{\overline{IN}}$ = V_{CC} or 0V	-20		+20	-20		+20	-20		+20	µA
Input Common-Mode Voltage	V_{CM}	Figure 1	0.05		V_{CC} - 0.05	0.05		V_{CC} - 0.05	0.05		V_{CC} - 0.05	V
LVPECL OUTPUTS (OUT1, $\overline{OUT1}$)												
Single-Ended Output High Voltage	V_{OH}	Figure 3	V_{CC} - 1.085	V_{CC} - 1.035	V_{CC} - 0.880	V_{CC} - 1.025	V_{CC} - 0.985	V_{CC} - 0.880	V_{CC} - 1.025	V_{CC} - 0.976	V_{CC} - 0.880	V
Single-Ended Output Low Voltage	V_{OL}	Figure 3	V_{CC} - 1.830	V_{CC} - 1.745	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.694	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.681	V_{CC} - 1.620	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 3	595	710		595	710		595	710		mV
LVDS OUTPUTS (OUT2, $\overline{OUT2}$)												
Differential Output Voltage	V_{OD}	Figure 2	250	366	450	250	352	450	250	339	450	mV
Change in Magnitude of V_{OD} Between Complementary Output States	$\|\Delta V_{OD}\|$	Figure 2		1.0	20		1.0	20		1.0	20	mV
Offset Common-Mode Voltage	V_{OS}	Figure 2	1.125		1.375	1.125	1.250	1.375	1.125		1.375	V
Change in Magnitude of V_{OS} Between Complementary Output States	$\|\Delta V_{OS}\|$	Figure 2		1.0	20		1.0	20		1.0	20	mV
Output Short-Circuit Current, Either Output Shorted to GND	$\|I_{OS}\|$	V_{ID} = ±100mV, one output GND, other output open or shorted to GND		19	24		18	24		18	24	mA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 3.0V, input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage V_{CM} = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V), LVDS outputs terminated with 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Notes 2, 3, 4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Short-circuit Current, Outputs Shorted Together	$\|I_{OSAB}\|$	V_{ID} = ±100mV, V_{OUT_+} = V_{OUT_-}		4.0	12		4.0	12		4.0	12	mA
SUPPLY												
Supply Current	I_{CC}	All pins open except V_{CC} and GND with LVDS outputs (OUT2, $\overline{OUT2}$) loaded with differential 100Ω		24	40		29	40		31	40	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input frequency ≤ 1.34GHz, differential input transition time = 125ps (20% to 80%), input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage (V_{CM}) = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V), LVDS outputs terminated with 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVPECL OUTPUTS						
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 250mV	2.0	2.5		GHz
Propagation Delay Low to High	t_{PLH}	Figure 3	250	421	600	ps
Propagation Delay High to Low	t_{PHL}	Figure 3	250	421	600	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figure 3 (Note 6)		6	30	ps
Output Low-to-High Transition	t_R	Figure 3		116	220	ps
Output High-to-Low Transition	t_F	Figure 3		119	220	ps
Added Random Jitter	t_{RJ}	f_{IN} = 1.34GHz (Note 7)		0.7	2	$ps_{(RMS)}$
LVDS OUTPUTS						
Switching Frequency	f_{MAX}	V_{OD} ≥ 250mV	2.0	2.5		GHz
Propagation Delay Low to High	t_{PLH}	Figure 3	250	363	600	ps
Propagation Delay High to Low	t_{PHL}	Figure 3	250	367	600	ps
Pulse Skew $\|t_{PLH} - t_{PHL}\|$	t_{SKEW}	Figure 3 (Note 6)		5	30	ps
Output Low-to-High Transition Time (20% to 80%)	t_R	Figure 2		93	220	ps
Output High-to-Low Transition Time (20% to 80%)	t_F	Figure 2		91	220	ps

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, differential input voltage $|V_{ID}|$ = 0.1V to 1.2V, input frequency ≤ 1.34GHz, differential input transition time = 125ps (20% to 80%), input voltage (V_{IN}, $V_{\overline{IN}}$) = 0 to V_{CC}, input common-mode voltage (V_{CM}) = 0.05V to (V_{CC} - 0.05V), LVPECL outputs terminated with 50Ω ±1% to (V_{CC} - 2.0V), LVDS outputs terminated with 100Ω ±1%, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, $|V_{ID}|$ = 0.2V, input common-mode voltage V_{CM} = 1.2V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Added Random Jitter	t_{RJ}	f_{IN} = 1.34GHz (Note 7)		0.8	2	ps(RMS)

Note 2: Measurements are made with the device in thermal equilibrium. All voltages are referenced to ground except V_{THD}, V_{ID}, V_{OD}, and ΔV_{OD}.

Note 3: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 4: DC parameters production tested at T_A = +25°C and guaranteed by design and characterization over the full operating temperature range.

Note 5: Guaranteed by design and characterization, not production tested. Limits are set at ±6 sigma.

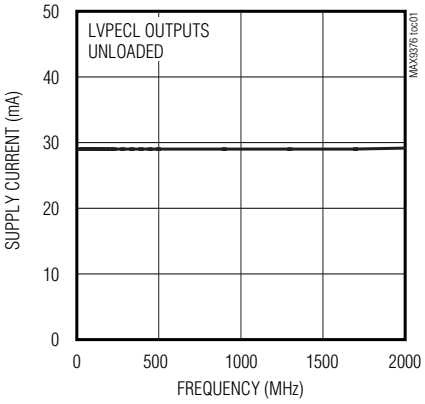
Note 6: t_{SKEW} is the magnitude difference of differential propagation delays for the same output under same conditions; $t_{SKEW} = |t_{PHL} - t_{PLH}|$.

Note 7: Device jitter added to the input signal.

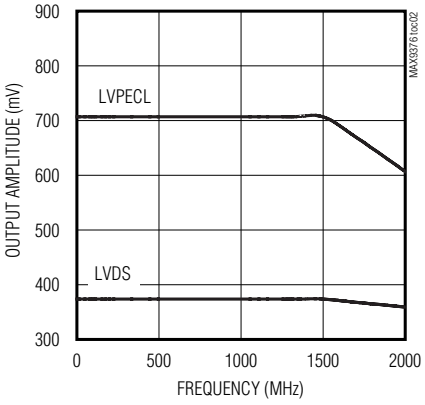
Typical Operating Characteristics

(V_{CC} = +3.3V, differential input voltage $|V_{ID}|$ = 0.2V, V_{CM} = 1.2V, input frequency = 500MHz, LVPECL outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, LVDS outputs terminated with 100Ω ±1%, T_A = +25°C, unless otherwise noted.)

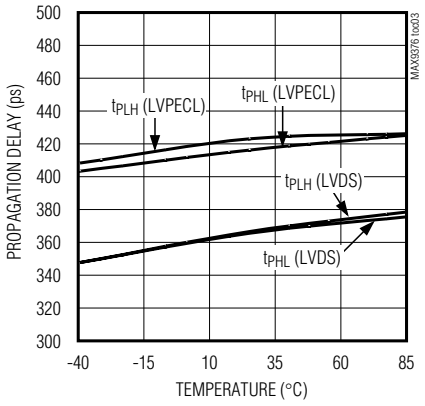
SUPPLY CURRENT vs. FREQUENCY



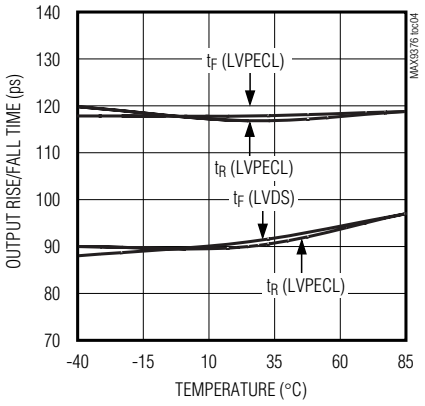
OUTPUT AMPLITUDE vs. FREQUENCY



PROPAGATION DELAY vs. TEMPERATURE



OUTPUT RISE/FALL TIME vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	IN1	Differential LVDS/Anything Noninverting Input 1
2	$\overline{IN1}$	Differential LVDS/Anything Inverting Input 1
3	OUT2	Differential LVDS Noninverting Output 2. Terminate with 100Ω ±1% to $\overline{OUT2}$.
4	$\overline{OUT2}$	Differential LVDS Inverting Output 2. Terminate with 100Ω ±1% to OUT2.
5	GND	Ground
6	$\overline{IN2}$	Differential LVDS/Anything Inverting Input 2
7	IN2	Differential LVDS/Anything Noninverting Input 2
8	$\overline{OUT1}$	Differential LVPECL Inverting Output. Terminate with 50Ω ±1% to V_{CC} - 2V.
9	OUT1	Differential LVPECL Noninverting Output. Terminate with 50Ω ±1% to V_{CC} - 2V.
10	V_{CC}	Positive Supply. Bypass from V_{CC} to GND with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Detailed Description

The MAX9376 is a fully differential, high-speed, LVDS/anything-to-LVPECL/LVDS dual translator designed for signal rates up to 2GHz. One channel is LVDS/anything-to-LVPECL translator and the other channel is LVDS/anything-to-LVDS translator. The MAX9376's extremely low propagation delay and high speed make it ideal for various high-speed network routing and backplane applications.

The MAX9376 accepts any differential input signal within the supply rails and with a minimum amplitude of 100mV. Inputs are fully compatible with the LVDS, LVPECL, HSTL, and CML differential signaling standards. LVPECL outputs have sufficient current to drive 50Ω transmission lines. LVDS outputs conform to the ANSI EIA/TIA-644 LVDS standard.

Inputs

Inputs have a wide common-mode range of 0.05V to V_{CC} - 0.05V, which accommodates any differential signals within rails, and requires a minimum of 100mV to switch the outputs. This allows the MAX9376 inputs to support virtually any differential signaling standard.

LVPECL Outputs

The MAX9376 LVPECL outputs are emitter followers that require external resistive paths to a voltage source (V_T = V_{CC} - 2.0V typ) more negative than worst-case V_{OL} for proper static and dynamic operation. When properly terminated, the outputs generate steady-state voltage levels, V_{OL} or V_{OH} with fast transition edges between state levels. Output current always flows into the termination during proper operation.

LVDS Outputs

The MAX9376 LVDS outputs require a resistive load to terminate the signal and complete the transmission loop. Because the device switches current and not voltage, the actual output voltage swing is determined by the value of the termination resistor. With a 3.5mA typical output current, the MAX9376 produces an output voltage of 350mV when driving a 100Ω load.

LVDS/Anything-to-LVPECL/LVDS Dual Translator

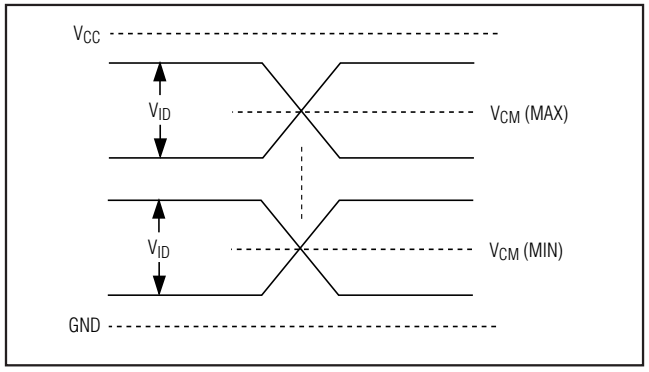


Figure 1. Input Definition

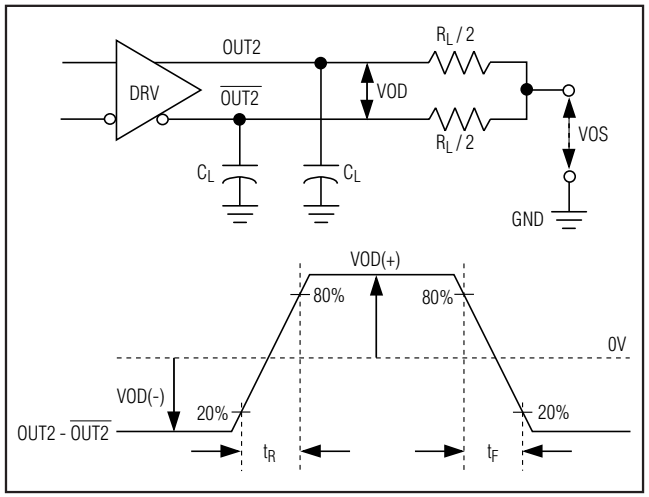


Figure 2. LVDS Output Load and Transition Times

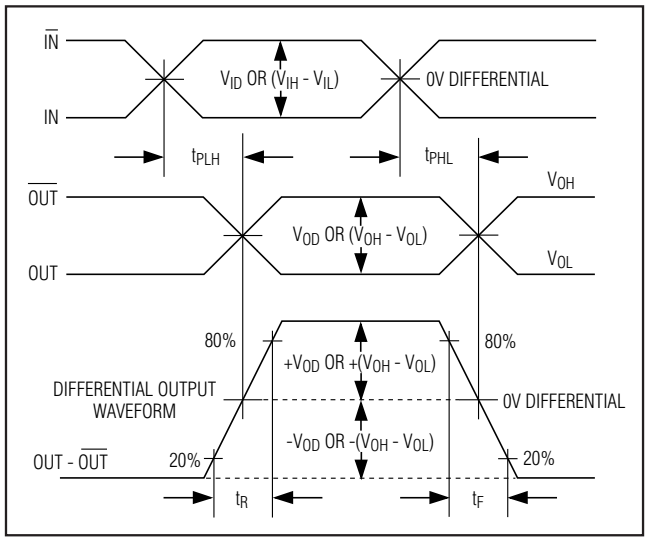


Figure 3. Differential Input-to-Output Propagation Delay Timing Diagram

Applications Information

LVPECL Output Termination

Terminate the MAX9376 LVPECL outputs with 50Ω to (V_{CC} - 2V) or use equivalent Thevenin terminations. Terminate OUT1 and $\overline{OUT1}$ with identical termination on each for low output distortion. When a single-ended signal is taken from the differential output, terminate both OUT1 and $\overline{OUT1}$.

Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

LVDS Output Termination

The MAX9376 LVDS outputs are current-steering devices; no output voltage is generated without a termination resistor. The termination resistors should match the differential impedance of the transmission line. Output voltage levels are dependent upon the value of the termination resistor. The MAX9376 is optimized for point-to-point interface with 100Ω termination resistors at the receiver inputs. Termination resistance values may range between 90Ω and132Ω, depending on the characteristic impedance of the transmission medium.

Supply Bypassing

Bypass V_{CC} to ground with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Chip Information

PROCESS: Bipolar

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
10µMAX	U10+2	21-0061

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/03	Initial release	—
1	10/09	Updated *Ordering Information* and *Absolute Maximum Ratings*	1, 2