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19-2688; Rev 0; 1/03

MAXIM

Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers

General Description

The MAX9389 is a fully differential, high-speed, low-jitter, 8-to-1 ECL/PECL multiplexer (mux) with dual output buffers. The device is designed for clock and data distribution applications, and features extremely low propagation delay (310ps typ) and output-to-output skew (30ps max).

Three single-ended select inputs, SEL0, SEL1, and SEL2, control the mux function. The mux select inputs are compatible with ECL/PECL logic, and are internally referenced to the on-chip reference output (V_{BB1}, V_{BB2}), nominally V_{CC} - 1.425V. The select inputs accept signals between V_{CC} and V_{EE}. Internal pulldowns to V_{EE} ensure a low default condition if the select inputs are left open.

The differential inputs D_, $\overline{D}$_ can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference output (V_{BB1}, V_{BB2}). All the differential inputs have internal bias and clamping circuits that ensure a low output state when the inputs are left open.

The MAX9389 operates with a wide supply range V_{CC} - V_{EE} of 2.375V to 5.5V. The device is offered in 32-pin TQFP and thin QFN packages, and operates over the -40°C to +85°C extended temperature range.

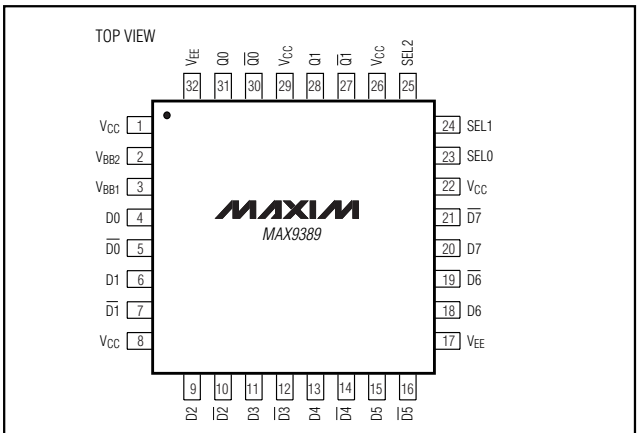
Applications

High-Speed Telecom and Datacom Applications

Central-Office Backplane Clock Distribution

DSLAM/DLC

Pin Configurations



TQFP

Pin Configurations continued at end of data sheet.

Features

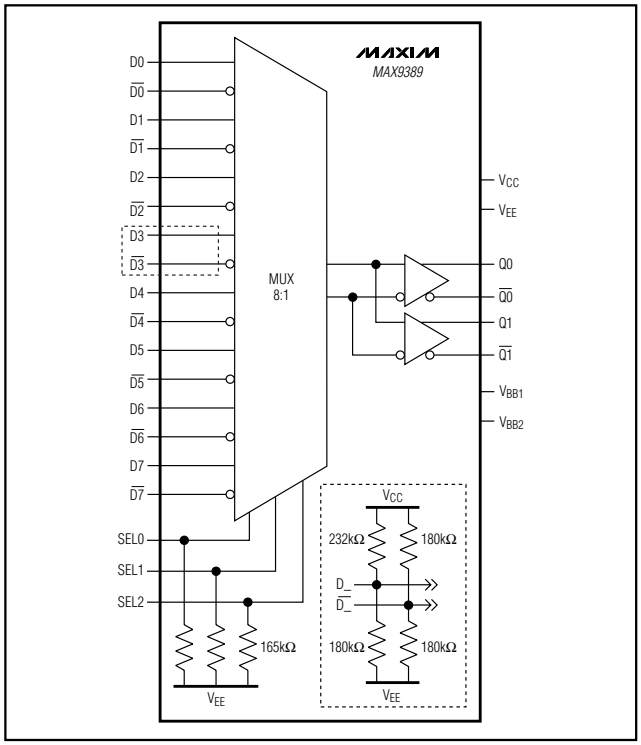
- **310ps Propagation Delay**
- **Guaranteed 2.7GHz Operating Frequency**
- **0.3ps$_{RMS}$ Random Jitter**
- **<30ps Output-to-Output Skew**
- **-2.375V to -5.5V Supplies for Differential LVECL/ECL**
- **+2.375V to +5.5V Supplies for Differential LVPECL/PECL**
- **Outputs Low for Open Inputs**
- **Dual Output Buffers**
- **>2kV ESD Protection (Human Body Model)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9389EHJ	-40°C to +85°C	32 TQFP
MAX9389ETJ*	-40°C to +85°C	32 Thin QFN

**Future product—contact factory for availability.*

Functional Diagram



Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} .....-0.3V to +6.0V
Inputs (D_, $\overline{D}$_, SEL_) to V_{EE} .....-0.3V to (V_{CC} + 0.3V)
D_ to $\overline{D}$_.....±3.0V
Continuous Output Current.....50mA
Surge Output Current.....100mA
V_{BB}_ Sink/Source Current .....±600µA
Continuous Power Dissipation (T_A = +70°C)
32-Lead TQFP (derate 13.1mW/°C above +70°C) ...1047mW
θ_{JA} in Still Air.....+76°C/W
θ_{JC} .....+25°C/W
32-Lead QFN (derate 21.3mW/°C above +70°C) 1702mW
θ_{JA} in Still Air.....+47°C/W
θ_{JC} .....+2°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (D_, $\overline{D}$_, Q_, $\overline{Q}$_, SEL_, V_{BB}_) .....≥2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT (D_, $\overline{D}$_, SEL_)												
Single-Ended Input High Voltage	V_{IH}	V_{BB}_ connected to the unused input, Figure 1	V_{CC} - 1.225		V_{CC} - 0.880	V_{CC} - 1.225		V_{CC} - 0.880	V_{CC} - 1.225		V_{CC} - 0.880	V
Single-Ended Input Low Voltage	V_{IL}	V_{BB}_ connected to the unused input, Figure 1	V_{CC} - 1.945		V_{CC} - 1.625	V_{CC} - 1.945		V_{CC} - 1.625	V_{CC} - 1.945		V_{CC} - 1.625	V
Differential Input High Voltage	V_{IHD}	Figure 1	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 1	V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	V
Differential Input Voltage	V_{IHD} - V_{ILD}	Figure 1, V_{CC} - V_{EE} < 3.0V	0.095		V_{CC} - V_{EE}	0.095		V_{CC} - V_{EE}	0.095		V_{CC} - V_{EE}	V
		Figure 1, V_{CC} - V_{EE} ≥ 3.0V	0.095		3.000	0.095		3.000	0.095		3.000	
Input Current	I_{IN}	V_{IH}, V_{IL}, V_{IHD}, V_{ILD}	-60		+60	-60		+60	-60		+60	µA
OUTPUT (Q_, $\overline{Q}$_)												
Single-Ended Output High Voltage	V_{OH}	Figure 2	V_{CC} - 1.145		V_{CC} - 0.895	V_{CC} - 1.145		V_{CC} - 0.895	V_{CC} - 1.145		V_{CC} - 0.895	V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V. Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, unless otherwise noted.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Single-Ended Output Low Voltage	V_{OL}	Figure 2	V_{CC} - 1.945		V_{CC} - 1.695	V_{CC} - 1.945		V_{CC} - 1.695	V_{CC} - 1.945		V_{CC} - 1.695	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 2	650	830		650	840		650	840		mV
REFERENCE OUTPUT ($V_{BB\_}$)												
Reference Voltage Output	V_{BB1} V_{BB2}	I_{BB1} + I_{BB2} = ±0.5mA (Note 5)	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V_{CC} - 1.525	V_{CC} - 1.425	V_{CC} - 1.325	V
POWER SUPPLY												
Supply Current	I_{EE}	(Note 6)		50	70		53	70		55	70	mA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, V_{IHD} - V_{ILD} = 0.15V to 1V, f_{IN} ≤ 2.5GHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, f_{IN} = 622 MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%.)) (Note 7)

PARAMETER	SYMBOL	CONDITIONS		-40°C			+25°C			+85°C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD}, t_{PHLD}	Figure 2		216	301	370	237	310	416	255	329	456	ps
SEL_-to-Output Delay	t_{PLH2}, t_{PHL2}	Figure 4, input transition time = 500ps (20% to 80%) (Note 8)			1.34	2		1.25	2		1.44	2	ns
Output-to-Output Skew	t_{SKOO}	Figure 5 (Note 9)				15			15			30	ps
Input-to-Output Skew	t_{SKIO}	Figure 6 (Note 10)				50			50			55	ps
Part-to-Part Skew	t_{SKPP}	(Note 11)				125			150			160	ps
Added Random Jitter (Note 12)	t_{RJ}	Clock pattern	f_{IN} = 156MHz		0.3	1.15		0.3	1.15		0.3	1.15	ps_{RMS}
			f_{IN} = 622MHz		0.3	1.15		0.3	1.15		0.3	1.15	
			f_{IN} = 2.5GHz		0.3	1.15		0.3	1.15		0.3	1.15	
Added Deterministic Jitter (Note 12)	T_{DJ}	PRBS 2^{23} - 1	f_{IN} = 156Mbps		33	95		33	95		33	95	ps_{P-P}
			f_{IN} = 622Mbps		21	61		21	61		21	61	

Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} - V_{EE} = 2.375V to 5.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, V_{IHD} - V_{ILD} = 0.15V to 1V, f_{IN} ≤ 2.5GHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%). Typical values are at V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, f_{IN} = 622 MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%.)) (Note 7)

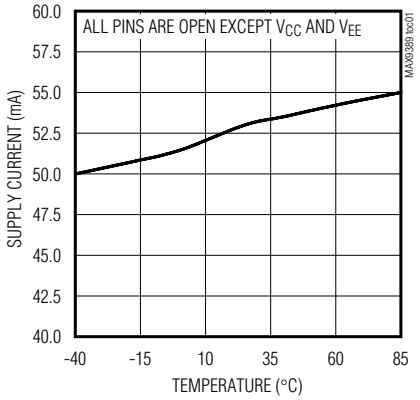
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV, Figure 2	2.7			2.7			2.7			GHz
Select Toggle Frequency	f_{SEL}	V_{OH} - V_{OL} ≥ 300mV, Figure 4	100			100			100			MHz
Output Rise and Fall Time (20% to 80%)	t_R, t_F	Figure 2	67	105	138	74	117	155	81	128	165	ps

Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into an I/O pin is defined as positive. Current out of an I/O pin is defined as negative.
Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design over the full operating temperature range.
Note 4: Single-ended data input operation using $V_{BB\_}$ is limited to (V_{CC} - V_{EE}) ≥ 3.0V.
Note 5: Use $V_{BB\_}$ only for inputs that are on the same device as the $V_{BB\_}$ reference.
Note 6: All pins open except V_{CC} and V_{EE}.
Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 8: Measured from the 50% point of the input signal with the 50% point equal to V_{BB}, to the 50% point of the output signal.
Note 9: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 10: Measured between input-to-output paths of the same part at the signal crossing points for a same-edge transition of the differential input signal.
Note 11: Measured between outputs of different parts at the signal crossing points under identical conditions for a same-edge transition.
Note 12: Device jitter added to the differential input signal.

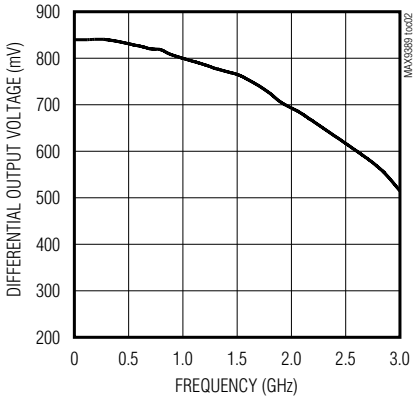
Typical Operating Characteristics

(V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, f_{IN} = 622MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%), unless otherwise noted.)

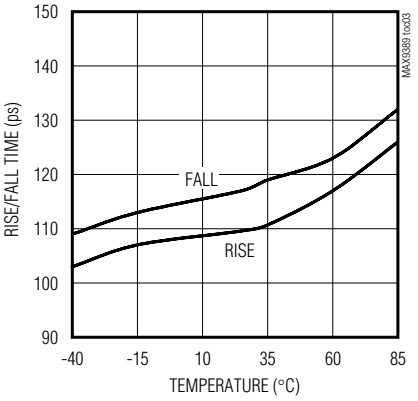
SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL OUTPUT VOLTAGE (V_{OH} - V_{OL}) vs. FREQUENCY



OUTPUT RISE/FALL TIME vs. TEMPERATURE

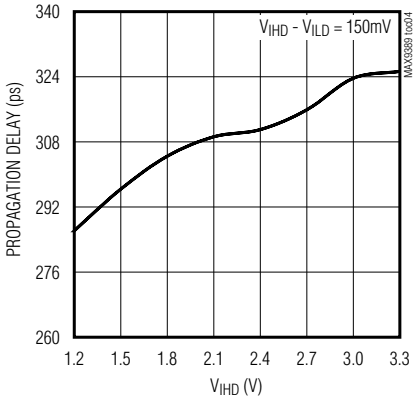


Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers

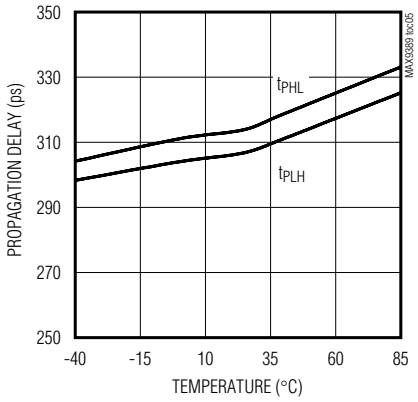
Typical Operating Characteristics (continued)

(V_{CC} - V_{EE} = 3.3V, V_{IHD} = V_{CC} - 1V, V_{ILD} = V_{CC} - 1.5V, outputs loaded with 50Ω ±1% to V_{CC} - 2V, f_{IN} = 622MHz, input duty cycle = 50%, input transition time = 125ps (20% to 80%), unless otherwise noted.)

PROPAGATION DELAY vs. HIGH VOLTAGE OF DIFFERENTIAL INPUT (V_{IHD})



PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 8, 22, 26, 29	V_{CC}	Positive Supply Input. Bypass each V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	V_{BB2}	Reference Output Voltage 2. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass V_{BB2} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
3	V_{BB1}	Reference Output Voltage 1. Connect to the inverting or noninverting data input to provide a reference for single-ended operation. When used, bypass V_{BB1} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
4	D0	Noninverting Differential Input 0. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
5	$\overline{D0}$	Inverting Differential Input 0. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
6	D1	Noninverting Differential Input 1. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
7	$\overline{D1}$	Inverting Differential Input 1. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
9	D2	Noninverting Differential Input 2. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
10	$\overline{D2}$	Inverting Differential Input 2. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
11	D3	Noninverting Differential Input 3. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
12	$\overline{D3}$	Inverting Differential Input 3. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
13	D4	Noninverting Differential Input 4. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
14	$\overline{D4}$	Inverting Differential Input 4. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
15	D5	Noninverting Differential Input 5. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
16	$\overline{D5}$	Inverting Differential Input 5. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
17, 32	V_{EE}	Negative Supply Input
18	D6	Noninverting Differential Input 6. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
19	$\overline{D6}$	Inverting Differential Input 6. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.

Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers

Pin Description (continued)

PIN	NAME	FUNCTION
20	D7	Noninverting Differential Input 7. Internal 232kΩ to V_{CC} and 180kΩ to V_{EE}.
21	$\overline{D7}$	Inverting Differential Input 7. Internal 180kΩ to V_{CC} and 180kΩ to V_{EE}.
23	SEL0	Select Logic Input 0. Internal 165kΩ pulldown to V_{EE}.
24	SEL1	Select Logic Input 1. Internal 165kΩ pulldown to V_{EE}.
25	SEL2	Select Logic Input 2. Internal 165kΩ pulldown to V_{EE}.
27	$\overline{Q1}$	Inverting Output 1. Typically terminate with 50Ω resistor to V_{CC} - 2V.
28	Q1	Noninverting Output 1. Typically terminate with 50Ω resistor to V_{CC} - 2V.
30	$\overline{Q0}$	Inverting Output 0. Typically terminate with 50Ω resistor to V_{CC} - 2V.
31	Q0	Noninverting Output 0. Typically terminate with 50Ω resistor to V_{CC} - 2V.
—	EP	Exposed Pad (QFN Package Only). Connect to V_{EE}.

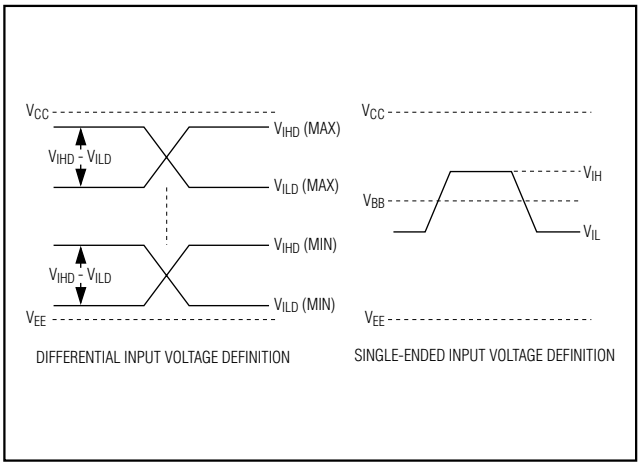


Figure 1. Input Definitions

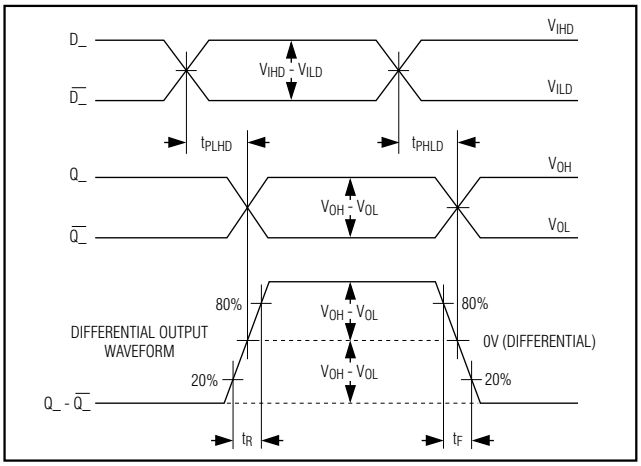


Figure 2. Differential Input-to-Output Propagation Delay Timing Diagram

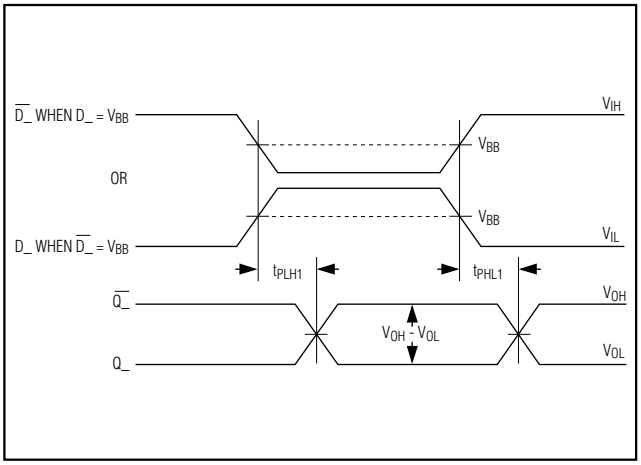


Figure 3. Single-Ended Input-to-Output Propagation Delay Timing Diagram

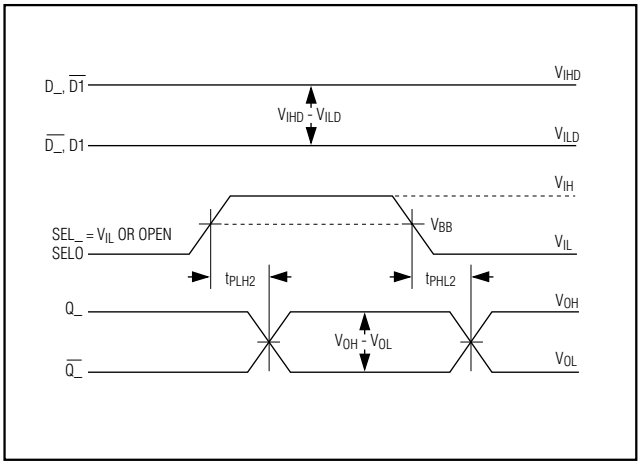


Figure 4. Select Input (SEL0) to Output (Q_, $\overline{Q\_}$) Delay Timing Diagram

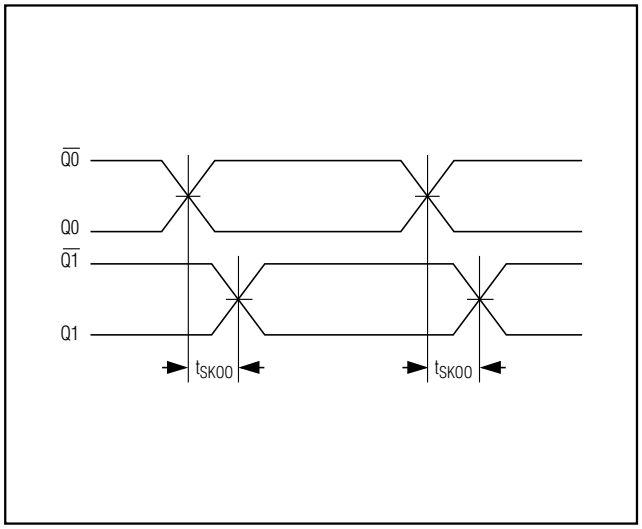


Figure 5. Output-to-Output Skew (t_{SKOO}) Definition

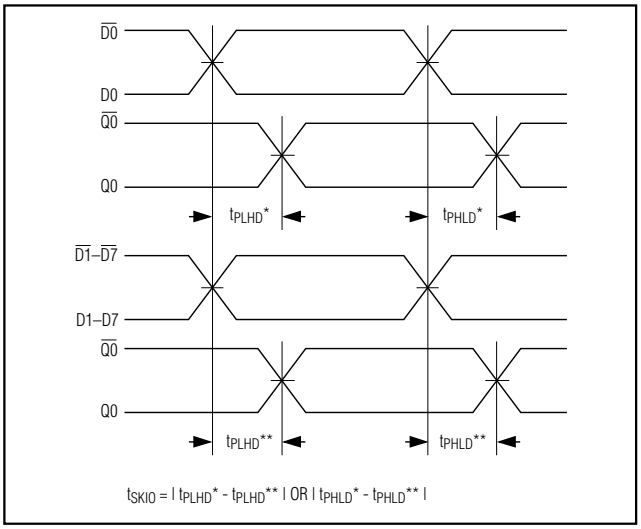


Figure 6. Input-to-Output Skew (t_{SKIO}) Definition

Detailed Description

The MAX9389 is a fully differential, high-speed, low-jitter 8-to-1 ECL/PECL mux with dual output buffers. The device is designed for clock and data distribution applications, and features extremely low propagation delay (310ps typ) and output-to-output skew (30ps max).

Three single-ended select inputs, SEL0, SEL1, and SEL2, control the mux function (see Table 1). The mux select inputs are compatible with ECL/PECL logic, and are internally referenced to the on-chip reference output (V_{BB1}, V_{BB2}), nominally V_{CC} - 1.425V. The select inputs accept signals between V_{CC} and V_{EE}. Internal 165kΩ pulldowns to V_{EE} ensure a low default condition if the select inputs are left open. Leaving SEL0, SEL1, and SEL2 open selects the D0, $\overline{D0}$ inputs by default.

The differential inputs D_, $\overline{D}$_ can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference voltage (V_{BB1}, V_{BB2}). Voltage reference outputs V_{BB1} and V_{BB2} provide the reference voltage needed for single-ended operations. A single-ended input of at least V_{BB}_ ±100mV or a differential input of at least 100mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics* table. The maximum magnitude of the differential input from D_ to $\overline{D}$_ is ±3.0V. This limit also applies to the difference between a single-ended input and any reference voltage input.

Table 1. Mux Select Input Truth Table

DATA OUTPUT	SEL0	SEL1	SEL2
D0*	L or open	L or open	L or open
D1	H	L or open	L or open
D2	L or open	H	L or open
D3	H	H	L or open
D4	L or open	L or open	H
D5	H	L or open	H
D6	L or open	H	H
D7	H	H	H

**Default output when SEL0, SEL1, and SEL2 are left open.*

Single-Ended Operation

The recommended supply voltage for single-ended operation is 3.0V to 3.8V. The differential inputs (D_, $\overline{D}$_) can be configured to accept single-ended inputs when operating at supply voltages greater than 2.725V. In single-ended mode operation, the unused complementary input needs to be connected to the on-chip reference voltage, V_{BB1} or V_{BB2}, as a reference. For example, the differential D_, $\overline{D}$_ inputs are converted to a noninverting, single-ended input by connecting V_{BB1} or V_{BB2} to $\overline{D}$_ and connecting the single-ended input to D_. Similarly, an inverting input is obtained by connecting V_{BB1} or V_{BB2} to D_ and connecting the single-ended input to $\overline{D}$_. The single-ended input can be driven to V_{CC} or V_{EE} or with a single-ended LVPECL/LVECL signal.

Differential 8:1 ECL/PECL Multiplexer with Dual Output Buffers

In single-ended operation, ensure that the supply voltage (V_{CC} -V_{EE}) is greater than 2.725V. The input high minimum level must be at least (V_{EE} + 1.2V) or higher for proper operation. The reference voltage V_{BB} must be at least (V_{EE} + 1.2V) because it becomes the high-level input when a single-ended input swings below it. The minimum V_{BB} output for the MAX9389 is (V_{CC} - 1.525V). Substituting the minimum V_{BB} output for (V_{BB} = V_{EE} + 1.2V) results in a minimum supply (V_{CC} - V_{EE}) of 2.725V. Rounding up to standard supplies gives the recommended single-ended operating supply ranges (V_{CC} - V_{EE}) of 3.0V to 5.5V.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If V_{BB} is not being used, leave it unconnected. The V_{BB} reference can source or sink a total of 0.5mA (shared between V_{BB1} and V_{BB2}), which is sufficient to drive eight inputs.

Applications Information

Output Termination

Terminate each output with a 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. Terminate each Q_ and $\overline{Q}$_ output with identical termination for minimal distortion. When a single-ended signal is taken from the differential output, terminate both Q_ and $\overline{Q}$_.

Ensure that the output current does not exceed the current limits specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should not be exceeded.

Supply Bypassing

Bypass each V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. For PECL, bypass each V_{CC} to V_{EE}. For ECL, bypass each V_{EE} to V_{CC}. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

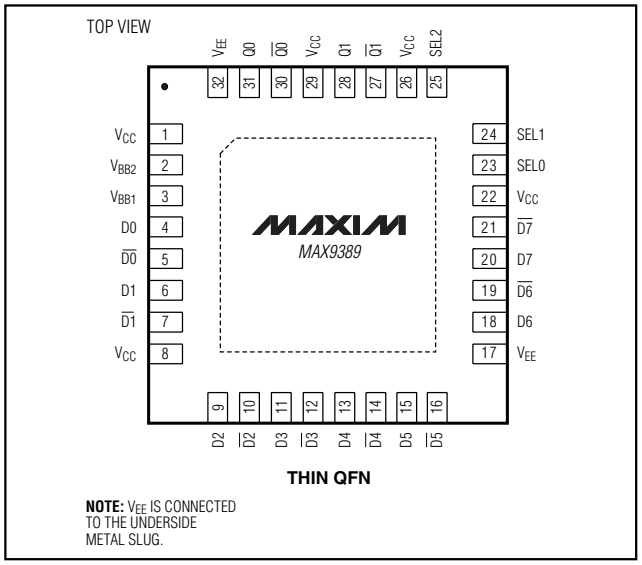
Use multiple vias when connecting the bypass capacitors to ground. When using the V_{BB1} or V_{BB2} reference outputs, bypass each one with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB1} or V_{BB2} reference outputs are not used, they can be left open.

Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Pin Configurations (continued)



THIN QFN

NOTE: V_{EE} IS CONNECTED TO THE UNDERSIDE METAL SLUG.

Chip Information

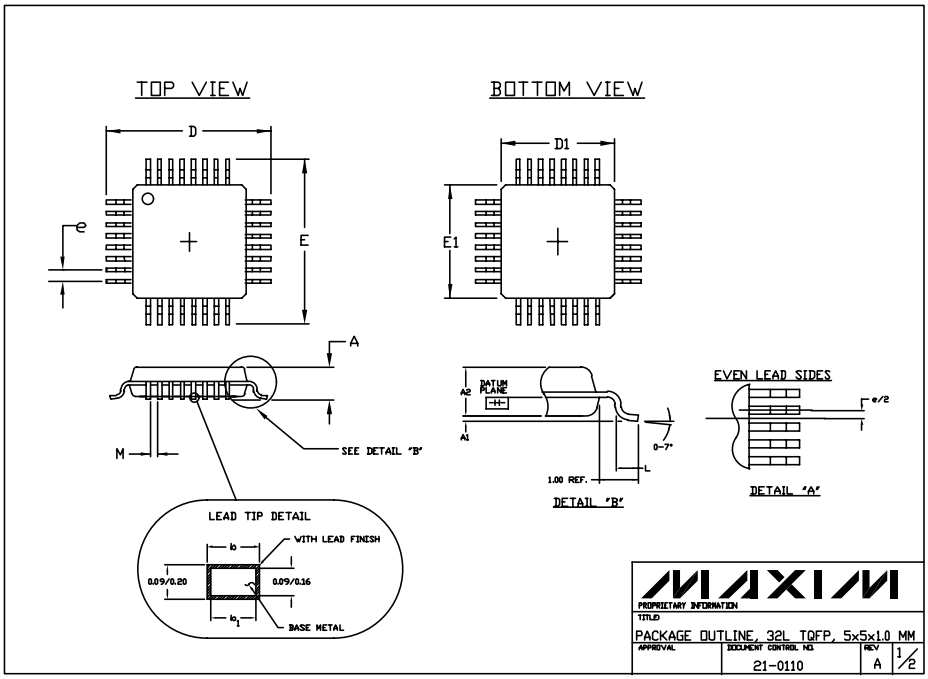
TRANSISTOR COUNT: 716

PROCESS: Bipolar

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

32L TQFP, 5x5x01.0.EPS



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~~	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	~~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

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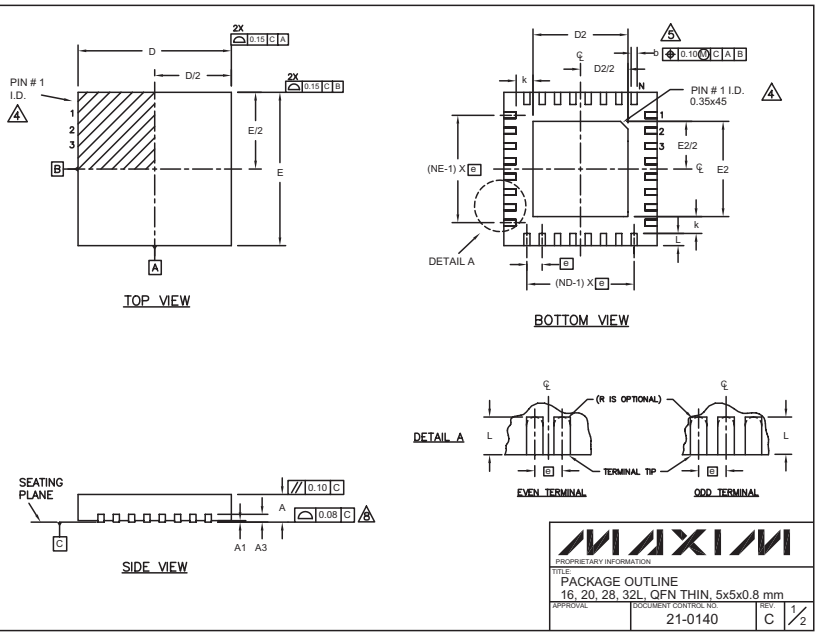
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm
APPROVAL
DOCUMENT CONTROL NO. 21-0140
REV. C
2/2