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19-0551; Rev 1; 7/06

14 Programmable Gamma Reference Buffers with Four Static References for TFT-LCD Displays

General Description

The MAX9590 provides 14 programmable voltage references and four static voltage references for gamma correction in TFT-LCD displays. Two register banks are provided to store two sets of gamma reference values. Gamma values are programmed into the banks through the I²C interface and the outputs can switch between values in 0.5µs.

The 14 programmable reference voltages are divided evenly into seven upper and seven lower voltages for the upper and lower gamma curves of LCD column drivers.

Each gamma reference voltage has an 8-bit digital-to-analog converter (DAC) and isolation buffer associated with it to ensure stable operation. Therefore, the reference voltages remain stable without synchronizing to the LCD horizontal timing. In addition, each buffer is able to provide a high current that further ensures a stable voltage when critical levels and patterns are displayed.

The 14 programmable buffers wake up in the high-impedance state until the registers are programmed. This protects the LCD system from high transient currents during the startup phase.

The MAX9590 is available in a 38-pin TQFN package and is specified for operation over the -40°C to +85°C temperature range.

Applications

TFT-LCD Displays

Industrial Reference Voltage Generators

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9590ETU+	-40°C to +85°C	38 TQFN-EP** (5mm x 7mm)	T3857-1

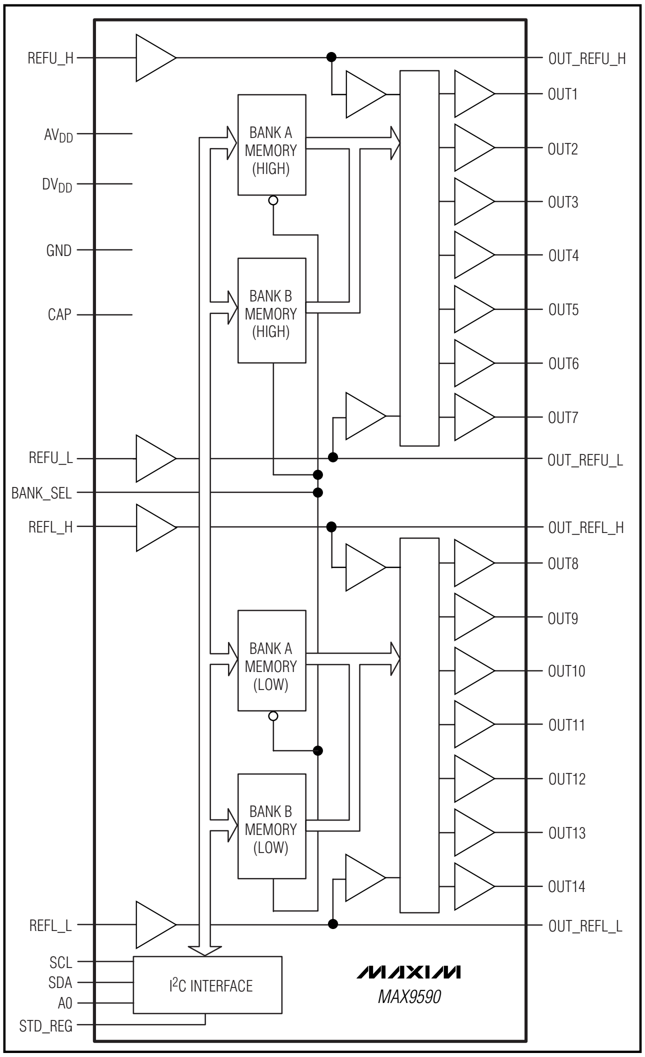
+Denotes lead-free package.

***EP = Exposed paddle.*

Features

- ♦ **14 Programmable Reference Voltages**
- ♦ **Four Static Reference Voltages**
- ♦ **Independent DACs with 8-Bit Resolution**
- ♦ **Two Register Banks for Two Sets of Gamma Values**
- ♦ **Fast Switching between Gamma Values**
- ♦ **16.5V (max) Operating Voltage**
- ♦ **Output Swing within 150mV of Rails**
- ♦ **Peak Current Greater than 200mA**
- ♦ **Output Channels Tri-Stated During Wake-Up**

Block Diagram



14 Programmable Gamma Reference Buffers with Four Static References for TFT-LCD Displays

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to GND ....-0.3V to +18V
DV_{DD} to GND ....-0.3V to +6V
REFU_H, REFU_L, REFL_H, REFL_L ....-0.3V to (AV_{DD} + 0.3V)
OUT1–OUT14...-0.3V to (AV_{DD} + 0.3V)
OUT_REFU_H, OUT_REFU_L,
OUT_REFL_H, OUT_REFL_L ....-0.3V to (AV_{DD} + 0.3V)
STD_REG, A0, SDA, SCL, BANK_SEL, CAP to GND....-0.3V to +6V
Continuous Current
SDA 50mA
CAP 20mA
OUT1–OUT14...400mA
OUT_REFU_H, OUT_REFU_L,
OUT_REFL_H, OUT_REFL_L 400mA
Short-Circuit Duration
Any Output to AV_{DD} or GND.................................Continuous
Continuous Power Dissipation (T_A = +70°C)
38-Pin TQFN (derate 26.3mW/°C above +70°C) 2195mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = 15V, DV_{DD} = 3.3V, V_{REFU_H} = 14V, V_{REFU_L} = 9V, V_{REFL_H} = 6V, V_{REFL_L} = 1V, GND = 0V, no load. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLIES						
Analog Supply Voltage Range	AV_{DD}	Guaranteed by power-supply rejection ratio specification	9.0		16.5	V
Digital Supply Voltage Range	DV_{DD}		2.7		5.5	V
Analog Quiescent Current	I_{AVDD}			21	32	mA
Undervoltage Lockout Threshold	UVLO	DV_{DD} undervoltage lockout threshold		1.5		V
Digital Quiescent Current	I_{DVDD}	During a register mode load event		200		µA
		No SCL or SDA transitions		46	100	
HIGH REFERENCE BUFFERS (REFU_H, REFL_H)						
Output Voltage Range	V_{OUT}	T_A = +25°C, sinking or sourcing 4mA	3.0		AV_{DD} - 0.15	V
Input Voltage Range	V_{CM}	T_A = +25°C, sinking or sourcing 4mA	3.0		AV_{DD}	V
Offset Voltage	V_{OS}	V_{OUT} = 5V		1	10	mV
Input Resistance	R_{IN}			100		MΩ
Load Regulation	R_{EG}	-12mA to +12mA		0.25		mV/mA
Power-Supply Rejection Ratio	PSRR	9V ≤ AV_{DD} ≤ 16.5V, outputs at 5V	60	90		dB
Short-Circuit Current	I_{SC}	To AV_{DD} or GND		400		mA
Slew Rate	SR	Swing $5V_{P-P}$ at input, 10% to 90% measurement on output		10		V/µs
LOW REFERENCE BUFFERS (REFU_L, REFL_L)						
Output-Voltage Range	V_{OUT}	T_A = +25°C, sinking or sourcing 4mA	GND + 0.15		AV_{DD} - 3.7	V
Input-Voltage Range	V_{CM}	T_A = +25°C, sinking or sourcing 4mA	GND		AV_{DD} - 3.7	V
Offset Voltage	V_{OS}	V_{OUT} = 5V		1	10	mV
Input Resistance	R_{IN}			100		MΩ
Load Regulation	R_{EG}	-12mA to +12mA		0.25		mV/mA
Power-Supply Rejection Ratio	PSRR	9V ≤ AV_{DD} ≤ 16.5V, outputs at 5V	60	90		dB
Short-Circuit Current	I_{SC}	To AV_{DD} or GND		400		mA
Slew Rate	SR	Swing $5V_{P-P}$ at input, 10% to 90% measurement on output		10		V/µs

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 15V, DV_{DD} = 3.3V, V_{REFU_H} = 14V, V_{REFU_L} = 9V, V_{REFL_H} = 6V, V_{REFL_L} = 1V, GND = 0V, no load. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC OUTPUTS (OUT1–OUT14)						
Resolution	RES	Linear	8			Bits
Integral Nonlinearity Error	INL			0.5		LSB
Differential Nonlinearity Error	DNL			0.25		LSB
Full-Scale Error	E_{FS}			0.5		LSB
Zero-Code Error	E_{ZC}			0.5		LSB
Output-Voltage Range	V_{OUT}	T_A = +25°C, sinking or sourcing 4mA	0.15		AV_{DD} - 0.15	V
Load Regulation		-12mA to +12mA		0.50		mV/mA
Power-Supply Rejection Ratio	PSRR	9V ≤ AV_{DD} ≤ 16.5V, outputs at 5V	60	90		dB
Short-Circuit Current	I_{SC1}	Outputs 1, 7, 8, 14 to AV_{DD} or GND		400		mA
	I_{SC2}	All other outputs to AV_{DD} or GND		200		
Output Impedance	Z_O	Output resistance of voltage source when buffer disabled		100		kΩ
Slew Rate	SR	Swing $5V_{P-P}$ at input, 10% to 90% measurement on OUT1–OUT14		22		V/µs
Settling Time		OUT1–OUT14 swing $5V_{P-P}$, and settled to ±0.5 LSB, switch from Bank A to Bank B or vice versa, R_L = 10kΩ to GND and C_L = 50pF to GND (Note 2)		0.5		µs
Channel-to-Channel Isolation	C_{XTLK}	f = 5MHz, all channels to all channels		80		dB
Noise	E_n	RMS noise voltage at any output (10MHz BW)		375		µV
Thermal Shutdown	Ts			+160		°C
Thermal Shutdown Hysteresis	Hys			15		°C
LOGIC INPUTS AND OUTPUTS (SDA, SCL, BANK_SEL, STD_REG, A0)						
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V or DV_{DD}	-1	+0.01	+1	µA
Input Capacitance		Guaranteed by design, not subject to production testing		5		pF
Power-Down Input Current	I_{IN}	DV_{DD} = 0V, V_{IN} = 1.98V (Note 3)	-10		+10	µA
SDA Output Low Voltage	V_{OL}	I_{SINK} = 6mA			0.4	V

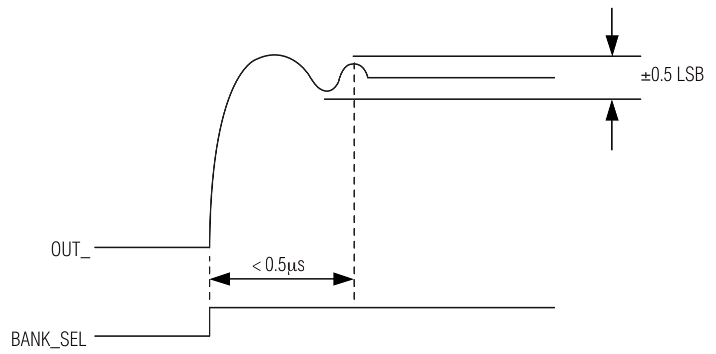
ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = 15V, DV_{DD} = 3.3V, V_{REFU_H} = 14V, V_{REFU_L} = 9V, V_{REFL_H} = 6V, V_{REFL_L} = 1V, GND = 0V, no load. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS (Figure 1)						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP (P) and START (S) Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START (S) Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge	0		0.9	µs
Data Setup Time	$t_{SU,DAT}$		100			ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}	Guaranteed by design, input filters on the SDA and SCL inputs suppress noise spikes less than 50ns		50		ns

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Reference voltages transition from Bank A to Bank B value in less than 500ns. The *Timing Diagram* shows the response at the output pin.
Note 3: Only SCL and SDA are high impedance.

Timing Diagram

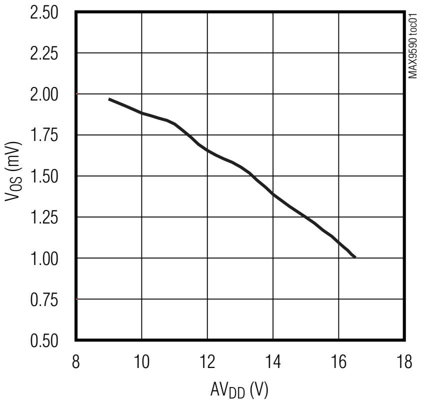


14 Programmable Gamma Reference Buffers with Four Static References for TFT-LCD Displays

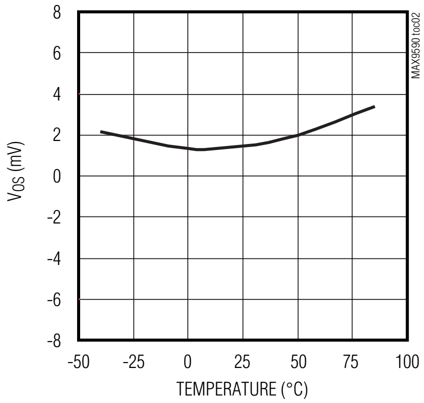
Typical Operating Characteristics

(AV_{DD} = 15V, DV_{DD} = 3.3V, V_{REFU_H} = 14V, V_{REFU_L} = 9V, V_{REFL_H} = 6V, V_{REFL_L} = 1V, GND = 0V, no load. T_A = +25°C, unless otherwise noted.)

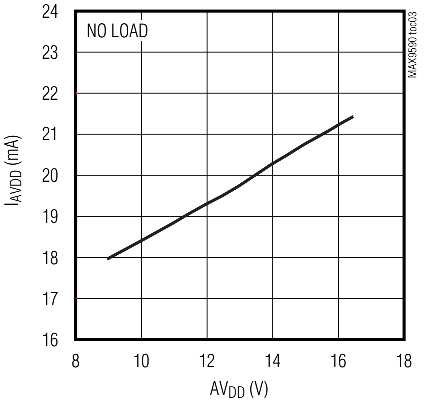
INPUT OFFSET VOLTAGE DEVIATION vs. SUPPLY VOLTAGE



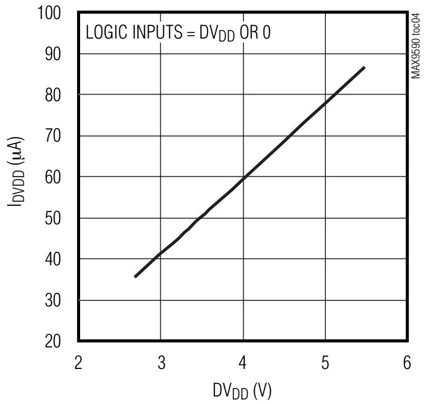
INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE



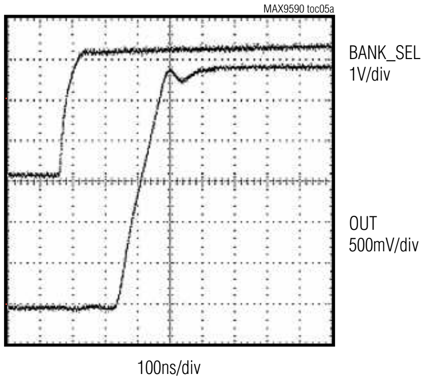
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE

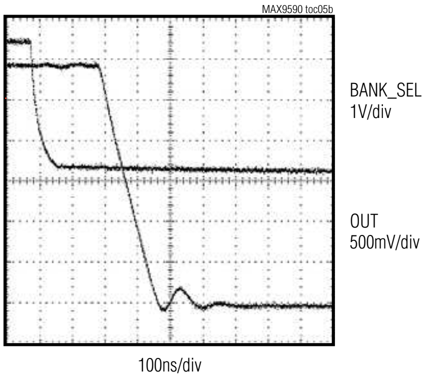


SETTLING TIME



OUT IS SWITCHING FROM 2V TO 5V. OUT IS LOADED WITH 1kΩ || 50pF TO GROUND.

SETTLING TIME

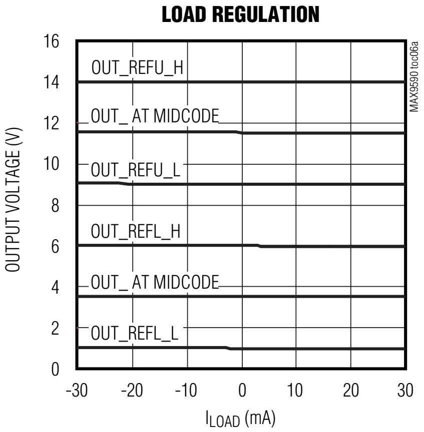


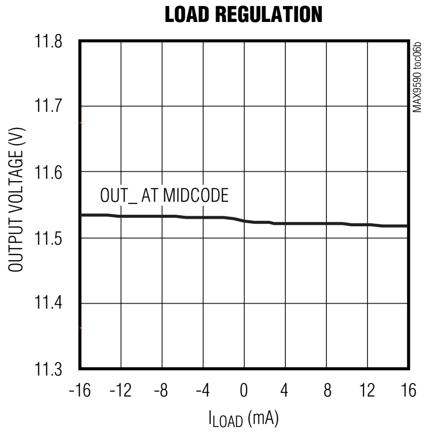
OUT IS SWITCHING FROM 5V TO 2V. OUT IS LOADED WITH 1kΩ || 50pF TO GROUND.

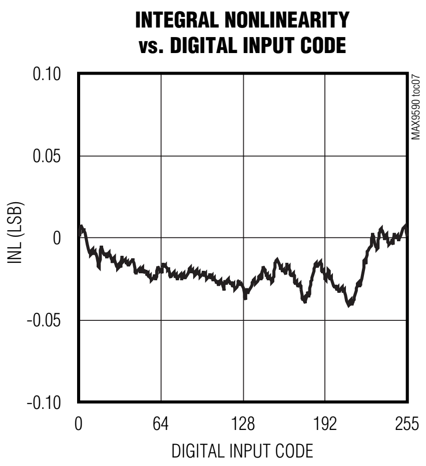
14 Programmable Gamma Reference Buffers with Four Static References for TFT-LCD Displays

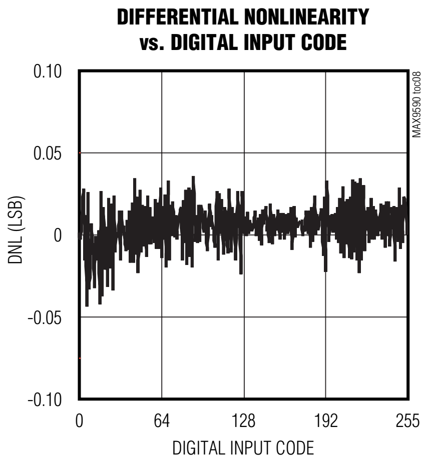
Typical Operating Characteristics (continued)

(AV_{DD} = 15V, DV_{DD} = 3.3V, V_{REFU_H} = 14V, V_{REFU_L} = 9V, V_{REFL_H} = 6V, V_{REFL_L} = 1V, GND = 0V, no load. T_A = +25°C, unless otherwise noted.)





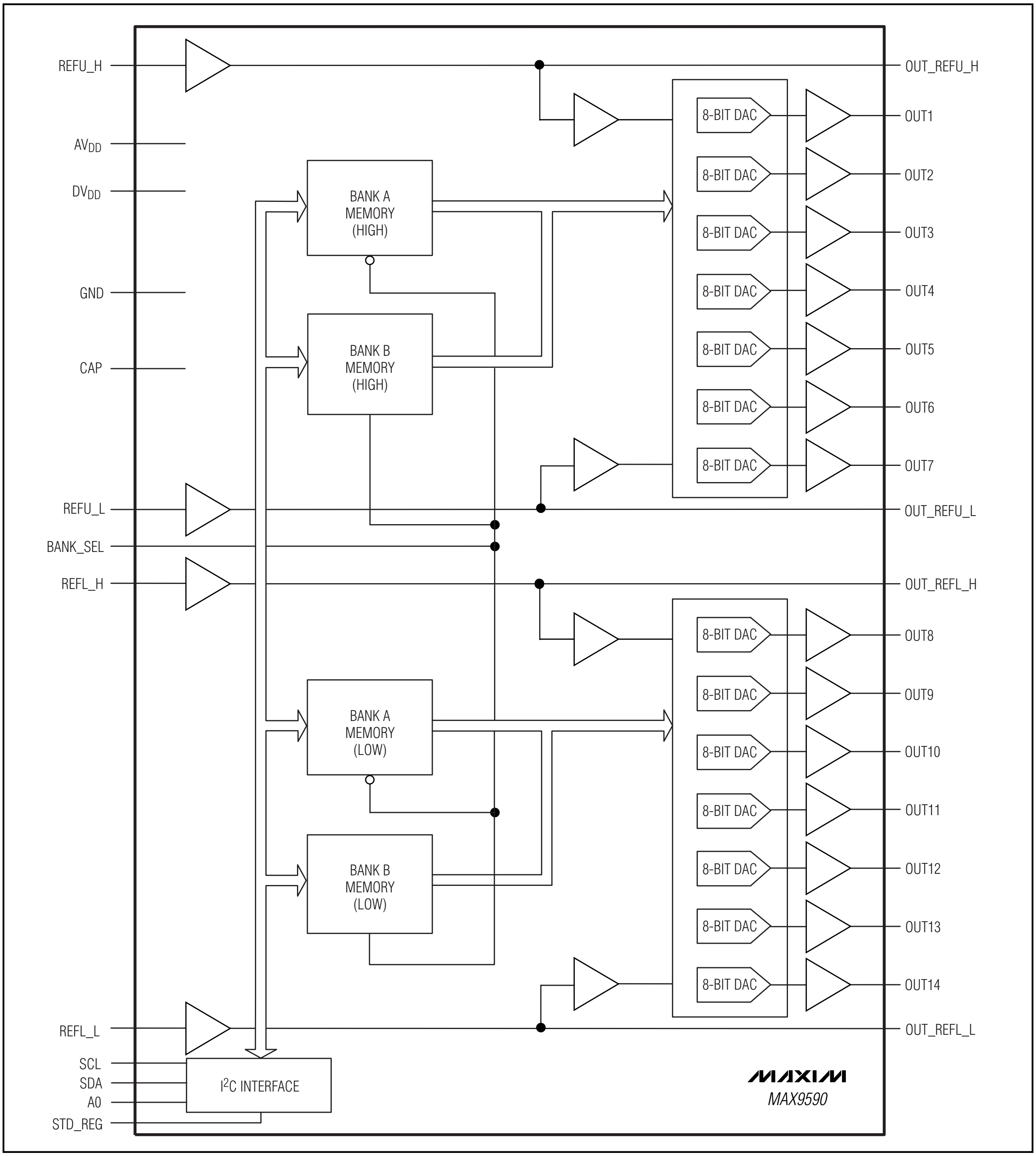




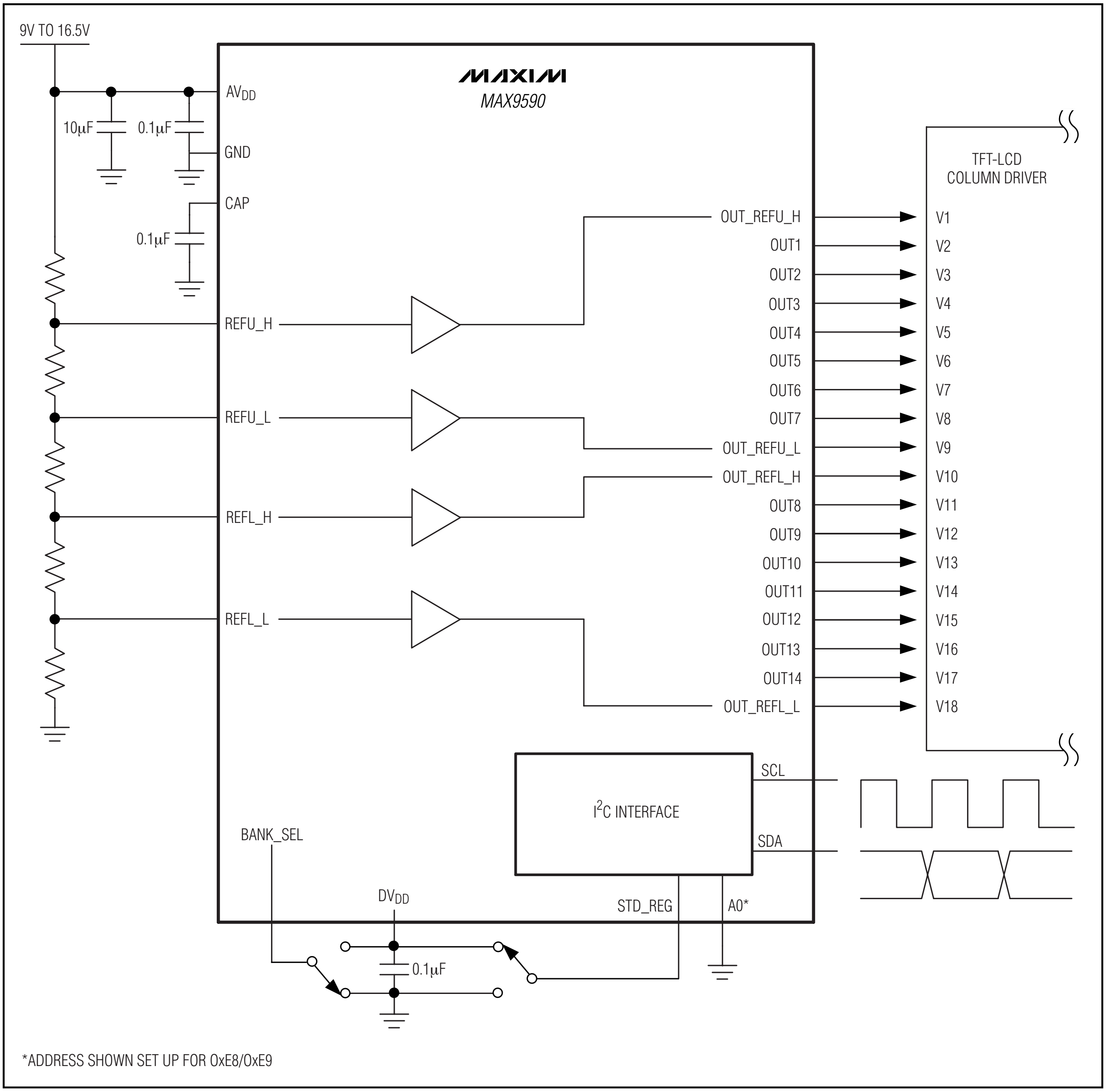
Pin Description

PIN	NAME	FUNCTION
1	OUT_REFU_H	REFU_H Buffered Output
2, 21	AV_{DD}	Analog Power Supply. Bypass to GND with 0.1µF and 10µF capacitors.
3	STD_REG	Operation Mode Select. Input that selects mode of operation. Set STD_REG = 0 to select register mode. Set STD_REG = 1 to select standard mode. See the *I²C Compatibility* section.
4	A0	I²C Slave ID Selector Input. Connect to SCL or SDA or DV_{DD} or GND.
5	SDA	I²C-Compatible Serial Data Input/Output
6	SCL	I²C-Compatible Serial Clock
7, 10, 24, 25	N.C.	No Connection. Not internally connected. Leave unconnected.
8	DV_{DD}	Digital Power Supply. Bypass to GND with a 0.1µF capacitor.
9	BANK_SEL	Bank Select. Logic input that selects the set of reference voltages buffered to the outputs. Set BANK_SEL = 0 to select Bank A. Set BANK_SEL = 1 to select Bank B.
11, 28, 30	GND	Ground
12	OUT_REFL_L	REFL_L Buffered Output
13	OUT14	Lower DAC Analog Output 14
14	OUT13	Lower DAC Analog Output 13
15	OUT12	Lower DAC Analog Output 12
16	OUT11	Lower DAC Analog Output 11
17	OUT10	Lower DAC Analog Output 10
18	OUT9	Lower DAC Analog Output 9
19	OUT8	Lower DAC Analog Output 8
20	OUT_REFL_H	REFL_H Buffered Output
22	REFU_H	Upper DAC High Reference Voltage Input
23	REFU_L	Upper DAC Low Reference Voltage Input
26	REFL_H	Lower DAC High Reference Voltage Input
27	REFL_L	Lower DAC Low Reference Voltage Input
29	CAP	Internal Voltage Reference. Bypass to GND with a 0.1µF capacitor (10V). Do not connect external loads.
31	OUT_REFU_L	REFU_L Buffered Output
32	OUT7	Upper DAC Analog Output 7
33	OUT6	Upper DAC Analog Output 6
34	OUT5	Upper DAC Analog Output 5
35	OUT4	Upper DAC Analog Output 4
36	OUT3	Upper DAC Analog Output 3
37	OUT2	Upper DAC Analog Output 2
38	OUT1	Upper DAC Analog Output 1
—	EP	Exposed Paddle. Internally connected to ground. Leave EP unconnected or connect the EP to the ground plane for improved thermal conductivity.

Functional Diagram



Typical Application Circuit



14 Programmable Gamma Reference Buffers with Four Static References for TFT-LCD Displays

Detailed Description

The MAX9590 provides 14 channels of programmable voltage references and four channels of static voltage references for gamma correction in TFT-LCD displays. Two register banks are provided to store two different sets of gamma reference values. Gamma values are programmed into the banks through the I^2C interface and the outputs can switch between values in 0.5µs.

Output Buffers

The 14 programmable reference voltages are divided evenly into seven upper and seven lower voltages for the upper and lower gamma curves of LCD column drivers.

The seven upper voltages cover the range between REFU_L to REFU_H. The seven lower voltages cover the range of REFL_L to REFL_H.

Each gamma reference voltage has an 8-bit DAC and isolation buffer associated with it to ensure stable operation. Therefore, the reference voltages remain stable without synchronization to the LCD horizontal timing. In addition, each buffer is able to provide a high current that further ensures a stable voltage when critical levels and patterns are displayed.

Each of the MAX9590 output buffers hold the reference voltages stable while providing the ability to source and sink current (200mA) into a capacitive load such as LCD column drivers. When switching from Bank A to Bank B or vice versa, the outputs settle to within ±0.5 LSB in less than 0.5µs.

8-Bit DAC

Each voltage is generated by an 8-bit DAC and programmed values are set through the I^2C interface. The input code data is used to set the output voltages of the MAX9590. See the *I^2C Compatibility* section.

The ideal transfer function of the upper reference voltages is:

$$V_{OUT1} \text{ to } V_{OUT2} = V_{REFU\_L} + \frac{D}{255} \times (V_{REFU\_H} - V_{REFU\_L})$$

while the ideal transfer function of the lower reference voltages is:

$$V_{OUT8} \text{ to } V_{OUT14} = V_{REFL\_L} + \frac{D}{255} \times (V_{REFL\_H} - V_{REFL\_L})$$

$$D = 2^7(B7) + 2^6(B6) + 2^5(B5) + 2^4(B4) + 2^3(B3) + 2^2(B2) + 2^1(B1) + 2^0(B0)$$

D is the decimal value of the input binary code. B7 is the most significant bit of the data byte and is clocked in first.

Table 1 shows the ideal output voltage of V_{OUT1} and V_{OUT14} with the following typical conditions:

$$V_{REFU\_H} = 14V,\ V_{REFU\_L} = 9V,\ V_{REFL\_H} = 6V, \text{ and } V_{REFL\_L} = 1V$$

Table 1. Ideal Output Voltage with Typical Conditions

BINARY INPUT	DECIMAL VALUE	V_{OUT1} (V)	V_{OUT14} (V)
0000 0000	0	9.00	1.00
0000 0001	1	9.019	1.019
0000 0011	3	9.058	1.058
0000 0111	7	9.136	1.136
0000 1111	15	9.292	1.292
0001 1111	31	9.605	1.605
0011 1111	63	10.230	2.230
0111 1111	127	11.480	3.480
1111 1111	255	14.00	6.00

Register Banks

The MAX9590 features two register banks: Bank A and Bank B. The user can program one set of gamma values into Bank A while Bank B is being used to drive the LCD column drivers and vice versa.

Set BANK_SEL = 0 to select Bank A and set BANK_SEL = 1 to select Bank B. The gamma voltage transition from Bank A to Bank B and vice versa takes place in less than 500ns. See the *Register Address* section for details on memory bank internal registers.

Power-On Reset (POR)

The MAX9590 contains an integrated POR circuit that ensures all registers are reset to a zero state on power-up. Once DV_{DD} rises above 1.5V (typ), the POR circuit releases the registers for normal operation. Should the DV_{DD} input drop to less than 1.5V (typ), the POR is activated.

After a POR, the outputs (OUT1–OUT14) are in high-impedance mode until a minimum of **two data bytes** have been written to **both** Bank A and Bank B in any order.

Thermal Shutdown

The MAX9590 features thermal-shutdown protection with temperature hysteresis. When the die temperature reaches +160°C, OUT1–OUT14 shut down. When the die cools down by 15°C, the device turns on again. When in thermal shutdown, the amplifier outputs (OUT1–OUT14) are high impedance. The four static buffers remain active. When exiting thermal shutdown, the amplifier outputs return to the programmed output voltages.

Serial Interface

The MAX9590 features an I²C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate bidirectional communication between the MAX9590 and the master at rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The MAX9590 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfer on the bus and generates SCL.

A master device communicates with the MAX9590 by transmitting the correct slave ID followed by a command and/or data words. Each transmit sequence is framed with a START (S) or repeated START (Sr) condition and a STOP (P) condition.

The SDA driver is an open-drain output, requiring a pullup resistor to generate a logic-high voltage. Optional resistors in series with SDA and SCL (i.e. 300Ω) protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot of the bus signals.

Bit Transfer

Each SCL rising edge transfers one data bit. The data on SDA must remain stable during the high portion of the SCL clock pulse (Figure 2). Changes in SDA while SCL is high are read as control signals (see the *START and STOP Conditions* section). When the serial interface is inactive, SDA and SCL idle high.

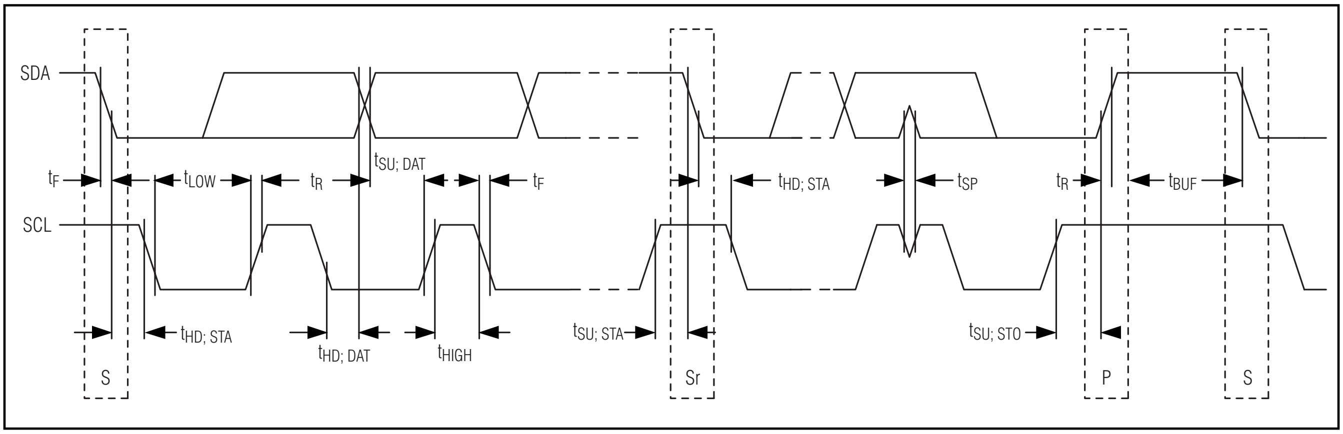


Figure 1. 2-Wire Serial-Interface Timing Diagram

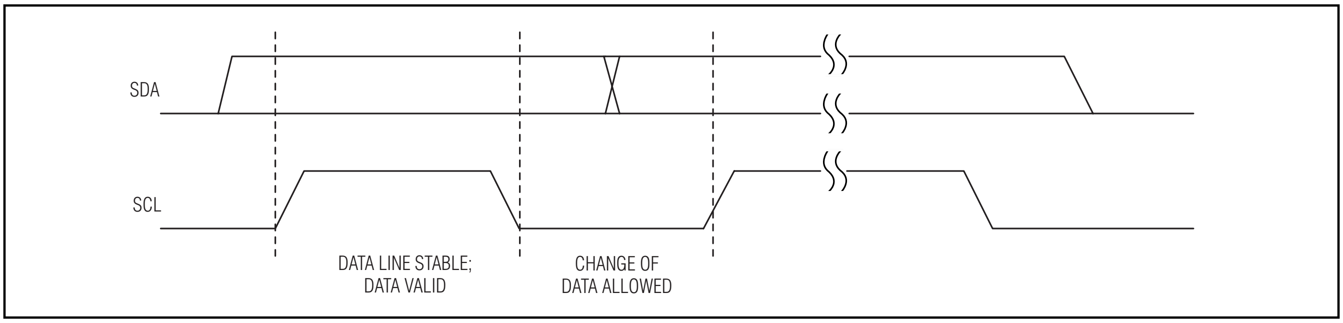


Figure 2. Bit Transfer

14 Programmable Gamma Reference Buffers with Four Static References for TFT-LCD Displays

START and STOP Conditions

A master device initiates communication by issuing a START condition which is a high-to-low transition on SDA with SCL high. A START condition from the master signals the beginning of a transmission to the MAX9590. The master terminates transmission by a STOP condition (see the *Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)* section). A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 3). The STOP condition frees the bus. If a repeated START condition is generated instead of a STOP condition, the bus remains active. When a STOP condition or incorrect slave ID is detected, the MAX9590 internally disconnects SCL from the serial interface until the next START or repeated START condition, minimizing digital noise and feedthrough.

Early STOP Conditions

The MAX9590 recognizes a STOP condition at any point during transmission except when a STOP condition occurs in the same high pulse as a START condition (Figure 4). This condition is not a legal I^2C format; at least one clock pulse must separate any START and STOP conditions. The MAX9590 discards any data received during a data transfer aborted by an early STOP condition.

Repeated START Conditions

A repeated START condition is used to indicate a change in direction of data flow (see the *Register Mode Read Operation* section). Repeated START may also be used when the bus master is writing to several I^2C devices and does not want to relinquish control of the bus. The MAX9590 serial interface supports continuous write operations with (or without) an Sr condition separating them.

Acknowledge Bit (ACK) and Not-Acknowledge Bit (NACK)

Successful data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX9590 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 5). If a master transmitter is involved in a data transfer, it must signal the end of data to the slave transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave transmitter must release the SDA to allow the master to generate a STOP or repeated START condition. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An

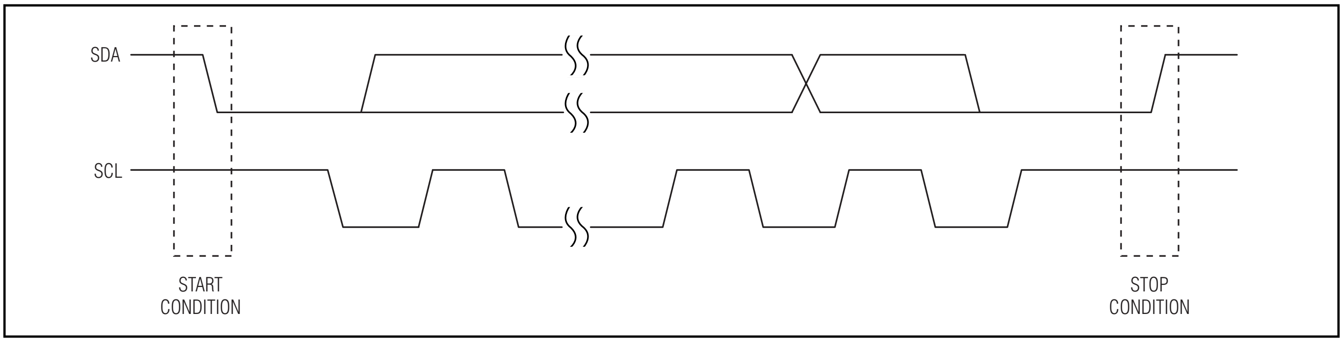


Figure 3. START/STOP Conditions

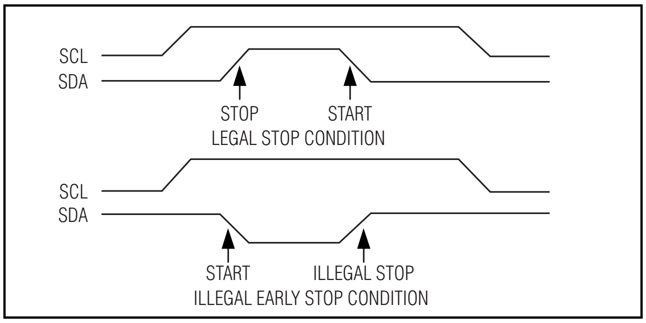


Figure 4. Early STOP Conditions

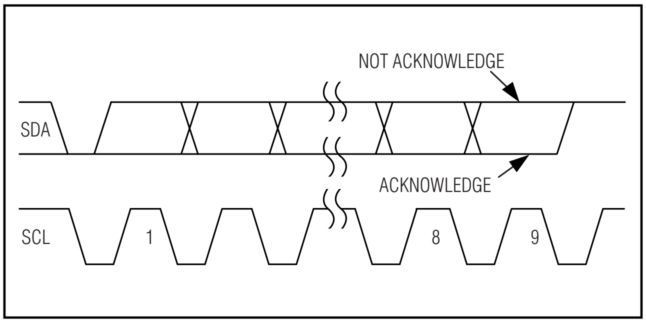


Figure 5. Acknowledge and Not Acknowledge Bits

unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the master should reattempt communication at a later time.

The MAX9590 generates an acknowledge when receiving an address or data by pulling SDA low during the ninth clock pulse. When transmitting data during a read, the MAX9590 does not drive SDA during the ninth clock pulse (i.e. the external pullups define the bus as a logic high) so that the receiver of the data can pull SDA low to acknowledge receipt of data. When the last byte of data is received by the master during a read, a not acknowledge is generated where the SDA line is not pulled low by the master receiver.

Slave ID

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave ID (Figure 6). When idle, the MAX9590 waits for a START condition followed by its slave ID. The serial interface compares each slave ID bit by bit, allowing the interface to power down and disconnect from SCL immediately if an incorrect slave ID is detected. After recognizing a start condition followed by the correct slave ID, the MAX9590 is programmed to accept or send data. The LSB of the slave ID word is the Read/$\overline{\text{Write}}$ ($R/\overline{W}$) bit. $R/\overline{W}$ indicates whether the master is writing to or reading from the MAX9590 ($R/\overline{W}$ = 0 selects a write condition, $R/\overline{W}$ = 1 selects a read condition). After receiving the proper slave ID, the MAX9590 issues an ACK by pulling SDA low for one clock cycle.

The MAX9590 slave ID consists of five fixed bits B7...B3 (set to 11101) and two programmable bits B2 and B1. The most significant slave ID bit (B7) is transmitted first, followed by the remaining bits. The MAX9590 slave ID is determined by connecting A0 to GND or DV_{DD} or SCL or SDA. Table 2 shows the four possible slave IDs of the device.

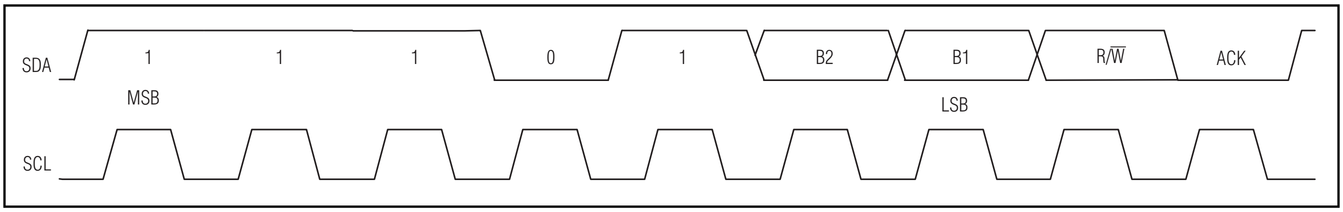


Figure 6. Slave ID Byte Definition

Table 2. Slave ID Description

A0	B7	B6	B5	B4	B3	B2	B1	B0	WRITE ADDRESS (Hex)	READ ADDRESS (Hex)
GND	1	1	1	0	1	0	0	$R/\overline{W}$	0xE8	0xE9
DVDD	1	1	1	0	1	0	1	$R/\overline{W}$	0xEA	0xEB
SCL	1	1	1	0	1	1	0	$R/\overline{W}$	0xEC	0xED
SDA	1	1	1	0	1	1	1	$R/\overline{W}$	0xEE	0xEF

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Register Address

The MAX9590 consists of two register banks A and B. Each register bank has 14 internal registers with addresses as shown in Table 3.

Control Data Byte

Use the control data byte to configure the MAX9590. The MAX9590 control byte contains a write-designator bit (C1) and a read-designator bit (C2). The rest of the bits (C0 and C3–C7) are don't-care bits. The most significant bit (B7) is transmitted first, followed by the remaining bits. Table 4 shows the control data byte.

The write-designator bit (C1) determines to which bank to write. '0' corresponds to Bank A while '1' corresponds to Bank B. At POR, C1 is set to 0. See Figures 7, 11, and 13 for more details.

The read-designator bit (C2) determines which bank to read from. A '0' corresponds to Bank A while a '1' corresponds to Bank B. At POR, C2 is set to 0. See Figures 7, 11, and 13 for more details.

After a POR, the outputs (OUT1–OUT14) are in high-impedance mode until a minimum of **two data bytes** have been written to **both** Bank A and Bank B in any order.

Table 3. Register Mapping

REGISTER	HEXADECIMAL CODE	POWER-ON DEFAULT VALUES	REGISTER ADDRESS							
			R7	R6	R5	R4	R3	R2	R1	R0
Control Byte	0X00	0X00	0	0	0	0	0	0	0	0
A01 or B01	0X01	0X00	0	0	0	0	0	0	0	1
A02 or B02	0X02	0X00	0	0	0	0	0	0	1	0
A03 or B03	0X03	0X00	0	0	0	0	0	0	1	1
A04 or B04	0X04	0X00	0	0	0	0	0	1	0	0
A05 or B05	0X05	0X00	0	0	0	0	0	1	0	1
A06 or B06	0X06	0X00	0	0	0	0	0	1	1	0
A07 or B07	0X07	0X00	0	0	0	0	0	1	1	1
A08 or B08	0X08	0X00	0	0	0	0	1	0	0	0
A09 or B09	0X09	0X00	0	0	0	0	1	0	0	1
A10 or B10	0X0A	0X00	0	0	0	0	1	0	1	0
A11 or B11	0X0B	0X00	0	0	0	0	1	0	1	1
A12 or B12	0X0C	0X00	0	0	0	0	1	1	0	0
A13 or B13	0X0D	0X00	0	0	0	0	1	1	0	1
A14 or B14	0X0E	0X00	0	0	0	0	1	1	1	0

Table 4. Control Byte Definition

CONTROL DATA BYTE: INDIVIDUAL BITS								DESCRIPTION
C7	C6	C5	C4	C3	C2	C1	C0	
X	X	X	X	X	0	0	X	Writes to Bank A given that the Read/$\overline{\text{Write}}$ bit is set low (R/$\overline{\text{W}}$ = 0); Reads from Bank A given that the Read/$\overline{\text{Write}}$ bit is set high (R/$\overline{\text{W}}$ = 1). (At power-on reset, C1 and C2 are set to 0).
X	X	X	X	X	0	1	X	Writes to Bank B given that the Read/$\overline{\text{Write}}$ bit is set low (R/$\overline{\text{W}}$ = 0); Reads from Bank A given that the Read/$\overline{\text{Write}}$ bit is set high (R/$\overline{\text{W}}$ = 1).
X	X	X	X	X	1	0	X	Writes to Bank A given that the Read/$\overline{\text{Write}}$ bit is set low (R/$\overline{\text{W}}$ = 0); Reads from Bank B given that the Read/$\overline{\text{Write}}$ bit is set high (R/$\overline{\text{W}}$ = 1).
X	X	X	X	X	1	1	X	Writes to Bank B given that the Read/$\overline{\text{Write}}$ bit is set low (R/$\overline{\text{W}}$ = 0); Reads from Bank B given that the Read/$\overline{\text{Write}}$ bit is set high (R/$\overline{\text{W}}$ = 1).

Modes of Operation (Standard Mode (STD_REG = 1))

Standard Mode Write Operation

For the standard mode write operation, send the slave ID as the first byte followed by the control byte and then a burst of 14 data bytes. The control byte specifies the bank (to be written to or read from). Once the MAX9590 receives the control byte, the device transfers the control byte data into the control byte register. After this operation, the register address is set to A01 for Bank A or B01 for Bank B. The address gets automatically incremented from A01 (or B01) and the 14 data bytes are written to the corresponding register addresses until A14 (or B14) is reached. If more than 14 data bytes are written, the excess is ignored. Only data written up to A14 or B14 will be accepted. Data written past A14 or B14 is ignored. Terminate the data transfer with a STOP condition. The standard mode write operation is shown in Figure 7.

The MAX9590's responses to burst-write operations for various scenarios are summarized in Table 5.

Standard Mode Read Operation

The standard mode read operation can be performed on the same bank or on the second bank. If the read operation does not require a bank change, send the slave ID with an R/$\overline{W}$ bit of 1. The register address is set internally to A01 (or B01) depending on the value of the previously written control byte. The control byte is not sent during a read operation unless a bank change is required. Read the 14 data bytes and then terminate the transmission using a STOP as shown in Figure 8.

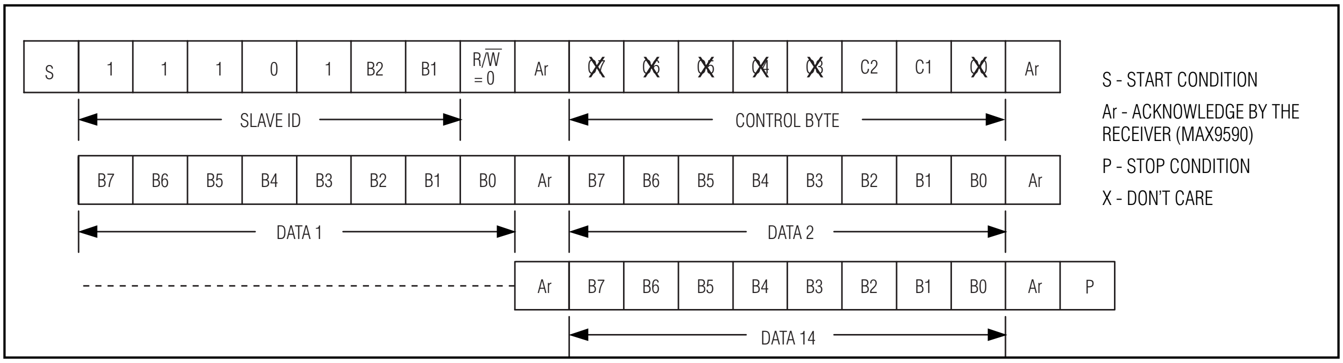

Figure 7. Standard Mode Write Operation

Table 5. Standard Mode Write Operation—Response to Burst Write

SCENARIO	RESPONSE
Burst-write operation involving more than 14 data bytes	The device writes data bytes into the corresponding register addresses in sequential order starting with the first register address (A01 or B01). The device ignores the excess bytes after register address A14 or B14.
Burst-write operation involving less than 14 data bytes	The device writes data bytes into the corresponding register addresses in sequential order, starting with the first register address (A01 or B01), until the specified number of data bytes have been written.

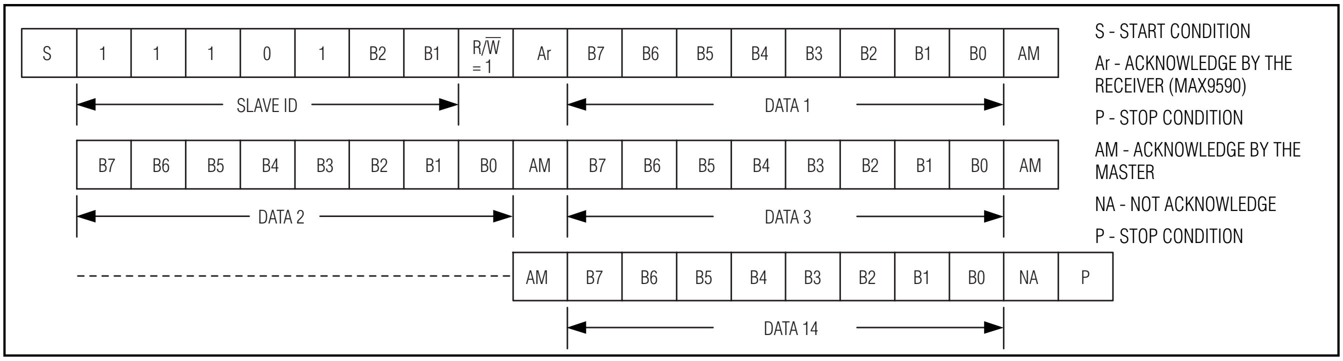

Figure 8. Standard Mode Read Operation

If a read operation requires a bank change, transmit the slave ID with a R/$\overline{W}$ bit of '0' and send the control byte to change the bank. After a repeated START signal, the 14 bytes are read from the respective bank as shown in Figure 9.

The MAX9590's responses to burst-read operations for various scenarios are summarized in Table 6.

Register Mode (STD_REG = 0)

Register Mode Write Operation

For the register mode single write operation, send the slave ID, register address, and then data. For the register mode burst-write operation, send the slave ID, register address, and then the burst of data bytes. The address gets automatically incremented internally from the address specified and the data is written to the corresponding register addresses. If more than 14 data bytes are written, the excess is ignored. Only data written up to A14 or B14 is accepted. Data written past A14 or B14 is ignored.

Figure 10 shows a single/burst-write operation in the register mode.

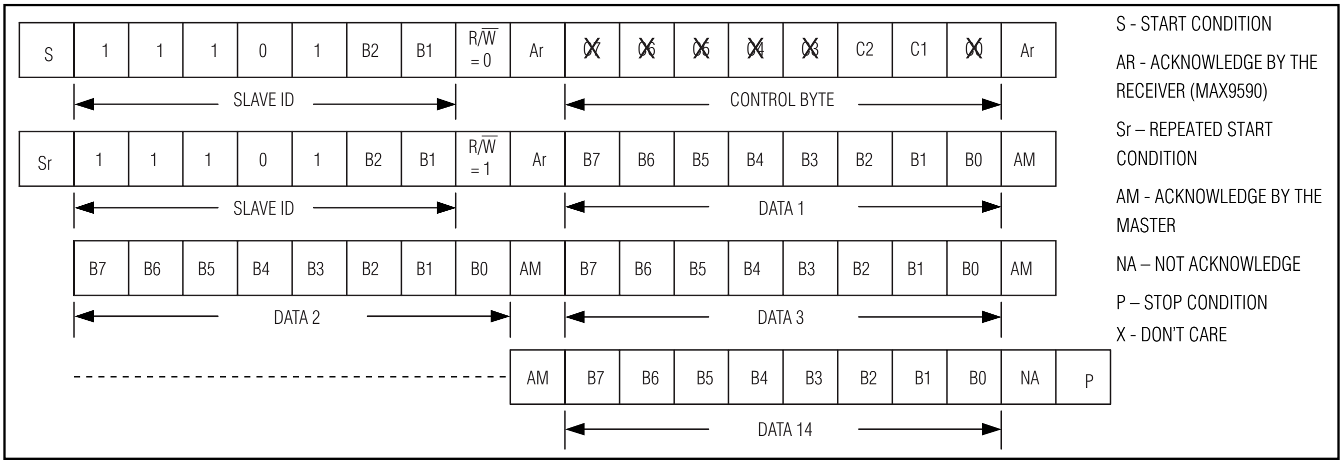

Figure 9. Standard Mode Bank Change Read Operation

Table 6. Standard Mode Read Operation—Response to Burst Read

SCENARIO	RESPONSE
Burst-read operation involving more than 14 data bytes	The device reads the valid data bytes starting from A01 (or B01) till A14 (or B14). The rest of the data bytes read are 0xFF (hexadecimal) indicating that those data are invalid.
Burst-read operation involving less than 14 data bytes	The device reads data bytes from the corresponding register addresses in sequential order starting with the first register address (A01 or B01) and stops after the specified number of data bytes have been read.

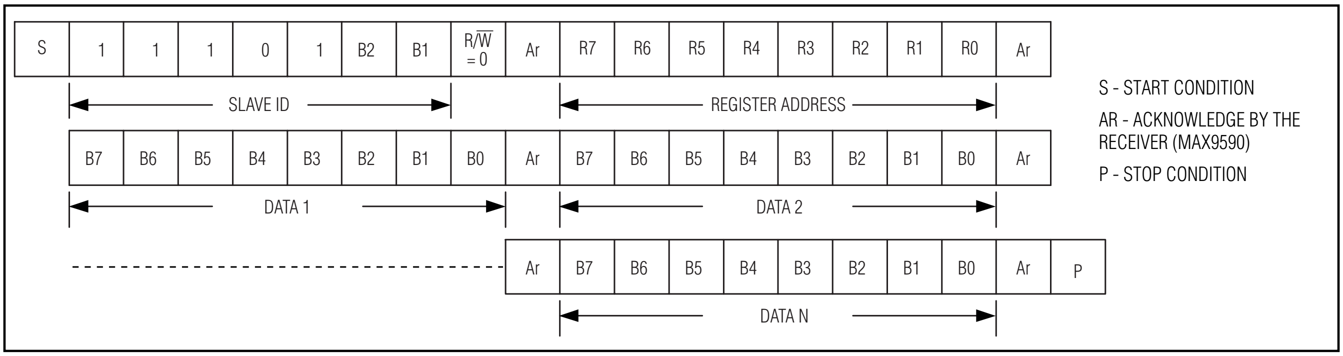

Figure 10. Register Mode (Single/Burst) Write Operation

If a write operation requires a bank change, the byte sent after the slave ID is the control register's address (0x00 in the MAX9590) and data following this address is the control byte data to switch banks. After switching banks, execute a normal register mode write operation as shown in Figure 11.

The MAX9590's responses to burst-write operations for various scenarios are summarized in Table 7.

Register Mode Read Operation

The read operation in the register mode is an ordinary I²C read operation if the bank is not changed. Send the slave ID followed by the register address. The register address needs to be the location from which the data byte is to be read. Use a repeated START to change the direction of data transfer. Send the slave ID with an R/$\overline{W}$ bit of 1 to facilitate a read operation. Read the required number of data bytes and terminate the transfer. The register mode read operation is shown in Figure 12.

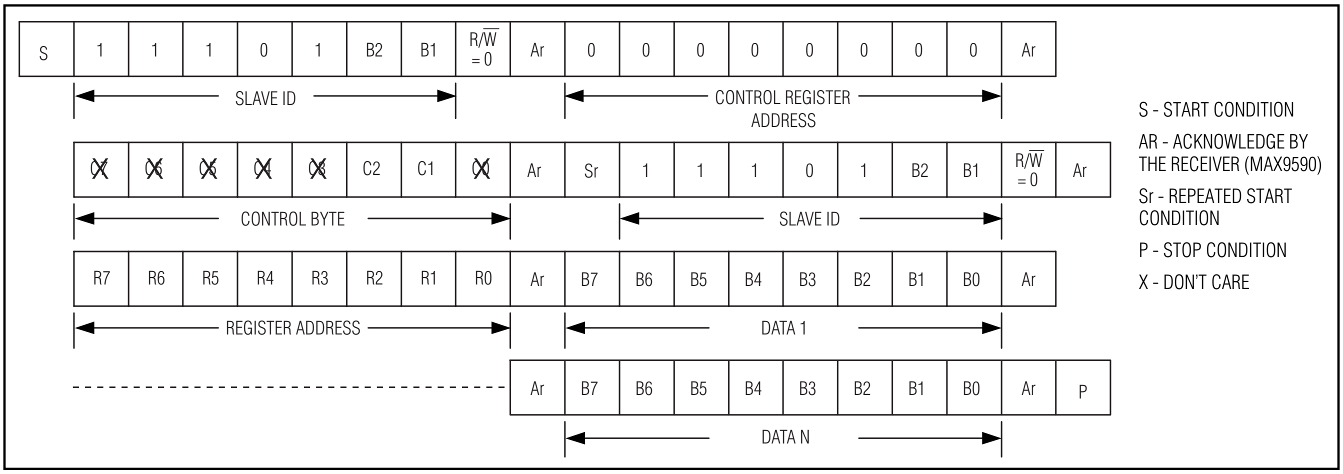

Figure 11. Register Mode Bank Change Write Operation

Table 7. Register Mode Write Operation—Response to Burst Write

SCENARIO	RESPONSE
Burst-write operation involving more data bytes than valid register address locations (A01–A14 or B01–B14). Illustration 1: Burst-write operation involving more than 14 data bytes starting with register address A01. Illustration 2: Burst-write operation involving more than 2 data bytes starting with register address A13.	The device ignores excess bytes after register address A14 or B14.

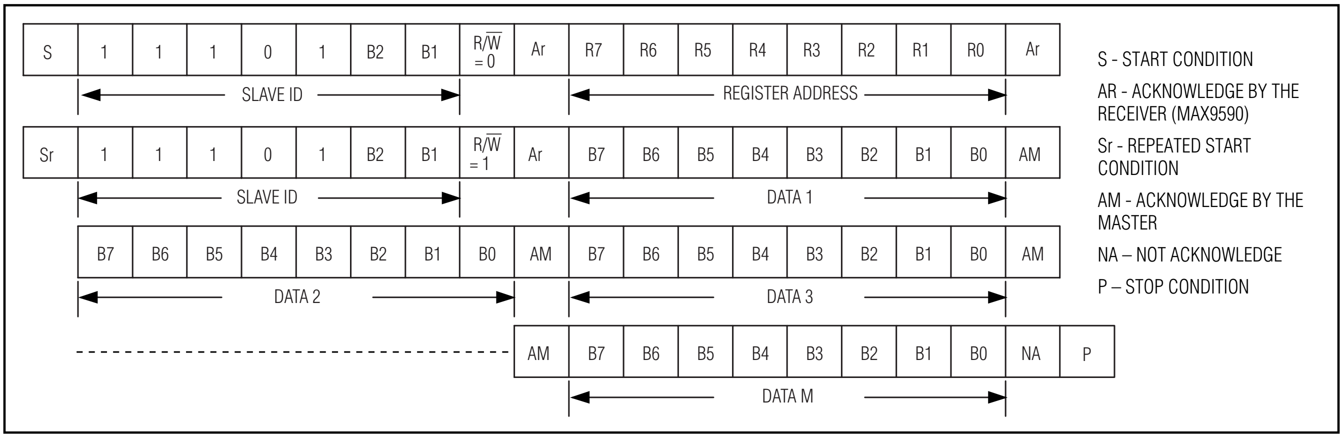

Figure 12. Register Mode Read Operation

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If a read operation requires a bank change, send the slave ID followed by the control register's address (0x00 in MAX9590) and then the control byte data to switch banks. After switching banks, execute a normal register mode read operation as shown in Figure 13

The MAX9590's responses to burst-read operations for various scenarios are summarized below in Table 8.

I^2C Compatibility

The MAX9590 is compatible with existing I^2C systems. SCL and SDA are high-impedance inputs; SDA has an open-drain output that pulls the data line low during the ninth clock pulse. The communication protocol supports standard I^2C 8-bit communications. The general call address is ignored, and CBUS formats are not supported. The devices' address is compatible with 7-bit I^2C addressing protocol only. No 10-bit address formats are supported. Repeated START protocol is supported.

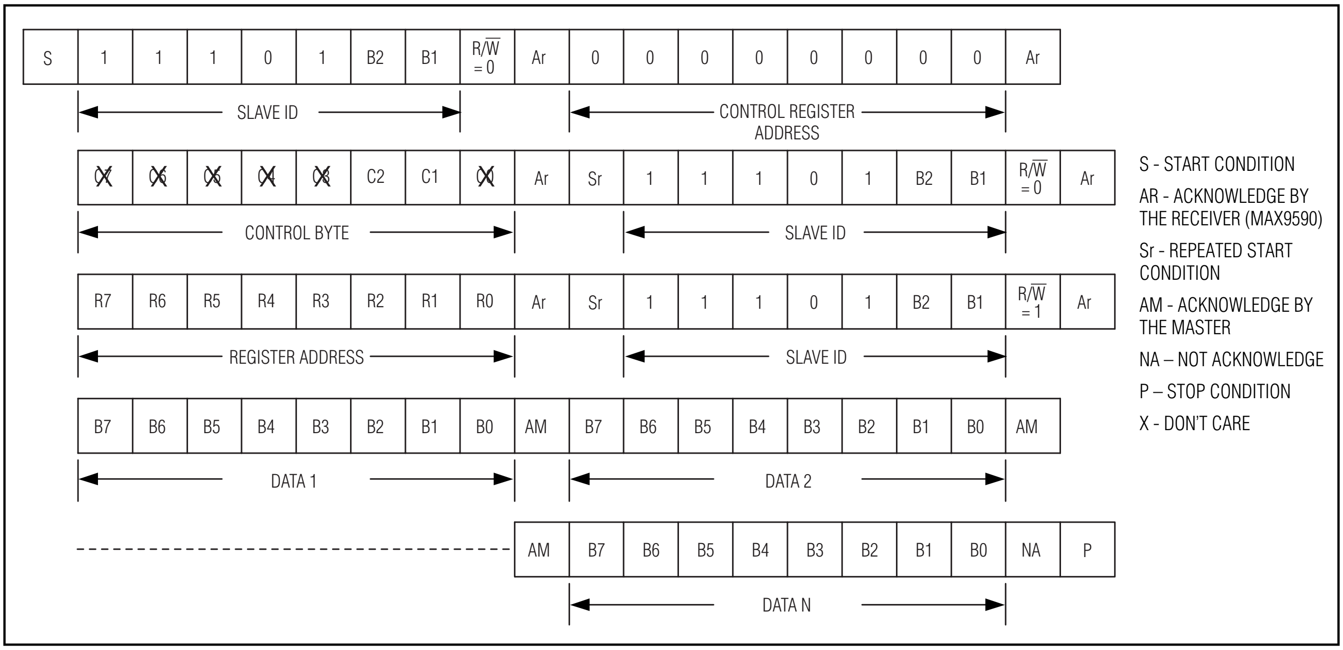


Figure 13. Register Mode Bank Change Read Operation

Table 8. Register Mode Read Operation—Response to Burst Read

SCENARIO	RESPONSE
Burst-read operation involving more than 14 data bytes	The device reads the valid data bytes starting from the specified register address until A14 (or B14). After A14 (or B14), the rest of the data bytes read are 0xFF (hexadecimal) indicating that those data are invalid.
Burst-read operation involving less than 14 data bytes	The device reads data bytes from the corresponding register addresses in sequential order starting with the specified register address and stops after the specified number of data bytes has been read.

Applications Information

Power Dissipation

The maximum power dissipation is the sum of analog circuitry power dissipation, digital circuitry power dissipation, and power dissipation due to the load calculated using a maximum operating voltage of AV_{DD} = 16.5V and DV_{DD} = 5.5V.

Total Power Dissipation = PD(analog) + PD (digital) + PD(load)

PD(analog) = 16.5V x 28mA = 462mW

PD(digital) = 5.5V x 0.75mA = 4.13mW

Each output buffer supplies an average load current of 5mA. The power dissipation per output buffer is therefore:

5mA x 16.5V / 2 (average) = 41.25mW

The device has a total of 18 output buffers therefore:

PD(load) = 41.25mW per output buffer x 18 buffers total = 742.5mW

PD(total) = 462mW + 4.13mW + 742.5mW = 1208.63mW

There will also be AC switching power dissipation, but because of the low duty cycle and the fast transition times involved, this should be minimal.

The maximum power dissipation of the 38-pin TQFN package is 2195mW with a derating factor of 26.5mW/°C above +70°C. Therefore, the maximum power dissipation of the 38-pin TQFN package at +85°C is 1800mW.

Power Supplies and Bypass Capacitors

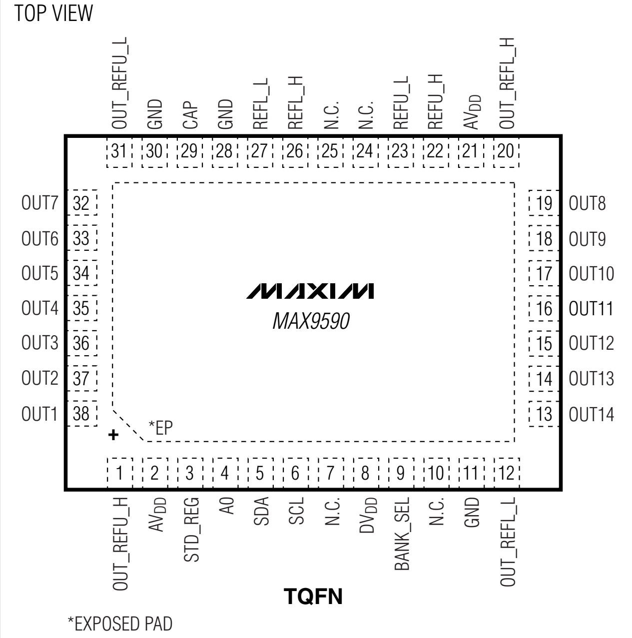
The MAX9590 operates from a single +9V to +16.5V analog supply and a +2.7 to +5.5V digital supply. Bypass AV_{DD} to GND with 0.1µF and 10µF capacitors in parallel. Use an extensive ground plane to ensure optimum performance. Bypass DV_{DD} to GND with a 0.1µF capacitor. Bypass CAP (pin 29) to GND with a 0.1µF capacitor.

Refer to the MAX9590 evaluation kit for a proven PC board layout.

Layout and Grounding

Solder the exposed paddle to a ground plane to provide a low thermal resistance to ground for heat dissipation. Do not route traces under these packages.

Pin Configuration



Chip Information

PROCESS: BiCMOS

Revision History

Pages changed at Rev 1: 1, 2, 7, 19

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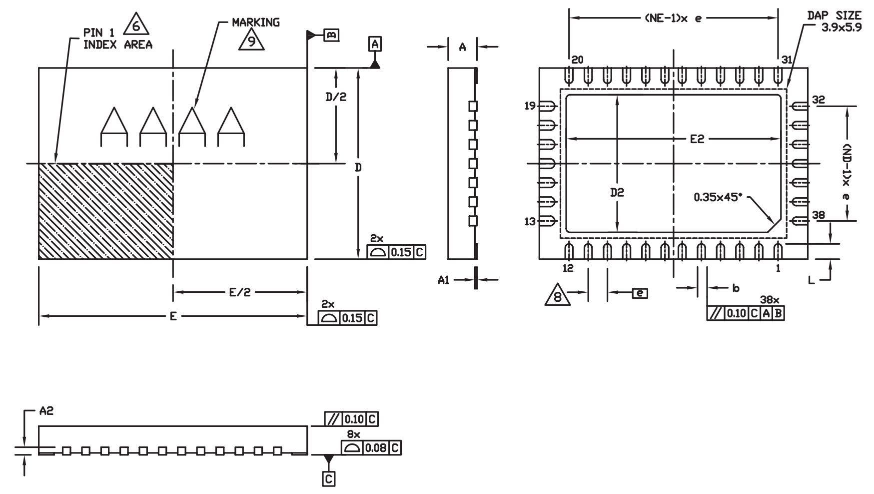
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

38L THIN QFN.EPS



DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 38L THIN QFN, 5x7x0.80mm

APPROVAL | DOCUMENT CONTROL NO. 21-0172 | REV. A | 1/2

-DRAWING NOT TO SCALE-

NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
5. REFER JEDEC MO-220, WHKD-1.
6. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
7. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
9. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

	COMMON DIMENSIONS		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A2	0.20 REF.		
b	0.20	0.25	0.30
D	4.90	5.00	5.10
e	0.50 BSC.		
E	6.90	7.00	7.10
L	0.35	0.40	.045
N	38		
ND	7		
NE	12		

	EXPOSED PAD DIMENSIONS					
	D2			E2		
PACKAGE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T3857-1	3.50	3.60	3.70	5.50	5.60	5.70

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 38L THIN QFN, 5x7x0.80mm

APPROVAL | DOCUMENT CONTROL NO. 21-0172 | REV. A | 2/2

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