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19-5569; Rev 1; 2/11

EVALUATION KIT AVAILABLE

Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

General Description

The MAX9626/MAX9627/MAX9628 are low-noise, low-distortion, and high-bandwidth differential amplifier/ADC drivers for use in applications from DC to 1.35GHz. The exceptional low input-referred noise and low distortion make these parts an excellent solution to drive high-speed 12-bit to 16-bit pipeline ADCs. The output common mode is set through the VOCM input pin, thus eliminating the need for a coupling transformer or AC-coupling capacitors. The ICs feature shutdown mode for power savings and are offered in a 12-pin, 3mm x 3mm TQFN package for operation over a -40°C to +125°C temperature range.

Applications

Communication

Medical Imaging

ATE

High-Performance Instrumentation

Features

- ♦ **Low-Voltage Noise Density 3.6nV/√Hz**
- ♦ **Low Harmonic Distortion**
  - **HD2/HD3 of -102/-105dB at 10MHz**
  - **HD2/HD3 of -86/-80dB at 125MHz**
- ♦ **Factory Set Gain Options: 1V/V, 2V/V, 4V/V**
- ♦ **1.35GHz Small-Signal Bandwidth**
- ♦ **Adjustable Output Common-Mode Voltage**
- ♦ **Differential-to-Differential or Single-Ended-to-Differential Operation**
- ♦ **25µA Shutdown Current**
- ♦ **+2.85V to +5.25V Single-Supply Voltage**
- ♦ **Small, 3mm x 3mm 12-Pin TQFN Package**

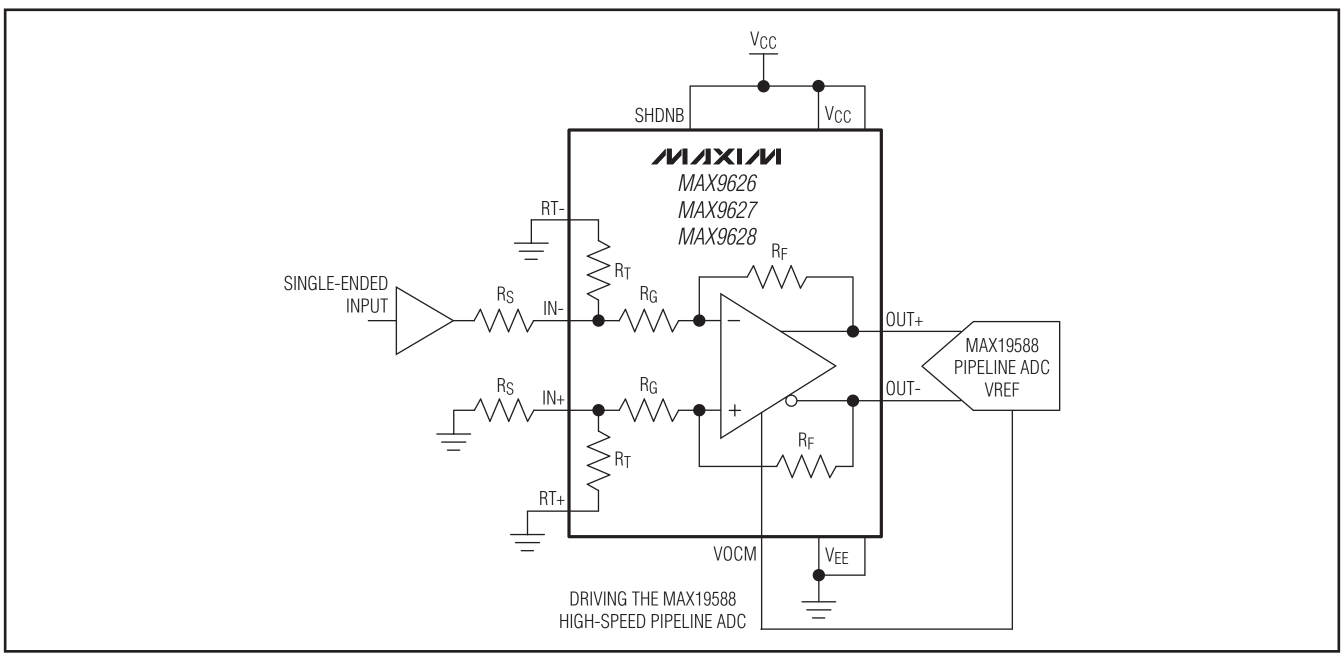
Ordering Information

PART	GAIN (dB)	PIN-PACKAGE	TOP MARK
MAX9626ATC+	1	12 TQFN-EP*	+ABS
MAX9627ATC+	2	12 TQFN-EP*	+ABT
MAX9628ATC+	4	12 TQFN-EP*	+ABU

Note: *All devices are specified over the -40°C to +125°C operating temperature range.*

**EP = Exposed pad.*

Typical Operating Circuit



DRIVING THE MAX19588 HIGH-SPEED PIPELINE ADC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})................................-0.3V to +5.5V
IN+, IN-..(V_{EE} - 2.5V) to (V_{CC} + 0.3V)
RT+, RT- ....(V_{EE} - 2.5V) to (V_{CC} + 0.3V)
RT- to IN- and RT+ to IN+.. ±2V
VOCM, $\overline{SHDN}$, OUT+, OUT- ....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration (OUT+ to OUT-)....................... 1s
Continuous Input Current
(any pin except V_{EE}, V_{CC}, OUT+, OUT-).................... ±20mA

Continuous Power Dissipation (T_A = +70°C)
12-Pin TQFN Multilayer Board (deration 16.7mW/°C
above +70°C)..1333.3mW
θ_{JA} ....60mW/°C
θ_{JC} ....11mW/°C
Operating Temperature Range .... -40°C to +125°C
Junction Temperature ....+150°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{VOCM} = V_{CC}/2, R_L = 500Ω (between OUT+ and OUT-), T_A = -40°C to +125°C. Typical values are at +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS							
Supply Voltage Range	V_{CC}	Guaranteed by PSRR		2.85		5.25	V
Supply Current	I_{CC}	$\overline{SHDN}$ = V_{CC}			59	80	mA
		$\overline{SHDN}$ = GND			25	50	µA
Power-Supply Rejection Ratio	PSRR	V_{VCOM} = V_{CC}/2, 2.85V ≤ V_{CC} ≤ 5.25V, -40°C ≤ T_A ≤ +85°C	MAX9626	66	89		dB
			MAX9627	66	92		
			MAX9628	64	92		
		V_{VCOM} = V_{CC}/2, 2.85V ≤ V_{CC} ≤ 5.25V, -40°C ≤ T_A ≤ +125°C	MAX9626	60	89		
			MAX9627	63	92		
			MAX9628	64	92		
Differential Voltage Gain	G_{DIFF}	V_{OUT+}, V_{OUT-} = -1V to +1V	MAX9626		1		V/V
			MAX9627		2		
			MAX9628		4		
Gain Error		V_{OUT+}, V_{OUT-} = -1V to +1V	MAX9626	-2	±0.2	+2	%
			MAX9627	-2	±0.2	+2	
			MAX9628	-2	±0.2	+2	
Input Offset Voltage		Differential input, V_{IN-} = V_{IN+} = V_{CC}/2, T_A = +25°C	MAX9626		2	±11	mV
			MAX9627		2	±8	
			MAX9628		2	±8	
		Differential input, V_{IN-} = V_{IN+} = V_{CC}/2 T_A = -40°C to +125°C	MAX9626		2	±13	
			MAX9627		2	±10	
			MAX9628		2	±10	
Common-Mode Input Voltage Range (Note 2)	V_{ICM}	Guaranteed by CMRR	MAX9626	-1.5		+1.5	V
			MAX9627	-0.75		+1.5	
			MAX9628	-0.4		+1.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{VOCM} = $V_{CC}/2$, R_L = 500Ω (between OUT+ and OUT-), T_A = -40°C to +125°C. Typical values are at +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	MAX9626		46	62		dB
		MAX9627		50	69		
		MAX9628		54	79		
Output Voltage Swing	V_{OH}	VOCM = V_{CC}		V_{CC} - 1	V_{CC} - 0.8		V
	V_{OL}	V_{VOCM} = 0V			V_{EE} + 0.65	V_{EE} + 0.9	
Output Current		Source: V_{CC} - V_{OUT} = 0.95V			100		mA
		Sink: V_{OUT} - V_{EE} = 0.95V			100		
Common-Mode Input Resistance		MAX9626			200		Ω
		MAX9627			225		
		MAX9628			312		
Differential Input Resistance		MAX9626			267		Ω
		MAX9627			225		
		MAX9628			209		
Input Termination Resistance		RT- to IN- and RT+ to IN+			64		Ω
AC SPECIFICATIONS							
3dB Large-Signal Bandwidth	LSB_{3dB}	V_{OUT+} - V_{OUT-} = 2.0V_{P-P}	MAX9626		1150		MHz
			MAX9627		1350		
			MAX9628		1000		
0.1dB Large-Signal Bandwidth	$LSB_{0.1dB}$	V_{OUT+} - V_{OUT-} = 2.0V_{P-P}	MAX9626		80		MHz
			MAX9627		80		
			MAX9628		90		
Slew Rate	SR	V_{OUT+} - V_{OUT-} = 2.0V_{P-P}	MAX9626		6500		V/µs
			MAX9627		6100		
			MAX9628		5500		
AC Power-Supply Rejection Ratio	AC PSRR	V_{VOCM} = 1.65V, f = 10MHz	MAX9626		64		dB
			MAX9627		65		
			MAX9628		62		
Input Voltage Noise	e_N	f = 10MHz	MAX9626		5.7		$nV/\sqrt{Hz}$
			MAX9627		4.3		
			MAX9628		3.6		
Noise Figure	NF	R_S = 50Ω	MAX9626		22.2		dB
			MAX9627		19.7		
			MAX9628		18.1		

Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{VOCM} = V_{CC}/2, R_L = 500Ω (between OUT+ and OUT-), T_A = -40°C to +125°C. Typical values are at +25°C, unless otherwise noted.) (Note 1)

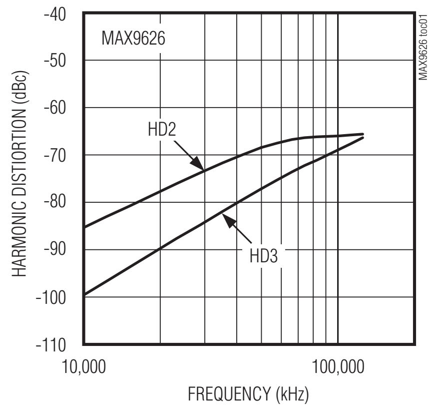
PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Harmonic Distortion	HD	f = 10MHz, V_{OUT+} - V_{OUT-} = 2.0V_{P-P}, V_{CC} = 5V	MAX9626	HD2		-98		dBc
				HD3		-103		
			MAX9627	HD2		-102		
				HD3		-105		
			MAX9628	HD2		-91		
				HD3		-97		
		f = 125MHz, V_{OUT+} - V_{OUT-} = 2.0V_{P-P}, V_{CC} = 5V	MAX9626	HD2		-80		
				HD3		-80		
			MAX9627	HD2		-86		
				HD3		-80		
			MAX9628	HD2		-80		
				HD3		-75		
Capacitive Load	C_{LOAD}	No sustained oscillation				10		pF
Power-Up Time						2.3		µs
VOCM INPUT PIN								
Input Voltage Range		Guaranteed by VOCM CMRR test			1.1		V_{CC} - 1.1	V
Output Common-Mode Rejection Ratio (Note 3)	$CMRR_{VOCM}$				52	64		dB
Output Common-Mode Gain (Note 3)	G_{VOCM}	V_{VOCM} = 1.1V to V_{CC} -1.1V, T_A = -40°C to +125°C			0.98	0.99	1.00	V/V
Input Offset Voltage (Note 3)						12	±21	mV
Input Bias Current						1	10	µA
Input Impedance						35		MΩ
Output Balance Error		ΔV_{OUT} = 1V_{PP} , f = 10MHz				-77		dB
-3dB Small-Signal Bandwidth		V_{VOCM} = 0.1V_{P-P}				700		MHz
$\overline{SHDN}$ INPUT PIN								
Input Voltage	V_{IL}						0.8	V
	V_{IH}				1.2			
Input Current	I_{IL}	$V_{\overline{SHDN}}$ = 0V				0.01	2	µA
	I_{IH}	$V_{\overline{SHDN}}$ = V_{CC}				3.3	20	
Turn-On Time	t_{ON}					0.6		µs
Turn-Off Time	t_{OFF}					0.2		

Note 1: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 2: Input voltage range is a function of VOCM. See the *Input Voltage Range* section for details.
Note 3: Limits are guaranteed by design based on bench characterization. Testing is functional using different limits.

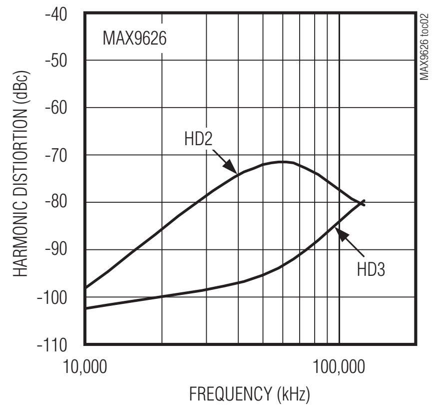
Typical Operating Characteristics

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

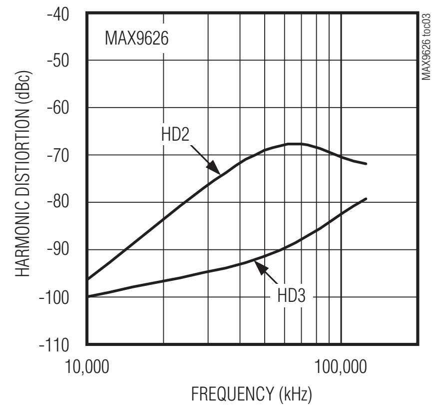
HARMONIC DISTORTION vs. FREQUENCY
R_L = 100Ω, V_{CC} = 5V



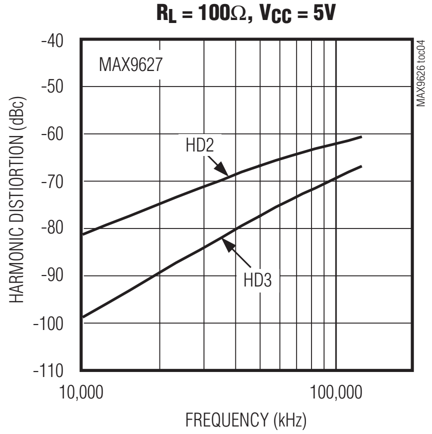
HARMONIC DISTORTION vs. FREQUENCY
R_L = 500Ω, V_{CC} = 5V



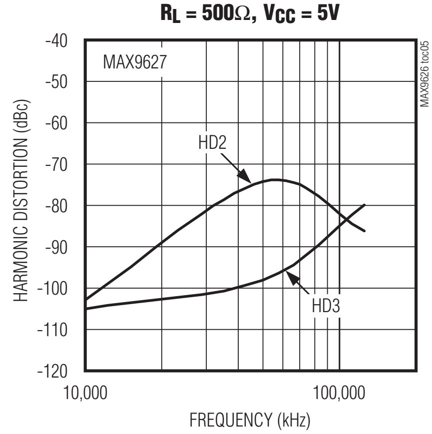
HARMONIC DISTORTION vs. FREQUENCY
R_L = 1kΩ, V_{CC} = 5V



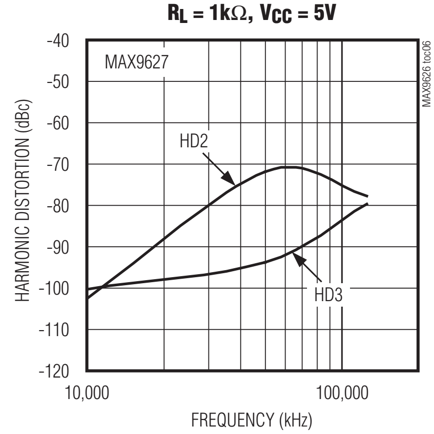
HARMONIC DISTORTION vs. FREQUENCY
R_L = 100Ω, V_{CC} = 5V



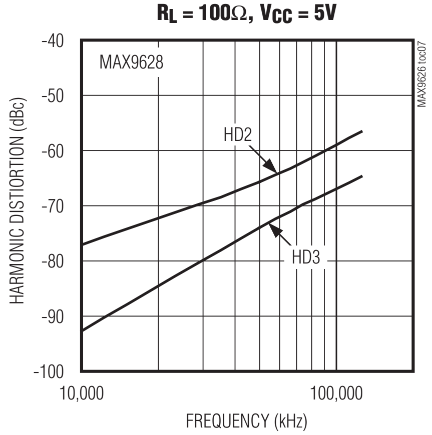
HARMONIC DISTORTION vs. FREQUENCY
R_L = 500Ω, V_{CC} = 5V



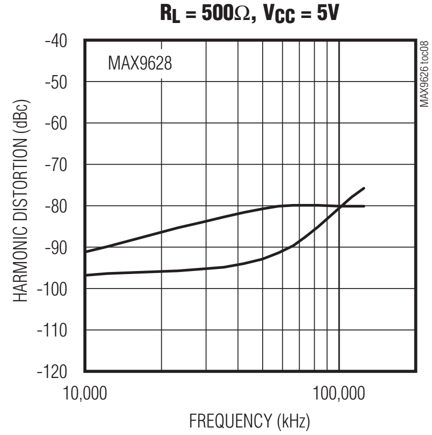
HARMONIC DISTORTION vs. FREQUENCY
R_L = 1kΩ, V_{CC} = 5V



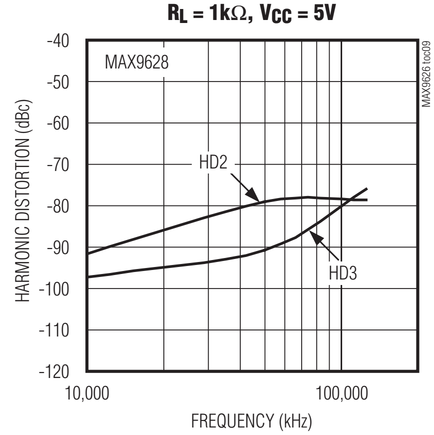
HARMONIC DISTORTION vs. FREQUENCY
R_L = 100Ω, V_{CC} = 5V



HARMONIC DISTORTION vs. FREQUENCY
R_L = 500Ω, V_{CC} = 5V



HARMONIC DISTORTION vs. FREQUENCY
R_L = 1kΩ, V_{CC} = 5V

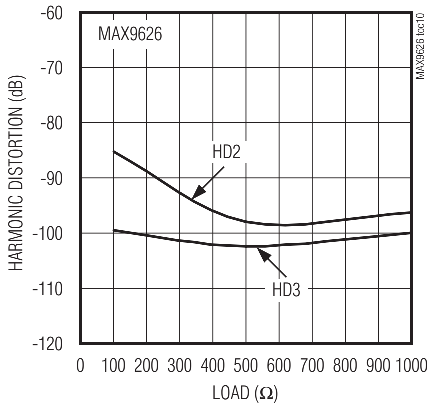


Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

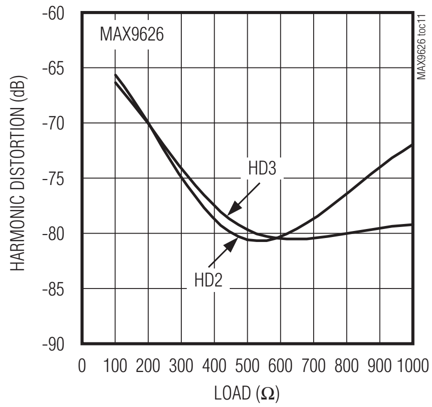
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

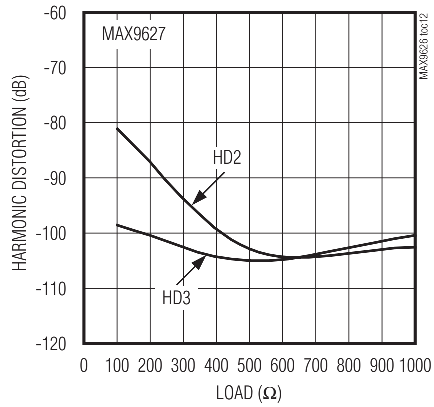
HARMONIC DISTORTION vs. LOAD
f = 10MHz, V_{CC} = 5V



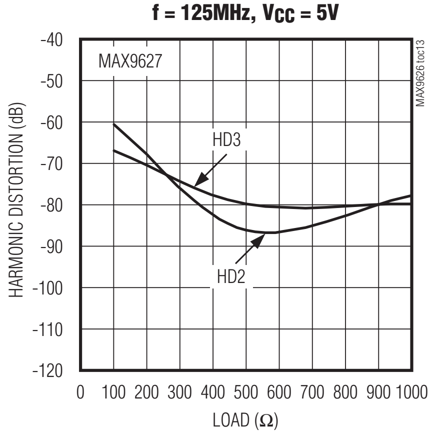
HARMONIC DISTORTION vs. LOAD
f = 125MHz, V_{CC} = 5V



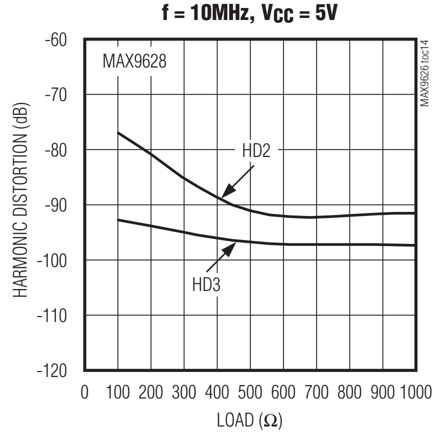
HARMONIC DISTORTION vs. LOAD
f = 10MHz, V_{CC} = 5V



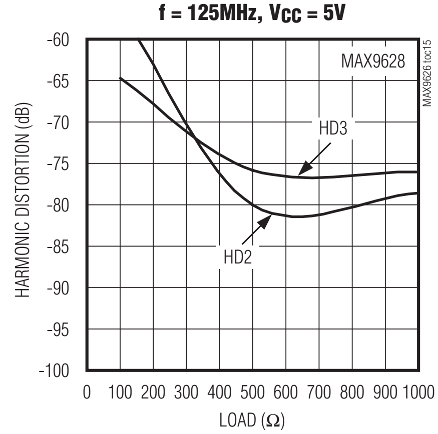
HARMONIC DISTORTION vs. LOAD
f = 125MHz, V_{CC} = 5V



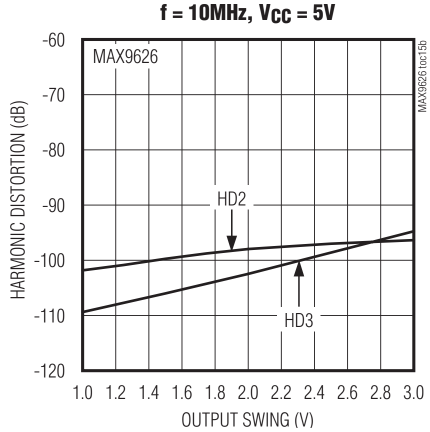
HARMONIC DISTORTION vs. LOAD
f = 10MHz, V_{CC} = 5V



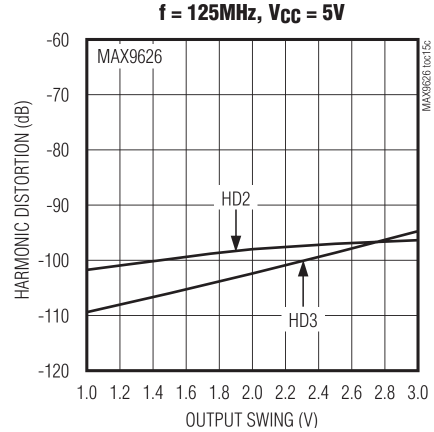
HARMONIC DISTORTION vs. LOAD
f = 125MHz, V_{CC} = 5V



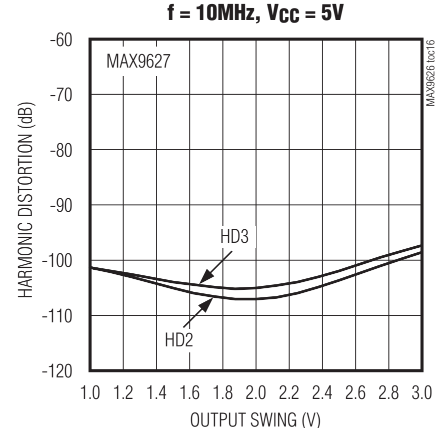
HARMONIC DISTORTION
vs. DIFFERENTIAL OUTPUT SWING
f = 10MHz, V_{CC} = 5V



HARMONIC DISTORTION
vs. DIFFERENTIAL OUTPUT SWING
f = 125MHz, V_{CC} = 5V



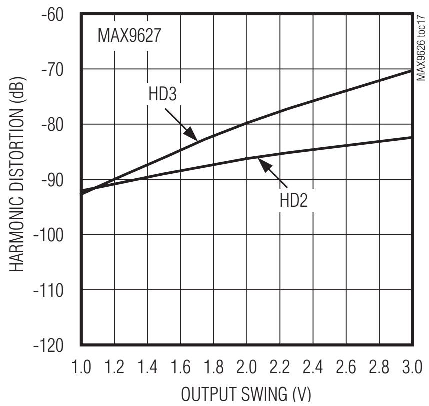
HARMONIC DISTORTION vs.
DIFFERENTIAL OUTPUT SWING
f = 10MHz, V_{CC} = 5V



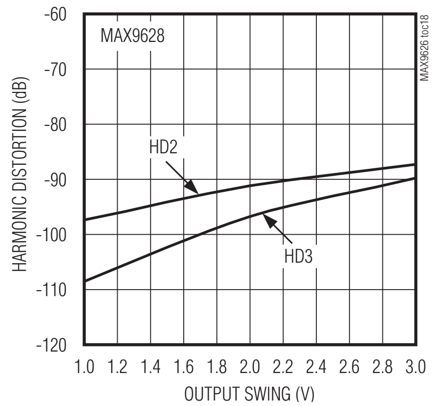
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

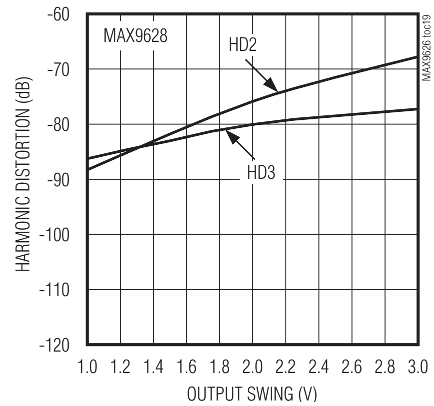
HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT SWING
f = 125MHz, V_{CC} = 5V



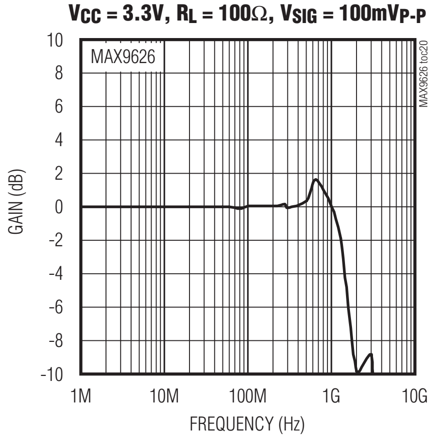
HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT SWING
f = 10MHz, V_{CC} = 5V



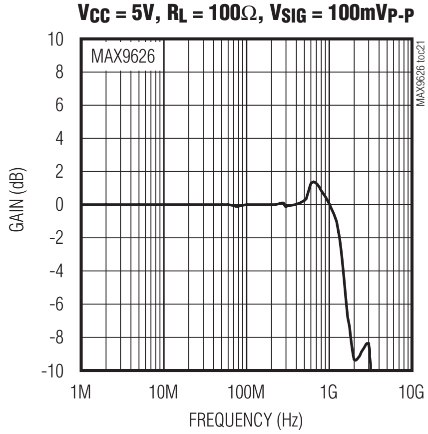
HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT SWING
f = 125MHz, V_{CC} = 5V



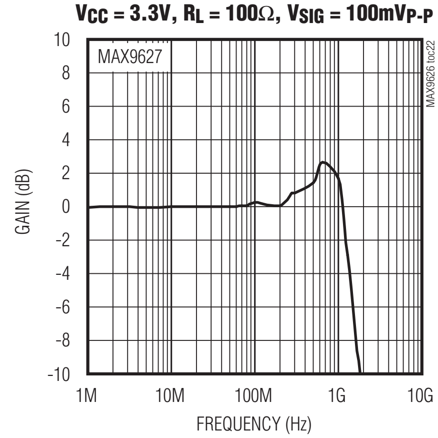
SMALL-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 3.3V, R_L = 100Ω, V_{SIG} = 100mV_{P-P}



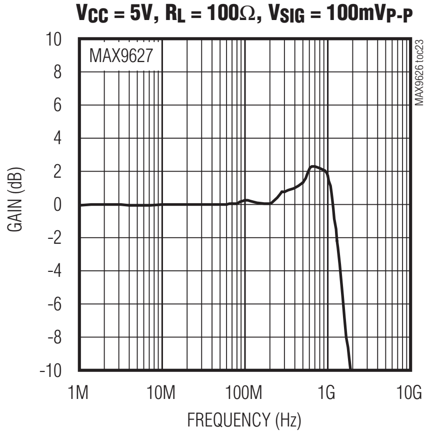
SMALL-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 5V, R_L = 100Ω, V_{SIG} = 100mV_{P-P}



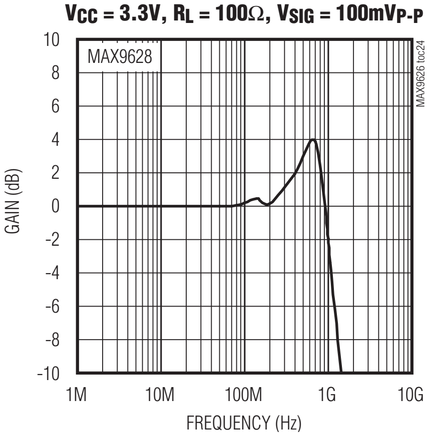
SMALL-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 3.3V, R_L = 100Ω, V_{SIG} = 100mV_{P-P}



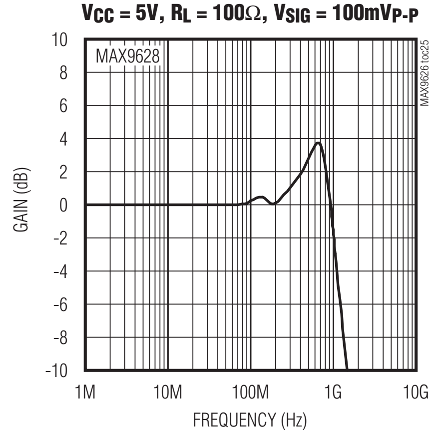
SMALL-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 5V, R_L = 100Ω, V_{SIG} = 100mV_{P-P}



SMALL-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 3.3V, R_L = 100Ω, V_{SIG} = 100mV_{P-P}



SMALL-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 5V, R_L = 100Ω, V_{SIG} = 100mV_{P-P}

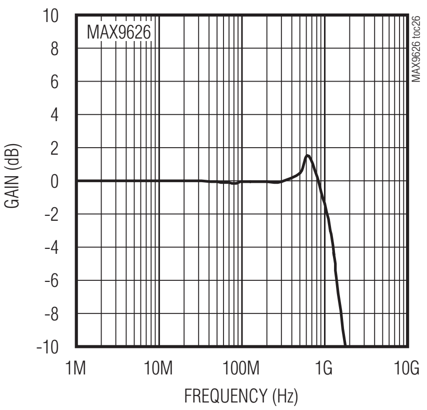


Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

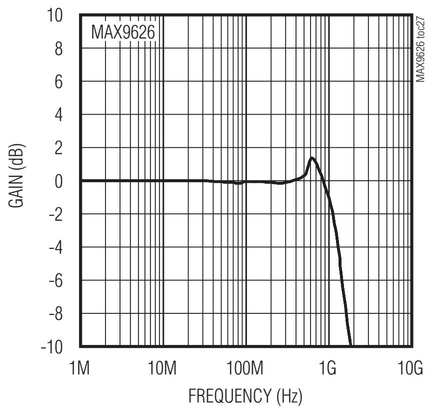
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

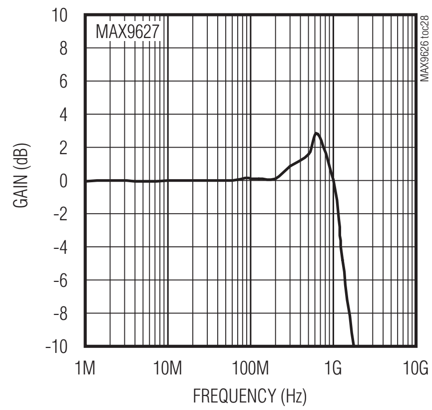
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 3.3V, R_L = 100Ω, V_{SIG} = 2V_{P-P}



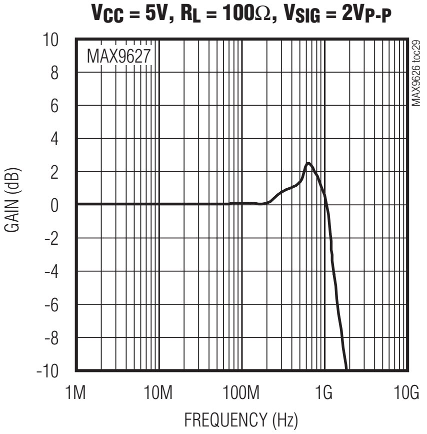
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 5V, R_L = 100Ω, V_{SIG} = 2V_{P-P}



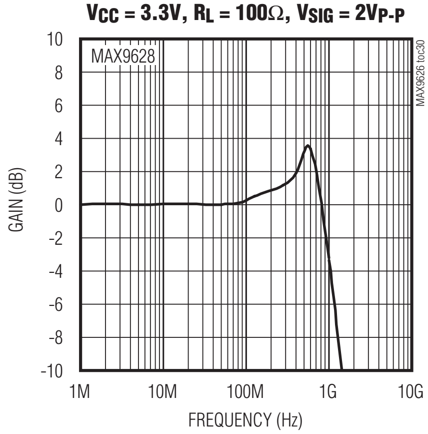
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 3.3V, R_L = 100Ω, V_{SIG} = 2V_{P-P}



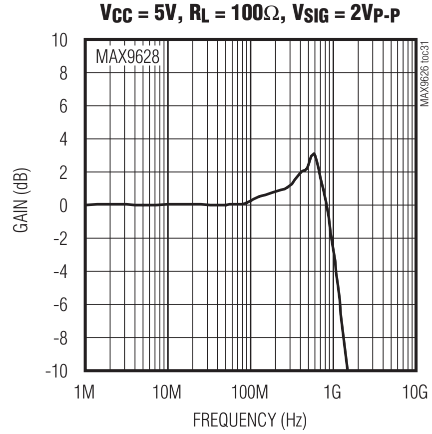
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 5V, R_L = 100Ω, V_{SIG} = 2V_{P-P}



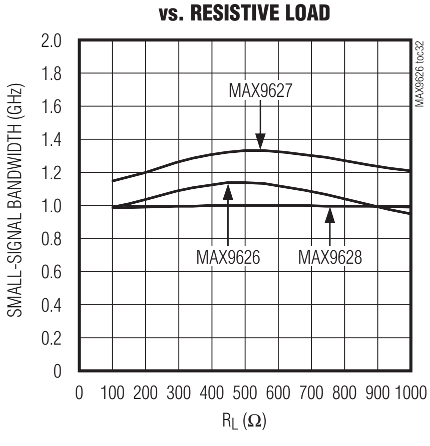
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 3.3V, R_L = 100Ω, V_{SIG} = 2V_{P-P}



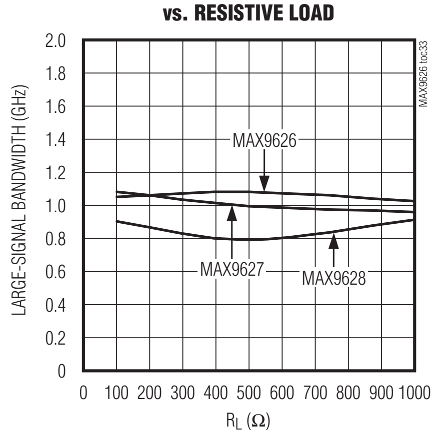
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY
V_{CC} = 5V, R_L = 100Ω, V_{SIG} = 2V_{P-P}



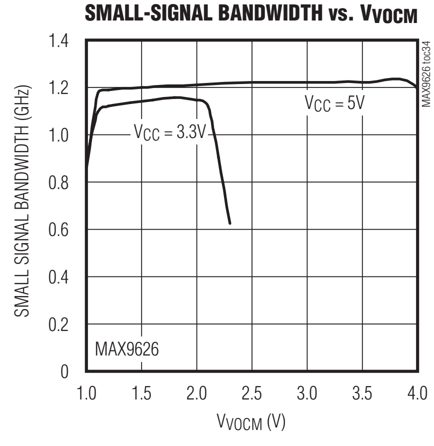
SMALL-SIGNAL BANDWIDTH
vs. RESISTIVE LOAD



LARGE-SIGNAL BANDWIDTH
vs. RESISTIVE LOAD



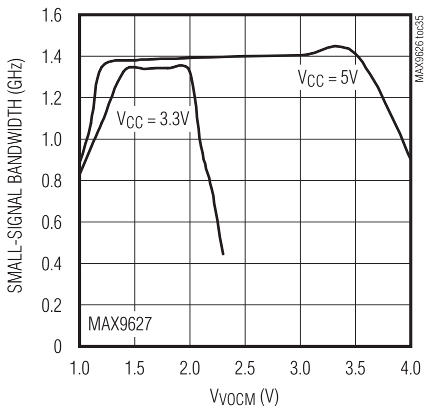
SMALL-SIGNAL BANDWIDTH vs. V_{VOCM}



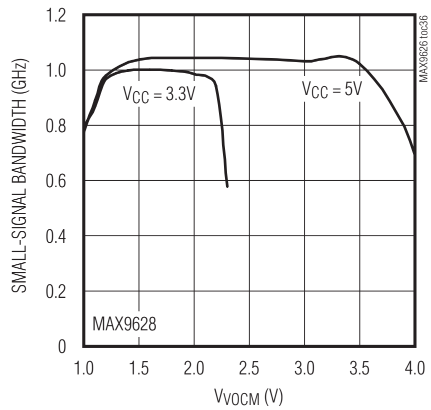
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

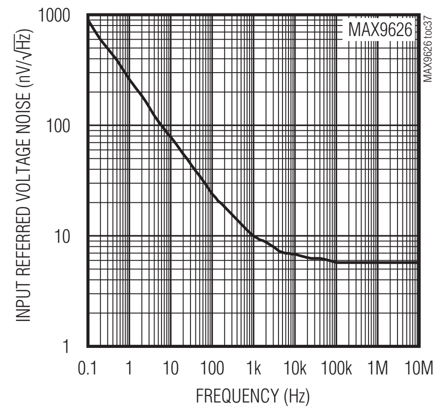
SMALL-SIGNAL BANDWIDTH vs. V_{VOCM}



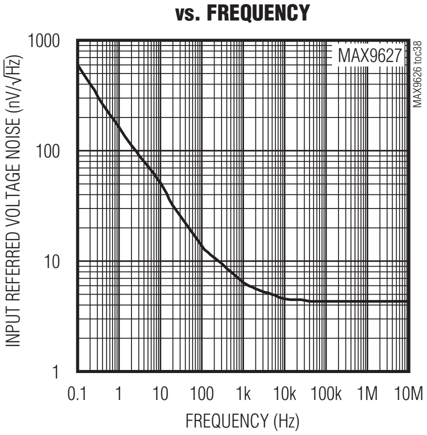
SMALL-SIGNAL BANDWIDTH vs. V_{VOCM}



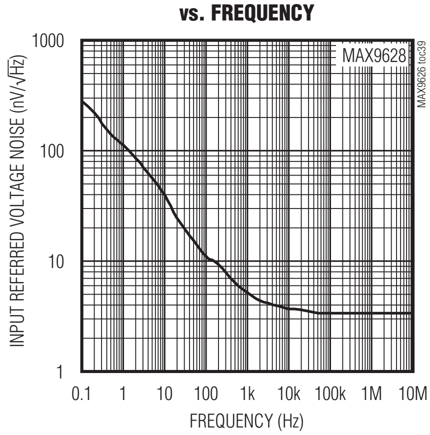
INPUT REFERRED VOLTAGE NOISE vs. FREQUENCY



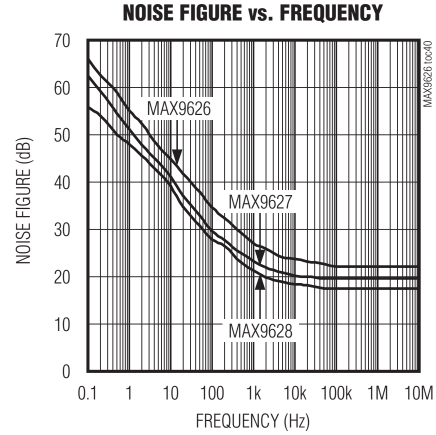
INPUT REFERRED VOLTAGE NOISE vs. FREQUENCY



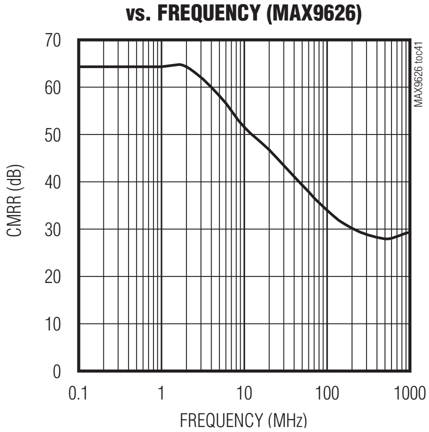
INPUT REFERRED VOLTAGE NOISE vs. FREQUENCY



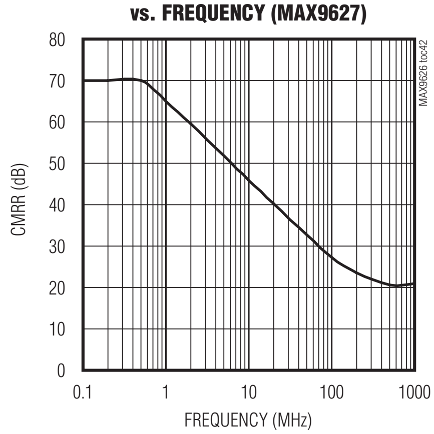
NOISE FIGURE vs. FREQUENCY



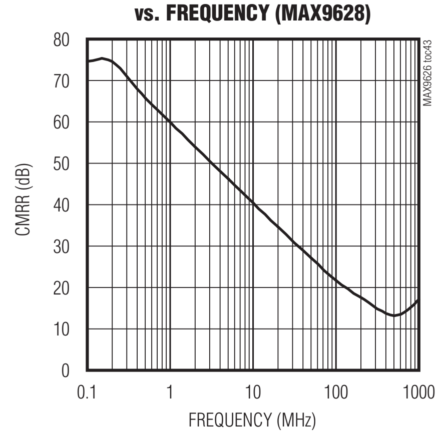
COMMON-MODE REJECTION RATIO vs. FREQUENCY (MAX9626)



COMMON-MODE REJECTION RATIO vs. FREQUENCY (MAX9627)



COMMON-MODE REJECTION RATIO vs. FREQUENCY (MAX9628)

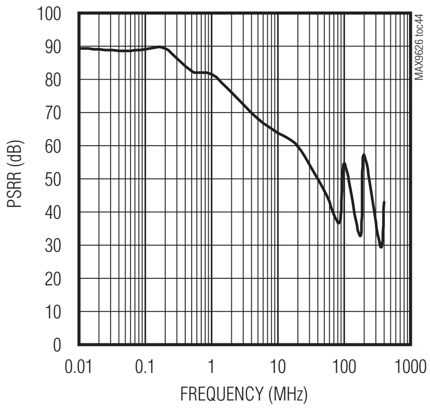


Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

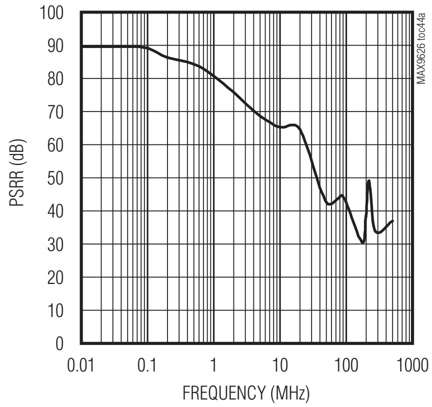
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = $V_{CC}/2$, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

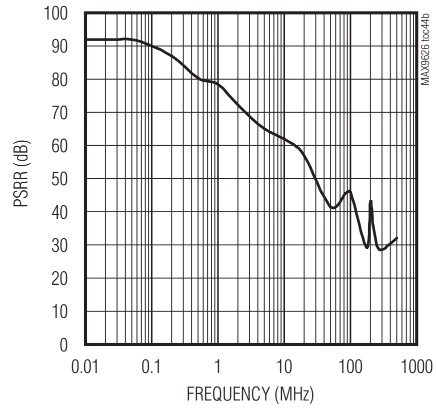
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MAX9626)



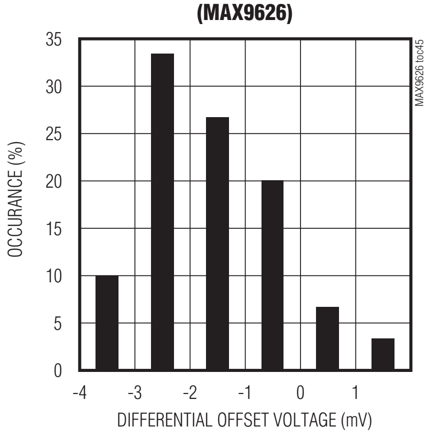
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MAX9627)



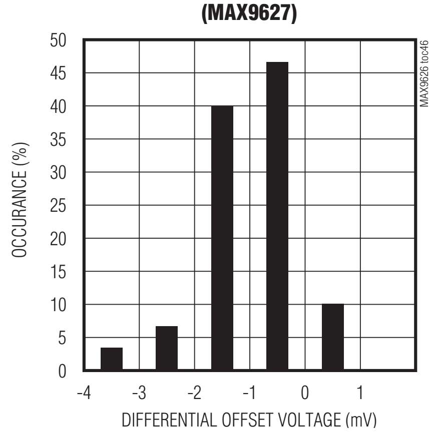
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MAX9628)



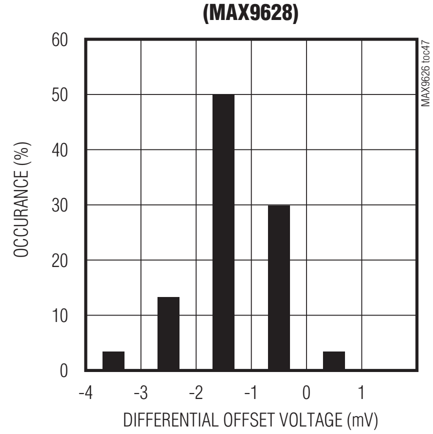
OFFSET VOLTAGE HISTOGRAM (MAX9626)



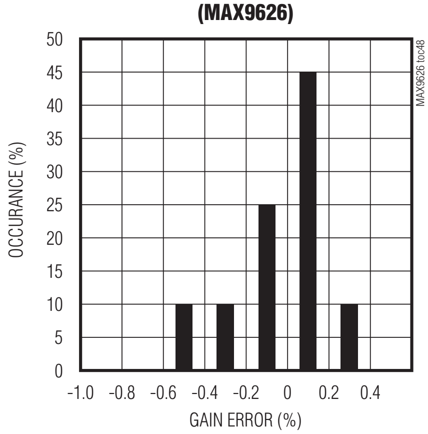
OFFSET VOLTAGE HISTOGRAM (MAX9627)



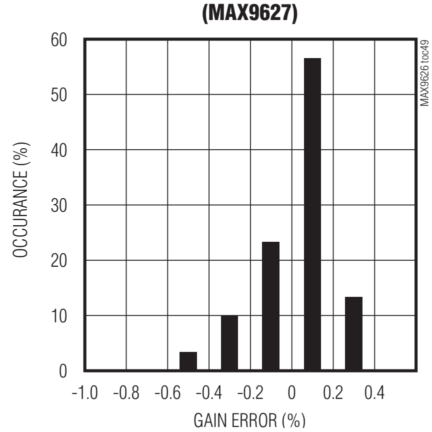
OFFSET VOLTAGE HISTOGRAM (MAX9628)



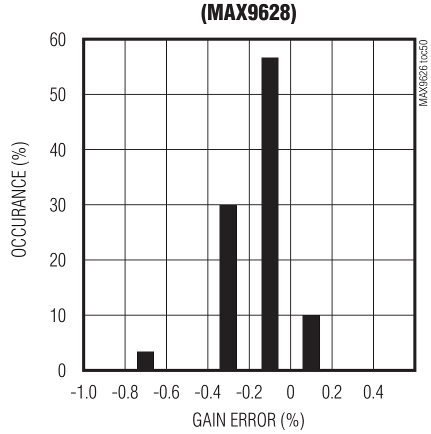
GAIN ERROR HISTOGRAM (MAX9626)



GAIN ERROR HISTOGRAM (MAX9627)



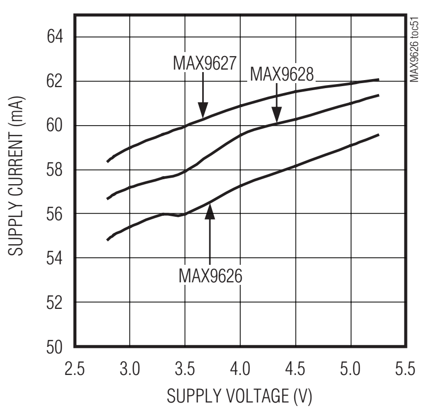
GAIN ERROR HISTOGRAM (MAX9628)



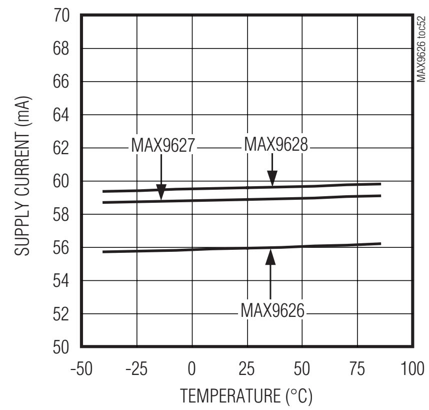
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

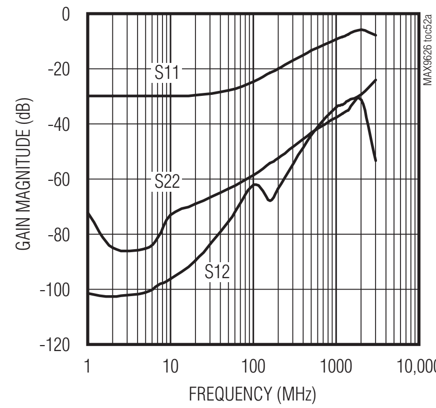
SUPPLY CURRENT vs. SUPPLY VOLTAGE



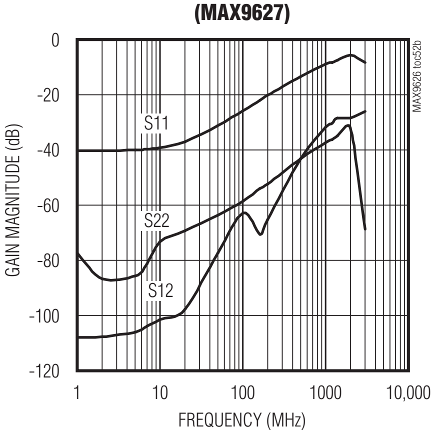
SUPPLY CURRENT vs. TEMPERATURE



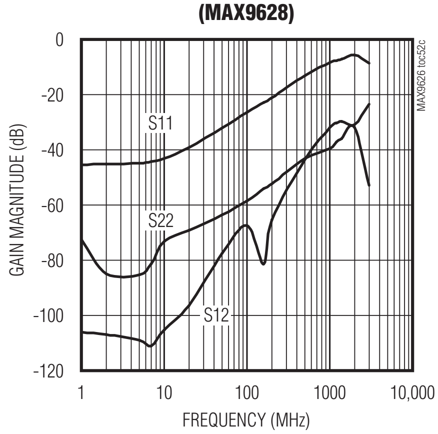
S PARAMETERS vs. FREQUENCY (MAX9626)



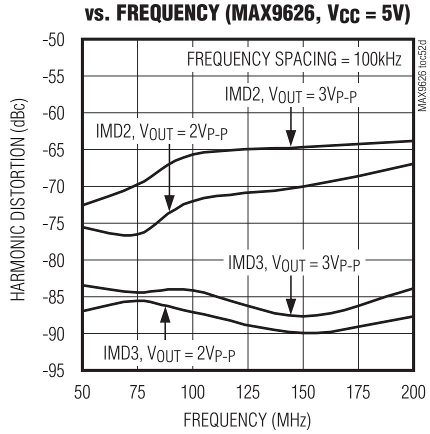
S PARAMETERS vs. FREQUENCY (MAX9627)



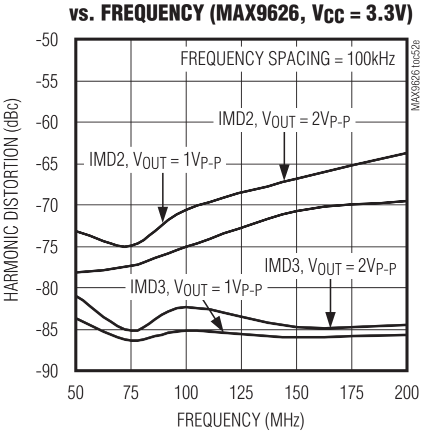
S PARAMETERS vs. FREQUENCY (MAX9628)



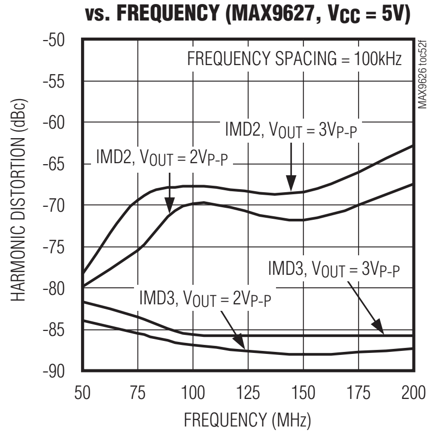
INTERMODULATION DISTORTION vs. FREQUENCY (MAX9626, V_{CC} = 5V)



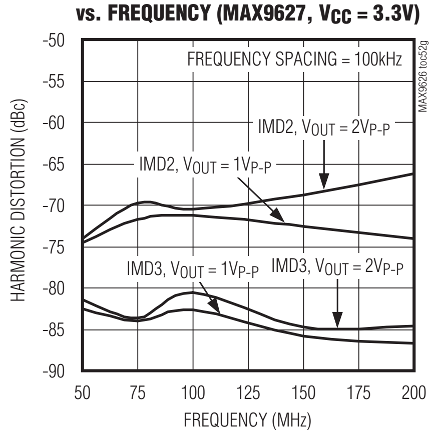
INTERMODULATION DISTORTION vs. FREQUENCY (MAX9626, V_{CC} = 3.3V)



INTERMODULATION DISTORTION vs. FREQUENCY (MAX9627, V_{CC} = 5V)



INTERMODULATION DISTORTION vs. FREQUENCY (MAX9627, V_{CC} = 3.3V)

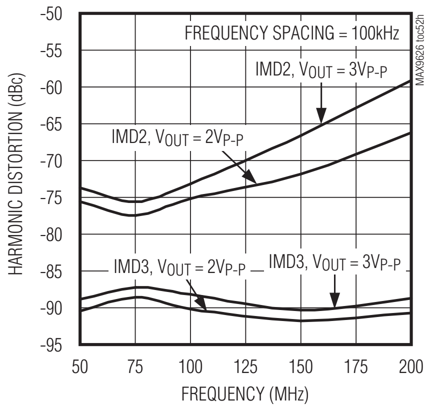


Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

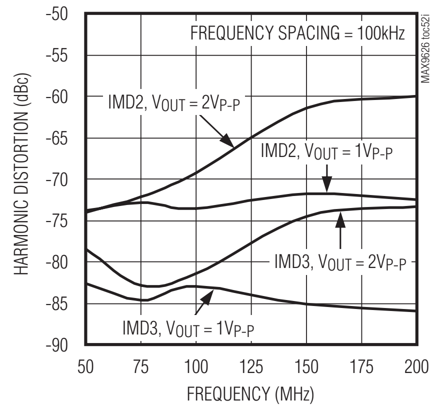
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = $V_{CC}/2$, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)

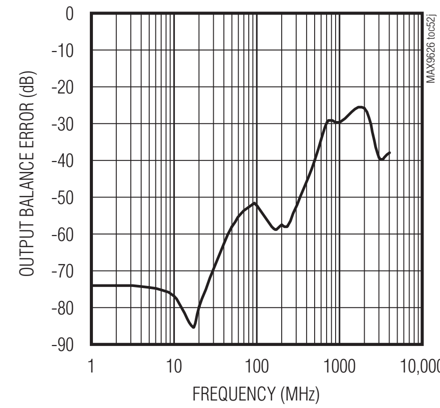
INTERMODULATION DISTORTION vs. FREQUENCY (MAX9628, V_{CC} = 5V)



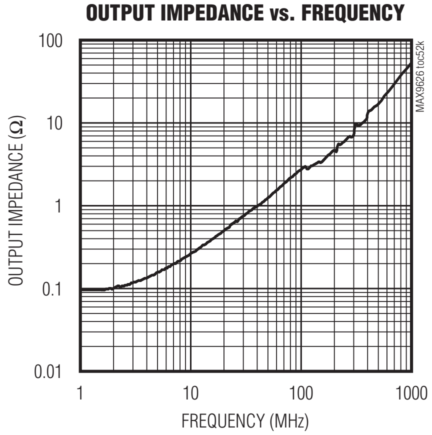
INTERMODULATION DISTORTION vs. FREQUENCY (MAX9628, V_{CC} = 3.3V)



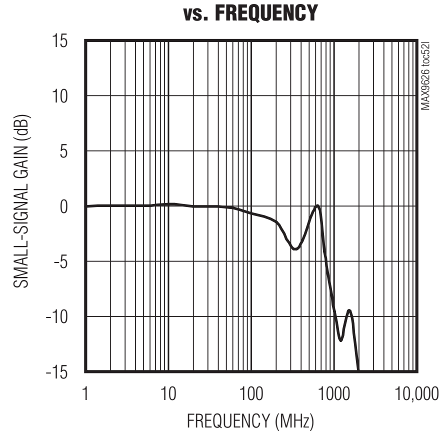
OUTPUT BALANCE ERROR vs. FREQUENCY



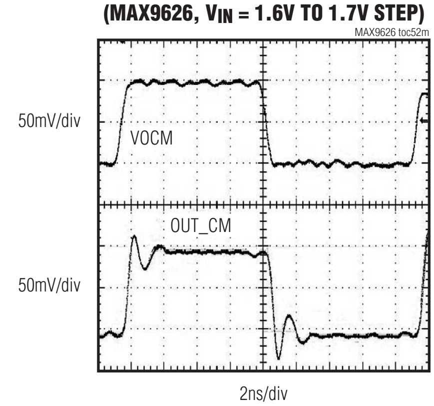
OUTPUT IMPEDANCE vs. FREQUENCY



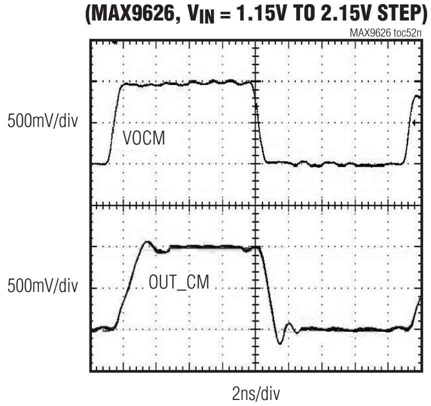
VCOM SMALL-SIGNAL GAIN vs. FREQUENCY



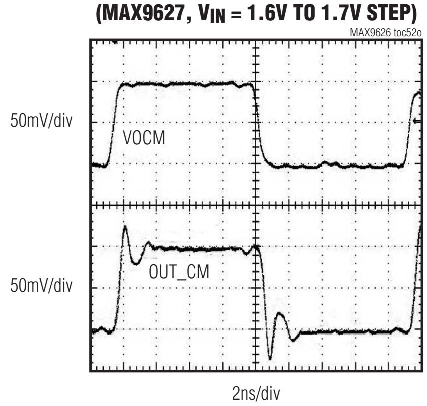
VOCM TRANSIENT RESPONSE (MAX9626, V_{IN} = 1.6V TO 1.7V STEP)



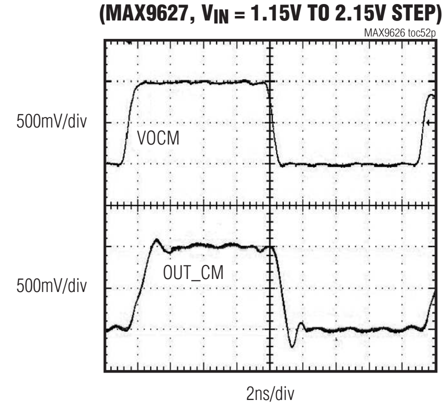
VOCM TRANSIENT RESPONSE (MAX9626, V_{IN} = 1.15V TO 2.15V STEP)



VOCM TRANSIENT RESPONSE (MAX9627, V_{IN} = 1.6V TO 1.7V STEP)



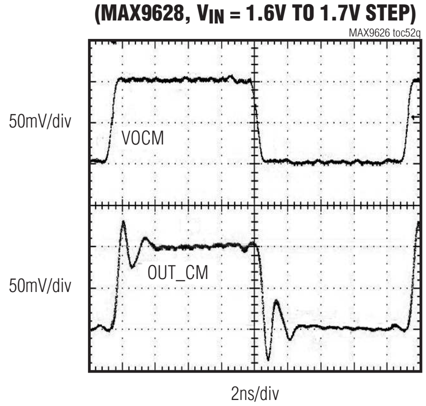
VOCM TRANSIENT RESPONSE (MAX9627, V_{IN} = 1.15V TO 2.15V STEP)



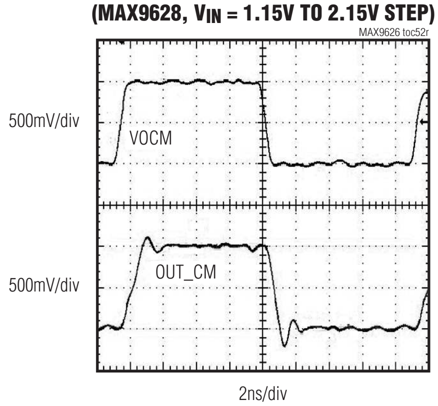
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, V_{EE} = 0V, V_{IN-} = V_{IN+} = 0V, $\overline{SHDN}$ = V_{CC}, V_{ICM} = 0V, V_{VOCM} = V_{CC}/2, R_L = 500Ω, single ended. Plot applies to all versions, unless noted otherwise.)versions, unless noted otherwise.)

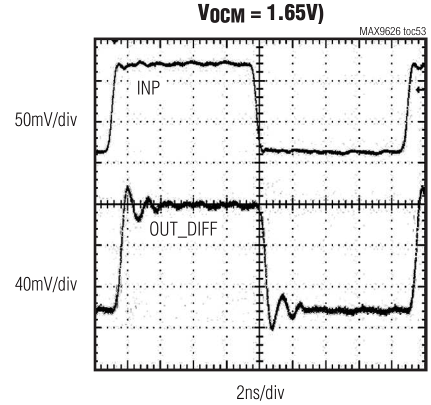
VOCM TRANSIENT RESPONSE (MAX9628, V_{IN} = 1.6V TO 1.7V STEP)



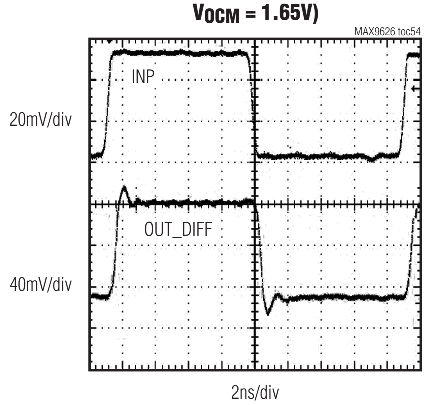
VOCM TRANSIENT RESPONSE (MAX9628, V_{IN} = 1.15V TO 2.15V STEP)



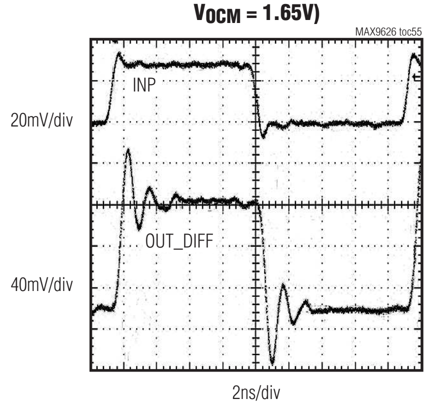
SMALL-SIGNAL TRANSIENT RESPONSE (MAX9626, V_{IN} = 0 TO 100mV STEP, V_{OCM} = 1.65V)



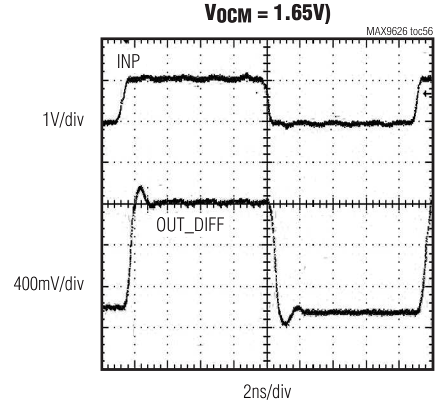
SMALL-SIGNAL TRANSIENT RESPONSE (MAX9627, V_{IN} = 0 TO 50mV STEP, V_{OCM} = 1.65V)



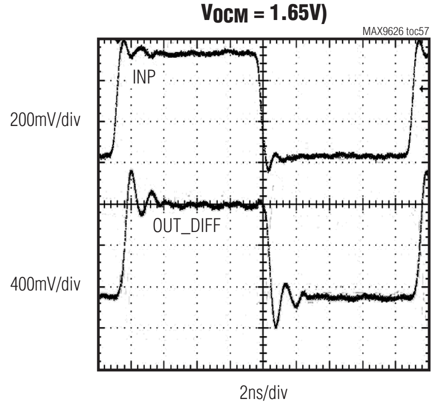
SMALL-SIGNAL TRANSIENT RESPONSE (MAX9628, V_{IN} = 0 TO 25mV STEP, V_{OCM} = 1.65V)



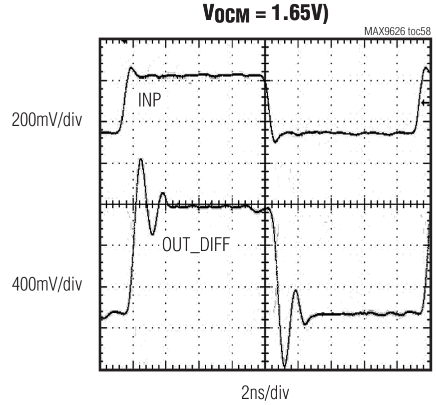
LARGE-SIGNAL TRANSIENT RESPONSE (MAX9626, V_{IN} = 0 TO 1V STEP, V_{OCM} = 1.65V)



LARGE-SIGNAL TRANSIENT RESPONSE (MAX9627, V_{IN} = 0 TO 500mV STEP, V_{OCM} = 1.65V)

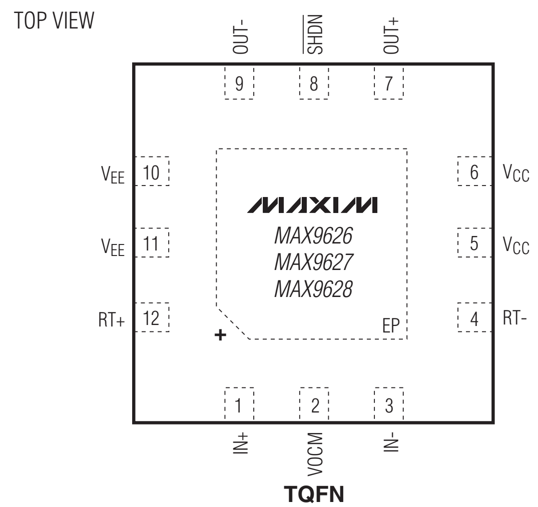


LARGE-SIGNAL TRANSIENT RESPONSE (MAX9628, V_{IN} = 0 TO 250mV STEP, V_{OCM} = 1.65V)



Low-Noise, Low-Distortion, 1.35GHz Fully Differential Amplifiers

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	IN+	Noninverting Differential Input
2	VOCM	Output Common-Mode Voltage Input
3	IN-	Inverting Differential Input
4	RT-	Termination Resistor Terminal for IN-
5, 6	V_{CC}	Positive Supply Voltage
7	OUT+	Noninverting Differential Output
8	$\overline{SHDN}$	Active-Low Shutdown Mode Input
9	OUT-	Inverting Differential Output
10, 11	V_{EE}	Negative Supply Voltage
12	RT+	Termination Resistor Terminal for IN+
—	EP	Exposed Pad. Connected to V_{EE}.

Detailed Description

The MAX9626/MAX9627/MAX9628 family employs voltage feedback to implement a differential-in to differential-out amplifier. On-chip feedback resistors set the gain of the amplifier. The use of on-chip resistors not only saves cost and space, but also maximizes the overall amplifier's performance.

There are two feedback loops within the amplifier circuit. The differential feedback loop employs the on-chip resistors to set the differential gain. The signal is applied differentially at the inputs and the output signal is obtained differentially at the outputs. The common-mode feedback loop controls the common-mode voltage at the outputs. Both inverting and noninverting outputs exhibit a common-mode voltage equal to the voltage applied at VOCM input, without affecting the differential output signal. The outputs are perfectly balanced having signals of equal amplitude and 180° apart in-phase.

Amplifier input impedance is determined by internal gain resistors. Therefore, source impedance does affect the gain of the amplifier. Input termination resistors are required to achieve source impedance match. If preferred, the customer has the choice of using the on-chip termination resistors. If they are used, then the amplifier's input impedance is 50Ω for single-ended input configuration. The amplifier's differential gain accuracy is directly affected by the source impedance value.

The ICs feature a proprietary circuit design. The use of predistortion and dynamic distortion cancellation greatly improves large-signal AC-performance at high frequency.

Fixed Gain Options for Best AC Performance

The ICs have internal gain resistors to achieve excellent bandwidth and distortion performance. Because the virtual ground nodes among the gain resistors and the inputs of the amplifier are internal to the device, the parasitic capacitors of such nodes are kept to the minimum. This enhances the AC performance of the device.

The ICs have three gain options with resistor values as per Table 1, while keeping the bandwidth constant.

Table 1. Amplifier's Gain Setting and Internal Resistor Values

GAIN (V/V)	R_G (Ω)	R_F (Ω)	3dB BANDWIDTH (GHz)
1	200	200	1
2	150	300	1.35
4	125	500	1.15

The differential gain is given by the equation: $G = R_F/R_G$

Internal Terminations

Use the internal R_T resistors in applications where the source impedance R_S is 50Ω and the input impedance of the amplifier has to match with it. For a perfectly balanced circuit driven by a differential source impedance, the input impedance of the amplifier is given by the simple equation $R_{IN} = 2 \times R_G$. For single-ended input applications, where the source impedance of 50Ω connects to either input, such as in the *Typical Operating Circuit*, the input impedance of the amplifier is given by the equation:

$$R_{IN} = \frac{R_G}{\left(1 - \frac{R_F}{2 \times (R_G + R_F)}\right)}$$

To match the input impedance R_S, the following condition must be met: $R_{IN} || R_T = R_S$

Therefore:

$$R_T = \frac{R_S}{\left(1 - \frac{0.5 \times \left(\frac{R_S}{R_G}\right)(R_F + 2 \times R_G)}{R_G + R_F}\right)}$$

From this equation it can be inferred that R_T is about 64Ω for all the cases of Table 1.

Table 2. Typical Gain Values When Using the Internal Termination Resistors (R_T and R_S = 50)

R_T (Ω)	R_G (Ω)	R_F (Ω)	GAIN (V/V)
64	200	200	0.48
64	150	300	0.95
64	125	500	1.85

The gain options with the internal termination resistors R_T are given by the following equation and typical numbers are summarized in Table 2. Gain values are dependent on actual source impedance and on-chip R_T, R_G, and R_F values. The latter are subject to process variation.

$$GAIN = \frac{R_F \times R_T}{R_T \times (R_S + R_G) + R_S \times R_G}$$

For single-ended to differential applications where the source impedance is 50Ω, such as the case of the *Typical Application Circuit*, connect an external 50Ω resistor at the other input to maintain symmetry and minimize the gain error.

Applications Information

Input Voltage Range

One of the typical applications is the translation of a single-ended input signal that is referenced to ground to a differential output signal that feeds a high-speed pipeline analog-to-digital converter (ADC) such as the one in the *Typical Application Circuit*. Because the input signal has 0V common mode, the majority of the amplifiers would require a negative supply. The ICs allow the input signal to be below ground even with single-supply operation (V_{EE} connected to GND). How far below ground depends on the gain option. See the *Electrical Characteristics* table and Figures 1, 2, and 3 for details.

Use the following equation to determine the input common-mode range:

$$V_{IN\_CM} = \frac{(V_{AMP} - V_{OUT\_CM})}{(G+1)} \times \frac{(G+1)}{G}$$

where V_{IN_CM} is the input common-mode voltage. V_{AMP} is the voltage at the input node of the internal amplifier. V_{OUT_CM} is the output common-mode voltage. G is the gain of the device.

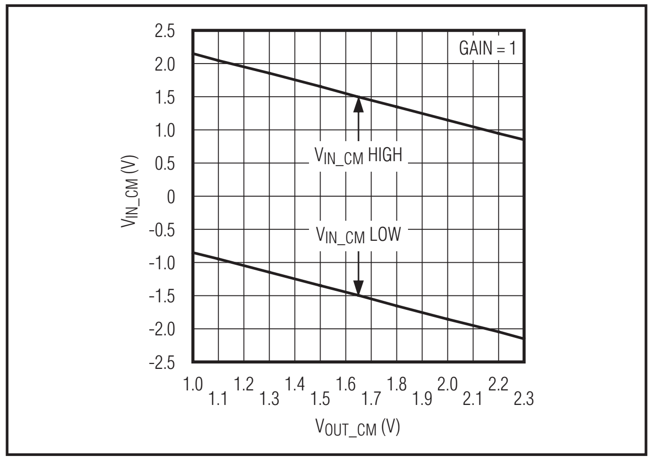


Figure 1. MAX9626 Input Common-Mode Voltage vs. Output Common-Mode Voltage of the Amplifier

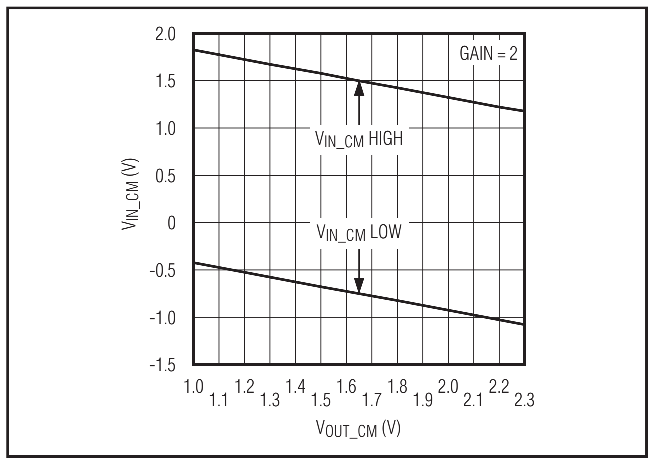


Figure 2. MAX9627 Input Common-Mode Voltage vs. Output Common-Mode Voltage of the Amplifier

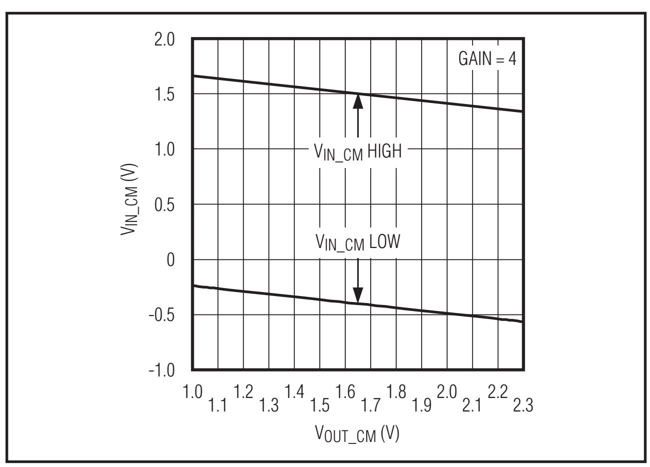


Figure 3. MAX9628 Input Common-Mode Voltage vs. Output Common-Mode Voltage of the Amplifier

Input Voltage Noise

The input referred voltage noise specification reported in the *Electrical Characteristics* table includes both the noise contribution of the amplifier and the contribution of all the internal resistive elements. Because such resistive elements change depending on the gain selection as per Table 1, the input voltage noise specification differs according to the gain options.

Setting the Output Common-Mode Voltage

The ICs feature an input, VOCM, that sets the differential output common-mode voltage. Its wide range from 1.1V to V_{CC} - 1.1V makes the amplifier family compatible with most of the high-speed pipeline differential input ADCs. While many of these ADCs accept an input common-mode around half of their supply voltage, some of them have input common-mode range shifted toward either ground or the positive supply.

The ICs can comfortably drive both 3.3V and 5V ADCs that have common-mode range around half supply. When powered with V_{CC} of 5V or higher, the ICs can also drive some of the popular ADCs with common-mode range higher than 3V.

The high bandwidth of VOCM makes the amplifier's output recover quickly from load transient conditions. Such conditions may occur when switching the ADC input capacitor during the track-and-hold phases. The input capacitor switching may cause a voltage glitch at the input of the ADC, which incurs a load transient condition for the driving amplifier.

Power-Supply Decoupling and Layout Techniques

The ICs are high-speed devices, sensitive to the PCB environment in which they operate. Realizing their superior performance requires attention to the details of high-speed PCB design.

The first requirement is a solid continuous ground plane on the second PCB layer, preferably with no signal or power traces. PCB layers 3 and 4 can be power-supply routing or signal routing, but preferably they should not be routed together.

For power-supply decoupling with single-supply operation, place a large capacitor by the V_{CC} supply node and then place a smaller capacitor as close as possible to the V_{CC} pin. For 1GHz decoupling, 22pF to 100pF are good values to use. When used with split supplies, place relevant capacitors on the V_{EE} supply as well.

Ground vias are critical to provide a ground return path for high frequency signals and should be placed near the decoupling capacitors. Place ground vias on the exposed pad as well, along the edges and near the pins to shorten the return path and maximize isolation. Vias should also be placed next to the input and output signal traces to maximize isolation. Finally, make sure that the layer 2 ground plane is not severely broken up by signal vias or power supply vias.

Signal routing should be short and direct to avoid parasitic effects. For very high-frequency designs, avoid using right angle connectors since they may introduce a capacitive discontinuity and ultimately limit the frequency response.

Recommended Pipeline ADCs

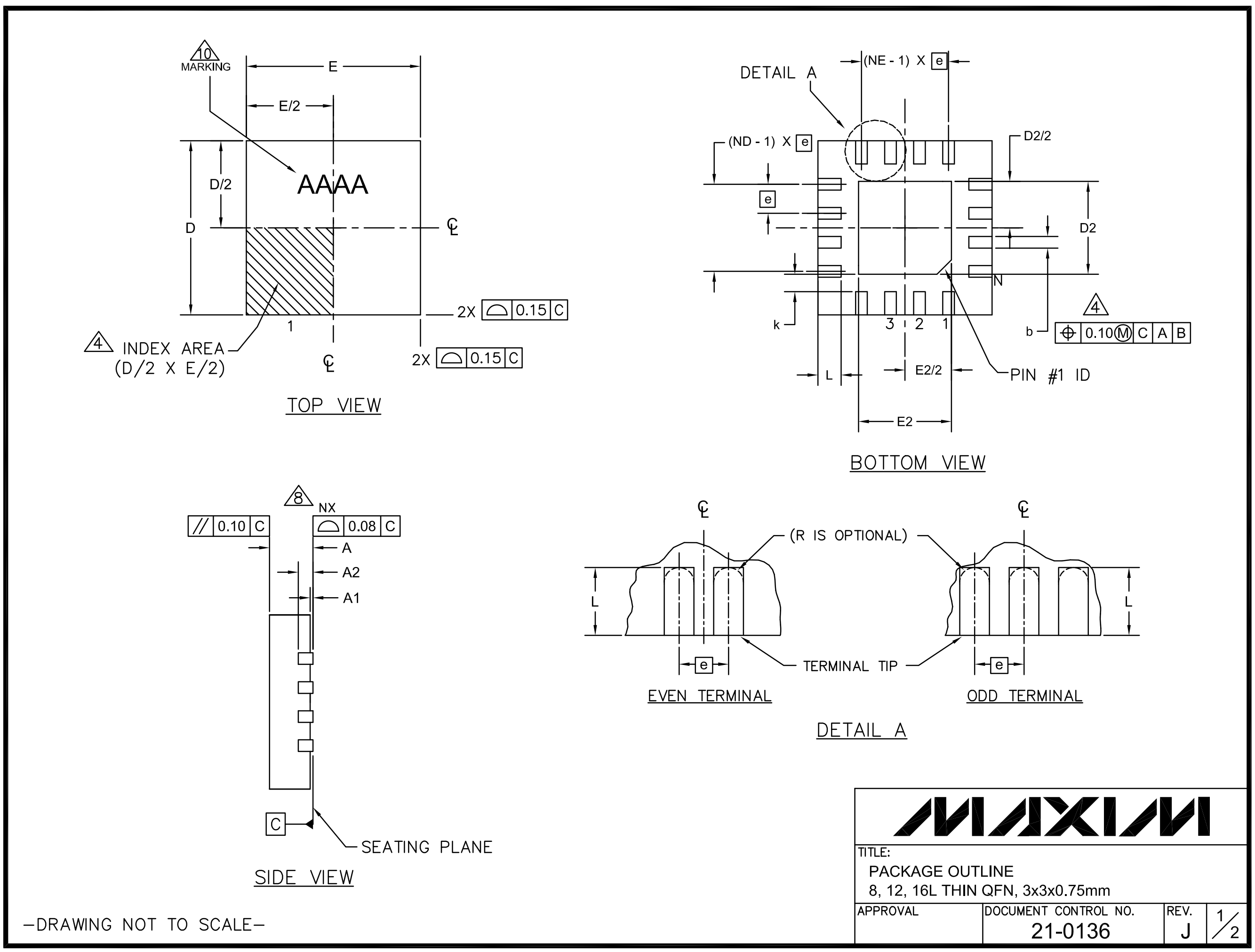
The MAX9626/MAX9627/MAX9628 family offers excellent bandwidth and distortion performance that is in line with the majority of high-speed and 16-bit resolution pipeline ADCs in the market. In particular, it is recommended in combination with the MAX19586/MAX19588 family of 16-bit and 100Msps pipeline ADCs.

For lower resolution applications, the MAX9626/MAX9627/MAX9628 family can also drive 10- to 14-bit ADCs such as the MAX12553/MAX12554/MAX12555, MAX12527/MAX12528/MAX12529 and MAX19505/MAX19506/MAX19507 families.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 TQFN	T1233+1	**21-0136**	**90-0066**



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND Pb FREE (+) PARTS.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE
8, 12, 16L THIN QFN, 3x3x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0136	J	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	2/11	Updated shutdown current value, updated *Electrical Characteristics* table, updated. *Internal Terminations* section, and added new typical operating characteristics	1–7, 14