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# MAX96705

# 16-Bit GMSL Serializer with High-Immunity/ Bandwidth Mode and Coax/STP Cable Drive

## General Description

The MAX96705 is a compact serializer with features especially suited for automotive camera applications. It is function and pin compatible with the MAX9271. In high-bandwidth mode, the parallel-clock maximum is 116MHz for 12-bit linear or combined HDR data types.

The embedded control channel operates at 9.6kbps to 1Mbps in UART, I²C, and mixed UART/I²C modes, allowing programming of serializer, deserializer, and camera registers independent of video timing.

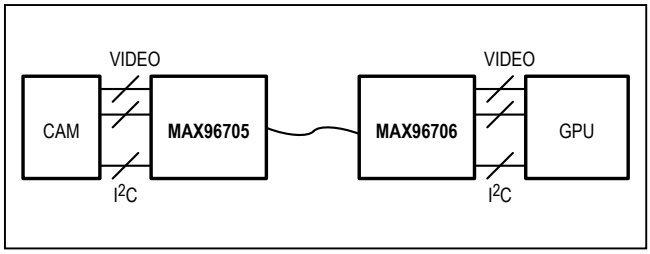
For driving longer cables, the IC has programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V, and the I/O supply range is 1.7V to 3.6V.

The MAX96705 is available in a 32-pin (5mm x 5mm) TQFN package with 0.5mm lead pitch, and operates over the -40°C to +115°C temperature range.

## Applications

- Automotive Camera Applications

## Simplified Block Diagram




*Ordering Information* ***appears at end of data sheet.***

## Benefits and Features

- Ideal for Safety Camera Applications
  - Works with Low-Cost 50Ω Coax (100Ω STP) Cables
  - Error Detection of Video/Control Data
  - High-Immunity Mode for Robust Control-Channel EMC Tolerance
  - Retransmission of Control Data Upon Error Detection
  - Best-in-Class Supply Current: 93mA (max)
  - Pre/Deemphasis Allows 15m Cable at Full Speed
  - 32-Pin (5mm x 5mm) TQFN Package with 0.5mm Lead Pitch
- High-Speed Data Serialization for Megapixel Cameras
  - Up to 1.74Gbps Serial-Bit Rate
  - 12.5MHz to 87MHz x 14 Bit + H/V Data
  - 36.66MHz to 116MHz x 12-Bit + H/V Data (through Internal Encoding)
- Multiple Modes for System Flexibility
  - 9.6kbps to 1Mbps Control Channel in UART, I²C (with Clock Stretch), or UART-to-I²C Modes
  - Crosspoint Switch Accepts Any Input Bitmap
  - Modes for Encoded VSYNC and HSYNC
- Reduces EMI and Shielding Requirements
  - Programmable Output Spread Spectrum
  - Tracks Spread Spectrum Applied at the Parallel Input
  - 1.7V to 3.6V I/O Supply
- Peripheral Features for Camera Power-Up and Verification
  - Built-In PRBS Generator for BER Testing
  - Dedicated GPO for Camera Frame-Sync Trigger and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets AEC-Q100 Automotive Specification
  - -40°C to +115°C Operating Temperature
  - ±8kV Contact and ±15kV Air IEC 61000-4-2 and ISO 10605 ESD Protection



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## LIST OF TABLES

## Absolute Maximum Ratings

AVDD to EP* .....-0.5V to +1.9V
DVDD to EP* .....-0.5V to +1.9V
IOVDD to EP* .....-0.5V to +3.9V
OUT+, OUT- to EP* .....-0.5V to +1.9V
All Other Pins to EP* .....-0.5V to (IOVDD + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply.....Continuous

Continuous Power Dissipation, $T_A$ = +70°C
TQFN (derate 34.5 mW/°C above +70°C) .....2758.6mW
Operating Temperature Range.....-40°C to +115°C
Junction Temperature.....+125°C
Storage Temperature Range..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

**EP connected to IC ground.*

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

### 32-Pin TQFN-EP

| | |
|---|---|
| Package Code | T3255+8 |
| Outline Number | **21-0140** |
| Land Pattern Number | **90-0013** |
| **Single-Layer Board:** | |
| Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) | 47 |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 1.7 |
| **Four-Layer Board:** | |
| Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) | 29 |
| Junction-to-Case Thermal Resistance ($\theta_{JC}$) | 1.7 |

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## DC Electrical Characteristics

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), $T_A$ = -40°C to +115°C, EP connected to PCB ground, typical values are at $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SINGLE-ENDED INPUTS (LCCEN, DIN_, PCLKIN, HS, VS, DE, BWS, DBL, HIM, MS, HVEN, PWDNB)** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.65 x $V_{IOVDD}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.35 x $V_{IOVDD}$ | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0 to $V_{IOVDD}$ | -20 | | +20 | µA |
| **THREE-LEVEL INPUTS (CONF0, CONF1)** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{IOVDD}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.3 x $V_{IOVDD}$ | V |
| Mid-Level Input Current | $I_{INM}$ | Open or connected to a driver with output in high impedance (Note 2) | -10 | | +10 | µA |
| Input Current | $I_{IN}$ | High or low, PWDNB high or low | -220 | | +220 | µA |
| **SINGLE-ENDED OUTPUT (GPO)** | | | | | | |
| High-Level Output Voltage | $V_{OH}$ | $I_{OH}$ = -2mA | $V_{IOVDD}$ - 0.2 | | | V |
| Low-Level Output Voltage | $V_{OL}$ | $I_{OL}$ = 2mA | | | 0.2 | V |
| Output Short-Circuit Current | $I_{OS}$ | $V_O$ = 0V, $V_{IOVDD}$ = 3.0V to 3.6V | -16 | -35 | -64 | mA |
| | | $V_O$ = 0V, $V_{IOVDD}$ = 1.7V to 1.9V | -3 | -12 | -21 | |
| **UART/I²C and GENERAL-PURPOSE I/Os (RX/SDA, TX/SCL, GPIO_) with OPEN-DRAIN OUTPUTS** | | | | | | |
| High-Level Input Voltage | $V_{IH}$ | | 0.7 x $V_{IOVDD}$ | | | V |
| Low-Level Input Voltage | $V_{IL}$ | | | | 0.3 x $V_{IOVDD}$ | V |
| Input Current | $I_{IN}$ | $V_{IN}$ = 0 to $V_{IOVDD}$ (Note 3), RX/SDA, TX/SCL | -110 | | +5 | µA |
| | | $V_{IN}$ = 0 to $V_{IOVDD}$ (Note 3), GPIO_ | -80 | | +5 | |
| Low-Level Open-Drain Output Voltage | $V_{OL}$ | $I_{OL}$ = 3mA, $V_{IOVDD}$ = 1.7V to 1.9V | | | 0.4 | V |
| | | $I_{OL}$ = 3mA, $V_{IOVDD}$ = 3.0V to 3.6V | | | 0.3 | |
| Input Capacitance | $C_{IN}$ | Each pin (Note 4) | | | 10 | pF |

## DC Electrical Characteristics (continued)

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), $T_A$ = -40°C to +115°C, EP connected to PCB ground, typical values are at, $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIFFERENTIAL OUTPUTS (OUT+, OUT-)** | | | | | | |
| Differential Output Voltage | $V_{OD}$ | Preemphasis off, high drive (Figure 1) | 300 | 400 | 500 | mV |
| | | 3.3dB preemphasis, high drive (Figure 2) | 350 | | 610 | |
| | | 3.3dB deemphasis, high drive (Figure 2) | 240 | | 425 | |
| Change in $V_{OD}$ Between Complementary Output States | $\Delta V_{OD}$ | | | | 25 | mV |
| Output Offset Voltage ($V_{OUT+}$ + $V_{OUT-}$)/2 = $V_{OS}$ | $V_{OS}$ | Preemphasis off | 1.1 | 1.4 | 1.56 | V |
| Change in $V_{OS}$ Between Complementary Output States | $\Delta V_{OS}$ | | | | 25 | mV |
| Output Short-Circuit Current | $I_{OS}$ | $V_{OUT+}$ or $V_{OUT-}$ = 0V | -60 | | | mA |
| | | $V_{OUT+}$ or $V_{OUT-}$ = 1.9V | | | 25 | |
| Magnitude of Differential Output Short-Circuit Current | $I_{OSD}$ | $V_{OD}$ = 0V | | | 25 | mA |
| Output-Termination Resistance (Internal) | $R_O$ | From OUT+ or OUT- to AVDD | 45 | 54 | 63 | Ω |
| **REVERSE CONTROL-CHANNEL RECEIVER OUTPUTS (OUT+, OUT-)** | | | | | | |
| High-Switching Threshold | $V_{CHR}$ | Legacy | | | 27 | mV |
| | | High immunity | | | 40 | |
| Low-Switching Threshold | $V_{CLR}$ | Legacy | -27 | | | mV |
| | | High immunity | -40 | | | |
| **SINGLE-ENDED SERIAL OUTPUTS (OUT+ or OUT-)** | | | | | | |
| Single-Ended Output Voltage | $V_O$ | Preemphasis off, high drive (Figure 3) | 375 | 500 | 625 | mV |
| | | 3.3dB preemphasis, high drive (Figure 2) | 435 | | 765 | |
| | | 3.3dB deemphasis, high drive (Figure 2) | 300 | | 535 | |
| Output Short-Circuit Current | $I_{OS}$ | $V_{OUT+}$ or $V_{OUT-}$ = 0V | -69 | | | mA |
| | | $V_{OUT+}$ or $V_{OUT-}$ = 1.9V | | | 32 | |
| Output-Termination Resistance (Internal) | $R_O$ | From OUT+ or OUT- to AVDD | 45 | 54 | 63 | Ω |

## DC Electrical Characteristics (continued)

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), $T_A$ = -40°C to +115°C, EP Connected to PCB ground, typical values are at, $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Supply Current, Worst-Case Pattern (Figure 4) | $I_{WCS}$ | $f_{PCLKIN}$ = 116MHz, HIBW = 0, BWS = 0, default register values, AVDD + DVDD (1.9V) | | 64 | 90 | mA |
| | | $f_{PCLKIN}$ = 116MHz, HIBW = 0, BWS = 0, default register values, IOVDD (3.6V) | | 1.8 | 2.7 | |
| | | $f_{PCLKIN}$ = 116MHz, HIBW = 0, BWS = 0, default register values, IOVDD (1.9V) (Note 4) | | 0.45 | 0.69 | |
| | | $f_{PCLKIN}$ = 116MHz, HIBW = 1, BWS = 0, default register values, AVDD + DVDD (1.9V) | | 62 | 83 | |
| | | $f_{PCLKIN}$ = 116MHz, HIBW = 1, BWS = 0, default register values, IOVDD (3.6V) | | 1.8 | 2.7 | |
| | | $f_{PCLKIN}$ = 116MHz, HIBW = 1, BWS = 0, default register values, IOVDD (1.9V) (Note 4) | | 0.45 | 0.69 | |
| | | $f_{PCLKIN}$ = 87MHz, BWS = 1, default register values, AVDD + DVDD (1.9V) | | 61 | 85 | |
| | | $f_{PCLKIN}$ = 87MHz, BWS = 1, default register values, IOVDD (3.6V) | | 1.4 | 2.0 | |
| | | $f_{PCLKIN}$ = 87MHz, BWS = 1, default register values, IOVDD (1.9V) (Note 4) | | 0.37 | 0.61 | |
| Sleep-Mode Supply Current | $I_{CCS}$ | Wake-up receiver enabled | | 40 | 100 | µA |
| Power-Down Supply Current | $I_{CCZ}$ | PWDNB = low | | 15 | 70 | µA |
| **ESD PROTECTION** | | | | | | |
| OUT+, OUT- (Note 5) | $V_{ESD}$ | Human Body Model, $R_D$ = 1.5kΩ, $C_S$ = 100pF | | ±8 | | kV |
| | | IEC 61000-4-2, $R_D$ = 330Ω, $C_S$ = 150pF, Contact Discharge | | ±8 | | |
| | | IEC 61000-4-2, $R_D$ = 330Ω, $C_S$ = 150pF, Air Discharge | | ±15 | | |
| | | ISO 10605, $R_D$ = 2kΩ, $C_S$ = 330pF, Contact Discharge | | ±8 | | |
| | | ISO 10605, $R_D$ = 2kΩ, $C_S$ = 330pF, Air Discharge | | ±15 | | |
| All Other Pins (Note 6) | $V_{ESD}$ | Human Body Model, $R_D$ = 1.5kΩ, $C_S$ = 100pF | | ±4 | | kV |

## AC Electrical Characteristics

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), $T_A$ = -40°C to +115°C, EP connected to PCB ground, typical values are at, $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **PARALLEL CLOCK INPUT (PCLKIN)** | | | | | | |
| Clock Frequency | $f_{PCLKIN}$ | BWS = 0, HIBW = 0, single input | 16.66 | | 58 | MHz |
| | | BWS = 0, HIBW = 1, single input | 36.66 | | 58 | |
| | | BWS = 1, single input | 12.5 | | 43.5 | |
| | | BWS = 0, HIBW = 0, double input | 33.32 | | 116 | |
| | | BWS = 0, HIBW = 1, double input | 73.33 | | 116 | |
| | | BWS = 1, double input | 25 | | 87 | |
| Clock Duty Cycle | DC | $t_{HIGH}/t_T$ or $t_{LOW}/t_T$ (Note 4, Figure 5) | 35 | 50 | 65 | % |
| Clock Transition Time | $t_R$, $t_F$ | (Note 4, Figure 5) | | | 4 | ns |
| Clock Jitter | $t_J$ | 1.74Gbps bit rate, 300kHz sinusoidal jitter (Note 4) | | | 800 | ps |
| **I²C/UART PORT TIMING** | | | | | | |
| I²C/UART Bit Rate | | | 9.6 | | 1000 | kbps |
| Output Rise Time | $t_R$ | 30% to 70%, $C_L$ = 10pF to 100pF, 1kΩ pullup to IOVDD | 20 | | 150 | ns |
| Output Fall Time | $t_F$ | 70% to 30%, $C_L$ = 10pF to 100pF, 1kΩ pullup to IOVDD | 20 | | 150 | ns |
| **I²C TIMING (Figure 6)** | | | | | | |
| SCL Clock Frequency | $f_{SCL}$ | Low $f_{SCL}$ range: (I2CMSTBT = 010, I2CSLVSH = 10) | 9.6 | | 100 | kHz |
| | | Mid $f_{SCL}$ range: (I2CMSTBT 101, I2CSLVSH = 01) | > 100 | | 400 | |
| | | High $f_{SCL}$ range: (I2CMSTBT = 111, I2CSLVSH = 00) | > 400 | | 1000 | |
| START Condition Hold Time | $t_{HD:STA}$ | $f_{SCL}$ range, low | 4 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |
| Low Period of SCL Clock | $t_{LOW}$ | $f_{SCL}$ range, low | 4.7 | | | µs |
| | | $f_{SCL}$ range, mid | 1.3 | | | |
| | | $f_{SCL}$ range, high | 0.5 | | | |
| High Period of SCL Clock | $t_{HIGH}$ | $f_{SCL}$ range, low | 4 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |
| Repeated START Condition Setup Time | $t_{SU:STA}$ | $f_{SCL}$ range, low | 4.7 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |

## AC Electrical Characteristics (continued)

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), $T_A$ = -40°C to +115°C, EP connected to PCB ground, typical values are at, $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Data Hold Time | $t_{HD:DAT}$ | $f_{SCL}$ range, low | 0 | | | ns |
| | | $f_{SCL}$ range, mid | 0 | | | |
| | | $f_{SCL}$ range, high | 0 | | | |
| Data Setup Time | $t_{SU:DAT}$ | $f_{SCL}$ range, low | 250 | | | ns |
| | | $f_{SCL}$ range, mid | 100 | | | |
| | | $f_{SCL}$ range, high | 50 | | | |
| Setup Time for STOP Condition | $t_{SU:STO}$ | $f_{SCL}$ range, low | 4 | | | µs |
| | | $f_{SCL}$ range, mid | 0.6 | | | |
| | | $f_{SCL}$ range, high | 0.26 | | | |
| Bus-Free Time | $t_{BUF}$ | $f_{SCL}$ range, low | 4.7 | | | µs |
| | | $f_{SCL}$ range, mid | 1.3 | | | |
| | | $f_{SCL}$ range, high | 0.5 | | | |
| Data Valid Time | $t_{VD:DAT}$ | $f_{SCL}$ range, low | | | 3.45 | µs |
| | | $f_{SCL}$ range, mid | | | 0.9 | |
| | | $f_{SCL}$ range, high | | | 0.45 | |
| Data Valid-Acknowledge Time | $t_{VD:ACK}$ | $f_{SCL}$ range, low | | | 3.45 | µs |
| | | $f_{SCL}$ range, mid | | | 0.9 | |
| | | $f_{SCL}$ range, high | | | 0.45 | |
| Pulse Width of Spikes Suppressed | $t_{SP}$ | $f_{SCL}$ range, low | | | 50 | ns |
| | | $f_{SCL}$ range, mid | | | 50 | |
| | | $f_{SCL}$ range, high | | | 50 | |
| Capacitive Load of Each Bus Line | $C_B$ | Note 4 | | | 100 | pF |
| **SWITCHING CHARACTERISTICS (Note 4)** | | | | | | |
| Differential/Single-Ended Output Rise/Fall Time | $t_R$, $t_F$ | 20% to 80%, $V_{OD}$, 400mV differential $R_L$ = 100Ω, 500mV single-ended $R_L$ = 50Ω, serial bit rate = 1.74Gbps | | | 250 | ps |
| Total Serial-Output Jitter (Differential Output) | $t_{TSOJ1}$ | 1.74Gbps PRBS, measured at $V_{OD}$ = 0V differential, preemphasis disabled (Figure 7) | | 0.25 | | UI |
| Deterministic Serial-Output Jitter (Differential Output) | $t_{DSOJ2}$ | 1.74Gbps PRBS, measured at $V_{OD}$ = 0V differential, preemphasis disabled (Figure 7) | | 0.15 | | UI |
| Total Serial-Output Jitter (Single-Ended Output) | $t_{TSOJ1}$ | 1.74Gbps PRBS, measured at $V_O$/2, preemphasis disabled (Figure 3) | | 0.25 | | UI |
| Deterministic Serial-Output Jitter (Single-Ended Output) | $t_{DSOJ2}$ | 1.74Gbps PRBS, measured at $V_O$/2, preemphasis disabled (Figure 3) | | 0.15 | | UI |
| Parallel Data-Input Setup Time | $t_{SET}$ | (Figure 8) | 2 | | | ns |

## AC Electrical Characteristics (continued)

($V_{DVDD}$ = $V_{AVDD}$ = 1.7V to 1.9V, $V_{IOVDD}$ = 1.7V to 3.6V, $R_L$ = 100Ω ±1% (differential), $T_A$ = -40°C to +115°C, EP connected to PCB ground, typical values are at, $V_{DVDD}$ = $V_{AVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Parallel Data Input Hold Time | $t_{HOLD}$ | (Figure 8) (Note 4) | 1 | | | ns |
| GPI-to-GPO Delay | $t_{GPIO}$ | Deserializer GPI to serializer GPO (Figure 9) | | | 350 | µs |
| Serializer Delay | $t_{SD}$ | Spread spectrum enabled (Figure 10) (Notes 4, 7) | | | 2065 | Bits |
| | | Spread spectrum disabled (Figure 10) (Notes 4, 7) | | | 1095 | |
| Link Start Time | $t_{LOCK}$ | (Figure 11) | | | 2 | ms |
| Power-Up Time | $t_{PU}$ | (Figure 12) | | | 7 | ms |

**Note 1:** Limits are 100% production tested at $T_A$ = +115°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

**Note 2:** To provide a mid-level voltage, leave the input open; or, if driven, put the driver in high-impedance state. High-impedance leakage current must be less than ±10µA.

**Note 3:** $I_{IN}$ min is due to voltage drop across the internal pullup resistor.

**Note 4:** Not production tested. Guaranteed by design.

**Note 5:** Specified pin to ground.

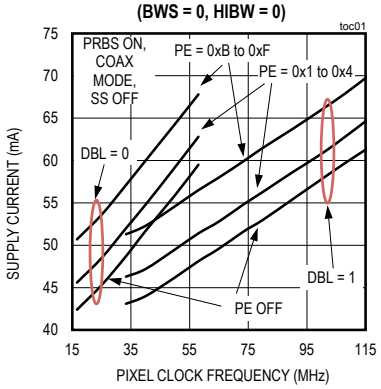
**Note 6:** Specified pin to all supply/ground.

**Note 7:** Measured in serial link bit times. Bit time = 1/(30 x $f_{PCLKIN}$) for BWS = 0; bit time = 1/(40 x $f_{PCLKIN}$) for BWS = 1.

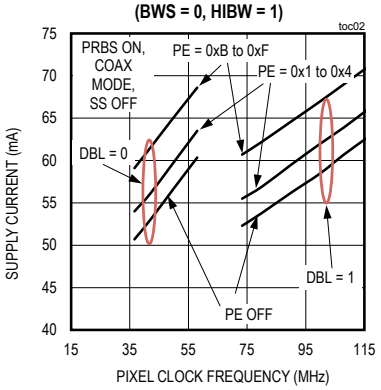
## Typical Operating Characteristics

($V_{AVDD}$ = $V_{DVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.)

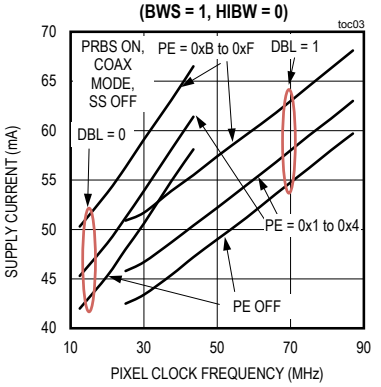
**SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 0)**



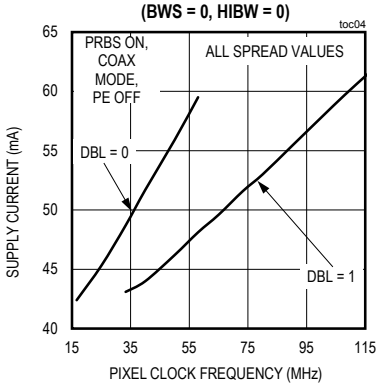

**SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 1)**



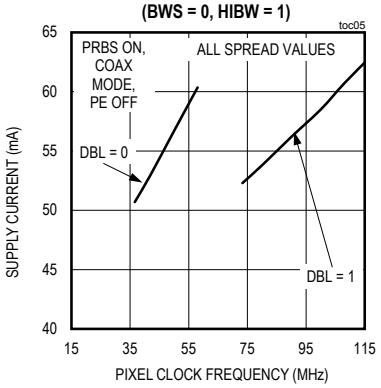

**SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 1, HIBW = 0)**



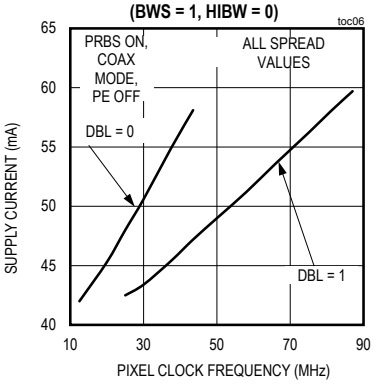

**SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 0)**




**SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 1)**



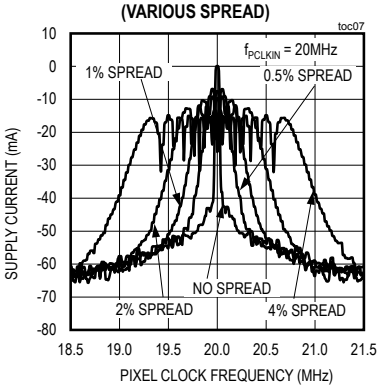

**SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 1, HIBW = 0)**



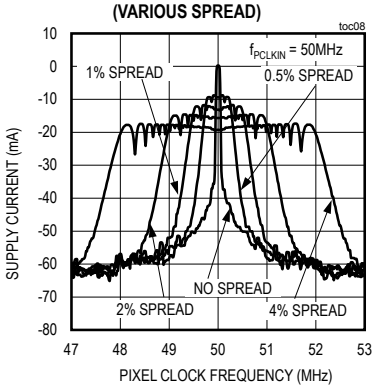
## Typical Operating Characteristics (continued)

($V_{AVDD}$ = $V_{DVDD}$ = $V_{IOVDD}$ = 1.8V, $T_A$ = +25°C, unless otherwise noted.)

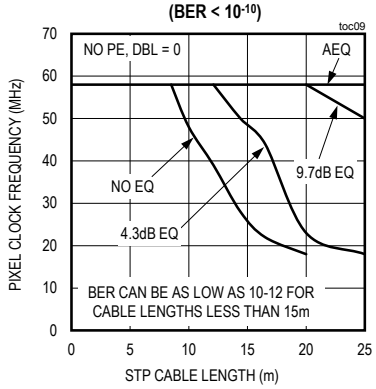
**OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS SPREAD)**



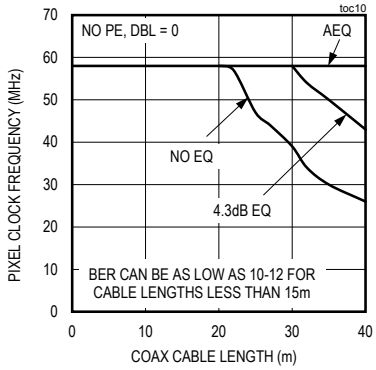

**OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS SPREAD)**



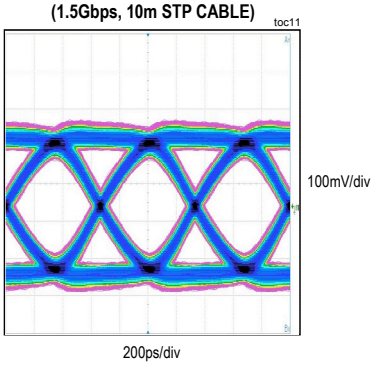

**MAXIMUM PIXEL CLOCK FREQUENCY vs. STP CABLE LENGTH (BER < $10^{-10}$)**



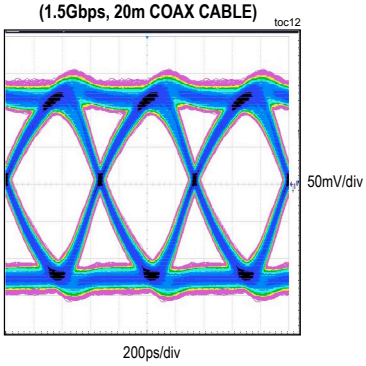

**MAXIMUM PIXEL CLOCK FREQUENCY vs. COAX CABLE LENGTH (BER < $10^{-10}$)**



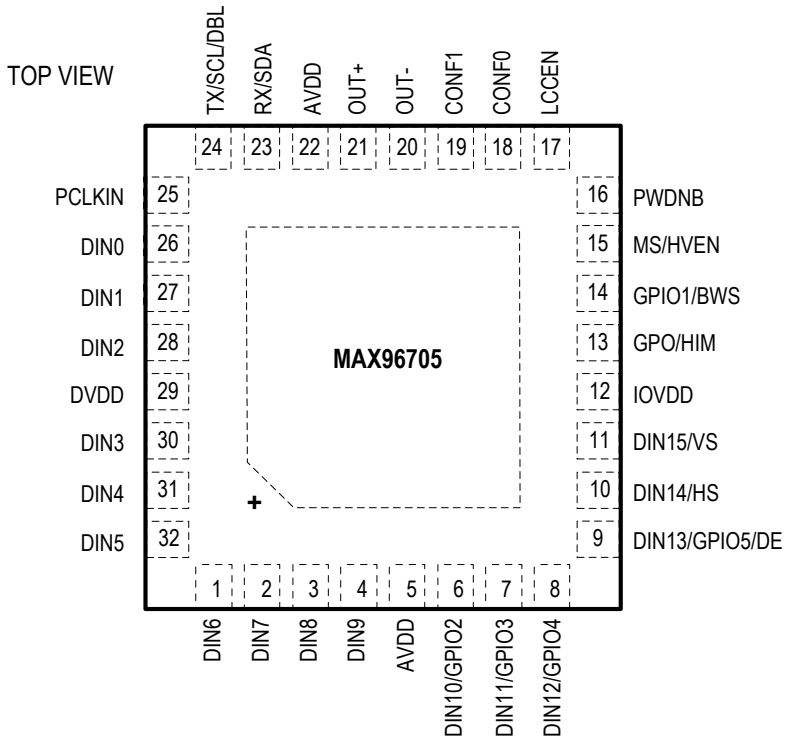

**SERIAL LINK SWITCHING PATTERN WITH 4.4dB PREEMPHASIS (1.5Gbps, 10m STP CABLE)**




**SERIAL LINK SWITCHING PATTERN WITH 3.3dB PREEMPHASIS (1.5Gbps, 20m COAX CABLE)**



## Pin Configuration




**TQFN**
**(5mm x 5mm)**

## Pin Description

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|---|---|---|---|---|
| **POWER** | | | | |
| 5, 22 | AVDD | 1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF, and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to AVDD. | | Power |
| 12 | IOVDD | I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to IOVDD. | | Power |
| 29 | DVDD | 1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF, and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD. | | Power |
| EP | — | Exposed Pad. EP is internally connected to device ground. Must connect EP to the PCB ground plane through a via array for proper thermal and electrical performance. | | Power |

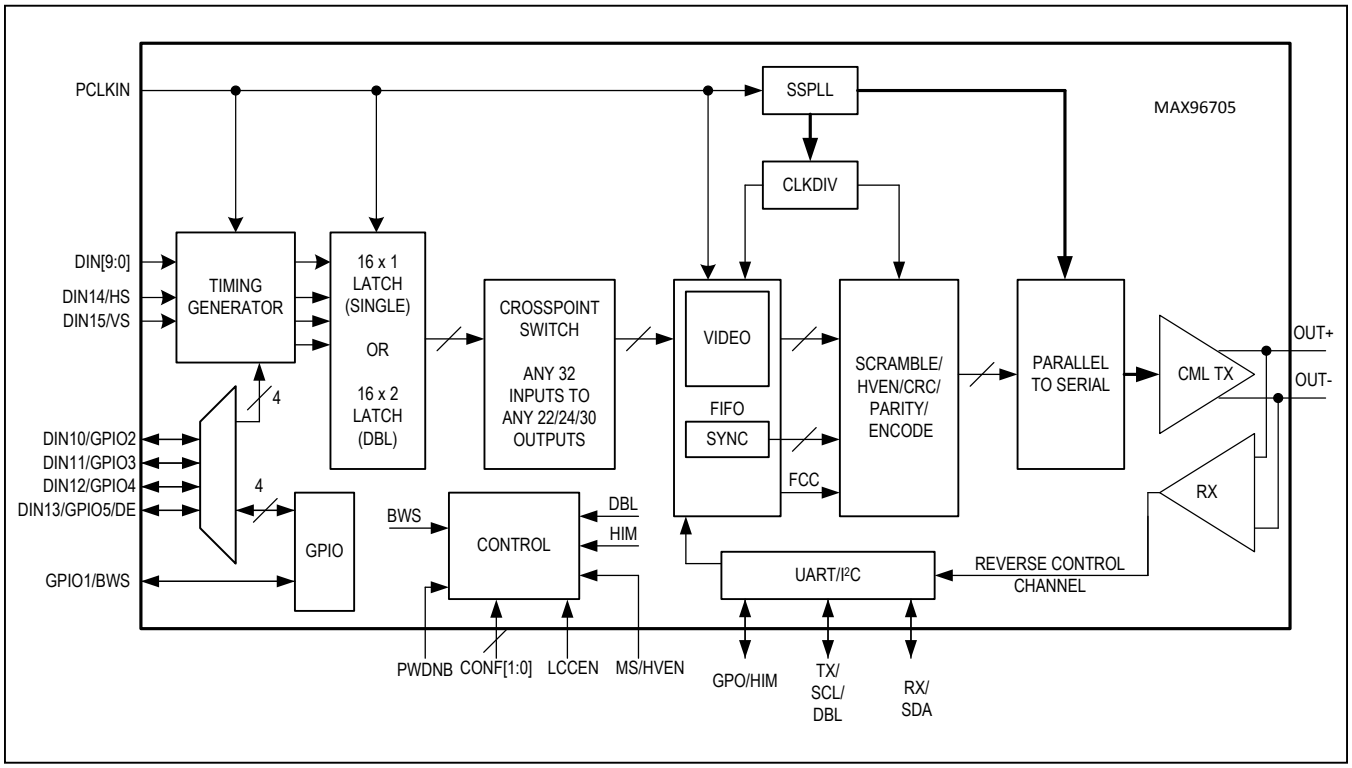
## Pin Description (continued)

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|---|---|---|---|---|
| **HIGH-SPEED DIGITAL** | | | | |
| **Single Function** | | | | |
| 1 | DIN6 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 2 | DIN7 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 3 | DIN8 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 4 | DIN9 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 25 | PCLKIN | Parallel Clock Input with Internal Pulldown to EP. Latches parallel data inputs and provides the PLL reference clock. | IOVDD | Digital |
| 26 | DIN0 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 27 | DIN1 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 28 | DIN2 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 30 | DIN3 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 31 | DIN4 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| 32 | DIN5 | Parallel Data Input. Internal pulldown to EP. | IOVDD | Digital |
| **Multifunction** | | | | |
| 6 | DIN10/GPIO2 | Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to EP. GPIO2 has an open-drain input/output with internal 60kΩ pullup to IOVDD. | IOVDD | Digital |
| 7 | DIN11/GPIO3 | Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to EP. GPIO3 has an open-drain input/output with internal 60kΩ pullup to IOVDD. | IOVDD | Digital |
| 8 | DIN12/GPIO4 | Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to EP. GPIO4 has an open-drain input/output with internal 60kΩ pullup to IOVDD. | IOVDD | Digital |
| 9 | DIN13/ GPIO5/DE | Parallel Data Input/GPIO/Data Enable with Internal Pulldown to EP. Defaults to parallel data input on power-up. GPIO5 has an open-drain input/output with internal 60kΩ pullup to IOVDD. Data enable input in high-bandwidth mode. | IOVDD | Digital |
| 10 | DIN14/HS | Parallel Data Input/Horizontal Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Defaults to horizontal-sync input when HS/VS encoding is enabled, or when in high-bandwidth mode. | IOVDD | Digital |
| 11 | DIN15/VS | Parallel Data Input/Vertical Sync with Internal Pulldown to EP. Defaults to parallel data input on power-up. Defaults to vertical-sync input when HS/VS encoding is enabled, or when in high-bandwidth mode. | IOVDD | Digital |
| **Multifunction Configuration (from LCCEN)** | | | | |
| 14 | GPIO1/BWS | GPIO1/Bus-Width Select Input. Function is determined by the state of LCCEN. GPIO1 (LCCEN = high): Open-drain, general-purpose input/output with internal 60kΩ pullup to IOVDD. BWS (LCCEN = low): Input with internal pulldown to EP. Set BWS = low for 22-bit input latch. Set BWS = high for 30-bit input latch. | IOVDD | Digital |

## Pin Description (continued)

| PIN | NAME | FUNCTION | REF SUPPLY | TYPE |
|---|---|---|---|---|
| 15 | MS/HVEN | Mode-Select/HS and VS Encoding Enable Input with Internal Pulldown to EP. Function is determined by the state of LCCEN. MS (LCCEN high): Set MS low to select base mode. Set MS high to select bypass mode. HVEN: (LCCEN low): Set HVEN = high to enable HS/VS encoding. Set HVEN = low to disable HS/VS encoding. | IOVDD | Digital |
| 17 | LCCEN | Local Control-Channel Enable input with internal Pulldown to EP. LCCEN = high enables the control-channel interface pins. LCCEN = low disables the control-channel interface pins and selects an alternate function on the indicated pins. | IOVDD | Digital |
| 24 | TX/SCL/DBL | Transmit/Serial Clock/Double Mode. Function is determined by the state of LCCEN. TX/SCL (LCCEN = high): Input/output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In $I^2C$ mode, TX/SCL is the SCL input/output of the serializer's $I^2C$ master/slave. TX/SCL has an open-drain driver and requires a pullup resistor. DBL (LCCEN = low): Input with internal pulldown to EP. Set DBL = high to use double-input mode. Set DBL = low to use single-input mode. | IOVDD | Digital |
| **Configuration and Interface** | | | | |
| 13 | GPO/HIM | General-Purpose Output/High-Immunity Mode Input with internal Pulldown to EP. HIM is latched at power-up or when resuming from power-down mode (PWDNB = low), and switches to GPO output automatically after power-up. Connect HIM to IOVDD with a 30kΩ resistor to set high, or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO output follows the state of the GPI (or INT) input on the GMSL deserializer. GPO is low upon power-up or when PWDNB is low. | IOVDD | Digital |
| 16 | PWDNB | Active-Low, Power-Down Input with Internal Pulldown to EP. To reduce power consumption, set PWDNB low to enter power-down mode. | IOVDD | Digital |
| 18 | CONF0 | Configuration 0. Three-level configuration input (Table 13). CONF0 pin value is latched at power-up, or when resuming from power-down mode. | IOVDD | 3-Level |
| 19 | CONF1 | Configuration 1. Three-level configuration input (Table 13). CONF1 pin value is latched at power up or when resuming from power-down mode. | IOVDD | 3-Level |
| 20 | OUT- | Inverting Coax/Twisted-Pair Serial Output. | | Digital |
| 21 | OUT+ | Noninverting Coax/Twisted-Pair Serial Output | | Digital |
| 23 | RX/SDA | Receive/Serial Data. Input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In $I^2C$ mode, RX/SDA is the SDA input/output of the serializer's $I^2C$ master/slave. RX/SDA has an open-drain driver and requires a pullup resistor. | IOVDD | Digital |

## Functional Block Diagram



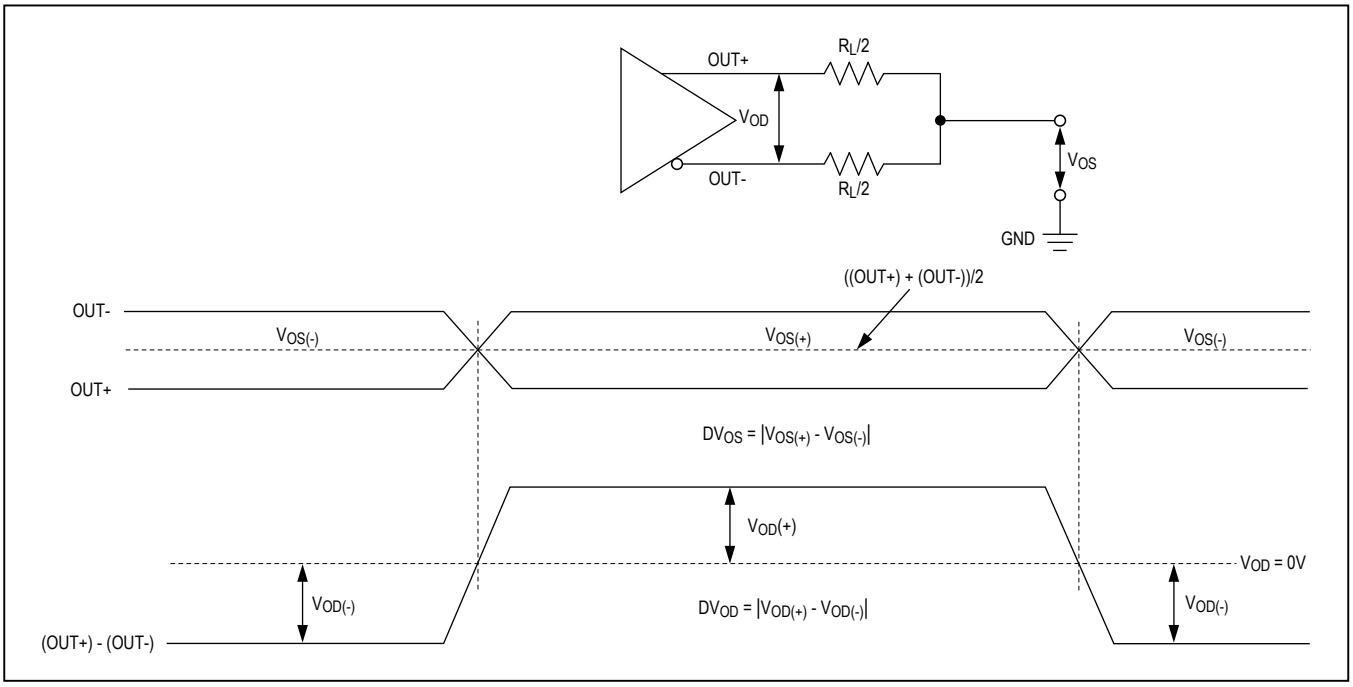




*Figure 1. Serial-Output Parameters*

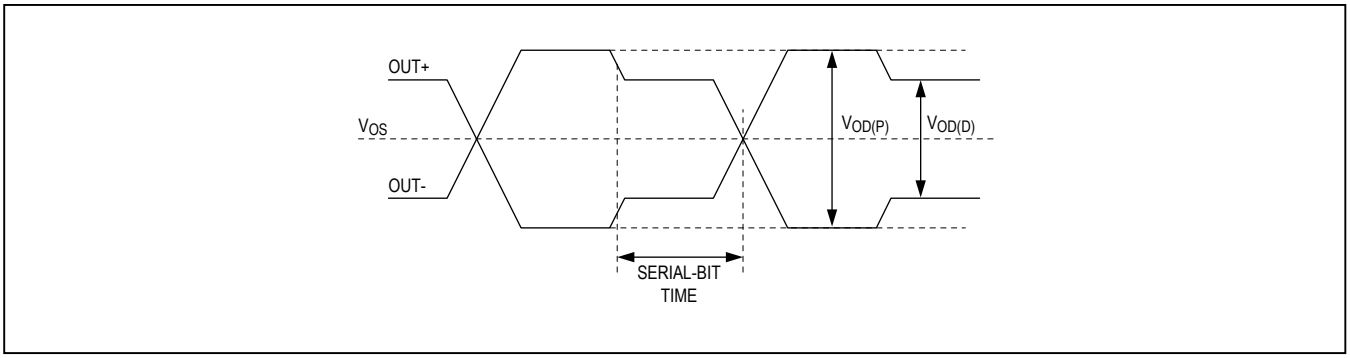



*Figure 2. Output Waveforms at OUT+, OUT-*

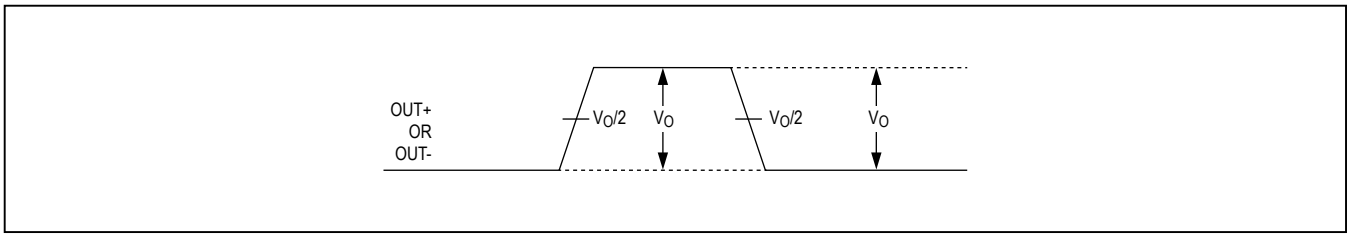



*Figure 3. Single-Ended Output Template*

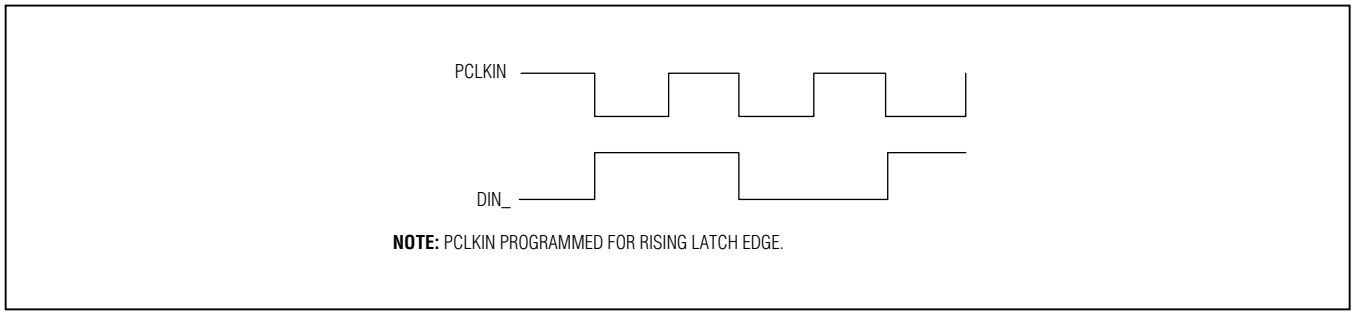



*Figure 4. Worst-Case Pattern Input*

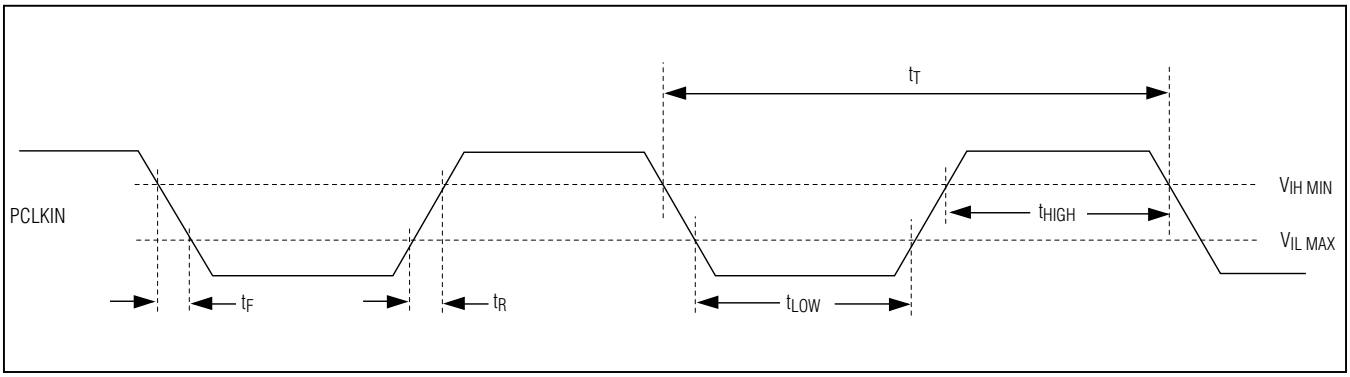



*Figure 5. Parallel Clock Input Requirements*

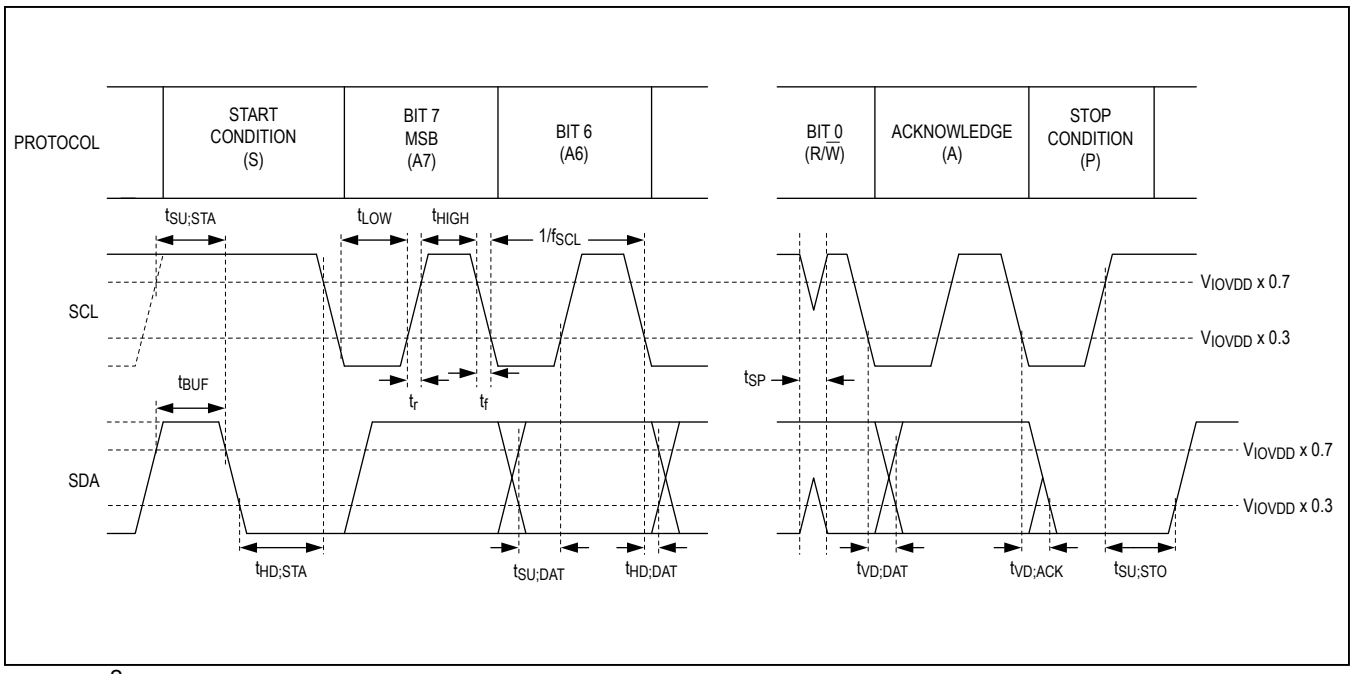



*Figure 6. $I^2C$ Timing Parameters*

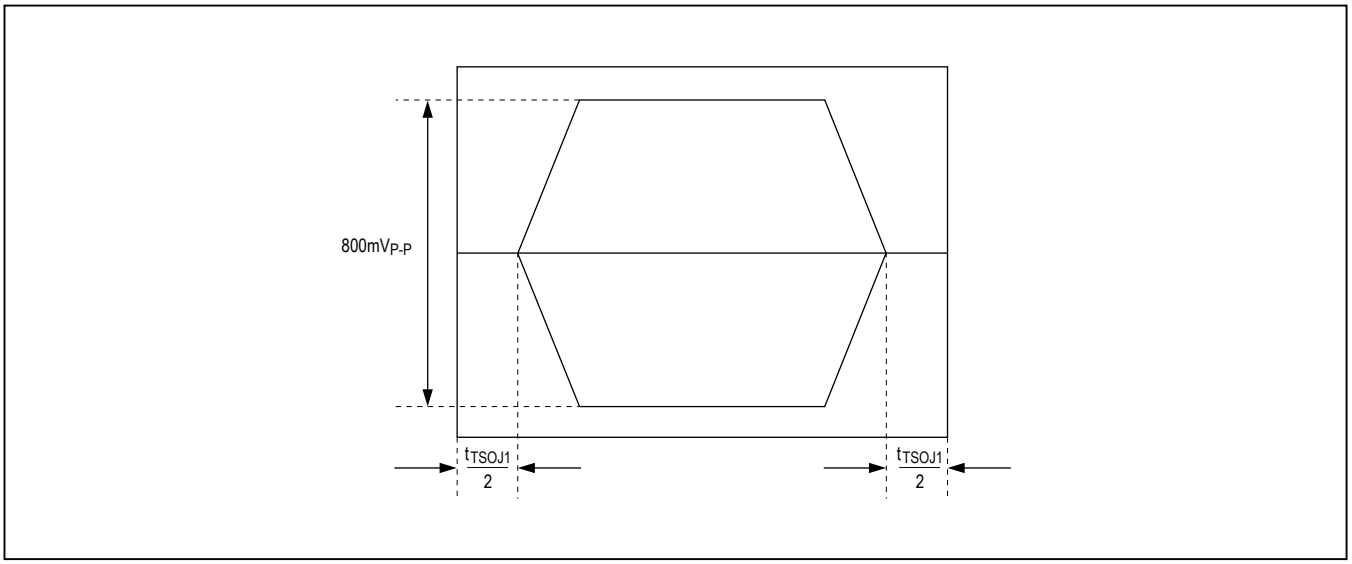



*Figure 7. Differential Output Template*

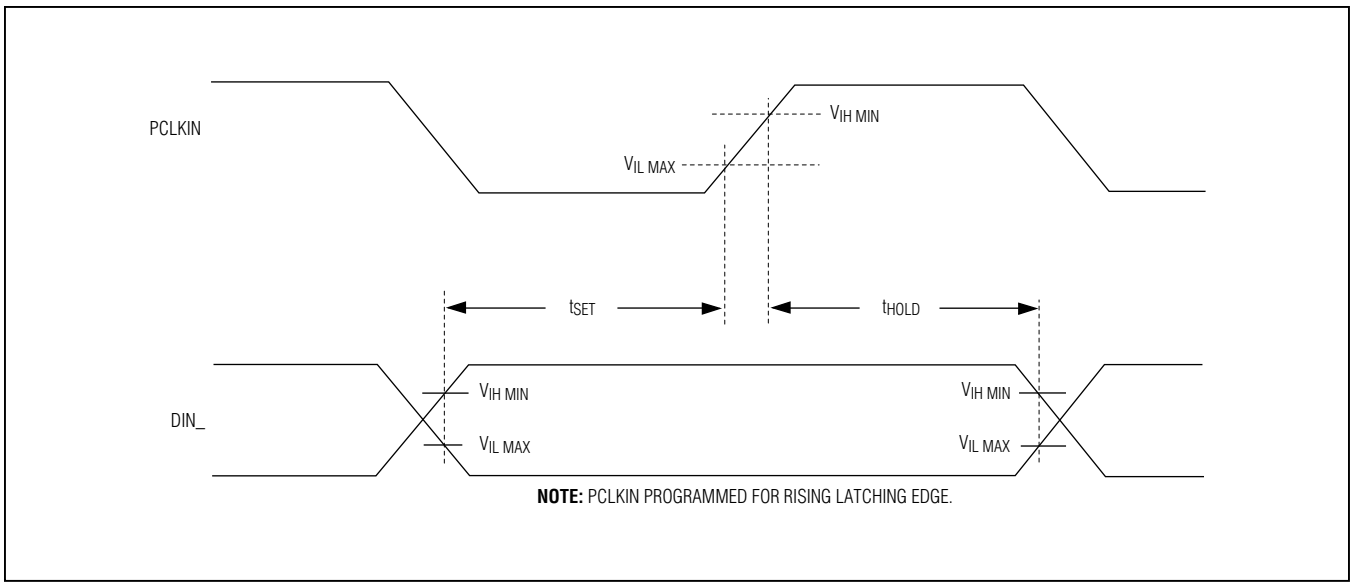



*Figure 8. Input Setup and Hold Times*

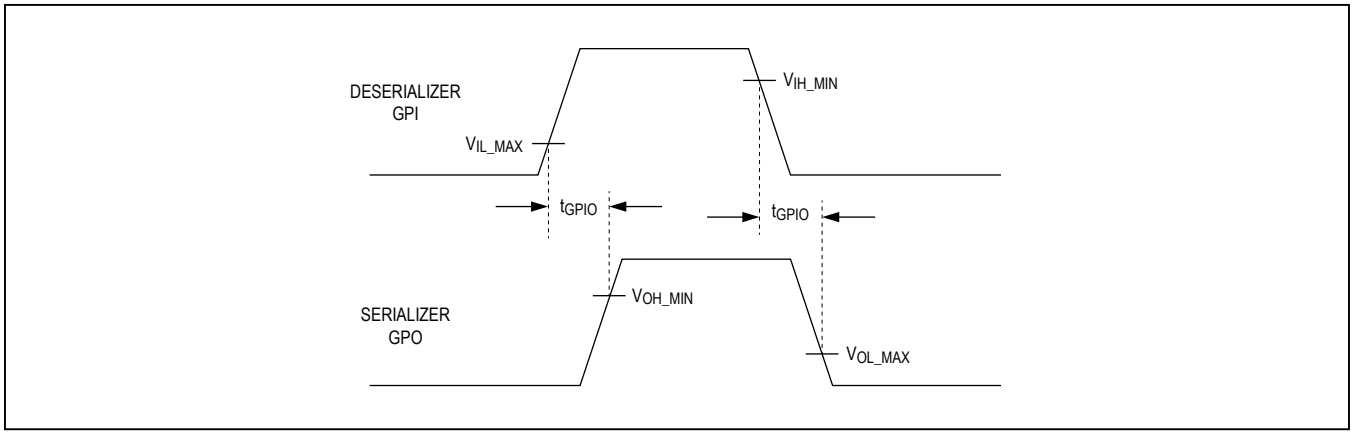



*Figure 9. GPI-to-GPO Delay*

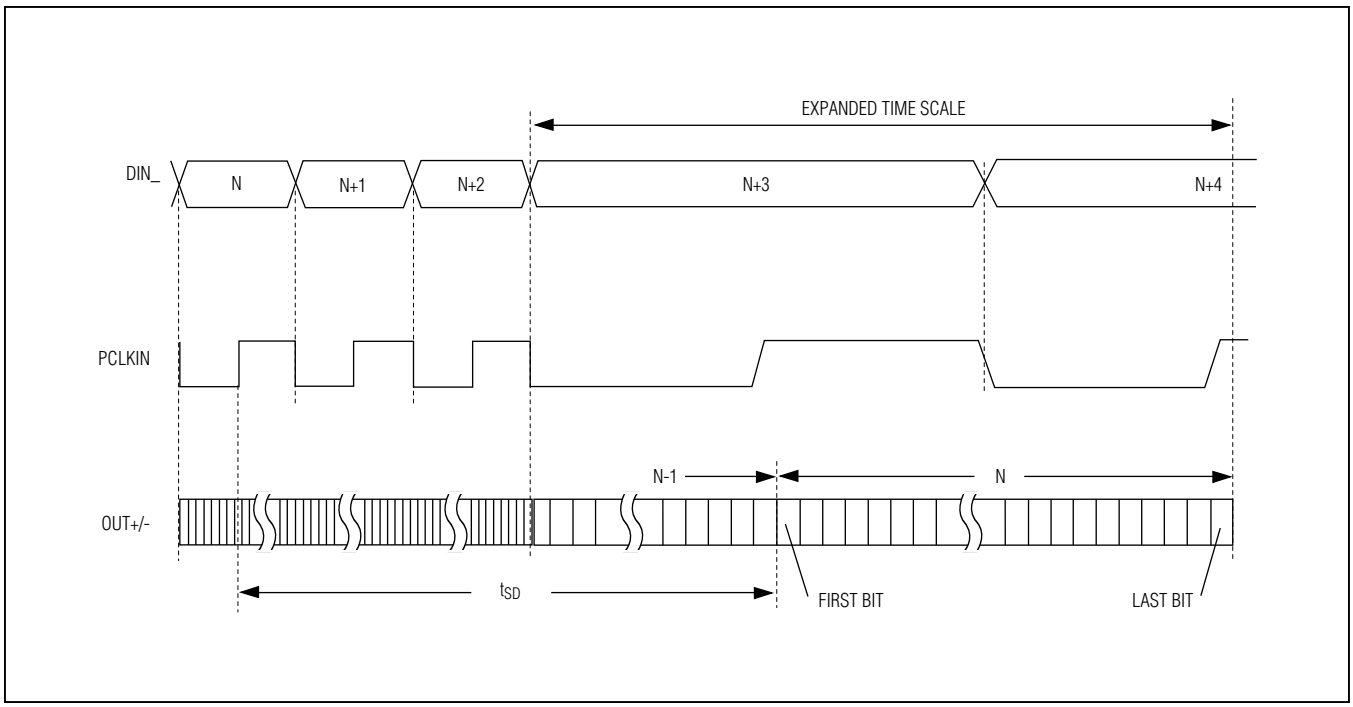



*Figure 10. Serializer Delay*

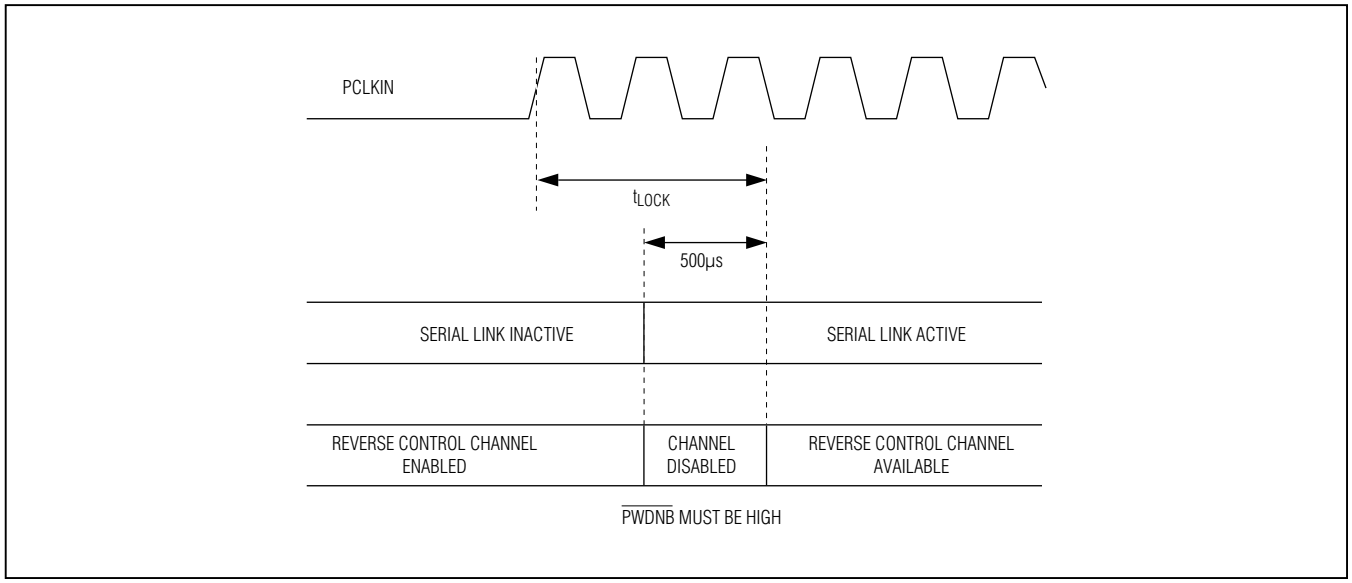



*Figure 11. Link Startup Time*

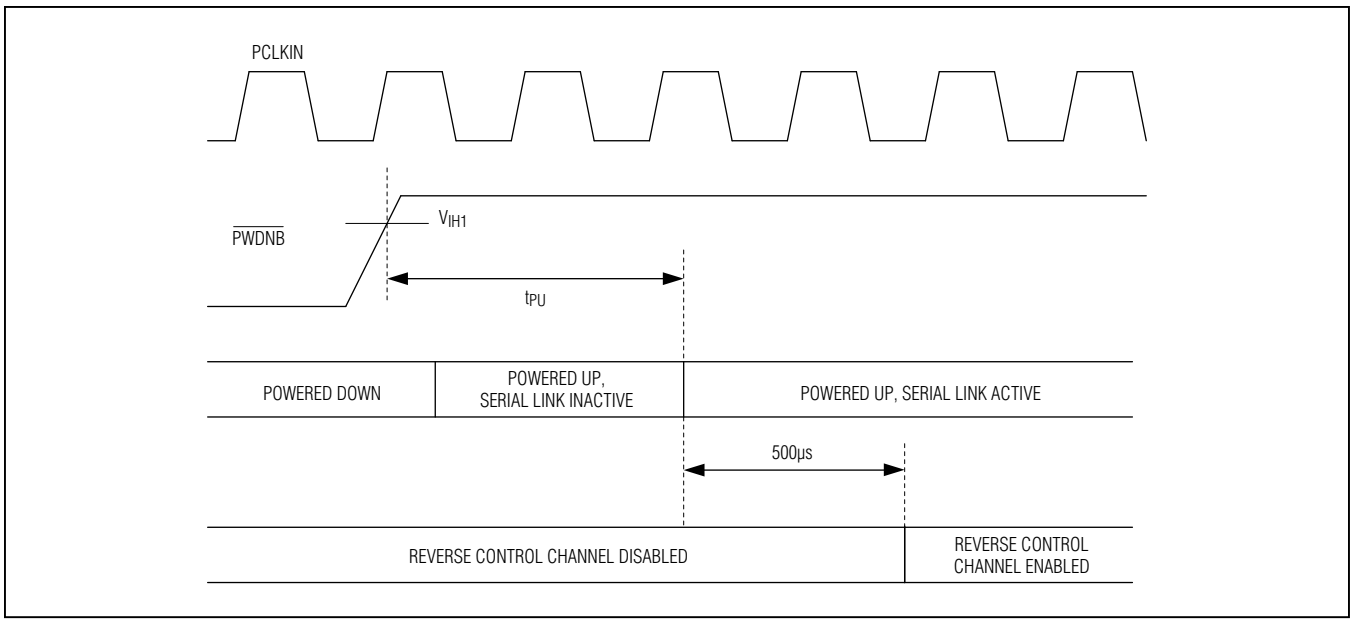



*Figure 12. Power-Up Delay*

## Detailed Description

The MAX96705 is a compact device with features especially suited for automotive camera applications. The device operates at a variety of input widths and word rates up to a total serial-data rate up to 1.74Gbps. High-bandwidth mode offers a 116MHz parallel clock rate with 12 bits of video data and 2 bits of sync (HS/VS) data. An embedded 9.6kbps to 1Mbps control channel programs the serializer, deserializer, and any attached UART or I2C peripherals.

To promote safety applications, the device features CRC protection of video and control data. In addition, control-channel retransmission and high-immunity modes reduce the effects of bit errors corrupting communication. Preemphasis and a PRBS tester allow for in-system evaluation and optimization of the link quality.

This MAX96705 operates over the -40°C to +115°C automotive temperature range.

### Serial Link Signaling and Data Format

The serializer scrambles the input parallel data and combines this with the forward control data. The data is then encoded for transmission and output as a single-serialized bitstream at several times the input word rate (depending on bus width). The deserializer receives the serial data and recovers the clock signal. The data is then deserialized, decoded, and descrambled into parallel output data and forward control data.

### Operating Modes

The GMSL devices are configurable to operate in many modes depending on the application. These modes allow for a more efficient use of serial bandwidth. Most of these settings are set during system design, and are configured using the external configuration pins or through register bits.

### Video/Configuration Link

In normal operation, the serializer runs in video link mode (serializer SEREN = 1) with video data and control data sent across the serial link. Set SEREN = 0 in the serializer to turn off serialization. The serializer powers up in video link mode and requires a valid PCLK for operation.

A configuration link is available to set up the serializer, deserializer, and peripherals when PCLK is not available. Set SEREN = 0 and CLINK = 1 in the serializer to enable the configuration link (SEREN = 1 forces the serializer into video link mode). Once PCLK has been established, turn on the video link (SEREN = 1).

By default, video link mode requires a valid PCLK for operation. Set AUTO_CLINK bit = 1 and SEREN = 1 in the serializer to have the device automatically switch between the video link and configuration link whenever PCLK is not present.

### Single/Double Mode

Single-/double-mode operation configures the available 1.74Gbps bandwidth into a variety of widths and word rates. Single-mode operation is compatible with all GMSL devices and serializers, yielding one parallel word for each serial word. Double mode serializes two half-width parallel words for each serial word, resulting in a 2x increase in the parallel word rate range (compared to single mode). Set DBL = 0 for single-mode operation and DBL = 1 for double-mode operation.

### HS/VS Encoding

By default, GMSL assigns a video bit slot to HSYNC, VSYNC, and DE (if used). With HS/VS encoding, the device instead encodes special packets to sync signals to free up additional video bit slots. HS/VS encoding is on by default when the device is in high-bandwidth mode (HIBW = 1). DE is encoded only when HIBW = 1 and DE_EN = 1. Set HVEN = 1 to turn on HS/VS encoding when HIBW = 0 (DE, if enabled, uses up a video bit). HS/VS encoding requires that HSYNC, VSYNC, and DE (if used) remain high during the active video and low during the blanking period. Use HS/VS inversion when using reverse-polarity sync signals.

### Error Detection

The serial link's 8b/10b encoding/decoding and 1-bit parity detect bit errors that occur on the serial link. An optional 6-bit CRC check is available at the expense of 6 video bits (when HIBW = 0). To activate 6-bit CRC mode, set PXL_CRC = 1 in the remote-side device first, then in the local-side device. When using 6-bit CRC mode, the available internal bus width is reduced by 6 bits in single-input mode (DBL = 0) and 3 bits in double-input mode (DBL = 1). Note that the input bus width may already have been reduced due to pin availability of the serializer or deserializer; thus, the reduction of bandwidth from CRC may not be visible (see Table 3).

An additional 32-bit video line CRC is available by setting LINE_CRC_EN = 1. When enabled, the serializer calculates the 32-bit CRC of the video line and sends this information during the blanking period. The deserializer compares the received CRC with the video line data. The deserializer's LINE_CRC_ERR bit latches when a CRC error is detected. LINE_CRC_ERR clears when read.

### Bus Widths

The serial link has multiple bus-width settings that determine the parallel bus width and the resulting parallel word rate. The serial link operates to a maximum serial bit rate of 1.74Gbps. The BWS bit determines if each serial packet is 30 or 40 bits long, which translates to a maximum serial packet rate (and resulting maximum parallel word rate) of 58MHz or 43.5MHz when BWS = 0 or 1 respectively. Encoding translates the 24, 27, or 32 parallel bits into 30- or 40-bit serial packets. One bit is used for parity, while a second is reserved for the control channel. An additional 6 bits are used during optional 6-bit CRC. In addition, double mode splits the remaining word size in half, if used. The remaining bits can be used for video bits (minus any sync bits if H/V encoding is not used)

The following modes list the internal bus widths. The number of available input and output pins may limit the actual bus width available.

- **24-Bit Mode (Figure 13)**

When BWS = 0 and HIBW = 0, the 30-bit serial packet corresponds with three 8b/10b symbols representing 24 bits (24-bit mode). After the parity and control channel, this leaves 16/22 bits of video data if CRC is/or is not used (single mode), or 8/11 bits of video data if CRC is/or is not used (double mode).

- **27-Bit High-Bandwidth Mode (Figure 14)**

When BWS = 0 and HIBW = 1 (high-bandwidth mode), the 30-bit serial packet represents three 9b/10b symbols representing 27 bits. After the parity and control channel, this leaves 19/25 bits of video data if CRC is/or is not used (single mode), or 9/12 bits of video data if CRC is/or is not used (double mode).

- **32-Bit Mode (Figure 15)**

When BWS = 1, the 40-bit serial packet corresponds with four 8b/10b symbols representing 32 bits (32-bit mode). After parity and control channel, this leaves 24/30 bits of video data if CRC is/or is not used (single mode), or 12/15 bits of video data if CRC is/or is not used (double mode).

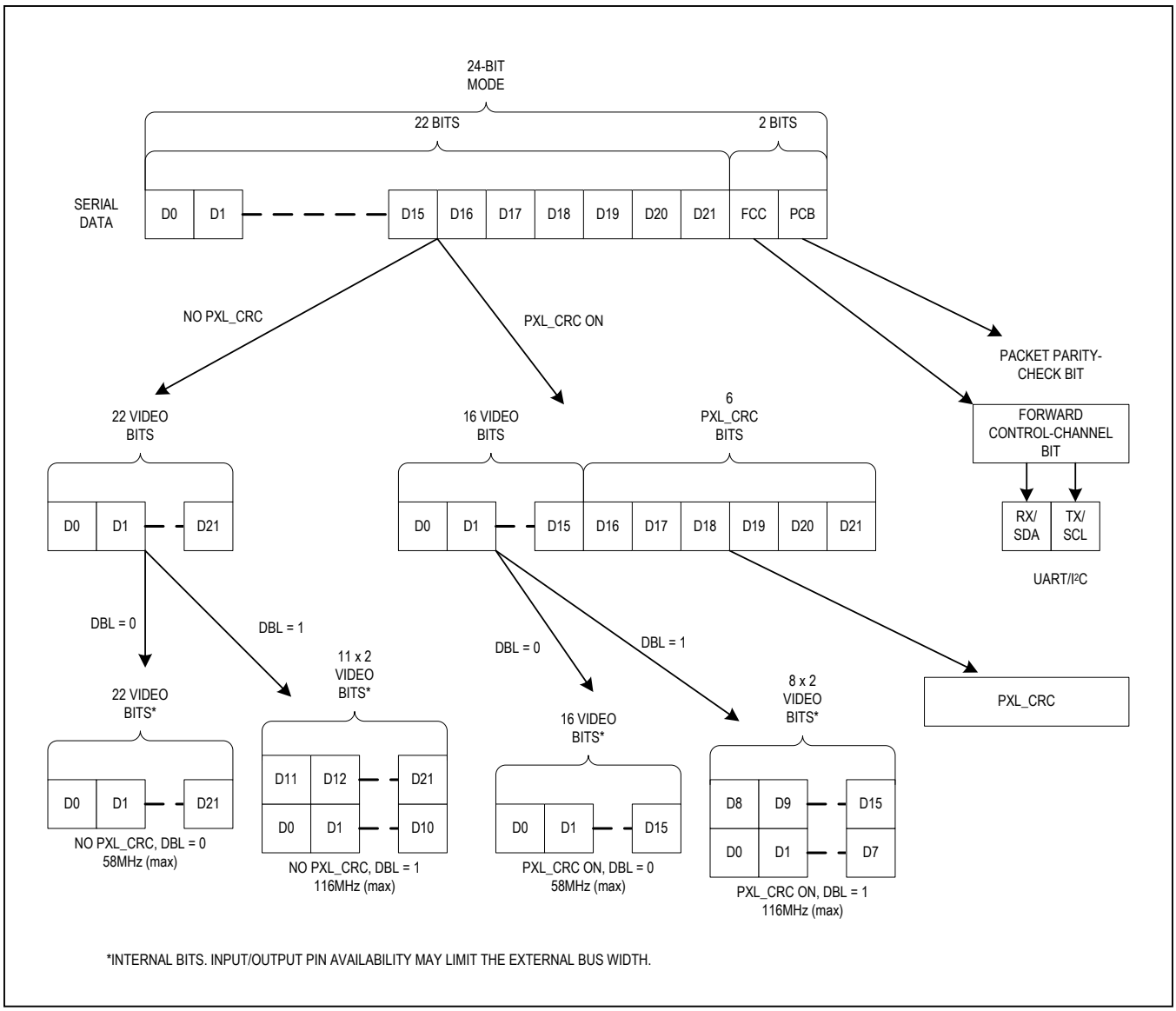



*Figure 13. 24-Bit Mode Serial-Data Format*