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MAX96707

14-Bit GMSL Serializer with High-Immunity/ Bandwidth Mode and Coax/STP Cable Drive

General Description

The MAX96707 is a compact serializer in a 4mm x 4mm TQFN package especially suited for automotive camera applications. In high-bandwidth mode, the parallel-clock maximum is 116MHz for 12-bit linear or combined HDR data types.

The embedded control channel operates at 9.6kbps to 1Mbps in I²C mode, allowing programming of serializer, deserializer (SerDes), and camera registers independent of video timing.

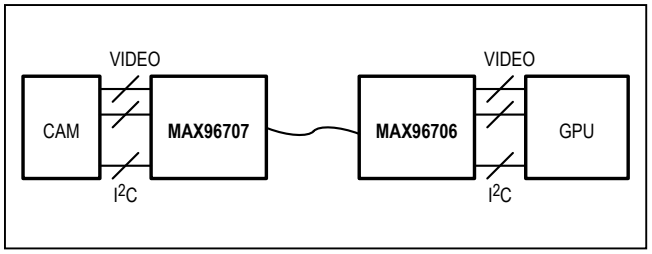
For driving longer cables, the IC has programmable pre/deemphasis. Programmable spread spectrum is available on the serial output. The serial output meets ISO 10605 and IEC 61000-4-2 ESD standards. The supply range is 1.7V to 1.9V.

The MAX96707 is available in a 24-pin TQFN package with 0.5mm lead pitch, and operates over the -40°C to +115°C temperature range.

Applications

- Automotive Camera Applications

Simplified Block Diagram



Ordering Information **appears at end of data sheet.**

Benefits and Features

- Ideal for Safety Camera Applications
  - Works with Low-Cost 50Ω Coax (100Ω STP) Cables
  - Error Detection of Video/Control Data
  - High-Immunity Mode for Robust Control-Channel EMC Tolerance
  - Retransmission of Control Data Upon Error Detection
  - Best-in-Class Supply Current: 88mA (max)
  - Pre/Deemphasis Allows 15m Cable at Full Speed
  - 24-Pin (4mm x 4mm) TQFN Package with 0.5mm Lead Pitch
- High-Speed Data Serialization for Megapixel Cameras
  - Up to 1.74Gbps Serial-Bit Rate
  - 12.5MHz to 87MHz x 12-Bit + H/V Data
  - 36.66MHz to 116MHz x 12-Bit + H/V Data (through Internal Encoding)
- Multiple Modes for System Flexibility
  - 9.6kbps to 1Mbps Control Channel in I²C Mode (with Clock Stretch)
  - Crosspoint Switch Accepts Any Input Bitmap
  - Modes for Encoded VSYNC and HSYNC
- Reduces EMI and Shielding Requirements
  - Programmable Output Spread Spectrum
  - Tracks Spread Spectrum Applied at the Parallel Input
  - 1.7V to 1.9V I/O Supply
- Peripheral Features for Camera Power-Up and Verification
  - Built-In PRBS Generator for BER Testing
  - Dedicated GPO for Camera Frame-Sync Trigger and Other Uses
  - Remote/Local Wake-Up from Sleep Mode
- Meets AEC-Q100 Automotive Specification
  - -40°C to +115°C Operating Temperature
  - ±8kV Contact and ±15kV Air IEC 61000-4-2 and ISO 10605 ESD Protection

19-7766; Rev 0; 2/16

maxim integrated™

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

AVDD to GND* .....-0.5V to +1.9V
DVDD to GND*.....-0.5V to +1.9V
OUT+, OUT- to GND*.....-0.5V to +1.9V
All Other Pins to GND*.....-0.5V to (DVDD + 0.5V)
OUT+, OUT- Short Circuit to Ground or Supply.....Continuous

Continuous Power Dissipation, T_A = +70°C
TQFN (derate 27.8 mW/°C above +70°C) 2222.2mW
Operating Temperature Range.....-40°C to +115°C
Junction Temperature.....+125°C
Storage Temperature Range..... -40°C to +150°C
Soldering Temperature (reflow).....+260°C

**EP externally connected to GND.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

24-Pin TQFN-EP

Package Code	**T2444+4**
Outline Number	**21-0139**
Land Pattern Number	**90-0022**
Single-Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	48
Junction-to-Case Thermal Resistance (θ_{JC})	3
Four-Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	36
Junction-to-Case Thermal Resistance (θ_{JC})	3

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (DIN_, PCLKIN, HS, VS, HIM, MS)						
High-Level Input Voltage	V_{IH}		0.65 x V_{DVDD}			V
Low-Level Input Voltage	V_{IL}				0.35 x V_{DVDD}	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DVDD}	-20		+20	µA
SINGLE-ENDED OUTPUT (GPO)						
High-Level Output Voltage	V_{OH}	I_{OH} = -2mA	V_{DVDD} - 0.2			V
Low-Level Output Voltage	V_{OL}	I_{OL} = 2mA			0.2	V
Output Short-Circuit Current	I_{OS}	V_O = 0V	3	12	21	mA
I^2C and GENERAL-PURPOSE I/Os (SDA, SCL, GPIO_) with OPEN-DRAIN OUTPUTS						
High-Level Input Voltage	V_{IH}		0.7 x V_{DVDD}			V
Low-Level Input Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Current	I_{IN}	V_{IN} = 0 to V_{DVDD} (Note 2), SDA, SCL	-110		+5	µA
		V_{IN} = 0 to V_{DVDD} (Note 2), GPIO_	-80		+5	
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Input Capacitance	C_{IN}	Each pin (Note 3)			10	pF

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL OUTPUTS (OUT+, OUT-)						
Differential Output Voltage	V_{OD}	Preemphasis off, high drive (Figure 1)	300	400	500	mV
		3.3dB preemphasis, high drive (Figure 2)	350		610	
		3.3dB deemphasis, high drive (Figure 2)	240		425	
Change in V_{OD} Between Complementary Output States	ΔV_{OD}				25	mV
Output Offset Voltage (V_{OUT+} + V_{OUT-})/2 = V_{OS}	V_{OS}	Preemphasis off	1.1	1.4	1.56	V
Change in V_{OS} Between Complementary Output States	ΔV_{OS}				25	mV
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-60			mA
		V_{OUT+} or V_{OUT-} = 1.9V			25	
Magnitude of Differential Output Short-Circuit Current	I_{OSD}	V_{OD} = 0V			25	mA
Output-Termination Resistance (Internal)	R_O	From OUT+ or OUT- to AVDD	45	54	63	Ω
REVERSE CONTROL-CHANNEL RECEIVER OUTPUTS (OUT+, OUT-)						
High-Switching Threshold	V_{CHR}	Legacy			27	mV
		High immunity			40	
Low-Switching Threshold	V_{CLR}	Legacy	-27			mV
		High immunity	-40			
SINGLE-ENDED SERIAL OUTPUTS (OUT+ or OUT-)						
Single-Ended Output Voltage	V_O	Preemphasis off, high drive (Figure 3)	375	500	625	mV
		3.3dB preemphasis, high drive (Figure 2)	435		765	
		3.3dB deemphasis, high drive (Figure 2)	300		535	
Output Short-Circuit Current	I_{OS}	V_{OUT+} or V_{OUT-} = 0V	-69			mA
		V_{OUT+} or V_{OUT-} = 1.9V			32	
Output-Termination Resistance (Internal)	R_O	From OUT+ or OUT- to AVDD	45	54	63	Ω

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Current, Worst-Case Pattern (Figure 4)	I_{WCS}	f_{PCLKIN} = 116MHz, HIBW = 0, BWS = 0, default register values, AVDD + DVDD (1.9V)		66	88	mA
		f_{PCLKIN} = 116MHz, HIBW = 1, BWS = 0, default register values, AVDD + DVDD (1.9V)		63	83	
		f_{PCLKIN} = 87MHz, BWS = 1, default register values, AVDD + DVDD (1.9V)		62	83	
Sleep-Mode Supply Current	I_{CCS}	Wake-up receiver enabled		40	100	µA
ESD PROTECTION						
OUT+, OUT- (Note 4)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF, Contact Discharge		±8		
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF, Air Discharge		±15		
		ISO 10605, R_D = 2kΩ, C_S = 330pF, Contact Discharge		±8		
		ISO 10605, R_D = 2kΩ, C_S = 330pF, Air Discharge		±15		
All Other Pins (Note 5)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4		kV

AC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL CLOCK INPUT (PCLKIN)						
Clock Frequency	f_{PCLKIN}	BWS = 0, HIBW = 0, single input	16.66		58	MHz
		BWS = 0, HIBW = 1, single input	36.66		58	
		BWS = 1, single input	12.5		43.5	
		BWS = 0, HIBW = 0, double input	33.32		116	
		BWS = 0, HIBW = 1, double input	73.33		116	
		BWS = 1, double input	25		87	
Clock Duty Cycle	DC	t_{HIGH}/t_T or t_{LOW}/t_T (Note 3, Figure 5)	35	50	65	%
Clock Transition Time	t_R, t_F	(Note 3, Figure 5)			4	ns
Clock Jitter	t_J	1.74Gbps bit rate, 300kHz sinusoidal jitter (Note 3)			800	ps
I²C PORT TIMING						
I²C Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to DVDD	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to DVDD	20		150	ns
I²C TIMING (Figure 6)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)	> 100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)	> 400		1000	
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			

AC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, low	0			ns
		f_{SCL} range, mid	0			
		f_{SCL} range, high	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, low	250			ns
		f_{SCL} range, mid	100			
		f_{SCL} range, high	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range, low	4			µs
		f_{SCL} range, mid	0.6			
		f_{SCL} range, high	0.26			
Bus-Free Time	t_{BUF}	f_{SCL} range, low	4.7			µs
		f_{SCL} range, mid	1.3			
		f_{SCL} range, high	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Data Valid-Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, low			3.45	µs
		f_{SCL} range, mid			0.9	
		f_{SCL} range, high			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, low			50	ns
		f_{SCL} range, mid			50	
		f_{SCL} range, high			50	
Capacitive Load of Each Bus Line	C_B	(Note 3)			100	pF
SWITCHING CHARACTERISTICS (Note 3)						
Differential/Single-Ended Output Rise/Fall Time	t_R, t_F	20% to 80%, V_{OD}, 400mV differential R_L = 100Ω, 500mV single-ended R_L = 50Ω, serial bit rate = 1.74Gbps			250	ps
Total Serial-Output Jitter (Differential Output)	t_{TSOJ1}	1.74Gbps PRBS, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)		0.25		UI
Deterministic Serial-Output Jitter (Differential Output)	t_{DSOJ2}	1.74Gbps PRBS, measured at V_{OD} = 0V differential, preemphasis disabled (Figure 7)		0.15		UI
Total Serial-Output Jitter (Single-Ended Output)	t_{TSOJ1}	1.74Gbps PRBS, measured at V_O/2, preemphasis disabled (Figure 3)		0.25		UI
Deterministic Serial-Output Jitter (Single-Ended Output)	t_{DSOJ2}	1.74Gbps PRBS, measured at V_O/2, preemphasis disabled (Figure 3)		0.15		UI
Parallel Data-Input Setup Time	t_{SET}	(Figure 8)	2			ns

AC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7V to 1.9V, R_L = 100Ω ±1% (differential), T_A = -40°C to +115°C, EP connected to GND, typical values are at V_{DVDD} = V_{AVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

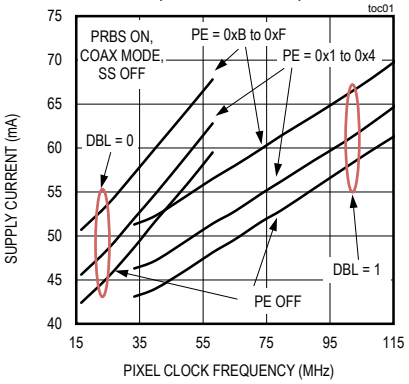
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Parallel Data Input Hold Time	t_{HOLD}	(Figure 8) (Note 3)	1			ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (Figure 9)			350	µs
Serializer Delay	t_{SD}	Spread spectrum enabled (Figure 10) (Notes 3, 6)			2065	Bits
		Spread spectrum disabled (Figure 10) (Notes 3, 6)			1095	
Link Start Time	t_{LOCK}	(Figure 11)			2	ms
Power-Up Time	t_{PU}	(Figure 12)			7	ms

Note 1: Limits are 100% production tested at T_A = +115°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.
Note 2: I_{IN} min is due to voltage drop across the internal pullup resistor.
Note 3: Not production tested. Guaranteed by design.
Note 4: Specified pin to ground.
Note 5: Specified pin to all supply/ground.
Note 6: Measured in serial link bit times. Bit time = 1/(30 x f_{PCLKIN}) for BWS = 0; bit time = 1/(40 x f_{PCLKIN}) for BWS = 1.

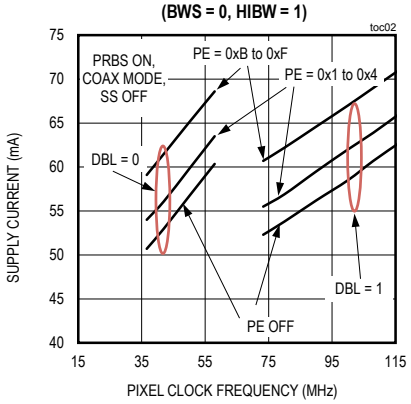
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

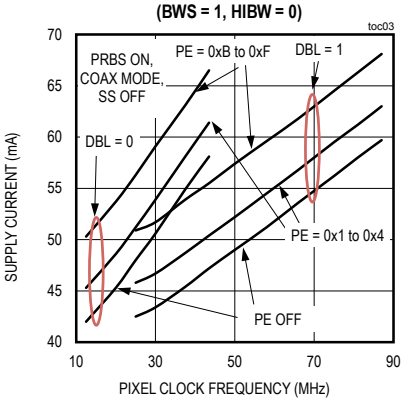
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 0)



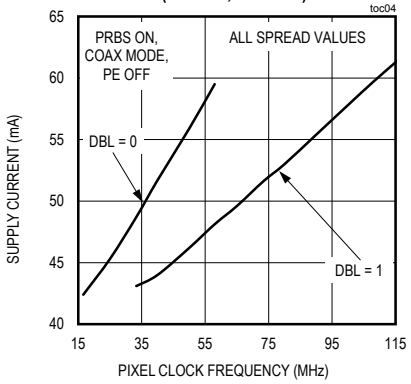
SUPPLY CURREN vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 1)



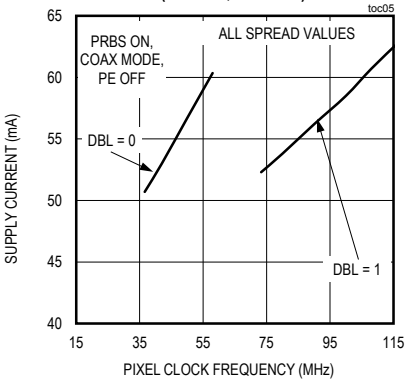
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 1, HIBW = 0)



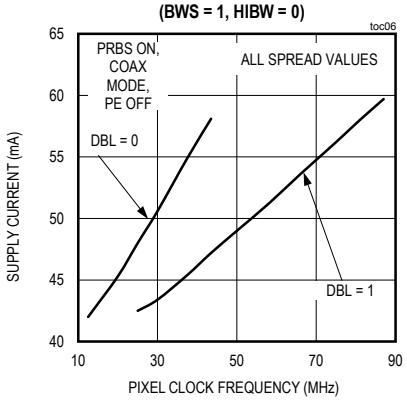
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 0)



SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 0, HIBW = 1)



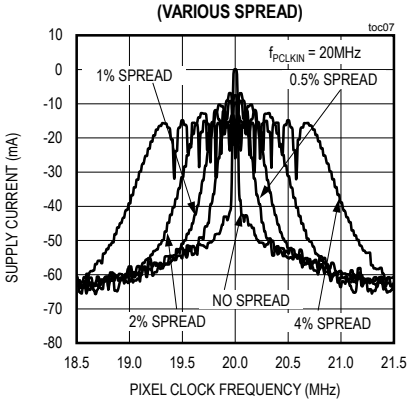
SUPPLY CURRENT vs. PIXEL CLOCK FREQUENCY (BWS = 1, HIBW = 0)



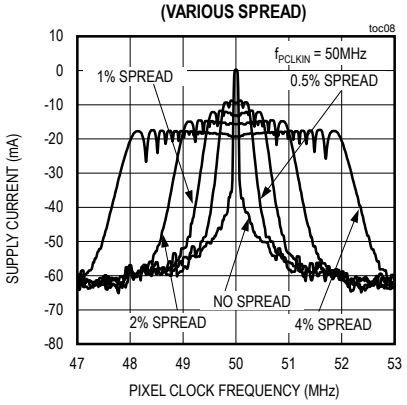
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

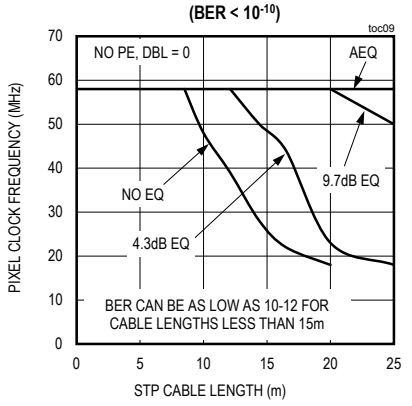
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS SPREAD)



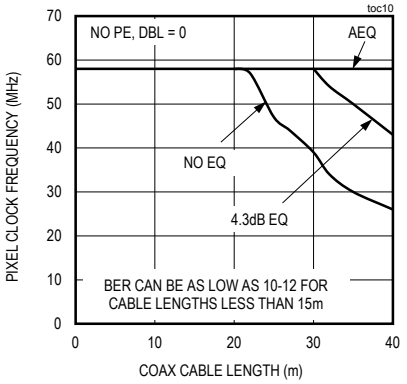
OUTPUT POWER SPECTRUM vs. PCLK FREQUENCY (VARIOUS SPREAD)



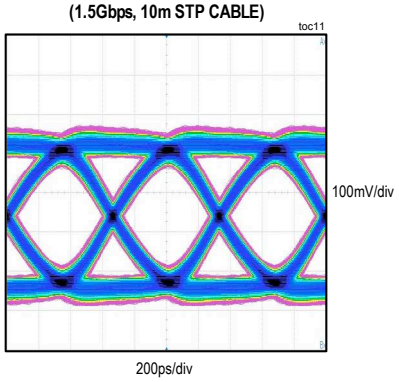
MAXIMUM PIXEL CLOCK FREQUENCY vs. STP CABLE LENGTH (BER < 10^{-10})



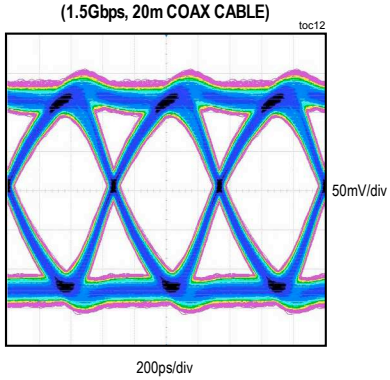
MAXIMUM PIXEL CLOCK FREQUENCY vs. COAX CABLE LENGTH (BER < 10^{-10})



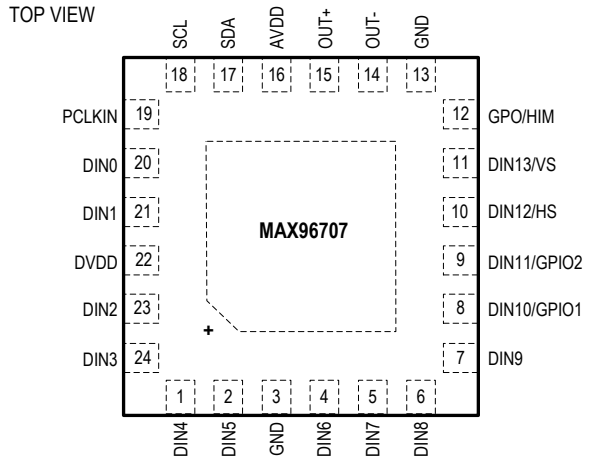
SERIAL LINK SWITCHING PATTERN WITH 4.4dB PREEMPHASIS (1.5Gbps, 10m STP CABLE)



SERIAL LINK SWITCHING PATTERN WITH 3.3dB PREEMPHASIS (1.5Gbps, 20m COAX CABLE)



Pin Configuration



TQFN

(4mm x 4mm)

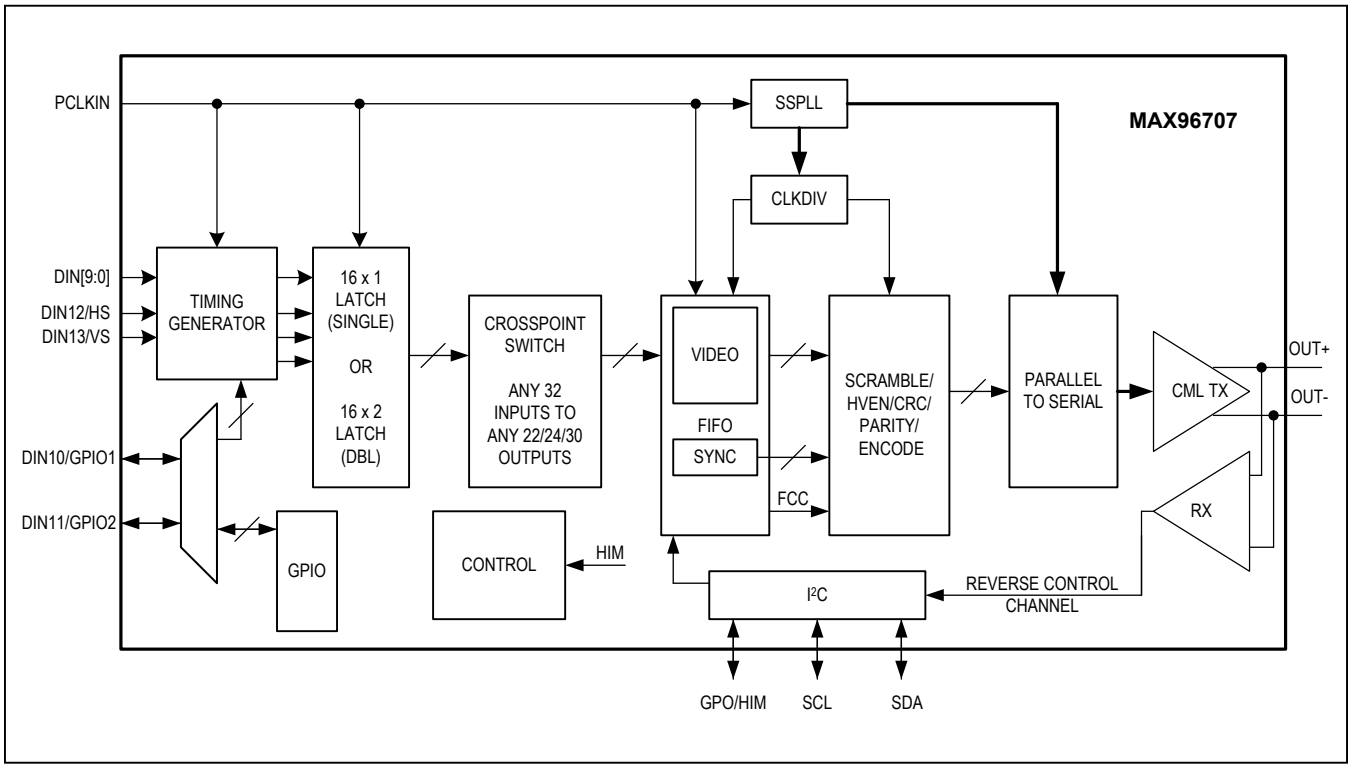
Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
POWER				
3, 13	GND	Analog and Digital Ground		Power
16	AVDD	1.8V Analog Power Supply. Bypass AVDD to GND with 0.1µF, and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to AVDD.		Power
22	DVDD	1.8V Digital Power Supply. Bypass DVDD to GND with 0.1µF, and 0.001µF capacitors as close as possible to the device with the smaller value capacitor closest to DVDD.		Power
EP	—	Exposed Pad. EP is internally connected to device ground. Must connect EP to the PCB ground plane through a via array for proper thermal and electrical performance.		Power
HIGH-SPEED DIGITAL				
Single Function				
1	DIN4	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
2	DIN5	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
4	DIN6	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
5	DIN7	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
6	DIN8	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
7	DIN9	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
19	PCLKIN	Parallel Clock Input with Internal Pulldown to GND. Latches parallel data inputs and provides the PLL reference clock.	DVDD	Digital
20	DIN0	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
21	DIN1	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
23	DIN2	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
24	DIN3	Parallel Data Input. Internal pulldown to GND.	DVDD	Digital
Multifunction				
8	DIN10/GPIO1	Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to GND. GPIO1 has an open-drain input/output with internal 60kΩ pullup to DVDD.	DVDD	Digital
9	DIN11/GPIO2	Parallel Data Input/GPIO. Defaults to parallel data input on power-up. Parallel data input has internal pulldown to GND. GPIO2 has an open-drain input/output with internal 60kΩ pullup to DVDD.	DVDD	Digital
10	DIN12/HS	Parallel Data Input/Horizontal Sync with Internal Pulldown to GND. Defaults to parallel data input on power-up. Defaults to horizontal-sync input when HS/VS encoding is enabled, or when in high-bandwidth mode.	DVDD	Digital
11	DIN13/VS	Parallel Data Input/Vertical Sync with Internal Pulldown to GND. Defaults to parallel data input on power-up. Defaults to vertical-sync input when HS/VS encoding is enabled, or when in high-bandwidth mode.	DVDD	Digital
Configuration and Interface				
12	GPO/HIM	General-Purpose Output/High-Immunity Mode Input with internal Pulldown to GND. HIM is latched at power-up and switches to GPO output automatically after power-up. Connect HIM to DVDD with a 30kΩ resistor to set high, or leave open to set low. HIGHIMM can be programmed to a different value after power-up. HIGHIMM in the deserializer must be set to the same value. GPO output follows the state of the GPI (or INT) input on the GMSL deserializer. GPO is low upon power-up.	DVDD	Digital
14	OUT-	Inverting Coax/Twisted-Pair Serial Output	—	Digital
15	OUT+	Noninverting Coax/Twisted-Pair Serial Output	—	Digital
17	SDA	Serial Data. Input/output with internal 30kΩ pullup to DVDD. SDA is the SDA input/output of the serializer's I^2C master/slave. SDA has an open-drain driver and requires a pullup resistor.	DVDD	Digital
18	SCL	Serial Clock. Input/output with internal 30kΩ pullup to DVDD. SCL is the SCL input/output of the serializer's I^2C master/slave. SCL has an open-drain driver and requires a pullup resistor.	DVDD	Digital

Functional Block Diagram



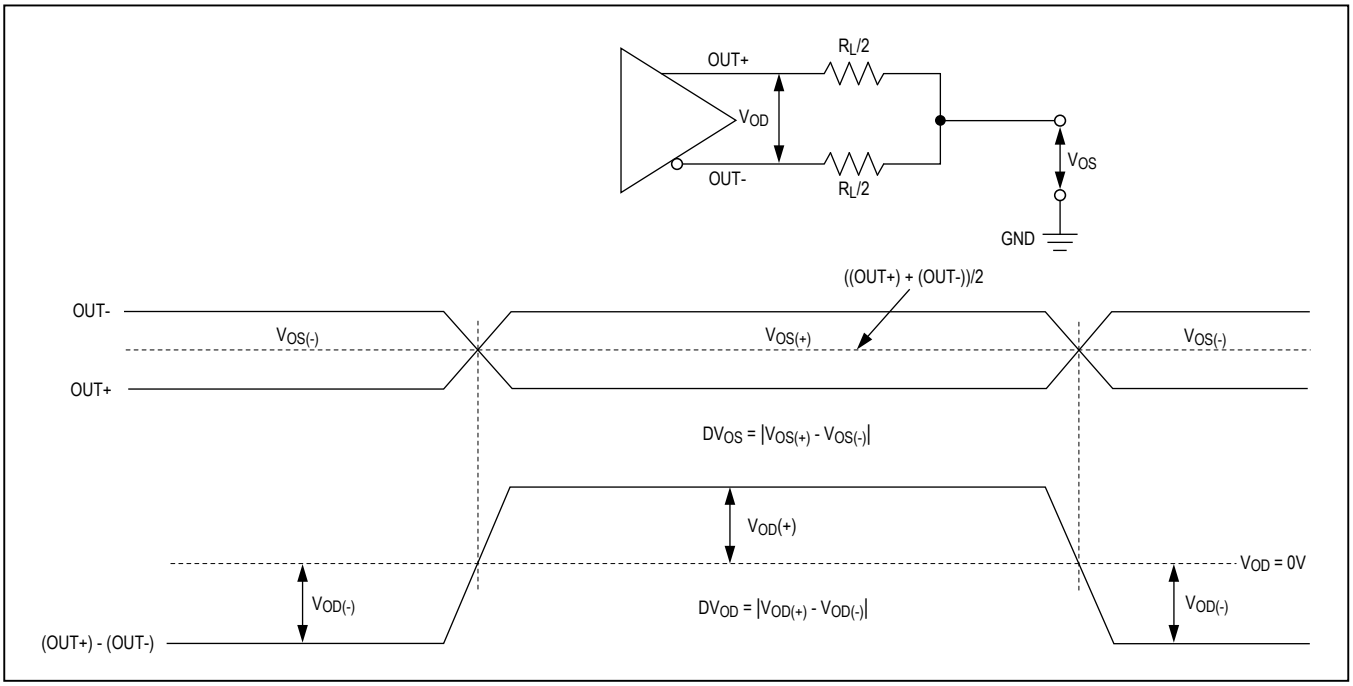


Figure 1. Serial-Output Parameters

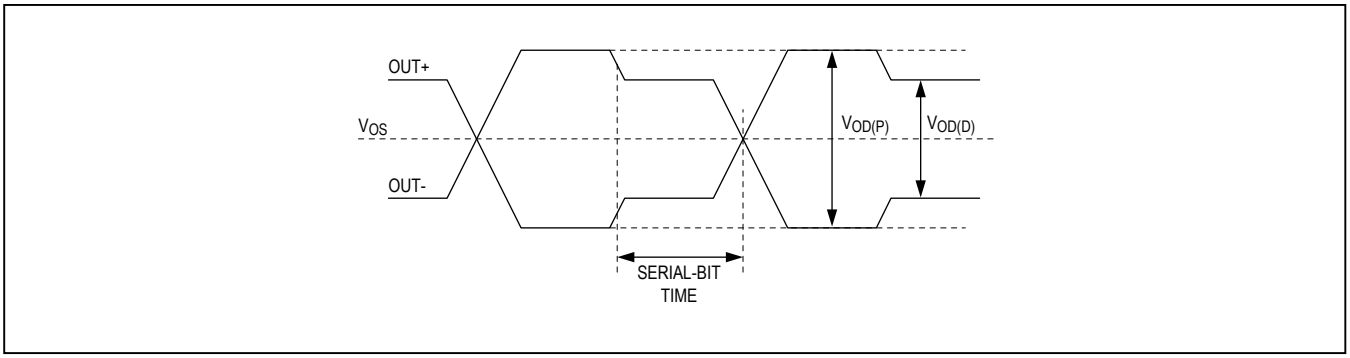


Figure 2. Output Waveforms at OUT+, OUT-

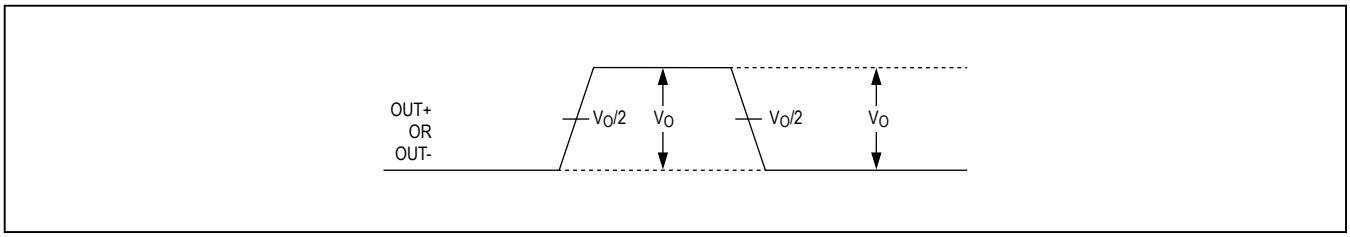


Figure 3. Single-Ended Output Template

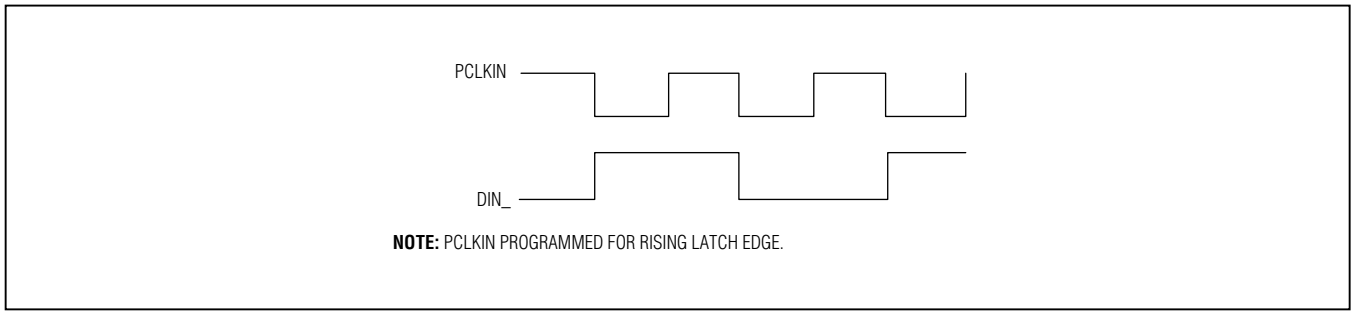


Figure 4. Worst-Case Pattern Input

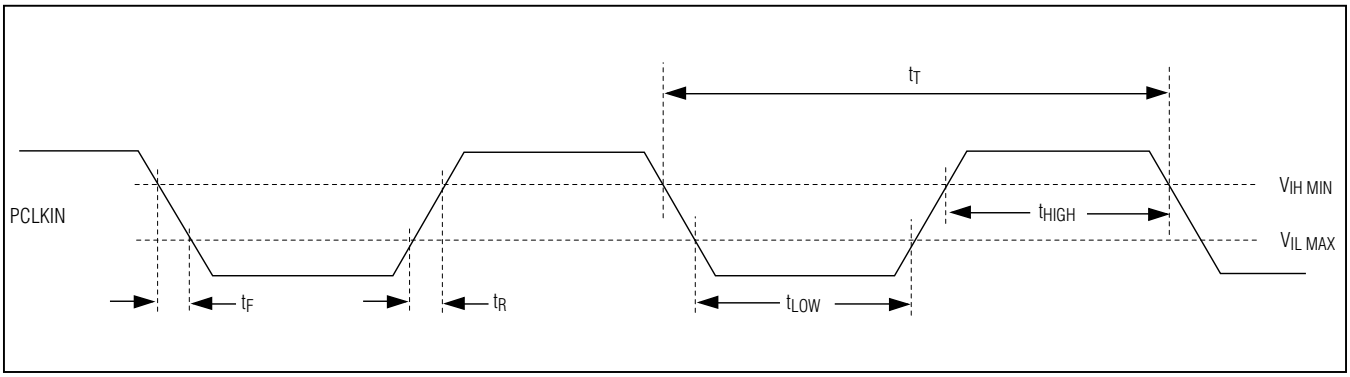


Figure 5. Parallel Clock Input Requirements

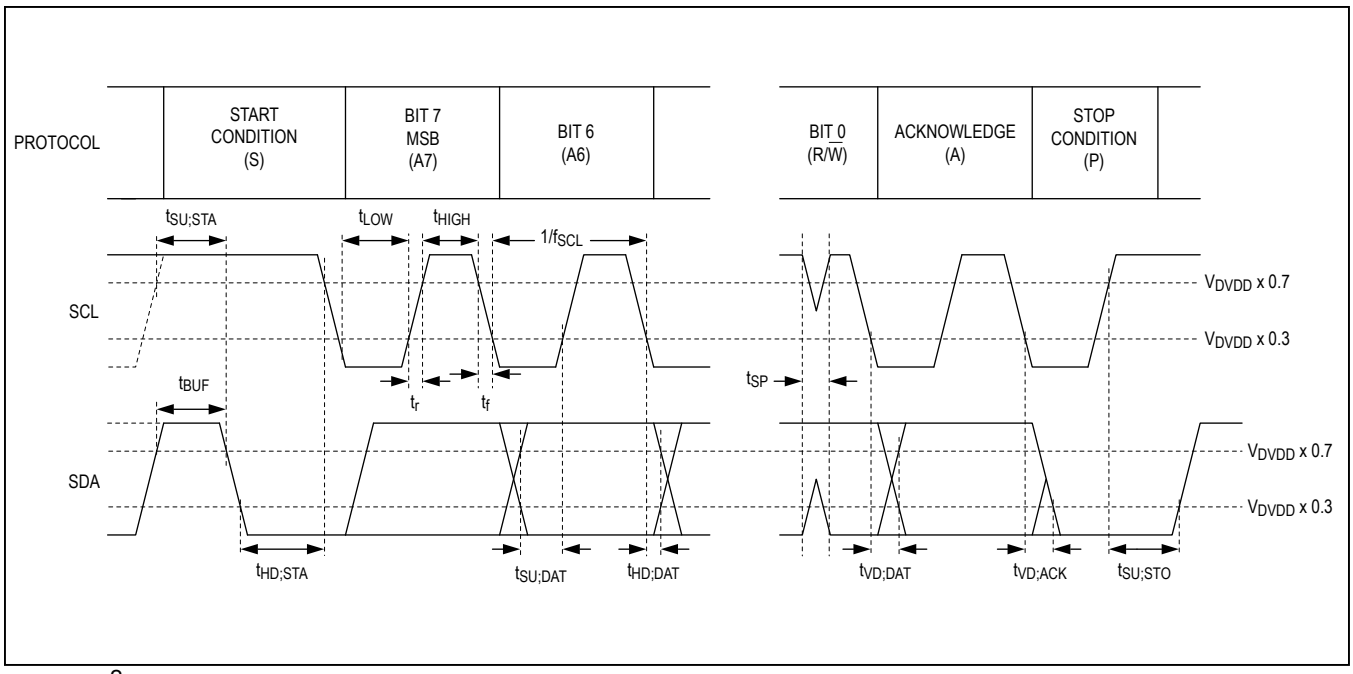


Figure 6. I²C Timing Parameters

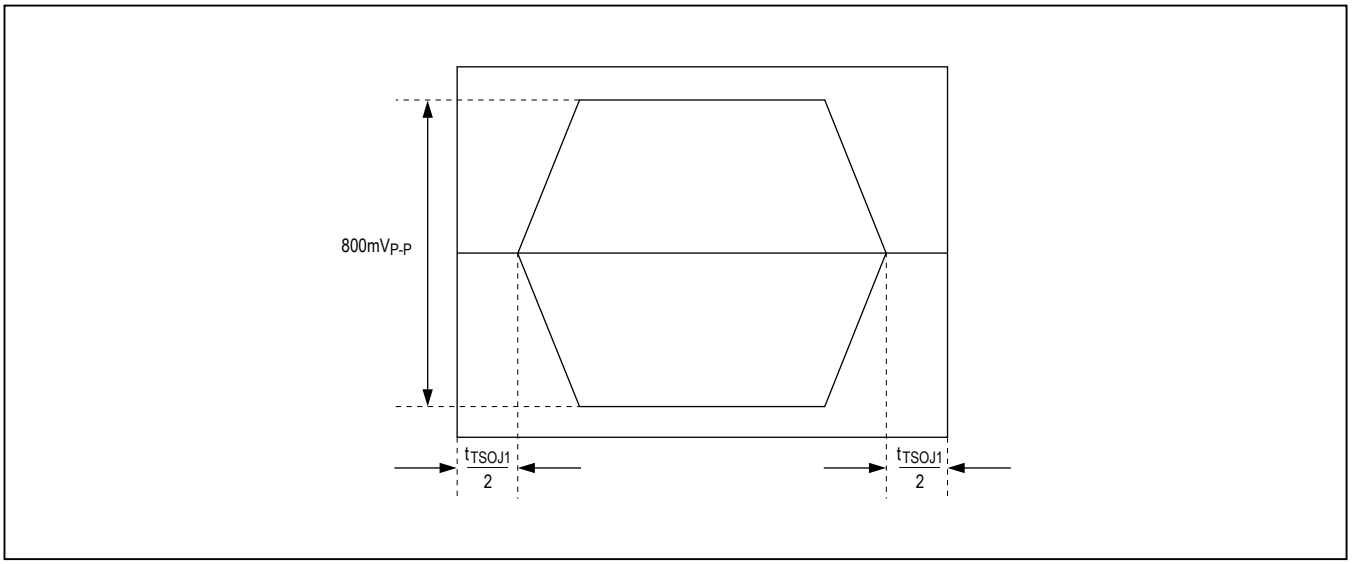


Figure 7. Differential Output Template

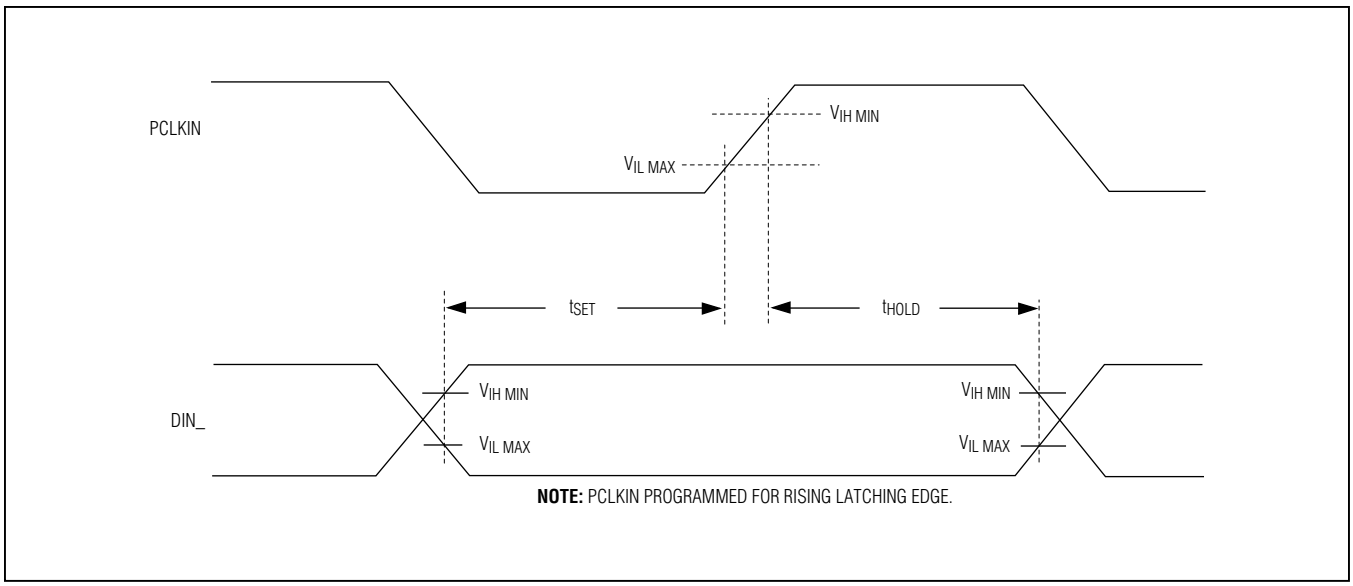


Figure 8. Input Setup and Hold Times

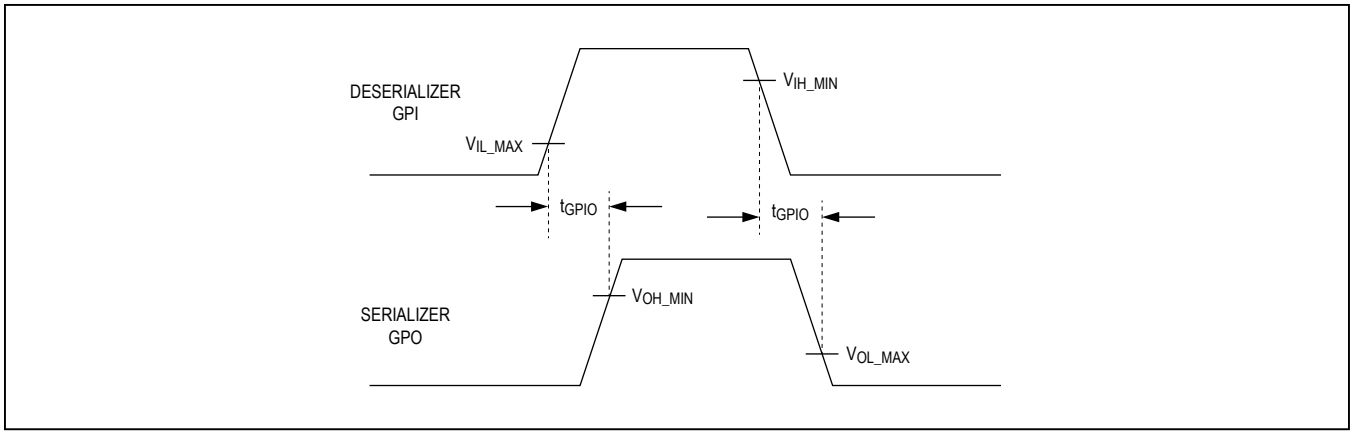


Figure 9. GPI-to-GPO Delay

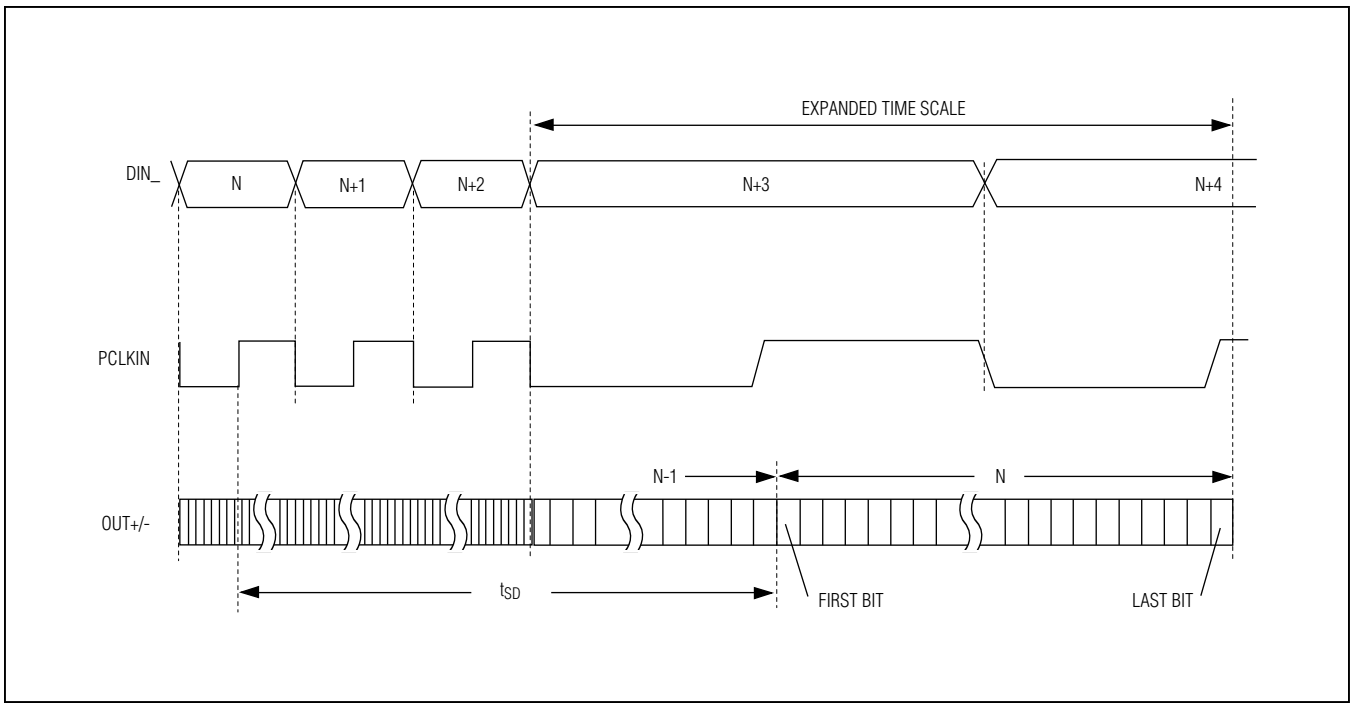


Figure 10. Serializer Delay

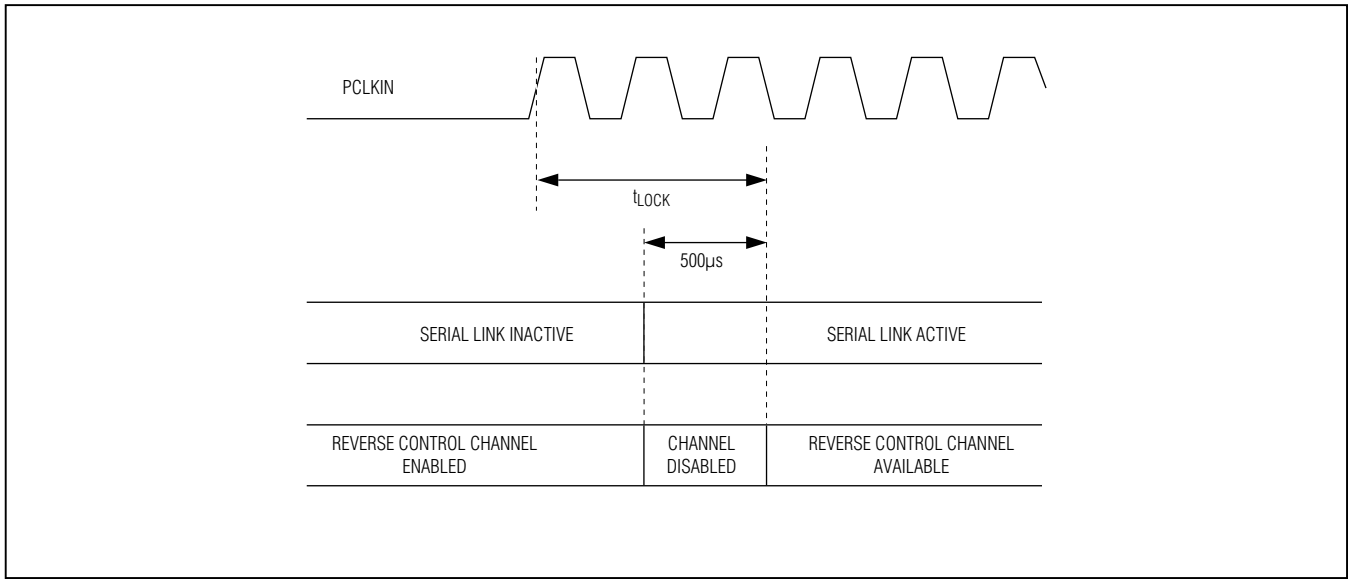


Figure 11. Link Startup Time

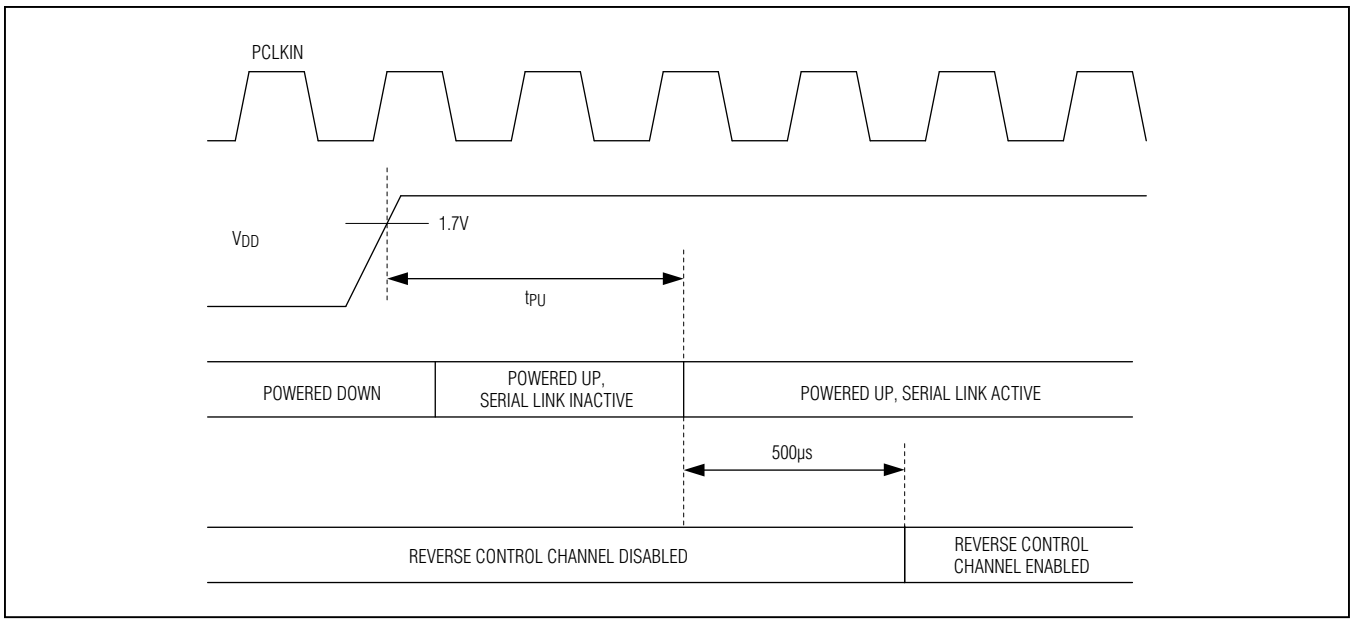


Figure 12. Power-Up Delay

Detailed Description

The MAX96707 is a compact device with features especially suited for automotive camera applications. The device operates at a variety of input widths and word rates up to a total serial-data rate up to 1.74Gbps. High- bandwidth mode offers a 116MHz parallel clock rate with 12 bits of video data and 2 bits of sync (HS/VS) data. An embedded 9.6kbps to 1Mbps control channel programs the serializer, deserializer, and any attached I²C peripherals.

To promote safety applications, the device features CRC protection of video and control data. In addition, control-channel retransmission and high-immunity modes reduce the effects of bit errors corrupting communication. Preemphasis and a PRBS tester allow for in-system evaluation and optimization of the link quality.

The MAX96707 operates over the -40°C to +115°C automotive temperature range.

Serial Link Signaling and Data Format

The serializer scrambles the input parallel data and combines this with the forward control data. The data is then encoded for transmission and output as a single-serialized bitstream at several times the input word rate (depending on bus width). The deserializer receives the serial data and recovers the clock signal. The data is then deserialized, decoded, and descrambled into parallel output data and forward control data.

Operating Modes

The GMSL devices are configurable to operate in many modes depending on the application. These modes allow for a more efficient use of serial bandwidth. Most of these settings are set during system design, and are configured through register bits.

Video/Configuration Link

In normal operation, the serializer runs in video link mode (serializer SEREN = 1) with video data and control data sent across the serial link. Set SEREN = 0 in the serializer to turn off serialization. The serializer powers up in video link mode and requires a valid PCLK for operation.

A configuration link is available to set up the serializer, deserializer, and peripherals when PCLK is not available. Set SEREN = 0 and CLINK = 1 in the serializer to enable the configuration link (SEREN = 1 forces the serializer into video link mode). Once PCLK has been established, turn on the video link (SEREN = 1).

By default, video link mode requires a valid PCLK for operation. Set AUTO_CLINK bit = 1 and SEREN = 1 in the serializer to have the device automatically switch between the video link and configuration link whenever PCLK is not present.

Single/Double Mode

Single-/double-mode operation configures the available 1.74Gbps bandwidth into a variety of widths and word rates. Single-mode operation is compatible with all GMSL devices and serializers, yielding one parallel word for each serial word. Double mode serializes two half-width parallel words for each serial word, resulting in a 2x increase in the parallel word rate range (compared to single mode). Set DBL = 0 for single-mode operation and DBL = 1 for double-mode operation.

HS/VS Encoding

By default, GMSL assigns a video bit slot to HSYNC, VSYNC, and DE (if used). With HS/VS encoding, the device instead encodes special packets to sync signals to free up additional video bit slots. HS/VS encoding is on by default when the device is in high-bandwidth mode (HIBW = 1). DE is encoded only when HIBW = 1 and DE_EN = 1. Set HVEN = 1 to turn on HS/VS encoding when HIBW = 0 (DE, if enabled, uses up a video bit). HS/VS encoding requires that HSYNC, VSYNC, and DE (if used) remain high during the active video and low during the blanking period. Use HS/VS inversion when using reverse-polarity sync signals.

Error Detection

The serial link's 8b/10b encoding/decoding and 1-bit parity detect bit errors that occur on the serial link. An optional 6-bit CRC check is available at the expense of 6 video bits (when HIBW = 0). To activate 6-bit CRC mode, set PXL_CRC = 1 in the remote-side device first, then in the local-side device. When using 6-bit CRC mode, the available internal bus width is reduced by 6 bits in single-input mode (DBL = 0) and 3 bits in double-input mode (DBL = 1). Note that the input bus width may already have been reduced due to pin availability of the serializer or deserializer; thus, the reduction of bandwidth from CRC may not be visible (see Table 3).

An additional 32-bit video line CRC is available by setting LINE_CRC_EN = 1. When enabled, the serializer calculates the 32-bit CRC of the video line and sends this information during the blanking period. The deserializer compares the received CRC with the video line data. The deserializer's LINE_CRC_ERR bit latches when a CRC error is detected. LINE_CRC_ERR clears when read.

Bus Widths

The serial link has multiple bus-width settings that determine the parallel bus width and the resulting parallel word rate. The serial link operates to a maximum serial bit rate of 1.74Gbps. The BWS bit determines if each serial packet is 30 or 40 bits long, which translates to a maximum serial packet rate (and resulting maximum parallel word rate) of 58MHz or 43.5MHz when BWS = 0 or 1 respectively. Encoding translates the 24, 27, or 32 parallel bits into 30- or 40-bit serial packets. One bit is used for parity, while a second is reserved for the control channel. An additional 6 bits are used during optional 6-bit CRC. In addition, double mode splits the remaining word size in half, if used. The remaining bits can be used for video bits (minus any sync bits if H/V encoding is not used)

The following modes list the internal bus widths. The number of available input and output pins may limit the actual bus width available.

- 24-Bit Mode (Figure 13)

When BWS = 0 and HIBW = 0, the 30-bit serial packet corresponds with three 8b/10b symbols representing 24 bits (24-bit mode). After the parity and control channel, this leaves 16/22 bits of video data if CRC is/or is not used (single mode), or 8/11 bits of video data if CRC is/or is not used (double mode).

- 27-Bit High-Bandwidth Mode (Figure 14)

When BWS = 0 and HIBW = 1 (high-bandwidth mode), the 30-bit serial packet represents three 9b/10b symbols representing 27 bits. After the parity and control channel, this leaves 19/25 bits of video data if CRC is/or is not used (single mode), or 9/12 bits of video data if CRC is/or is not used (double mode)

- **32-Bit Mode (Figure 15)**

When BWS = 1, the 40-bit serial packet corresponds with four 8b/10b symbols representing 32 bits (32-bit mode). After parity and control channel, this leaves 24/30 bits of video data if CRC is/or is not used (single mode), or 12/15 bits of video data if CRC is/or is not used (double mode).