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MAX96708

14-Bit GMSL Deserializer with Coax or STP Cable Input

General Description

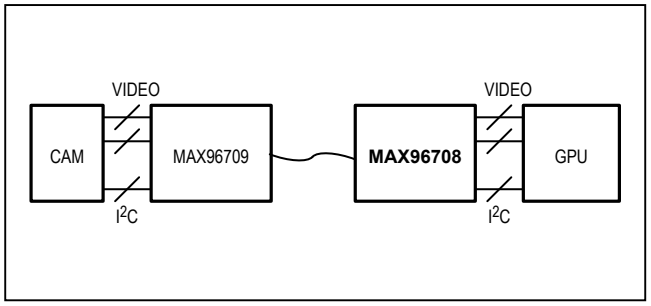
The MAX96708 is a compact deserializer especially suited for automotive camera applications. Features include adaptive equalization and an output crosspoint switch. An embedded control channel operates at 9.6kbps to 1Mbps in UART, I²C, and mixed UART/I²C modes, allowing programming of serializer, deserializer (SerDes), and camera registers, independent of video timing.

The deserializer can track data from a spread-spectrum serial input. The serial input meets ISO 10605 and IEC 61000-4-2 ESD standards. The core supply range is 1.7V to 1.9V and the I/O supply range is 1.7V to 3.6V. The device is available in a 32-pin (5mm x 5mm) TQFN package with 0.5mm lead pitch and operates over -40ºC to +115ºC temperature range.

Applications

- Automotive Camera Applications

Simplified Block Diagram



Ordering Information **appears at end of data sheet.**

Benefits and Features

- Ideal for Safety Camera Applications
  - Works with Low-Cost 50Ω Coax (100Ω STP) Cable
  - Error Detection of Video/Control Data
  - High-Immunity Mode for Robust Control-Channel EMC Tolerance
  - Best-in-Class Supply Current: 185mA (max)
  - Adaptive Equalization for 15m Cable at Full Speed
  - 32-Pin (5mm x 5mm) TQFN Package
  - Horizontal- and Vertical-Sync Encoding and Tracking
- High-Speed Deserialization for Megapixel Cameras
  - Up to 1.74Gbps Serial-Bit Rate
  - 6.25MHz to 87MHz x 12-Bit + H/V Data
  - 36.66MHz to 116MHz x 11-Bit + H/V Data
- Multiple Modes for System Flexibility
  - 9.6kbps to 1Mbps Control Channel in UART,
  - I²C (with Clock Stretch), or UART-to-I²C Modes
  - 2:1 Input Mux for Camera Selection
  - 15 Hardware-Selectable I²C-Device Addresses
  - Pairs with Any Maxim GMSL Serializer
  - Crosspoint Switch Maps Data to any Output
- Reduces EMI and Shielding Requirements
  - Spread-Spectrum Serial-Input Tracking and Transfer to the Parallel Output
  - 1.7V to 1.9V Core and 1.7V to 3.6V I/O Supply
- Peripheral Features for System Verification
  - Built-In PRBS Receiver for BER Testing
  - Dedicated “Up/Down” GPI for Camera Frame Sync Trigger and Other Uses
- Meets AEC-Q100 Automotive Specification
  - -40°C to +115°C Operating Temperature Range
  - ±8kV Contact and ±15kV Air IEC 61000-4-2 and ISO 10605 ESD Protection

19-7784; Rev 0; 3/16

maxim integrated™

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF FIGURES (CONTINUED)

LIST OF TABLES

Absolute Maximum Ratings

AVDD to EP* .....-0.5V to +1.9V
DVDD to EP* .....-0.5V to +1.9V
IOVDD to EP* .....-0.5V to +3.9V
LMN_ to EP* (15mA current limit) .....-0.5V to +3.9V
IN_+, IN_- to EP* .....-0.5V to +1.9V
All Other Pins to EP* ..... -0.5V to (IOVDD + 0.5V)V
IN_+, IN_- Short Circuit to Ground or Supply .....Continuous

Operating Temperature Range .....-40°C to +115°C
Junction Temperature .....+125°C
Storage Temperature Range ..... -40°C to +150°C
Soldering Temperature (reflow) .....+260°C
Continuous Power Dissipation T_A = +70°C, 32-pin TQFN (derate 34.5 mW/°C above +70°C.) 2758.6mW

**EP connected to IC ground.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

32-Pin TQFN-EP

PACKAGE CODE	T3255+8
Outline Number	**21-0140**
Land Pattern Number	**90-0013**
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	47
Junction-to-Case Thermal Resistance (θ_{JC})	1.7
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	29
Junction-to-Case Thermal Resistance (θ_{JC})	1.7

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SINGLE-ENDED INPUTS (GPI, CXTP, I2CSEL, ADD_, HIM, PWDNB, MS)						
High-Level Input Voltage	V_{IH1}		0.65 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL1}				0.35 x V_{IOVDD}	V
Input Current	I_{IN1}	V_{IN} = 0 to V_{IOVDD}	-20		20	µA
SINGLE-ENDED OUTPUTS (DOUT_, VS, HS, DE, PCLKOUT)						
High-Level Output Voltage	V_{OH1}	I_{OH} = -2mA, DCS = 0	V_{IOVDD} - 0.3			V
		I_{OH} = -2mA, DCS = 1	V_{IOVDD} - 0.2			
Low-Level Output Voltage	V_{OL1}	I_{OL} = 2mA, DCS = 0			0.3	V
		I_{OL} = 2mA, DCS = 1			0.2	
High-Impedance Output Current	I_{OZ}	OUTENB = 1, V_{OUT} = 0V or V_{IOVDD}	-20		20	µA
Output Short-Circuit Current	I_{OS}	DOUT_, V_O = 0V, DCS = 0, V_{IOVDD} = 3.0V to 3.6V	15	25	39	mA
		DOUT_, V_O = 0V, DCS = 0, V_{IOVDD} = 1.7V to 1.9V	3	7	13	
		DOUT_, V_O = 0V, DCS = 1, V_{IOVDD} = 3.0V to 3.6V	20	35	63	
		DOUT_, V_O = 0V, DCS = 1, V_{IOVDD} = 1.7V to 1.9V	5	10	21	
		PCLKOUT_, V_O = 0V, DCS = 0, V_{IOVDD} = 3.0V to 3.6V	15	33	50	
		PCLKOUT_, V_O = 0V, DCS = 0, V_{IOVDD} = 1.7V to 1.9V	5	10	17	
		PCLKOUT_, V_O = 0V, DCS = 1, V_{IOVDD} = 3.0V to 3.6V	30	54	97	
		PCLKOUT_, V_O = 0V, DCS = 1, V_{IOVDD} = 1.7V to 1.9V	9	16	32	

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UART/I²C and GENERAL-PURPOSE I/Os (RX/SDA, TX/SCL, GPIO_, ERRB, LOCK, LFLTB) with OPEN-DRAIN OUTPUTS						
High-Level Input Voltage	V_{IH2}		0.7 x V_{IOVDD}			V
Low-Level Input Voltage	V_{IL2}				0.3 x V_{IOVDD}	V
Input Current	I_{IN2}	V_{IN} = 0 to V_{IOVDD} (Note 2), RX/SDA, TX/SCL	-110		5	µA
	I_{IN}	V_{IN} = 0 to V_{IOVDD} (Note 2), GPIO_, ERRB, LOCK	-80		5	
Low-Level Open-Drain Output Voltage	V_{OL}	I_{OL} = 3mA, V_{IOVDD} = 1.7V to 1.9V			0.4	V
		I_{OL} = 3mA, V_{IOVDD} = 3.0V to 3.6V			0.3	
Input Capacitance	C_{IN}	Each pin (Note 3)			10	pF
OUTPUTS FOR REVERSE CONTROL CHANNEL (IN0+, IN0-, IN1+, IN1-)						
Differential High-Output Peak Voltage (V_{IN+} - V_{IN-})	V_{RODH}	Forward channel disabled, normal-immunity mode (Figure 1)	30		60	mV
		Forward channel disabled, high-immunity mode (Figure 1)	50		100	
Differential Low-Output Peak Voltage (V_{IN+} - V_{IN-})	V_{RODL}	Forward channel disabled, normal-immunity mode (Figure 1)	-60		-30	mV
		Forward channel disabled, high-immunity mode (Figure 1)	-100		-50	
Single-Ended High-Output Peak Voltage	V_{ROSH}	Forward channel disabled, normal-immunity mode (Figure 1)	30		60	mV
		Forward channel disabled, high-immunity mode (Figure 1)	50		100	
Single-Ended Low-Output Peak Voltage	V_{ROSL}	Forward channel disabled, normal-immunity mode (Figure 1)	-60		-30	mV
		Forward channel disabled, high-immunity mode (Figure 1)	-100		-50	

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIFFERENTIAL INPUTS (IN0+, IN0-, IN1+, IN1-)						
Differential High-Input Threshold Peak Voltage (V_{IN+} - V_{IN-})	$V_{IDH(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 2)			60	mV
		Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 2)			49	
Differential Low-Input Threshold Peak Voltage (V_{IN+} - V_{IN-})	$V_{IDL(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 2)	-60			mV
		Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 2)	-49			
Input Common-Mode Voltage (V_{IN+} + V_{IN-})/2	V_{CMR}		1	1.3	1.6	V
Differential-Input Resistance (Internal)	R_I		80	100	130	Ω
SINGLE-ENDED INPUTS (IN0+, IN0-, IN1+, IN1-)						
Single-Ended High-Input Threshold Peak Voltage	$V_{ISH(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 3)			43	mV
		Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 3)			33	
Single-Ended Low-Input Threshold Peak Voltage	$V_{ISL(P)}$	Activity detector, medium threshold (0x22 D[6:5] = 01) (Figure 3)	-43			mV
		Activity detector, low threshold (0x22 D[6:5] = 00) (Figure 3)	-33			
Input Resistance (Internal)	R_I		40	50	65	Ω
LINE FAULT DETECTION INPUTS (LMN0, LMN1)						
Short-to-Ground Threshold	V_{TG}	(Figure 4)			0.3	V
Normal Threshold	V_{TN}	(Figure 4)	0.57		1.07	V
Open Threshold	V_{TO}	(Figure 4)	1.45		V_{IO} + 0.06	V
Open-Input Voltage	V_{IO}	(Figure 4)	1.47		1.75	V
Short-to-Battery Threshold	V_{TE}	(Figure 4)	2.47			V

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Worst-Case Supply Current (Figure 5)	I_{WCS}	$f_{PCLKOUT}$ = 116MHz, BWS = 0, double output, AVDD + DVDD (1.9V)		95	115	
		$f_{PCLKOUT}$ = 116MHz, BWS = 0, double output, IOVDD (1.9V) C_L = 5pF (DCS = 0) (Note 3)		22	25	
		$f_{PCLKOUT}$ = 116MHz, BWS = 0, double output, IOVDD (1.9V), C_L = 10pF (DCS = 1) (Note 3)		31	35	
		$f_{PCLKOUT}$ = 116MHz, BWS = 0, double output, IOVDD (3.6V), C_L = 5pF (DCS = 0) (Note 3)		44	49	
		$f_{PCLKOUT}$ = 116MHz, BWS = 0, double output, IOVDD (3.6V), C_L = 10pF (DCS = 1) (Note 3)		63	70	
		$f_{PCLKOUT}$ = 87MHz, BWS = 1, double output, IOVDD (1.9V), AVDD + DVDD (1.9V)		95	115	
		$f_{PCLKOUT}$ = 87MHz, BWS = 1, double output, IOVDD (1.9V), C_L = 5pF (DCS = 0) (Note 3)		17	19	
		$f_{PCLKOUT}$ = 87MHz, BWS = 1, double output, IOVDD (1.9V), C_L = 10pF (DCS = 1) (Note 3)		24	27	
		$f_{PCLKOUT}$ = 87MHz, BWS = 1, double output, IOVDD (3.6V), C_L = 5pF (DCS = 0) (Note 3)		33	36	
		$f_{PCLKOUT}$ = 87MHz, BWS = 1, double output, IOVDD (3.6V), C_L = 10pF (DCS = 1) (Note 3)		44	49	
		$f_{PCLKOUT}$ = 58MHz, BWS = 0, single output, AVDD + DVDD (1.9V)		70	84	
		$f_{PCLKOUT}$ = 58MHz, BWS = 0, single output, IOVDD (1.9V), C_L = 5pF (DCS = 0) (Note 3)		11	13	
		$f_{PCLKOUT}$ = 58MHz, BWS = 0, single output, IOVDD (3.6V), C_L = 10pF (DCS = 1) (Note 3)		15	18	

DC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY (continued)						
Worst-Case Supply Current (Figure 5) (continued)	I_{WCS}	$f_{PCLKOUT}$ = 58MHz, BWS = 0, single output, IOVDD (3.6V), C_L = 5pF (DCS = 0) (Note 3)		22	25	mA
		$f_{PCLKOUT}$ = 58MHz, BWS = 0, single output, IOVDD (3.6V), C_L = 10pF (DCS = 1) (Note 3)		30	34	
		$f_{PCLKOUT}$ = 43.5MHz, BWS = 1, single output, AVDD + DVDD (1.9V)		70	84	
		$f_{PCLKOUT}$ = 43.5MHz, BWS = 1, single output, IOVDD (1.9V), C_L = 5pF (DCS = 0) (Note 3)		8	10	
		$f_{PCLKOUT}$ = 43.5MHz, BWS = 1, single output, IOVDD (1.9V), C_L = 10pF (DCS = 1) (Note 3)		12	14	
		$f_{PCLKOUT}$ = 43.5MHz, BWS = 1, single output, IOVDD (3.6V), C_L = 5pF (DCS = 0) (Note 3)		16	18	
		$f_{PCLKOUT}$ = 43.5MHz, BWS = 1, single output, IOVDD (3.6V), C_L = 10pF (DCS = 1) (Note 3)		22	25	
Sleep-Mode Supply Current	I_{CCS}	Wake-up receivers enabled		54	160	µA
		Wake-up receivers disabled		15	100	
Power-Down Supply Current	I_{CCZ}	PWDNB = low		15	100	µA
ESD PROTECTION						
IN+, IN- (Note 4)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±8		kV
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF, Contact discharge		±10		
		IEC 61000-4-2, R_D = 330Ω, C_S = 150pF, Air discharge		±15		
		ISO 10605, R_D = 2kΩ, C_S = 330pF, Contact discharge		±10		
		ISO 10605, R_D = 2kΩ, C_S = 330pF, Air discharge		±30		
All Other Pins (Note 5)	V_{ESD}	Human Body Model, R_D = 1.5kΩ, C_S = 100pF		±4		kV
		Machine Model		250		V

AC Electrical Characteristics

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL CLOCK OUTPUT (PCLKOUT)						
Clock Frequency	$f_{PCLKOUT}$	BWS = 1, DRS = 1, single output	6.25		12.5	MHz
		BWS = 0, DRS = 1, single output	8.33		16.66	
		BWS = 1, DRS = 0, single output	12.5		43.5	
		BWS = 0, DRS = 0, single output	16.66		58	
		BWS = 1, DRS = 0, double output	25		87	
		BWS = 0, DRS = 0, double output	33.33		116	
Data Valid Before Clock	t_{DVB}	PCLKOUT and DOUT_, DCS = 1, C_L = 10pF or DCS = 0, C_L = 5pF, nonstaggered DOUT_	0.4T	0.5T		ns
		PCLKOUT and DOUT_, DCS = 1, C_L = 10pF or DCS = 0, C_L = 5pF, staggered DOUT_	0.35T	0.4T		
Data Valid After Clock	t_{DVA}	PCLKOUT and DOUT_, DCS = 1, C_L = 10pF or DCS = 0, C_L = 5pF, nonstaggered DOUT_	0.35T	0.4T		ns
		PCLKOUT and DOUT_, DCS = 1, C_L = 10pF or DCS = 0, C_L = 5pF, staggered DOUT_	0.3T	0.35T		
Clock Jitter	t_J	RMS period jitter, spread off, 1.74Gbps PRBS pattern, UI = 1/$f_{PCLKOUT}$, DBL = 1, double output)		0.05		UI
		Period jitter; peak-to-peak, spread off, 1.74Gbps, PRBS pattern, UI = 1/$f_{PCLKOUT}$, DBL = 0, single output)		0.01		
I²C/UART PORT TIMING						
I²C/UART Bit Rate			9.6		1000	kbps
Output Rise Time	t_R	30% to 70%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
Output Fall Time	t_F	70% to 30%, C_L = 10pF to 100pF, 1kΩ pullup to IOVDD	20		150	ns
I²C TIMING (Figure 6)						
SCL Clock Frequency	f_{SCL}	Low f_{SCL} range: (I2CMSTBT = 010, I2CSLVSH = 10)	9.6		100	kHz
		Mid f_{SCL} range: (I2CMSTBT 101, I2CSLVSH = 01)	>100		400	
		High f_{SCL} range: (I2CMSTBT = 111, I2CSLVSH = 00)	>400		1000	

AC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
START Condition Hold Time	$t_{HD:STA}$	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Low Period of SCL Clock	t_{LOW}	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	1.3			
		f_{SCL} range, High	0.5			
High Period of SCL Clock	t_{HIGH}	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Repeated START Condition Setup Time	$t_{SU:STA}$	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Data Hold Time	$t_{HD:DAT}$	f_{SCL} range, Low	0			ns
		f_{SCL} range, Mid	0			
		f_{SCL} range, High	0			
Data Setup Time	$t_{SU:DAT}$	f_{SCL} range, Low	250			ns
		f_{SCL} range, Mid	100			
		f_{SCL} range, High	50			
Setup Time for STOP Condition	$t_{SU:STO}$	f_{SCL} range, Low	4			µs
		f_{SCL} range, Mid	0.6			
		f_{SCL} range, High	0.26			
Bus Free Time	t_{BUF}	f_{SCL} range, Low	4.7			µs
		f_{SCL} range, Mid	1.3			
		f_{SCL} range, High	0.5			
Data Valid Time	$t_{VD:DAT}$	f_{SCL} range, Low			3.45	µs
		f_{SCL} range, Mid			0.9	
		f_{SCL} range, High			0.45	
Data Valid Acknowledge Time	$t_{VD:ACK}$	f_{SCL} range, Low			3.45	µs
		f_{SCL} range, Mid			0.9	
		f_{SCL} range, High			0.45	
Pulse Width of Spikes Suppressed	t_{SP}	f_{SCL} range, Low			50	ns
		f_{SCL} range, Mid			50	
		f_{SCL} range, High			50	
Capacitive load each bus line	C_B				100	pF

AC Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.7 to 1.9V, V_{IOVDD} = 1.7V to 3.6V, R_L = 100Ω ±1% (differential), EP connected to PCB ground, T_A = -40°C to +115°C, Typical values are at, V_{DVDD} = V_{AVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS (Note 3)						
PCLKOUT Rise-and-Fall Time (Figure 7)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V, DCS = 1, C_L = 10pF	0.4		2.2	ns
		20% to 80%, V_{IOVDD} = 1.7V to 1.9V, DCS = 0, C_L = 5pF	0.5		2.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V, DCS = 1, C_L = 10pF	0.25		1.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V, DCS = 0, C_L = 5pF	0.3		2	
Parallel Data Rise-and-Fall Time (Figure 7)	t_R, t_F	20% to 80%, V_{IOVDD} = 1.7V to 1.9V, DCS = 1, C_L = 10pF	0.5		3.1	ns
		20% to 80%, V_{IOVDD} = 1.7V to 1.9V, DCS = 0, C_L = 5pF	0.6		3.8	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V, DCS = 1, C_L = 10pF	0.3		2.2	
		20% to 80%, V_{IOVDD} = 3.0V to 3.6V, DCS = 0, C_L = 5pF	0.4		2.4	
Deserializer Delay	t_{SD}	(Figure 8) (Note 6)			2160	Bits
Reverse Control-Channel Output Rise Time	t_R	No forward-channel data transmission	180		400	ns
Reverse Control-Channel Output Fall Time	t_F	No forward-channel data transmission	180		400	ns
GPI-to-GPO Delay	t_{GPIO}	Deserializer GPI to serializer GPO (Figure 9)			350	µs
Lock Time (Note 3)	t_{LOCK}	(Figure 10) AEQ on			1.6	ms
		(Figure 10) AEQ off			1	
Power-Up Time	t_{PU}	(Figure 11)			6.5	ms
Active Output to High-Impedance Time	t_{OAZ}	(Figure 12, Figure 13) CC write OUTENB =1			250	ns
Active High-Impedance to Output Time	t_{OZA}	(Figure 12, Figure 13) CC write OUTENB =0			250	ns

Note 1: Limits are 100% production tested at T_A = +115°C. Limits over the operating temperature range are guaranteed by design and characterization, unless otherwise noted.

Note 2: I_{IN} min is due to voltage drop across the internal pullup resistor.

Note 3: Not production tested. Guaranteed by design.

Note 4: Specified pin to ground.

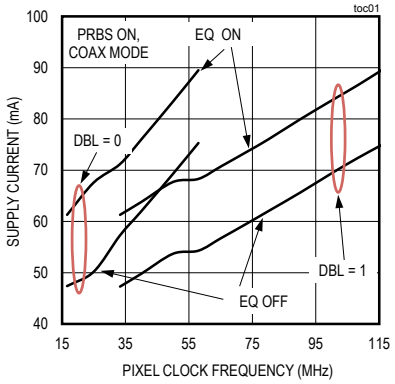
Note 5: Specified pin to all supply/ground.

Note 6: Measured in serial link bit times. Bit time = 1/(30 x $f_{PCLKOUT}$) for BWS = GND. Bit time = 1/(40 x $f_{PCLKOUT}$) for BWS = 1.

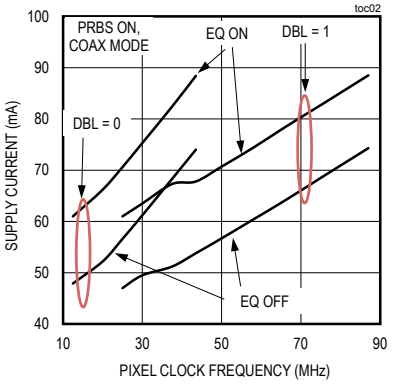
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{IOVDD} = 1.8V, T_A = +25°C, unless otherwise noted.)

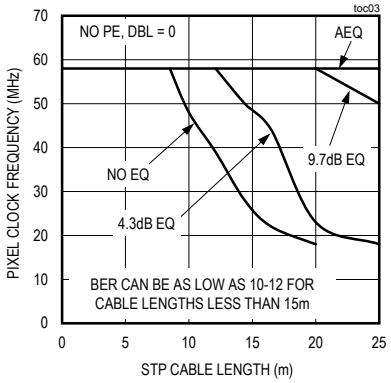
**SUPPLY CURRENT vs.
PIXEL CLOCK FREQUENCY (BWS = 0)**



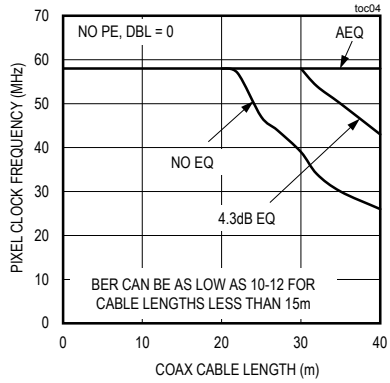
**SUPPLY CURRENT vs.
PIXEL CLOCK FREQUENCY (BWS = 1)**



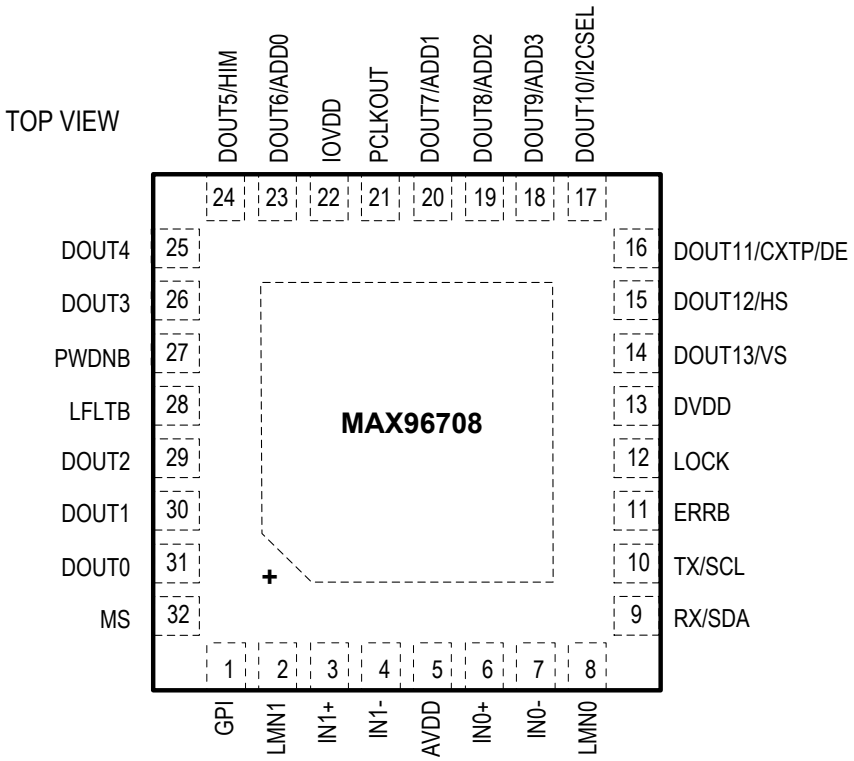
**MAXIMUM PIXEL CLOCK FREQUENCY vs.
STP CABLE LENGTH (BER < 10^{-10})**



**MAXIMUM PIXEL CLOCK FREQUENCY vs.
COAX CABLE LENGTH (BER < 10^{-10})**



Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
POWER				
5	AVDD	1.8V Analog Power Supply. Bypass AVDD to EP with 0.1µF and 0.001µF capacitors placed as close as possible to the device, with the smaller-value capacitor closest to AVDD.		Power
13	DVDD	1.8V Digital Power Supply. Bypass DVDD to EP with 0.1µF and 0.001µF capacitors placed as close as possible to the device, with the smaller-value capacitor closest to DVDD.		Power
22	IOVDD	I/O Supply Voltage. 1.8V to 3.3V logic I/O power supply. Bypass IOVDD to EP with 0.1µF and 0.001µF capacitors placed as close as possible to the device, with the smaller-value capacitor closest to IOVDD.		Power
EP	—	Exposed Pad. EP is internally connected to device ground. Must connect EP to the PCB ground plane through a via array for proper thermal and electrical performance.		Power
HIGH-SPEED DIGITAL				
High-Speed Digital / Multifunction				
14	DOUT13/VS	Parallel-Data/Vertical-Sync Output. Defaults to parallel-data output on power-up. Vertical-sync output when HS/VS encoding is enabled.	IOVDD	Digital
15	DOUT12/HS	Parallel-Data/Horizontal-Sync Output. Defaults to parallel-data output on power-up. Horizontal-sync output when HS/VS encoding is enabled.	IOVDD	Digital
16	DOUT11/ CXTP/DE	Parallel-Data Output/Cable-Type Input/Data-Enable Output with internal pulldown to EP. CX/TP is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel/data-enable output after power-up. Connect CXTP to IOVDD with a 30kΩ resistor to set high (coax mode), or leave open to set low (twisted-pair mode).	IOVDD	Digital
17	DOUT10/ I2CSEL	Parallel-Data Output/I^2C-Select Input with Internal Pulldown to EP. I2CSEL is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect I2CSEL to IOVDD with a 30kΩ resistor to set high (I^2C interface), or leave open to set low (UART interface).	IOVDD	Digital
18	DOUT9/ ADD3	Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD3 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD3 to IOVDD with a 30kΩ resistor to set high, or leave open to set low.	IOVDD	Digital
19	DOUT8/ ADD2	Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD2 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD2 to IOVDD with a 30kΩ resistor to set high, or leave open to set low.	IOVDD	Digital

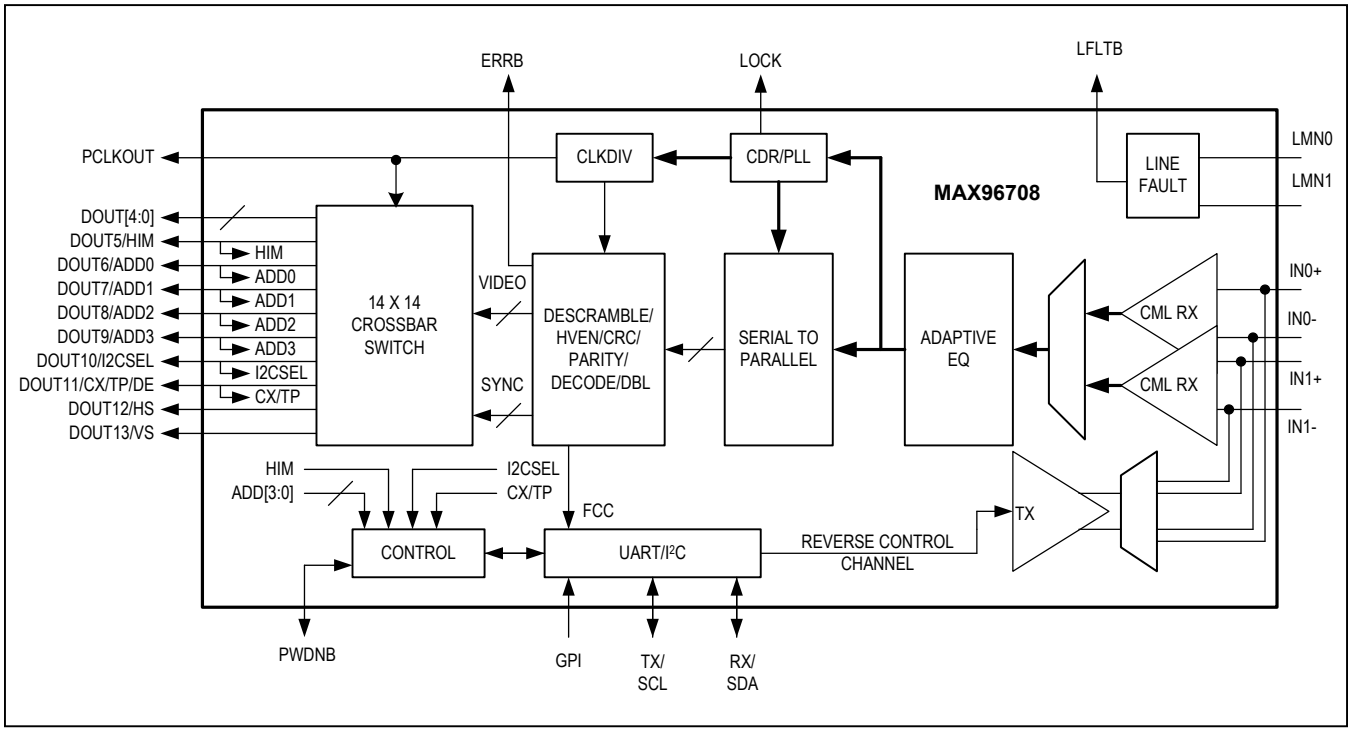
Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
20	DOUT7/ ADD1	Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD1 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD1 to IOVDD with a 30kΩ resistor to set high, or leave open to set low.	IOVDD	Digital
23	DOUT6/ ADD0	Parallel-Data Output/Address Input with Internal Pulldown to EP. ADD0 is latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect ADD0 to IOVDD with a 30kΩ resistor to set high, or leave open to set low.	IOVDD	Digital
24	DOUT5/HIM	Parallel-Data Output/High-Immunity Mode Input with Internal Pulldown to EP. HIM input latched at power-up, or when resuming from power-down mode (PWDNB = low), and switches to parallel-data output after power-up. Connect HIM to IOVDD with a 30kΩ resistor to set high, or leave open to set low. HIGHIMM in the serializer must be set to the same value.	IOVDD	Digital
High-Speed Digital / Single Function				
21	PCLKOUT	Parallel-Clock Output. Provides timing signal to latch parallel-data outputs to the input of another device.	IOVDD	Digital
25	DOUT4	Parallel-Data Output	IOVDD	Digital
26	DOUT3	Parallel-Data Output	IOVDD	Digital
29	DOUT2	Parallel-Data Output	IOVDD	Digital
30	DOUT1	Parallel-Data Output	IOVDD	Digital
31	DOUT0	Parallel-Data Output	IOVDD	Digital
LINE FAULT				
2	LMN1	Line-Fault Monitor Input 1 (see Figure 4)		Analog
8	LMN0	Line-Fault Monitor Input 0 (see Figure 4)		Analog
28	LFLTB	Line-Fault Output. LFLTB is active low, and has a 60kΩ internal pullup to IOVDD. LFLTB low indicates a line-fault condition at LMN0, or LMN1. LFLTB is output high when PWDNB is low.	IOVDD	Digital
OTHER PINS				
1	GPI	General-Purpose Input with Internal Pulldown to EP. Serializer GPO (or INT) output follows the state of the GPI.	IOVDD	Digital
3	IN1+	Noninverting CML Serial-Data Input 1. Coax input when CXTP is high.		
4	IN1-	Inverting CML Serial-Data Input 1		
6	IN0+	Noninverting CML Serial-Data Input 0. Coax input when CXTP is high.		
7	IN0-	Inverting CML Serial-Data Input 0		
9	RX/SDA	Receive/Serial Data. Input/output with internal 30kΩ pullup to IOVDD. In UART mode, RX/SDA is the Rx input of the serializer's UART. In I^2C mode, RX/SDA is the SDA input/output of the serializer's I^2C master/slave. RX/SDA has an open-drain driver and requires a pullup resistor.	IOVDD	Digital

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
10	TX/SCL	Transmit/Serial Clock. Input/output with internal 30kΩ pullup to IOVDD. In UART mode, TX/SCL is the Tx output of the serializer's UART. In I²C mode, TX/SCL is the SCL input/output of the serializer's I²C master/slave. TX/SCL has an open-drain driver and requires a pullup resistor.	IOVDD	Digital
11	ERRB	Error Output. Active-low, open-drain video data error output with internal pullup to IOVDD. ERRB goes low when decoding errors during normal operation exceed a programmed threshold, or when at least one PRBS error is detected during a PRBS test. ERRB is output high when PWDNB is low.	IOVDD	Digital
12	LOCK	Lock Output. Open-drain output with internal pullup to IOVDD. LOCK high indicates PLLs are locked with correct serial-word boundary alignment. LOCK low indicates PLLs are not locked, or incorrect serial-word boundary alignment. LOCK is low when the configuration link is active. LOCK is output high when PWDNB is low.	IOVDD	Digital
27	PWDNB	Active-Low, Power-Down Input with Internal Pulldown to EP. Set PWDNB low to enter power-down mode to reduce power consumption.	IOVDD	Digital
32	MS	Mode-Select Input with Internal Pulldown to EP. Set MS low to select base mode. Set MS high to select bypass mode.	IOVDD	Digital

Functional Diagrams



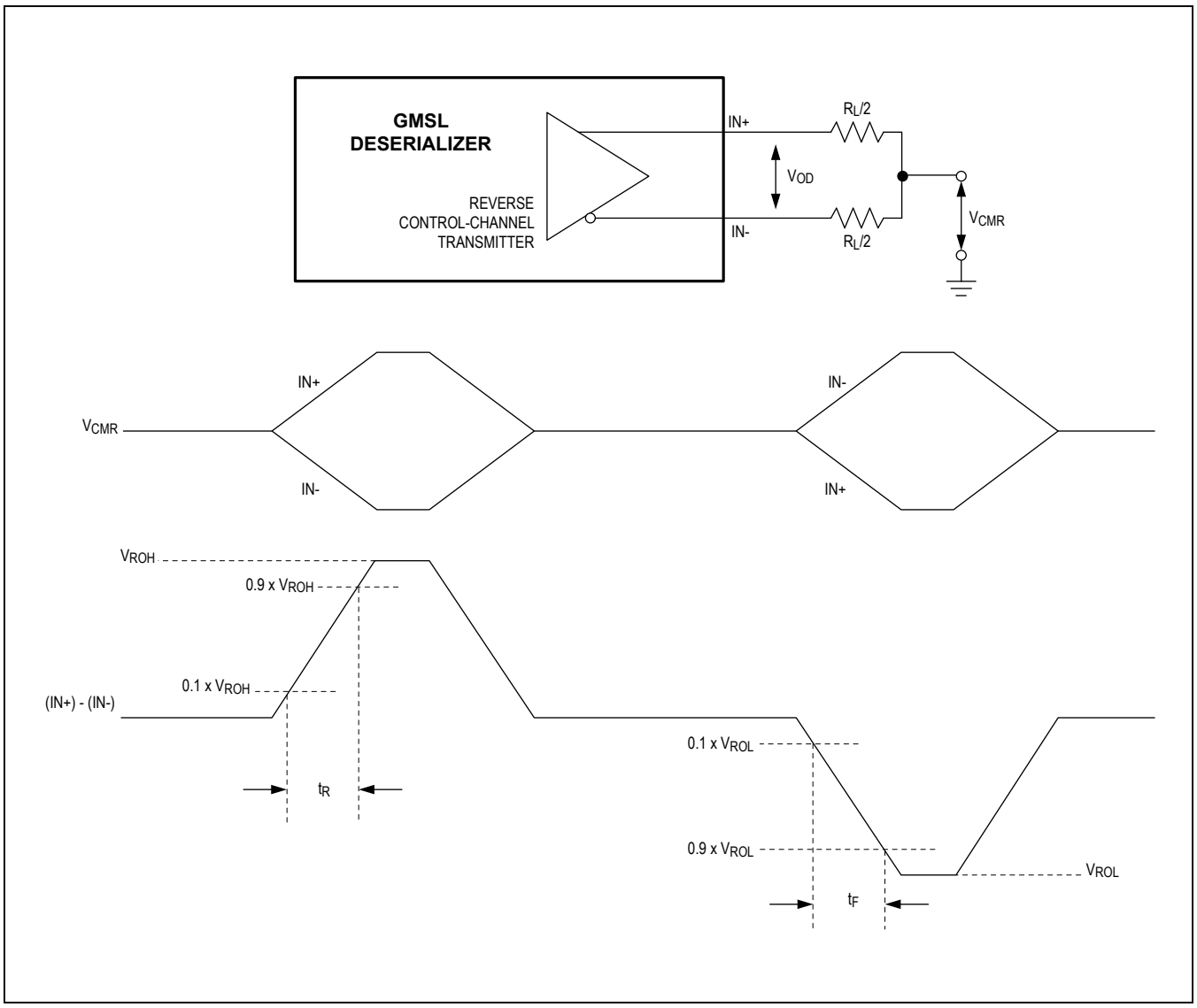


Figure 1. Reverse Control-Channel Output Parameters

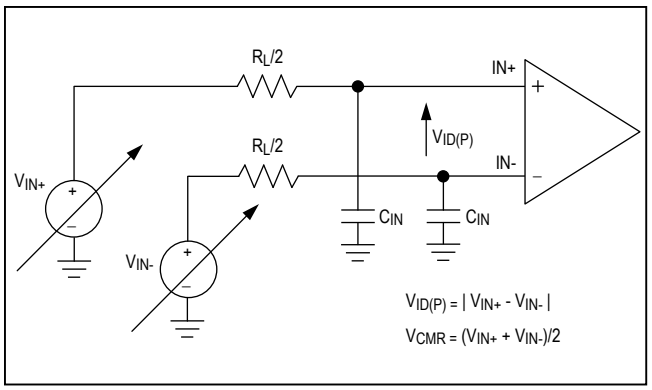


Figure 2. Test Circuit for Differential Input Measurement

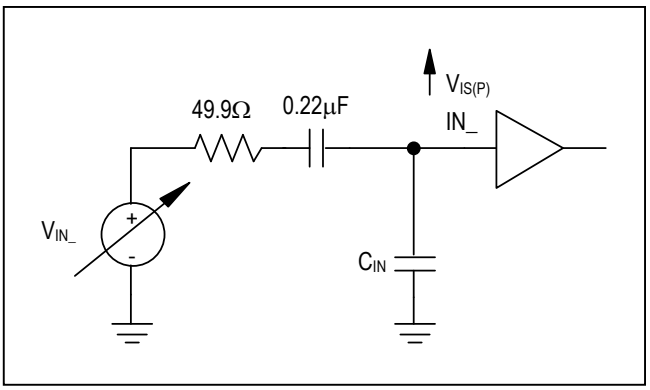


Figure 3. Test Circuit for Single-Ended Input Measurement

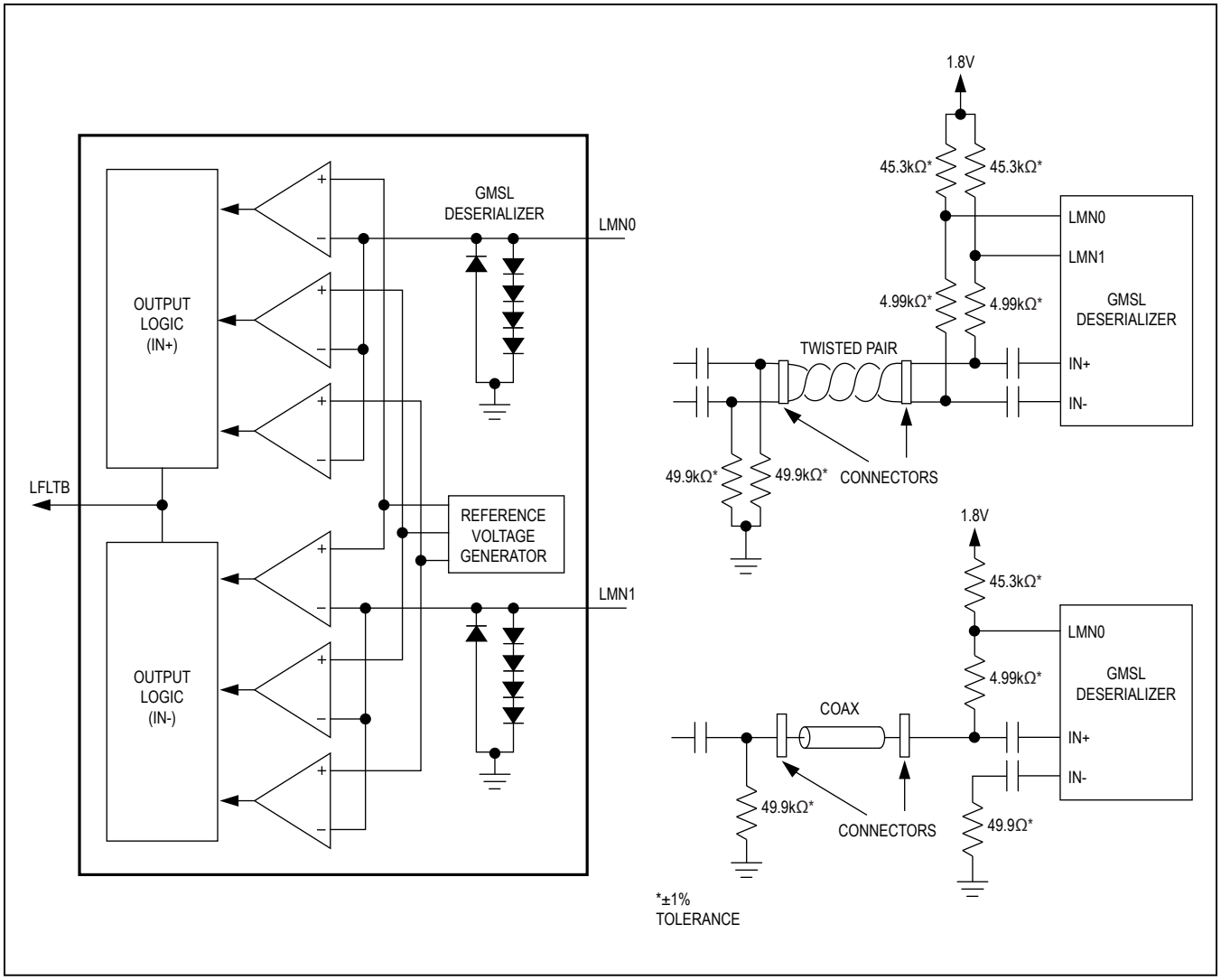


Figure 4. Line Fault

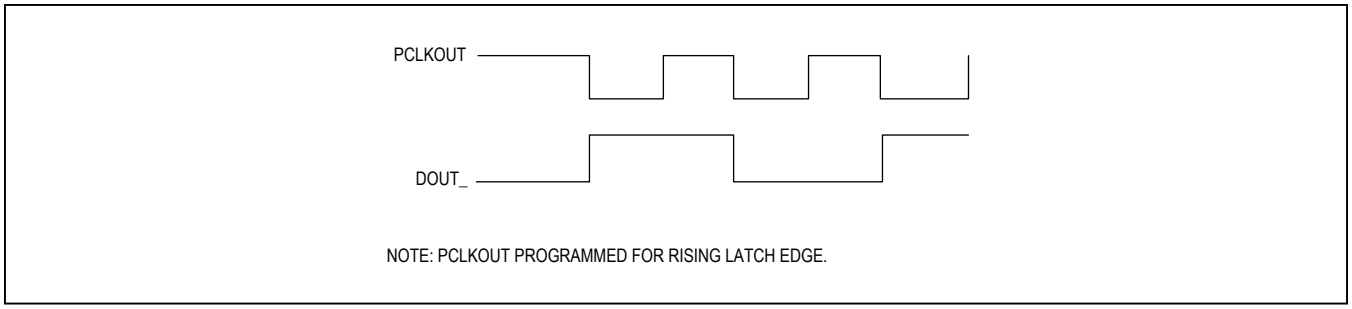


Figure 5. Worst-Case Pattern Output

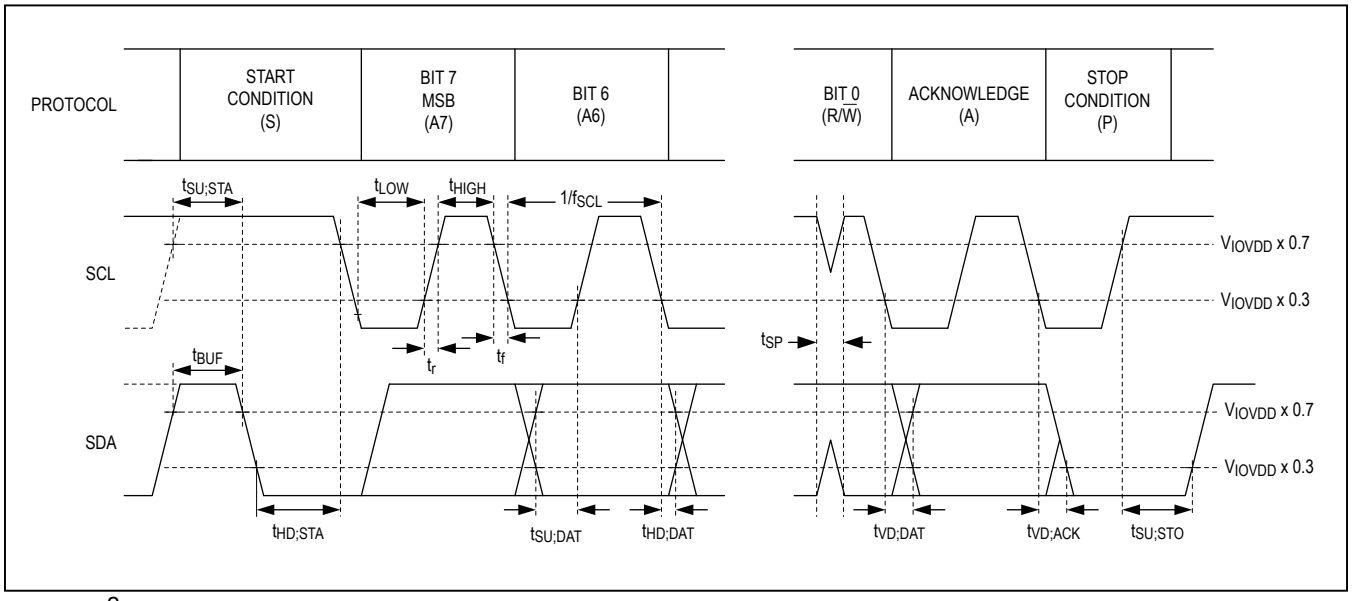


Figure 6. I^2C Timing Parameters

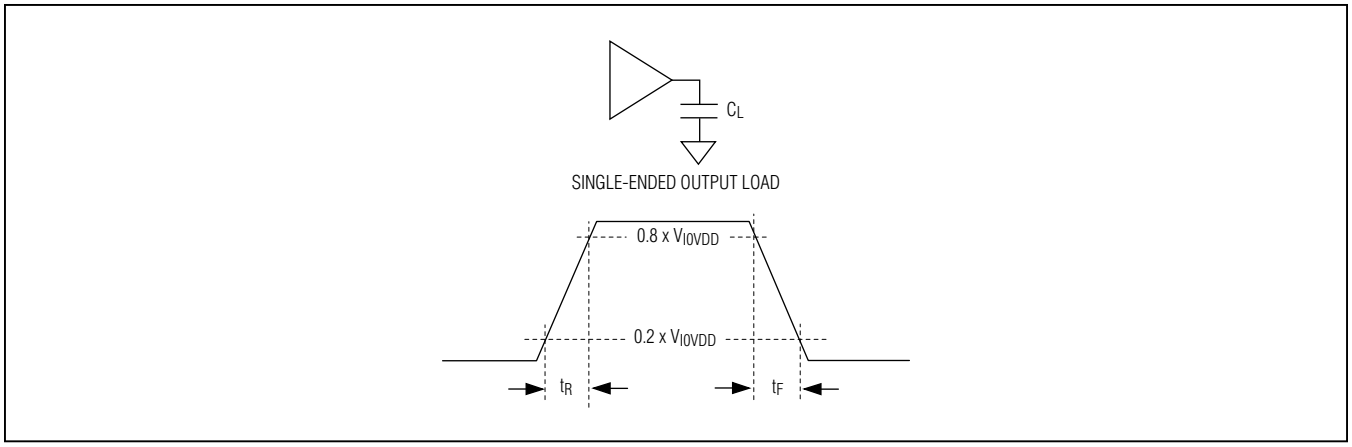


Figure 7. Output Rise-and-Fall Times

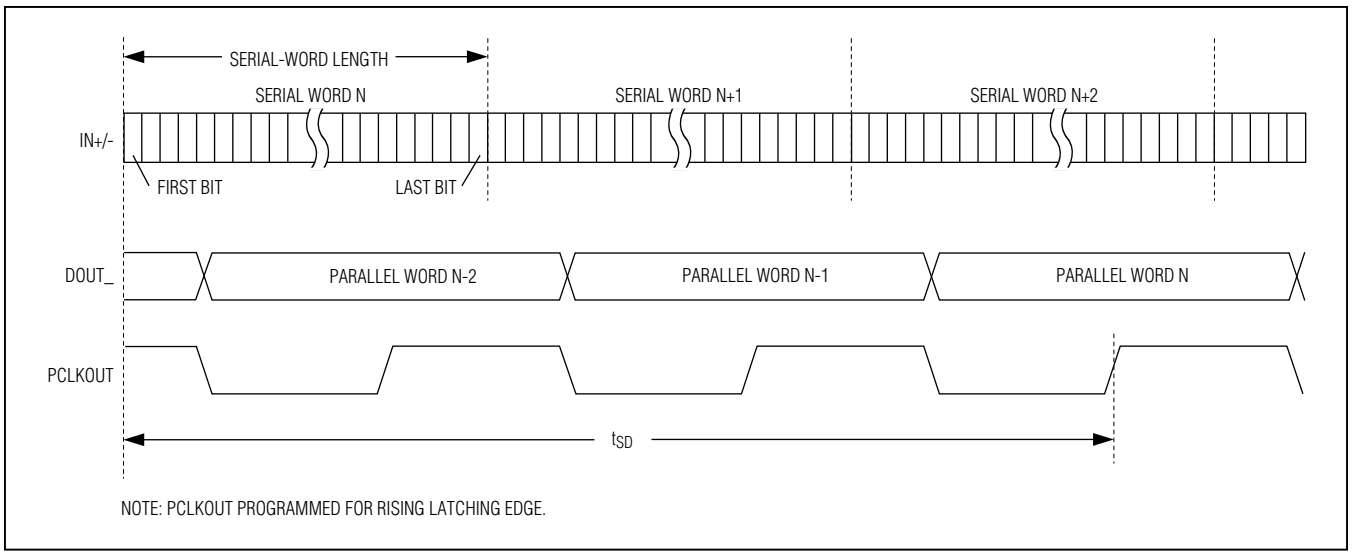


Figure 8. Deserializer Delay

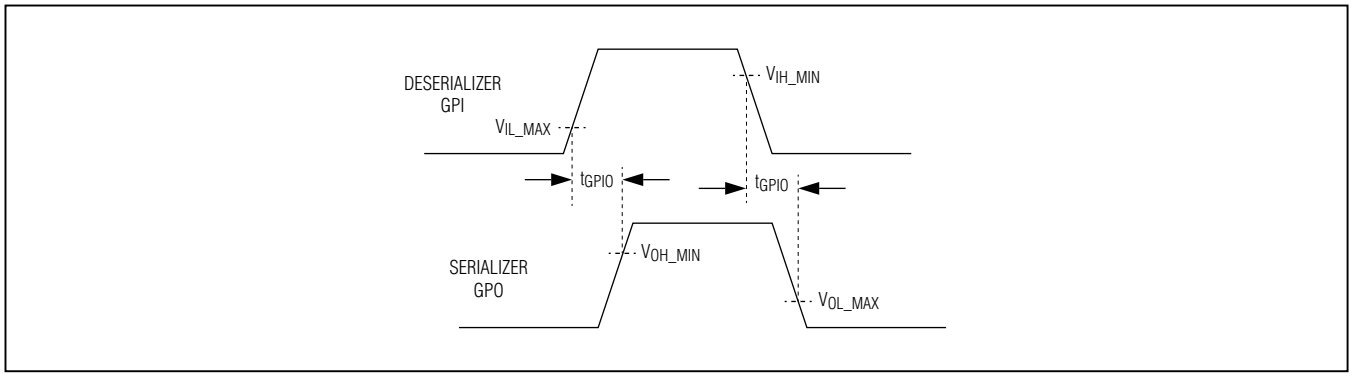


Figure 9. GPI-to-GPO Delay

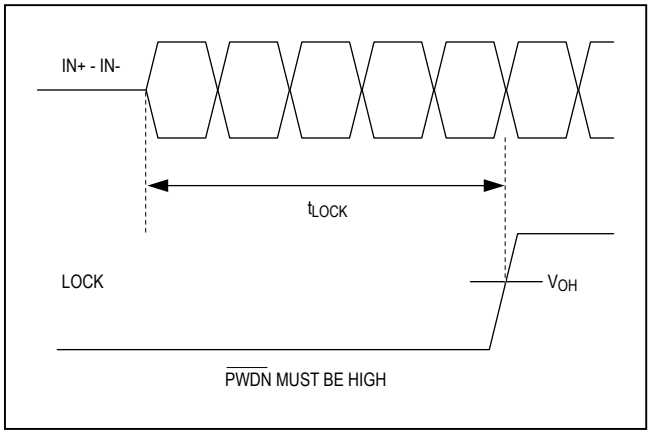


Figure 10. Lock Time

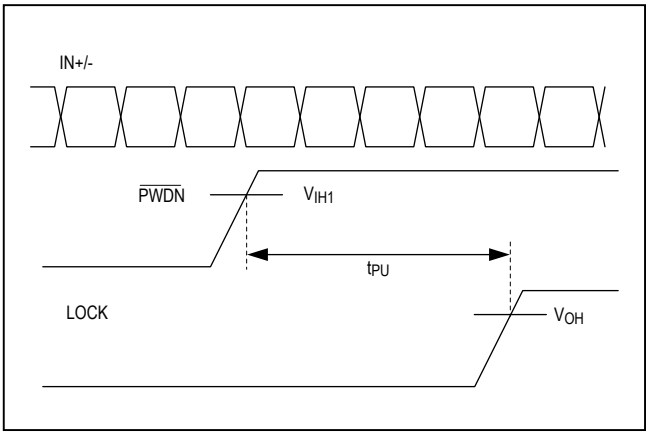


Figure 11. Power-Up Delay

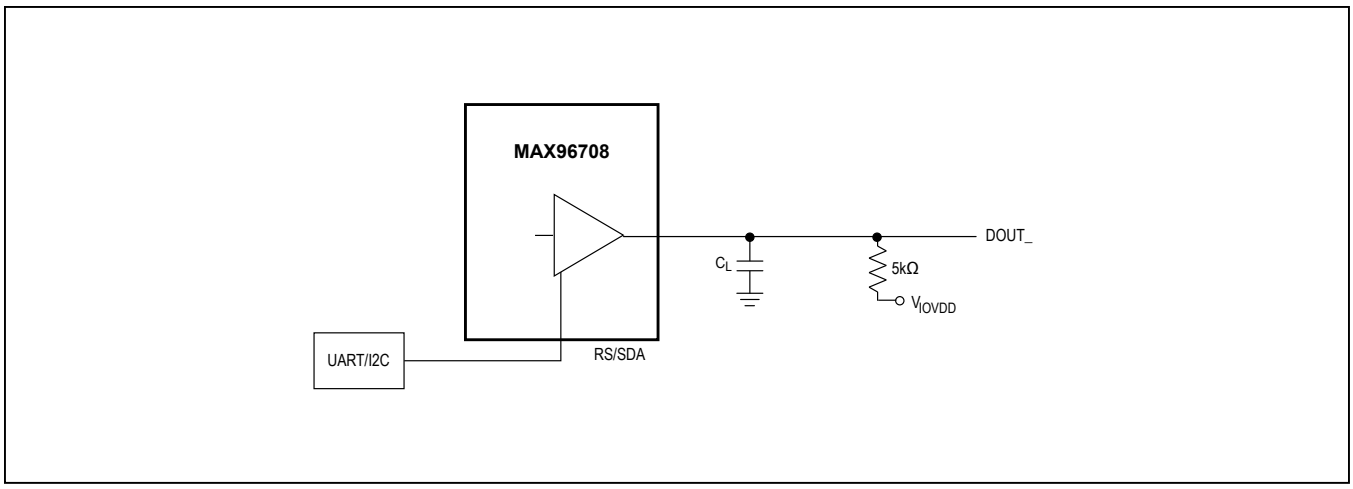


Figure 12. Active Output to High-Impedance Time, High Impedance to Active-Output Time Test Circuit

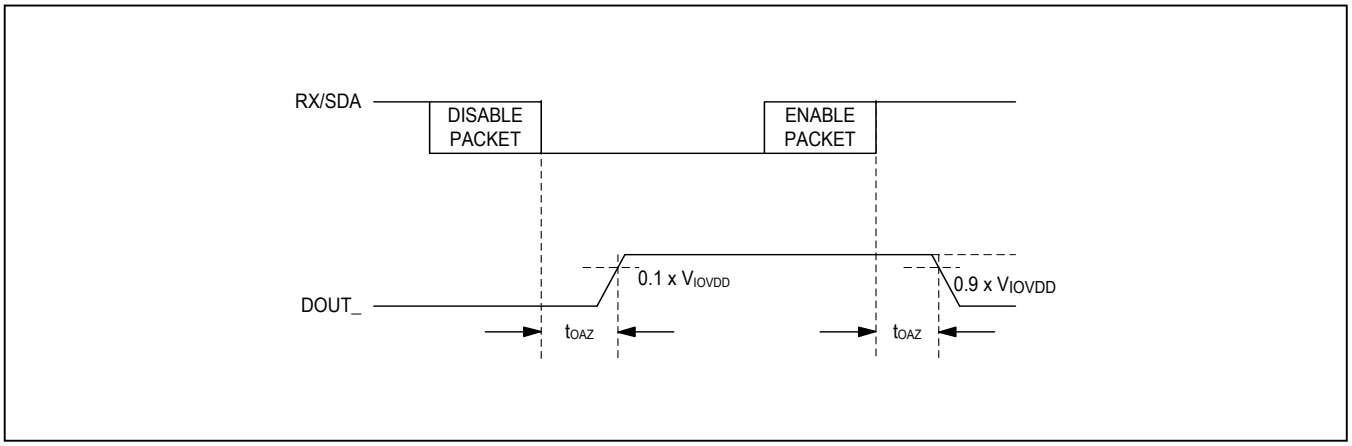


Figure 13. Active Output to High-Impedance Time, High Impedance to Active-Output Time