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19-5130; Rev 1; 7/10

EVALUATION KIT AVAILABLE

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

General Description

The MAX97001 mono audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier and an analog DPST switch. The headphone and speaker amplifiers have independent volume control and on/off control. The 4 inputs are configurable as 2 differential inputs or 4 single-ended inputs.

The entire subsystem is designed for maximum efficiency. The high-efficiency, 700mW, Class D speaker amplifier operates directly from the battery and consumes no more than 1µA in shutdown mode. The Class H headphone amplifier utilizes a dual-mode charge pump to maximize efficiency while outputting a ground-referenced signal that does not require output coupling capacitors.

The speaker amplifier incorporates a distortion limiter to automatically reduce the volume level when excessive clipping occurs. This allows high gain for low-level signals without compromising the quality of large signals.

All control is performed using the 2-wire I²C interface. The MAX97001 operates over the extended -40°C to +85°C temperature range, and is available in the 2mm x 2.5mm, 20-bump, WLP package (0.5mm pitch).

Applications

Cell Phones

Portable Multimedia Players

Features

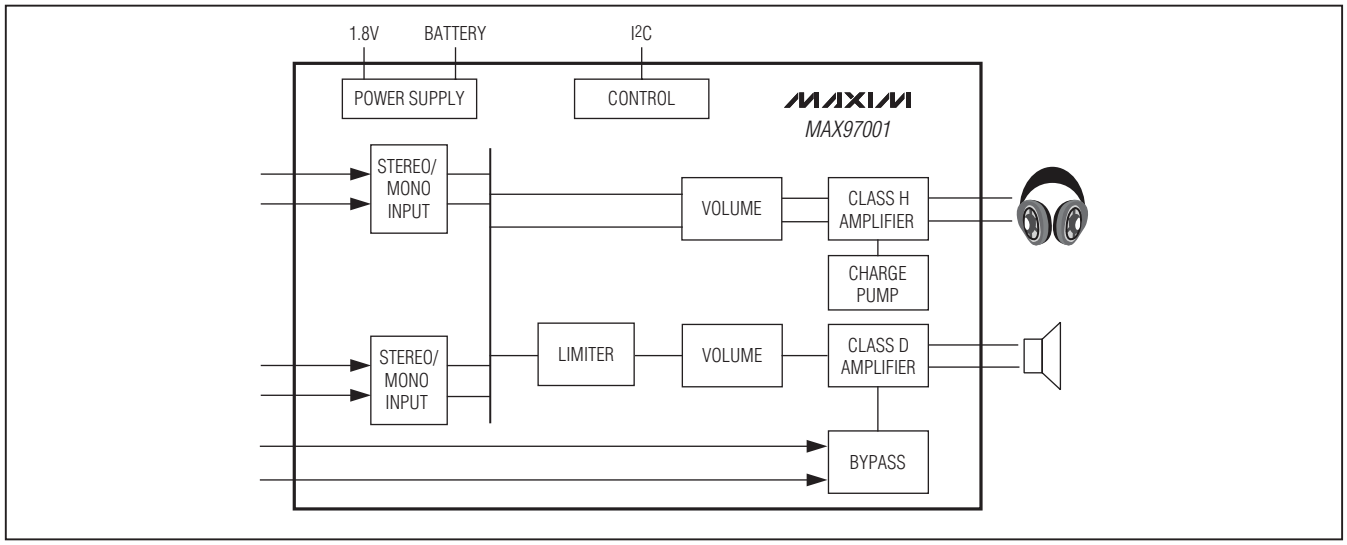
- **2.7V to 5.5V Speaker Supply Voltage**
- **1.6V to 2V Headphone Supply Voltage**
- **700mW Speaker Output (V_{PVDD} = 3.7V, Z_{SPK} = 8Ω + 68µH)**
- **37mW/Channel Headphone Output (R_{HP} = 16Ω)**
- **Low-Emission Class D Amplifier**
- **Efficient Class H Headphone Amplifier**
- **Ground-Referenced Headphone Outputs**
- **2 Stereo Single-Ended/Mono Differential Inputs**
- **Integrated Distortion Limiter (Speaker Outputs)**
- **Integrated DPST Analog Switch**
- **No Clicks and Pops**
- **TDMA Noise Free**
- **2mm x 2.5mm, 20-Bump, 0.5mm Pitch WLP Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX97001EWP+	-40°C to +85°C	20 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Simplified Block Diagram



Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

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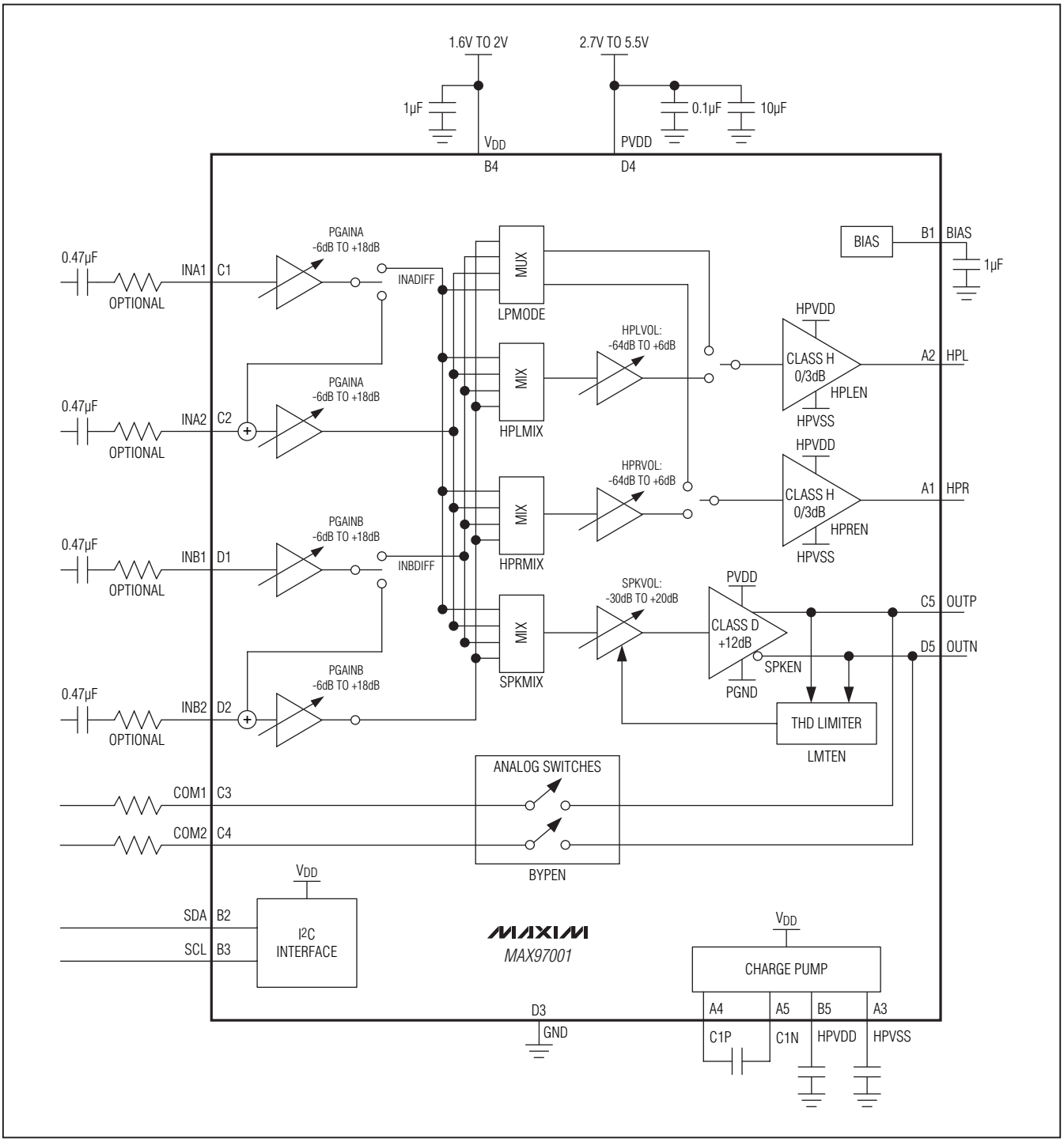
Functional Diagram/Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to GND.)

V_{DD}, HPVDD .....-0.3V to +2.2V
PVDD .....-0.3V to +6.0V
HPVSS .....-2.2V to +0.3V
C1N .....(HPVSS - 0.3V) to (HPVDD + 0.3V)
C1P.....-0.3V to (HPVDD + 0.3V)
HPL, HPR .....(HPVSS - 0.3V) to (HPVDD + 0.3V)
INA1, INA2, INB1, INB2, BIAS .....-0.3V to +6.0V
SDA, SCL .....-0.3V to +6.0V
COM1, COM2, OUTP, OUTN.....-0.3V to (PVDD + 0.3V)
Continuous Current In/Out of PVDD, GND, OUT_ ..... ±800mA
Continuous Current In/Out of HPR, HPL, V_{DD}..... ±140mA
Continuous Current In/Out of COM1, COM2 ..... ±150mA
Continuous Input Current (all other pins)..... ±20mA
Duration of OUT_ Short Circuit to GND or PVDD .....Continuous
Duration of Short Circuit Between
OUTP and OUTN.....Continuous
Duration of HP_ Short Circuit to GND or V_{DD}.....Continuous
Continuous Power Dissipation (T_A = +70°C)
20-Bump WLP Multilayer Board
(derate 13mW/°C above +70°C).....1040mW
Junction Temperature .....+150°C
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Speaker Amplifier Supply Voltage Range	PVDD	Guaranteed by PSRR test		2.7		5.5	V
Headphone Amplifier Supply Voltage Range	V_{DD}	Guaranteed by PSRR test		1.6		2	V
Quiecsent Supply Current		Low-power headphone mode, T_A = +25°C	I_{VDD}		1.35	1.85	mA
			I_{PVDD}		0.35	0.55	
		HP mode, T_A = +25°C, stereo SE input on INA, INB disabled	I_{VDD}		1.35	1.85	
			I_{PVDD}		0.75	1.15	
		SPK mode, T_A = +25°C mono differential Input on INB, INA disabled	I_{VDD}		0.32	0.6	
			I_{PVDD}		1.38	2.2	
		SPK + HP mode, T_A = +25°C, stereo SE input on INA, INB disabled	I_{VDD}		1.35	1.85	
			I_{PVDD}		1.8	2.7	
Shutdown Current	I_{SHDN}	T_A = +25°C, $V_{\overline{SHDN}}$ = 0V	I_{VDD} + I_{PVDD}			8	µA
			V_{VDD} = 0V, I_{PVDD}		< 1		
Turn-On Time	t_{ON}	Time from power-on to full operation, including soft-start			10		ms
Input Resistance	R_{IN}	T_A = +25°C, internal gain	Gain = -6dB, -3dB		41.2		kΩ
			Gain = 0dB, 3dB, 6dB, 9dB	16	20.6	27	
			Gain = +18dB	5.5	7.2	9.6	

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Resistance	R_F	T_A = +25°C, external gain		19	20	21	kΩ
Maximum Input Signal Swing		Preamp = 0dB			2.3		V_{P-P}
		Preamp = +18dB			0.29		
		Preamp = external gain			2.3 x RINEX/RF		
Common-Mode Rejection Ratio	CMRR	f = 1kHz (differential input mode), gain = 0dB			55		dB
		f = 1kHz (differential input mode), gain = 18dB			32		
Input DC Voltage		IN__ inputs		1.125	1.2	1.275	V
Bias Voltage	V_{BIAS}			1.13	1.2	1.27	V
SPEAKER AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C, SPKM = 1			±0.5	±4	mV
		T_A = +25°C, SPKMIX = 0x01, IN_DIFF = 0			±1.5		
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, volume at mute (Note 2)	Into shutdown		-70		dBV
			Out of shutdown		-70		
Power-Supply Rejection Ratio (Note 2)	PSRR	T_A = +25°C	V_{PVDD} = 2.7V to 5.5V	50	77		dB
			f = 217Hz, 200mV_{P-P} ripple		73		
			f = 1kHz, 200mV_{P-P} ripple		73		
			f = 20kHz, 200mV_{P-P} ripple		57		
Output Power (Note 3)		THD+N ≤ 1%, f = 1kHz, Z_{SPK} = 8Ω + 68µH	V_{PVDD} = 4.2V		920		mW
			V_{PVDD} = 3.7V		700		
			V_{PVDD} = 3.3V		550		
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, P_{OUT} = 360mW, T_A = +25°C, R_{SPK} = 8Ω			0.05	0.6	%
Signal-to-Noise Ratio	SNR	A-weighted, SPKMIX = 0x03, referenced to 700mW	IN_DIFF = 0 (single-ended)		96		dB
			IN_DIFF = 1 (differential)		96		
Oscillator Frequency	f_{OSC}				250		kHz
Spread-Spectrum Bandwidth					±20		kHz
Gain				11.5	12	12.5	dB
Current Limit					1.5		A

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Efficiency	η	P_{OUT} = 600mW, f = 1kHz			87		%
Output Noise		A-weighted, (SPKMIX = 0x01), IN_DIFF = 1, SPKVOL = -30dB			37		$µV_{RMS}$
CHARGE PUMP							
Charge-Pump Frequency		V_{HPL} = V_{HPR} = 0V, T_A = +25°C		80	83	85	kHz
		V_{HPL} = V_{HPR} = 0.2V			665		
		V_{HPL} = V_{HPR} = 0.5V			500		
Positive Output Voltage	V_{HPVDD}	V_{HPL}, V_{HPR} > V_{TH}			V_{DD}		V
		V_{HPL}, V_{HPR} < V_{TH}			$V_{DD}/2$		
Negative Output Voltage	V_{HPVSS}	V_{HPL}, V_{HPR} > V_{TH}			$-V_{DD}$		V
		V_{HPL}, V_{HPR} < V_{TH}			$-V_{DD}/2$		
Headphone Output Voltage Threshold	V_{TH1}	Output voltage at which the charge pump switches between fast and slow clock		$±V_{DD}$ x 0.05	$±V_{DD}$ x 0.08	$±V_{DD}$ x 0.13	V
	V_{TH2}	Output voltage at which the charge pump switches modes, V_{OUT} rising or falling		$±V_{DD}$ x 0.21	$±V_{DD}$ x 0.25	$±V_{DD}$ x 0.3	
Mode Transition Timeouts		Time it takes for the charge pump to transition from Invert to split mode			32		ms
		Time it takes for the charge pump to transition from split to invert mode			20		µs
HEADPHONE AMPLIFIERS							
Output Offset Voltage	V_{OS}	T_A = +25°C, volume at mute			±0.15	±0.6	mV
		T_A = +25°C, HP_MIX = 0x1, IN_DIFF = 0			±0.5		
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, volume at mute (Note 2)	Into shutdown		-74		dBV
			Out of shutdown		-74		
Power-Supply Rejection Ratio (Note 2)	PSRR	T_A = +25°C	V_{DD} = 1.62V to 1.98V	70	85		dB
			f = 217Hz, V_{RIPPLE} = $200mV_{P-P}$		84		
			f = 1kHz, V_{RIPPLE} = $200mV_{P-P}$		80		
			f = 20kHz, V_{RIPPLE} = $200mV_{P-P}$		69		

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power	P_{OUT}	THD+N = 1%, f = 1kHz	R_{HP} = 16Ω		37		mW
			R_{HP} = 32Ω		30		
Channel-to-Channel Gain Tracking		T_A = +25°C, HPL to HPR, HPLMIX = 0x01, HPRMIX = 0x02, IN_DIFF = 0			±0.3	±2.5	%
Total Harmonic Distortion Plus Noise	THD+N	P_{OUT} = 10mW, f = 1kHz	R_{HP} = 32Ω		0.02		%
			R_{HP} = 16Ω		0.03	0.1	
Signal-to-Noise Ratio	SNR	A-weighted, R_{HP} = 16Ω, HPLMIX = 0x01, HPRMIX = 0x02, IN_DIFF = 0			100		dB
Slew Rate	SR				0.35		V/µs
Capacitive Drive	C_L				200		pF
Crosstalk		HPL to HPR, HPR to HPL, f = 20Hz to 20kHz			68		dB
ANALOG SWITCH							
On-Resistance	R_{ON}	$I_{NC\_}$ = 20mA, $V_{COM\_}$ = 0V and PVDD, SWEN = 1	T_A = +25°C		1.6	4	Ω
			T_A = T_{MIN} to T_{MAX}			5.2	
Total Harmonic Distortion Plus Noise	THD+N	$V_{DIFCOM\_}$ = $2V_{P-P}$, $V_{CMCOM\_}$= $PV_{DD}/2$, f = 1kHz, SWEN = 1, Z_{SPK} = 8Ω + 68µH	10Ω in series with each switch		0.05		%
			No series resistors		0.3		
Off-Isolation		SWEN = 0, COM1 and COM2 to GND = 50Ω, f = 10kHz, referred to signal applied to OUTP and OUTN			90		dB
PREAMPLIFIER							
Gain		PGAIN_ = 000		-6.5	-6	-5.5	dB
		PGAIN_ = 001		-3.5	-3	-2.5	
		PGAIN_ = 010		-0.5	0	+0.5	
		PGAIN_ = 011		2.5	3	3.5	
		PGAIN_ = 100		5.5	6	6.5	
		PGAIN_ = 101		8.5	9	9.5	
		PGAIN_ = 110		17.5	18	18.5	
VOLUME CONTROL							
Volume Level		HP_VOL = 0x1F		5.5	6	6.5	dB
		HP_VOL = 0x00		-68	-64	-60	
		SPKVOL = 0x3F		19	20	-21	
		SPKVOL = 0x00		-31	-30	-29	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 1.8V, V_{PVDD} = 3.7V, V_{GND} = 0V. Input signal applied at INA configured single-ended, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB, speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. SDA and SCL pullup voltage = 1.8V. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Mute Attenuation		f = 1kHz	Speaker		100		dB
			Headphone		110		
Zero-Crossing Detection Timeout					100		ms
LIMITER							
Attack Time					1		ms
Release Time Constant		THDT1 = 0			1.4		s
		THDT1 = 1			2.8		

DIGITAL I/O CHARACTERISTICS

(V_{PVDD} = 3.7V, V_{GND} = 0V. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL)						
Input Voltage High	V_{IH}		0.75 x V_{DD}			V
Input Voltage Low	V_{IL}				0.35 x V_{DD}	V
Input Hysteresis	V_{HYS}			200		mV
Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}	T_A = +25°C			±1.0	µA
DIGITAL OUTPUTS (SDA Open Drain)						
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

I²C TIMING CHARACTERISTICS

(V_{PVDD} = 3.7V, V_{GND} = 0V. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 4)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 4)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	(Note 4)	20 + 0.1C_B		300	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 1: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Amplifier inputs are AC-coupled to GND.
Note 3: Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load.
Note 4: C_B is in pF.

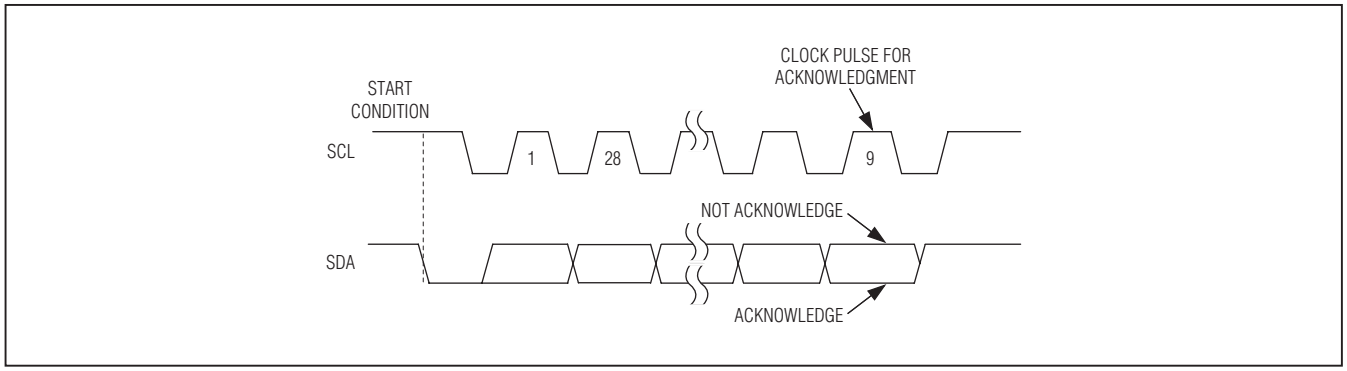


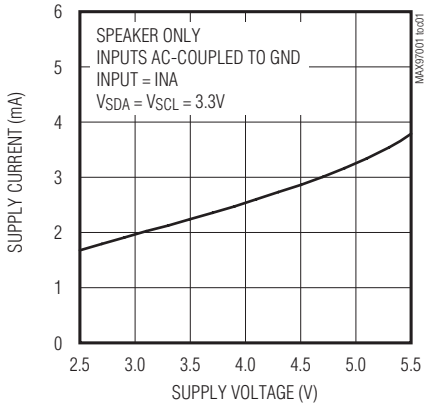
Figure 1. I²C Interface Timing Diagram

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

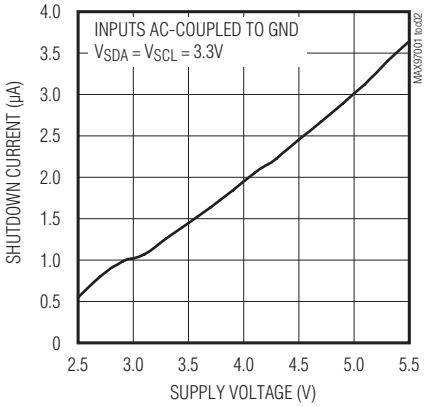
Typical Operating Characteristics

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

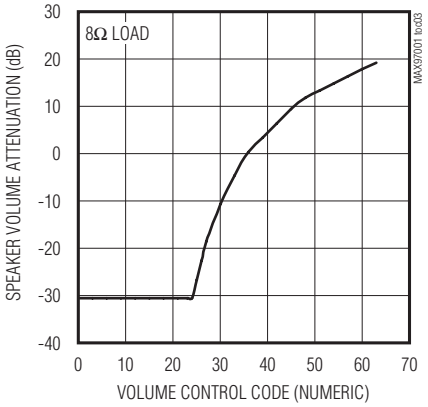
SUPPLY CURRENT vs. SUPPLY VOLTAGE



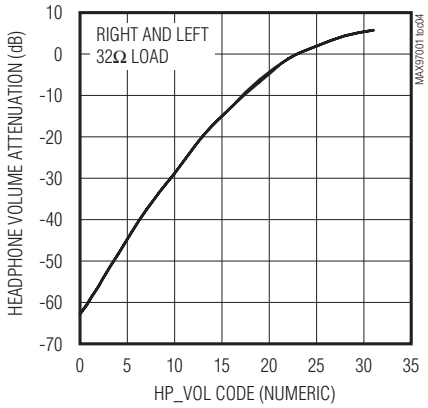
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



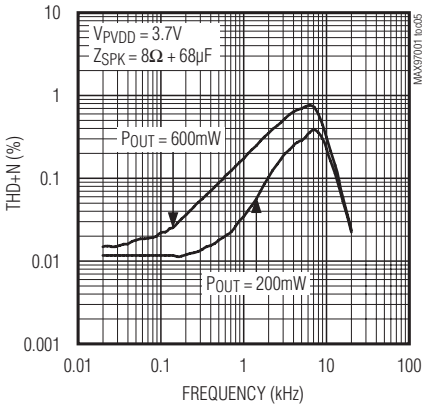
SPEAKER VOLUME ATTENUATION vs. VOLUME CONTROL CODE



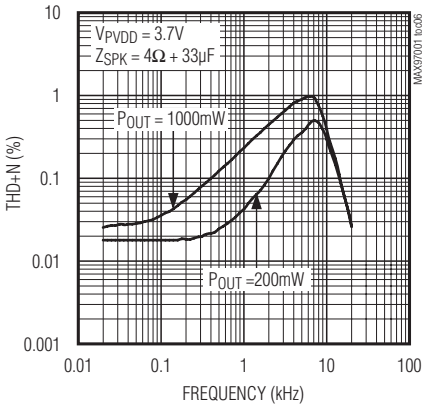
HEADPHONE VOLUME ATTENUATION vs. HP_VOL CODE



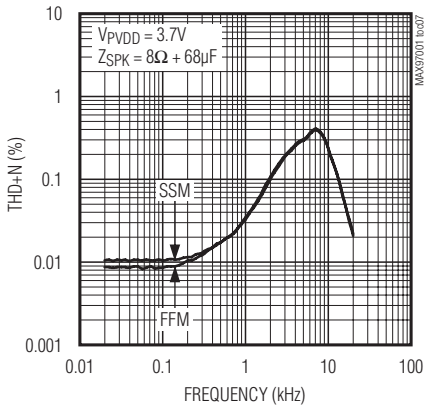
THD+N vs. FREQUENCY



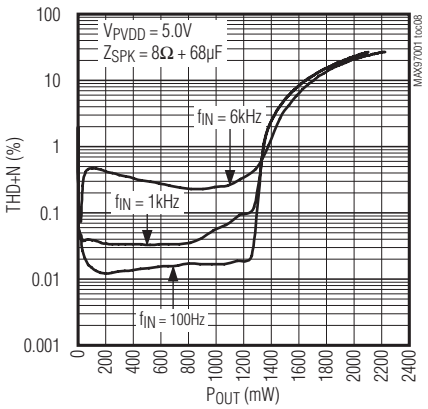
THD+N vs. FREQUENCY



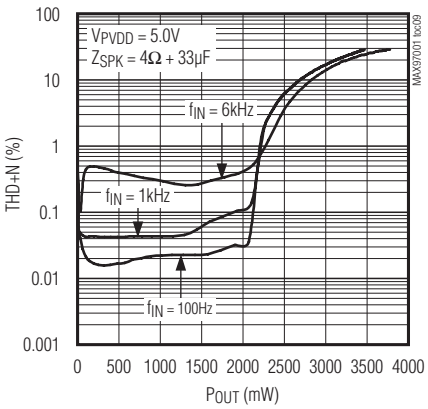
THD+N vs. FREQUENCY



THD+N vs. OUTPUT POWER



THD+N vs. OUTPUT POWER

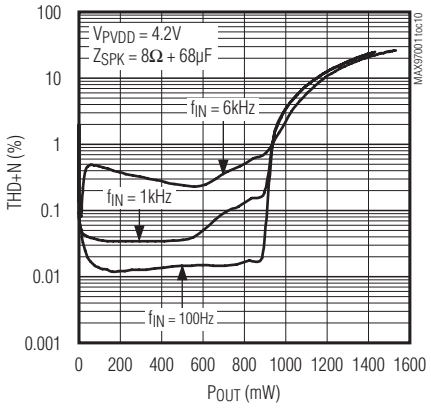


Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

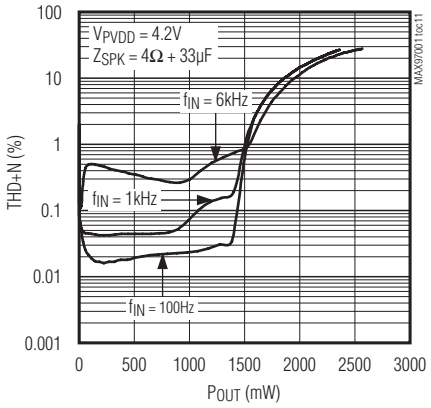
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

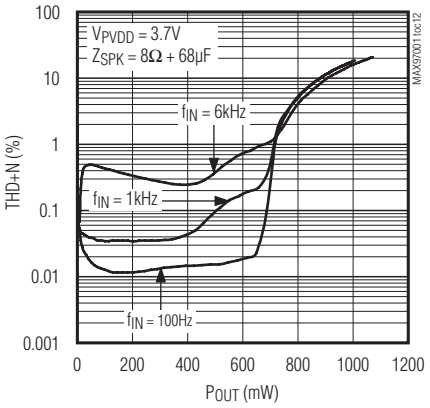
THD+N vs. OUTPUT POWER



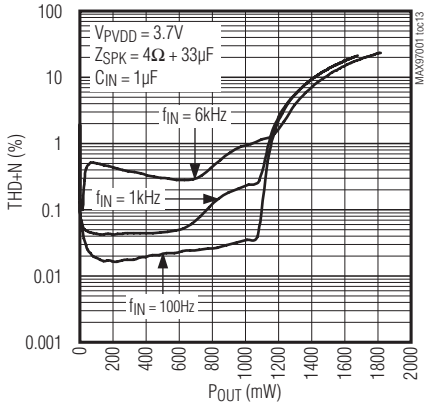
THD+N vs. OUTPUT POWER



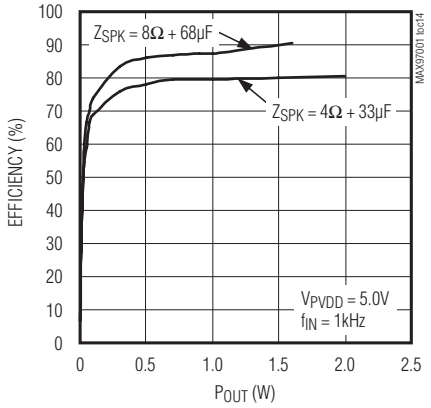
THD+N vs. OUTPUT POWER



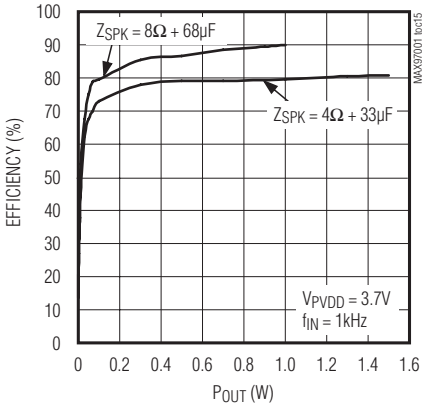
THD+N vs. OUTPUT POWER



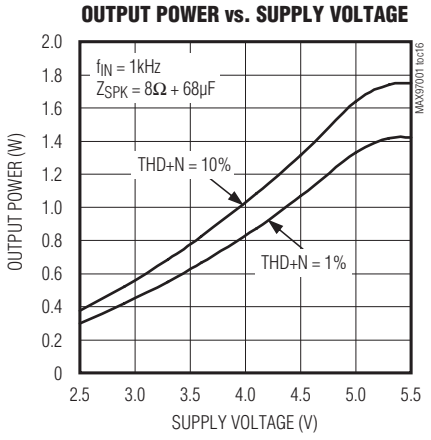
EFFICIENCY vs. OUTPUT POWER



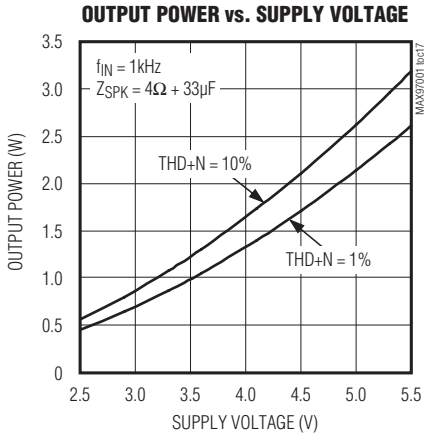
EFFICIENCY vs. OUTPUT POWER



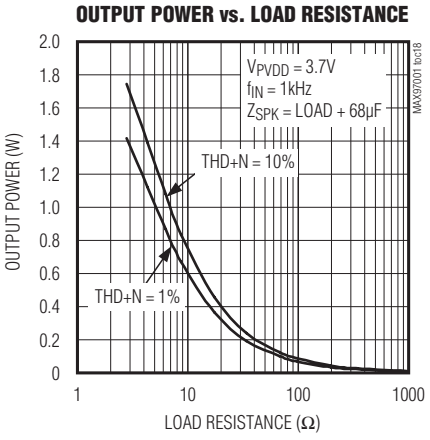
OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. LOAD RESISTANCE

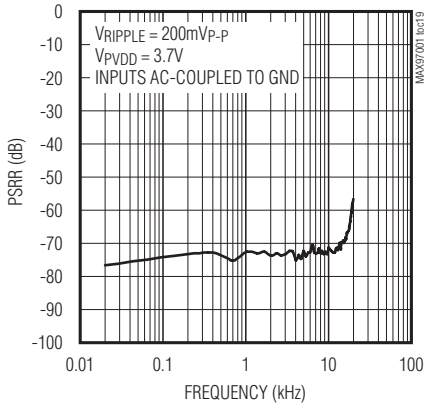


Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

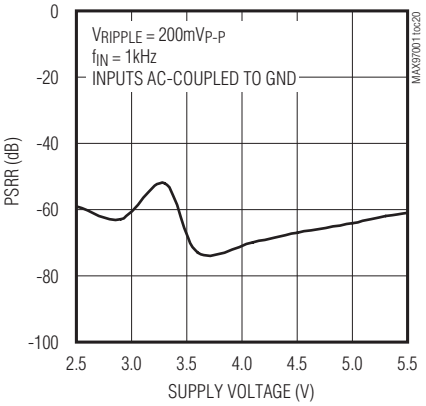
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

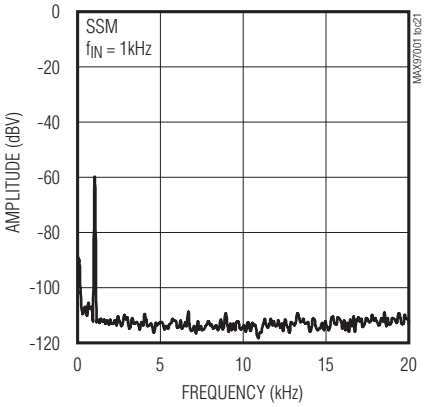
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



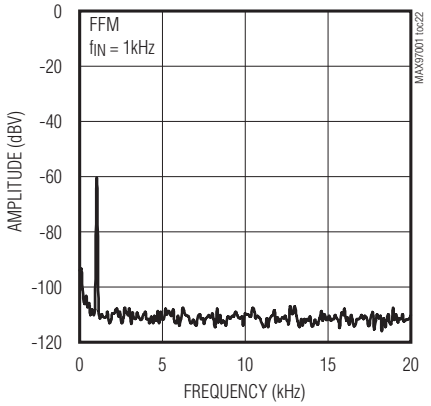
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



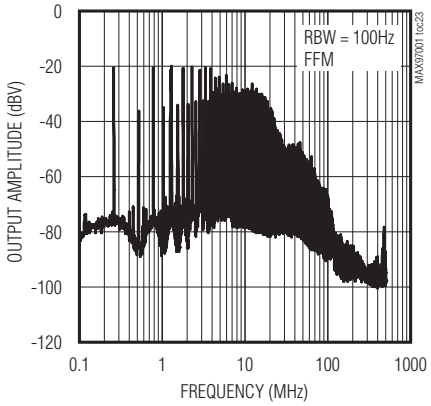
IN-BAND OUTPUT SPECTRUM



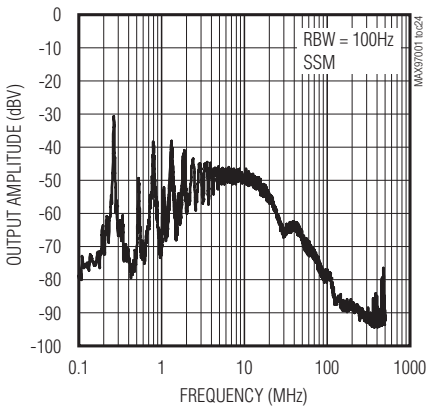
IN-BAND OUTPUT SPECTRUM



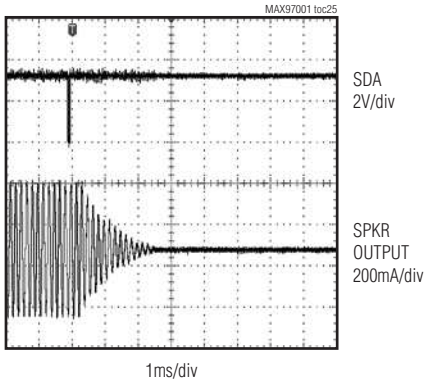
WIDEBAND OUTPUT SPECTRUM



WIDEBAND OUTPUT SPECTRUM



SOFTWARE SHUTDOWN RESPONSE

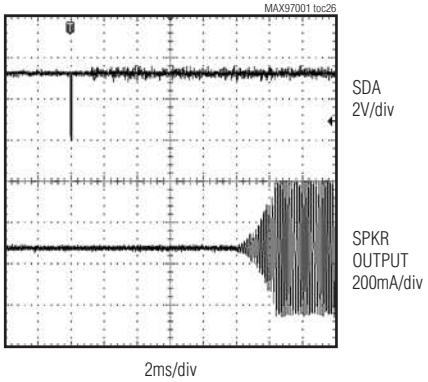


Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

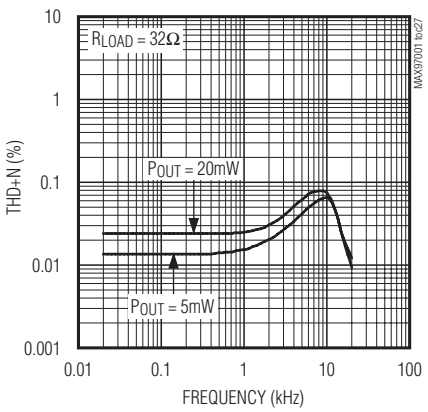
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

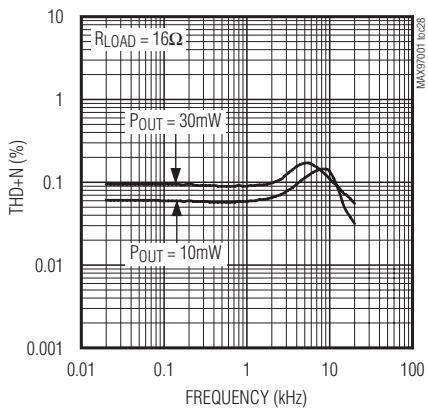
SOFTWARE TURN-ON RESPONSE



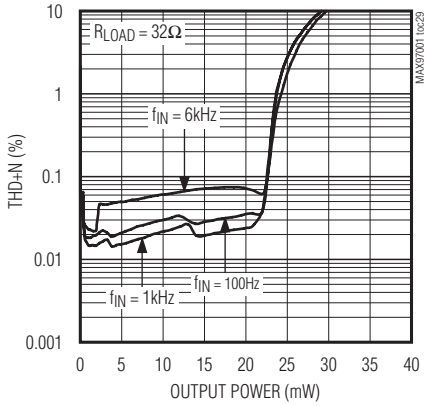
THD+N vs. FREQUENCY



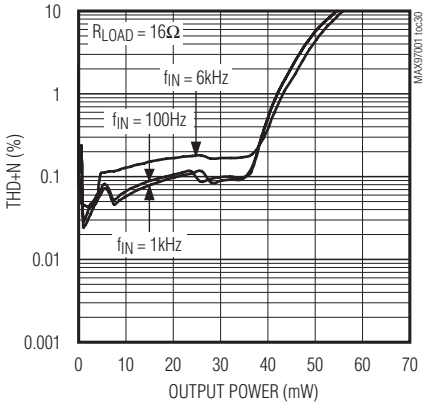
THD+N vs. FREQUENCY



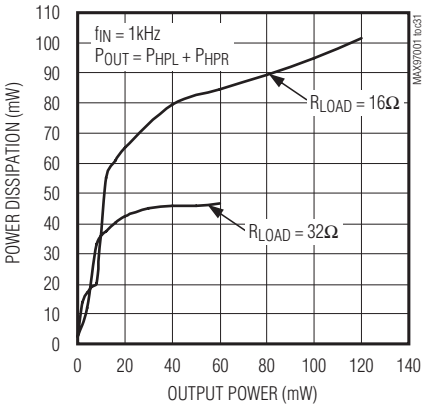
THD+N vs. OUTPUT POWER



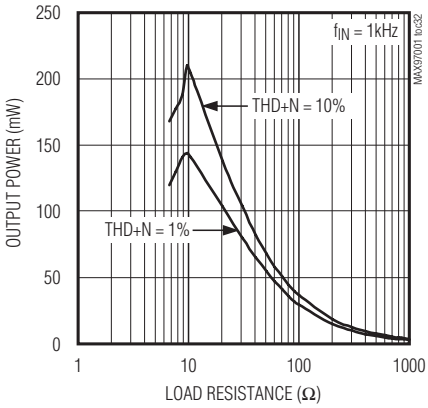
THD+N vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



OUTPUT POWER vs. LOAD RESISTANCE

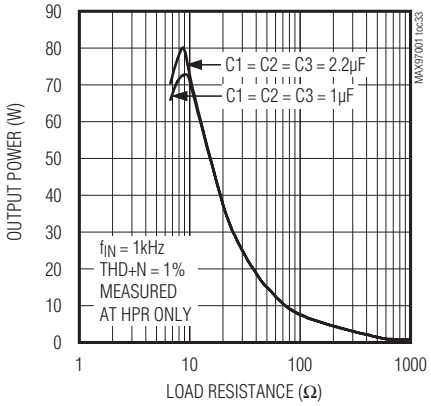


Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

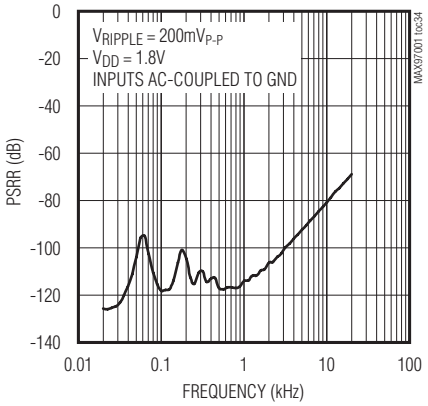
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

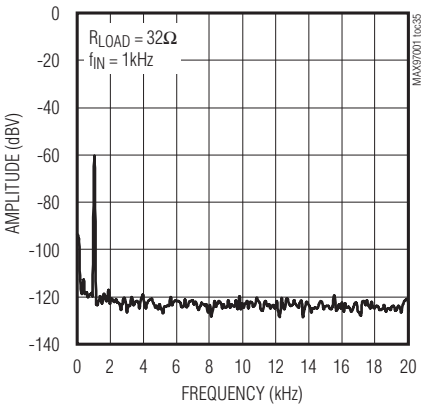
OUTPUT POWER vs. LOAD RESISTANCE



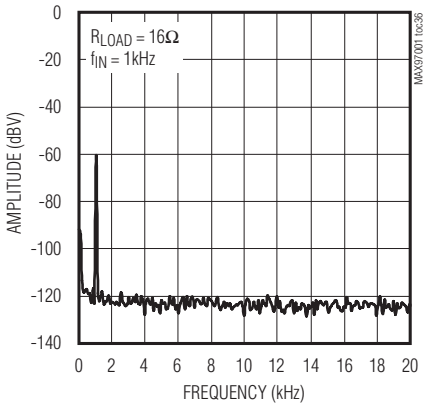
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



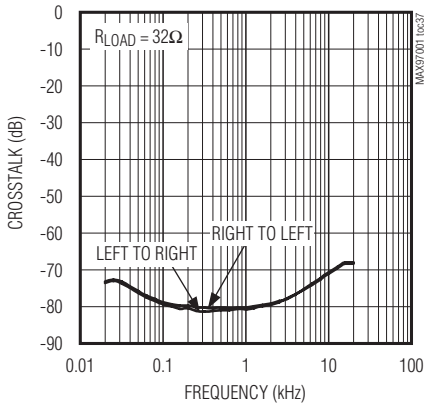
OUTPUT SPECTRUM



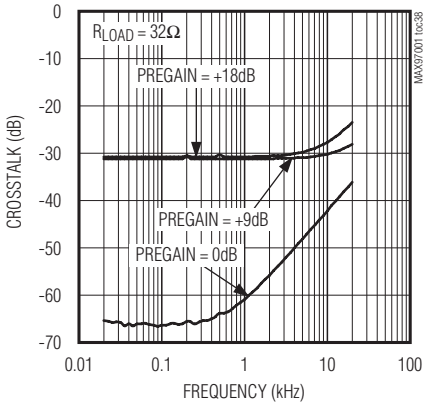
OUTPUT SPECTRUM



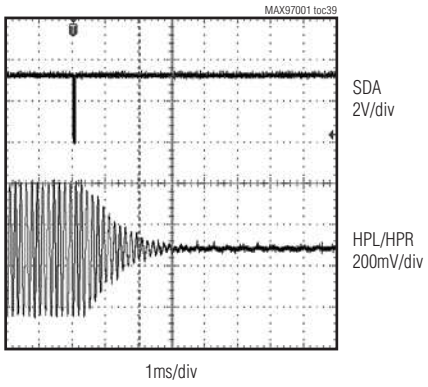
CROSSTALK vs. FREQUENCY



COMMON-MODE REJECTION RATIO vs. FREQUENCY



SOFTWARE SHUTDOWN RESPONSE

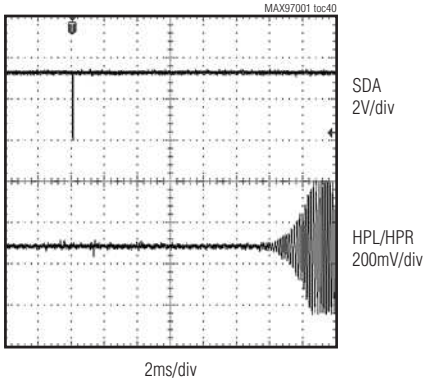


Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

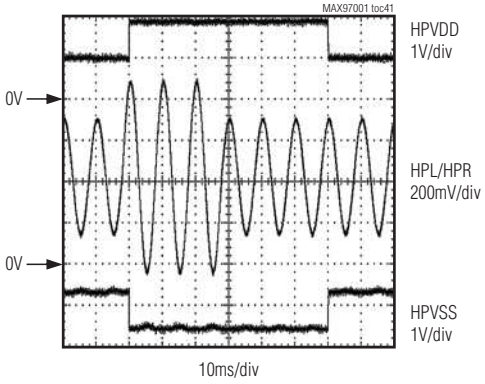
Typical Operating Characteristics (continued)

(V_{LDOIN} = V_{PVDD} = 3.7V, V_{GND} = V_{PGND} = 0V. Single-ended inputs, preamp gain = 0dB, HPLVOL = HPRVOL = SPKVOL = 0dB. Speaker loads (Z_{SPK}) connected between OUTP and OUTN. Headphone loads (R_{HP}) connected from HPL or HPR to GND. Z_{SPK} = ∞, R_{HP} = ∞. $C_{C1P-C1N}$ = C_{HPVDD} = C_{HPVSS} = C_{BIAS} = 1µF. T_A = +25°C, unless otherwise noted.)

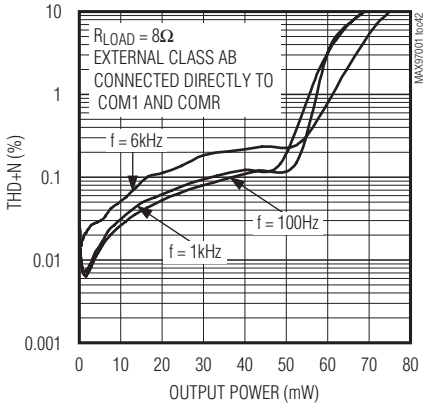
SOFTWARE STARTUP RESPONSE



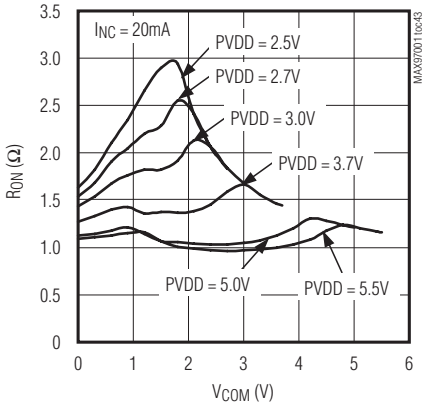
CLASS H OPERATION



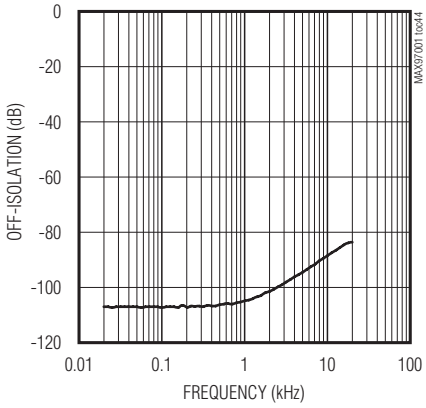
THD+N vs. OUTPUT POWER



ON-RESISTANCE vs. V_{COM}

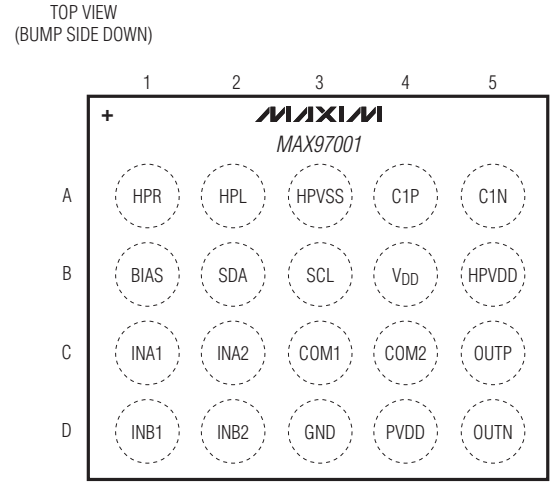


BYPASS SWITCH OFF-ISOLATION



Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
A1	HPR	Headphone Amplifier Left Output
A2	HPL	Headphone Amplifier Right Output
A3	HPVSS	Headphone Amplifier Negative Power Supply. Bypass with a 1µF capacitor to GND.
A4	C1P	Charge-Pump Flying Capacitor Positive Terminal. Connect a 1µF capacitor between C1P and C1N.
A5	C1N	Charge-Pump Flying Capacitor Negative Terminal. Connect a 1µF capacitor between C1P and C1N.
B1	BIAS	Common-Mode Bias. Bypass to GND with a 1µF capacitor.
B2	SDA	Serial-Data Input/Output. Connect a pullup resistor from SDA to DVDD.
B3	SCL	Serial-Clock Input. Connect a pullup resistor from SCL to DVDD.
B4	V_{DD}	Headphone Amplifier Supply. Bypass with a 1µF capacitor to GND.
B5	HPVDD	Headphone Amplifier Positive Power Supply. Bypass with a 1µF capacitor to GND.
C1	INA1	Input A1. Left input or negative input.
C2	INA2	Input A2. Right input or positive input.
C3	COM1	Positive Bypass Switch Input
C4	COM2	Negative Bypass Switch Input
C5	OUTP	Positive Speaker Output
D1	INB1	Input B1. Left input or negative input.
D2	INB2	Input B2. Right input or positive input.
D3	GND	Analog Ground
D4	PVDD	Class D Power Supply. Bypass with a 1µF capacitor to GND.
D5	OUTN	Negative Speaker Output

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Detailed Description

The MAX97001 mono audio subsystem combines a mono speaker amplifier with a stereo headphone amplifier and an analog DPST switch. The high-efficiency, 700mW, Class D speaker amplifier operates directly from the battery and consumes no more than 1µA when in shutdown mode. The headphone amplifier utilizes a dual-mode charge pump and a Class H output stage to maximize efficiency while outputting a ground-referenced signal that does not require output-coupling capacitors. The headphone and speaker amplifiers have independent volume control and on/off control. The 4 inputs are configurable as 2 differential inputs or 4 single-ended inputs. All control is performed using the 2-wire I²C interface.

The speaker amplifier incorporates a distortion limiter to automatically reduce the volume level when excessive clipping occurs. This allows high gain for low-level signals without compromising the quality of large signals.

Signal Path

The MAX97001 signal path consists of flexible inputs, signal mixing, volume control, and output amplifiers (Figure 2). The inputs can be configured for single-ended or differential signals (Figure 3). The internal preamplifiers feature programmable gain settings using internal resistors and an external gain setting using a trimmed internal feedback resistor. The external option allows any desired gain to be selected. Following preamplification, the input signals are mixed, volume adjusted, and routed to the headphone and speaker amplifiers based on the desired configuration.

Mixers

The MAX97001 features independent mixers for the left headphone, right headphone, and speaker paths. Each output can select any combination of any inputs. This allows for mixing two audio signals together and routing independent signals to the headphone and speaker amplifiers. If one of the inputs is not selected by either mixer, it is automatically powered down to save power.

Class D Speaker Amplifier

The MAX97001 Class D speaker amplifier utilizes active emissions limiting and spread-spectrum modulation to minimize the EMI radiated by the amplifier.

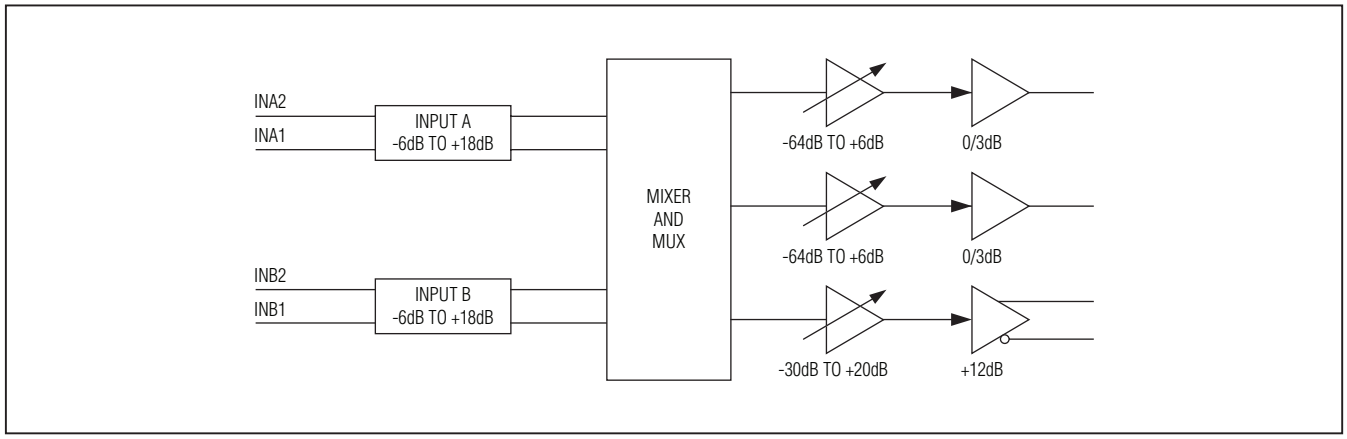


Figure 2. Signal Path

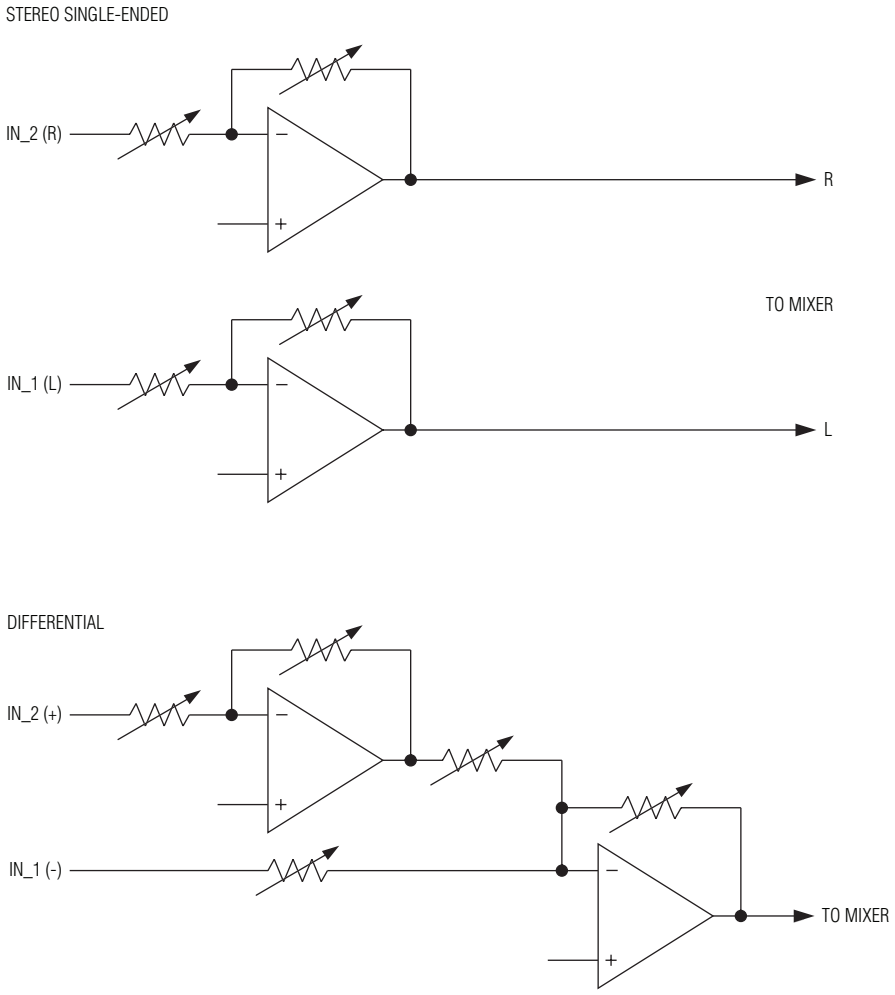


Figure 3. Differential and Stereo Single-Ended Input Configurations

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters or shielding in order to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions, while maintaining up to 87% efficiency. Maxim's spread-spectrum modulation mode flattens wideband spectral components, while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The MAX97001's spread-spectrum modulator randomly varies the switching frequency by ±20kHz around the center frequency (250kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (see Figure 4).

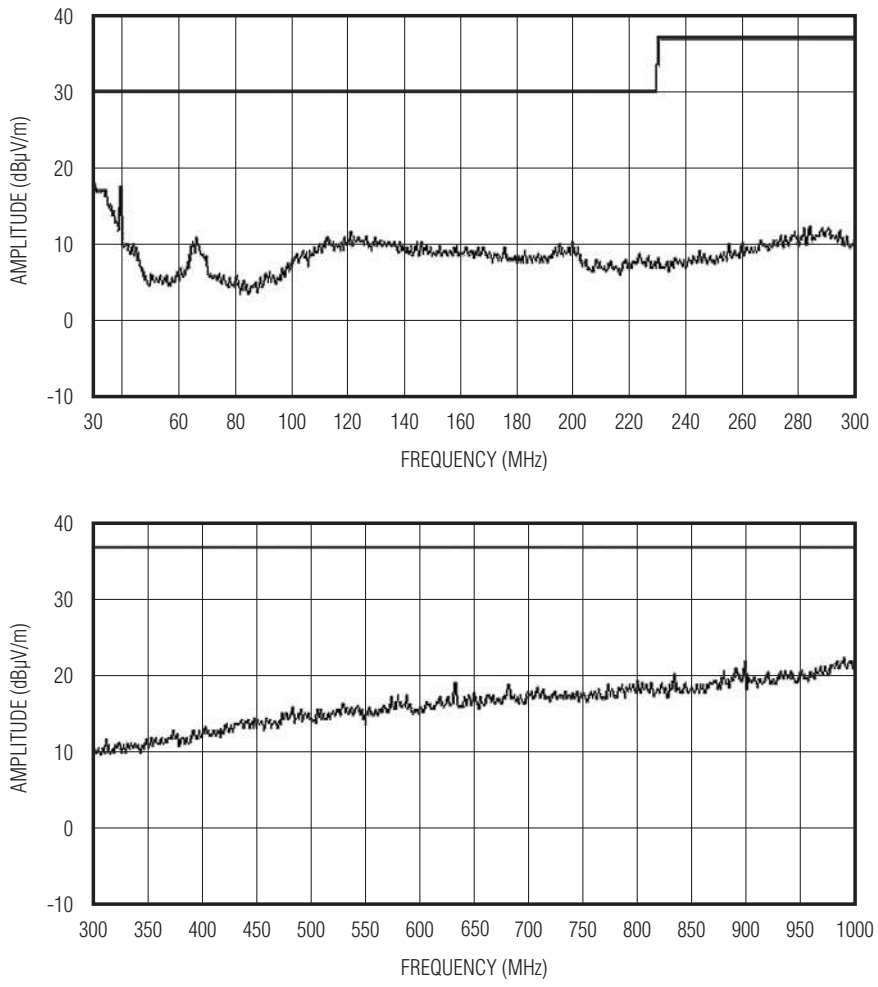


Figure 4. EMI with 15cm of Speaker Cable

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Distortion Limiter

The MAX97001 speaker amplifiers integrate a limiter to provide speaker protection and audio compression. When enabled, the limiter monitors the audio signal at the output of the Class D speaker amplifier and decreases the gain if the distortion exceeds the predefined threshold. The limiter automatically tracks the battery voltage to reduce the gain as the battery voltage drops.

Figure 5 shows the typical output vs. input curves with and without the distortion limiter. The dotted line shows the maximum gain for a given distortion limit without the distortion limiter. The solid line shows how, with the distortion limiter enabled, the gain can be increased without exceeding the set distortion limit. When the limiter is enabled, selecting a high gain level results in peak signals being attenuated while low signals are left unchanged. This increases the perceived loudness without the harshness of a clipped waveform.

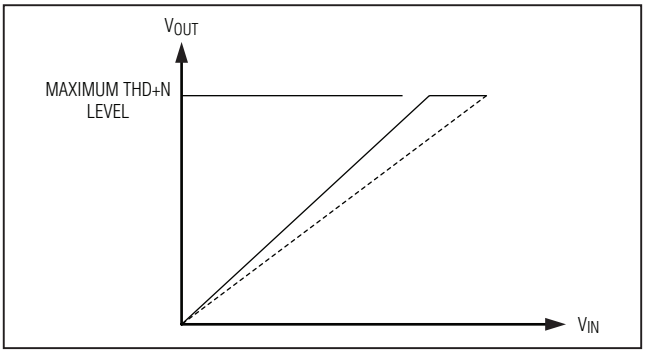


Figure 5. Limiter Gain Curve

Analog Switch

The MAX97001 integrates a DPST analog audio switch that connects COM1 and COM2 to OUTP and OUTN, respectively. Unlike discrete solutions, the switch design reduces coupling of Class D switching noise to the COM_ inputs. This eliminates the need for a costly T-switch. Drive COM1 and COM2 with a low-impedance source to minimize noise on the pins. In applications that do not require the analog switch, leave COM1 and COM2 unconnected. When applying signal on COM1 and COM2, disable the Class D amplifier before closing the switch.

Headphone Amplifier

DirectDrive

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply). Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive® architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the MAX97001 to be biased at GND while operating from a single supply (Figure 6). Without a DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) capacitors, the MAX97001 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the offset of the MAX97001 is typically ±0.6mV, which, when combined with a 32Ω load, results in less than 50µA of DC current flow to the headphones.

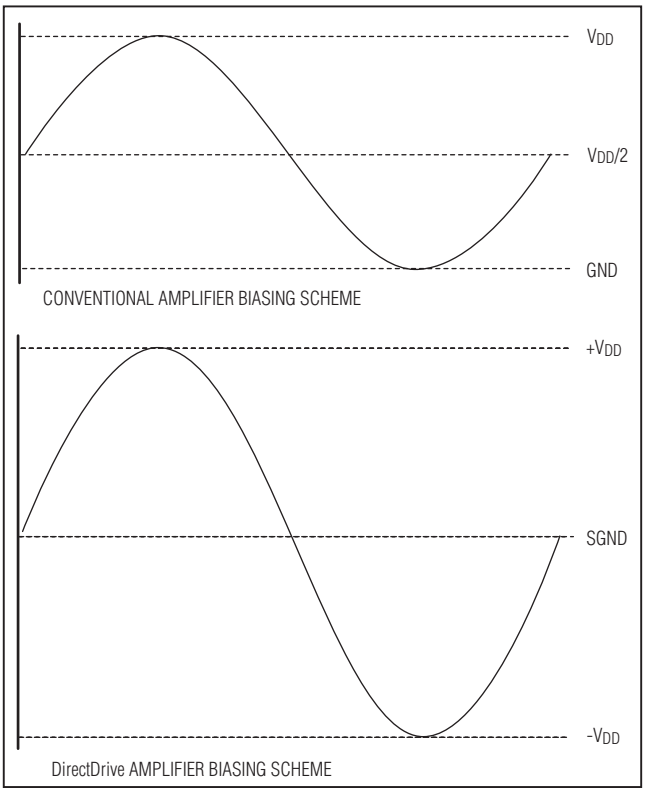


Figure 6. Traditional Amplifier Output vs. MAX97001 DirectDrive Output

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC-bias voltage of the headphone amplifiers. This method raises some issues:

- The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
- During an ESD strike, the amplifier's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full energy from an ESD strike.
- When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

Charge Pump

The MAX97001's dual-mode charge pump generates both the positive and negative power supply for the headphone amplifier. To maximize effficiency, both the charge pump's switching frequency and output voltage change based on signal level.

When the input signal level is less than 10% of V_{DD} the switching frequency is reduced to a low rate. This minimizes switching losses in the charge pump. When the input signal exceeds 10% of V_{DD}, the switching frequency increases to support the load current.

For input signals below 25% of V_{DD}, the charge pump generates $\pm(V_{DD}/2)$ to minimize the voltage drop across the amplifier's power stage and thus improves efficiency. Input signals that exceed 25% of V_{DD} cause the charge pump to output $\pm V_{DD}$. The higher output voltage allows for full output power from the headphone amplifier.

To prevent audible glitches when transitioning from the $\pm(V_{DD}/2)$ output mode to the $\pm V_{DD}$ output mode, the charge pump transitions very quickly. This quick change draws significant current from V_{DD} for the duration of the transition. The bypass capacitor on V_{DD} supplies the required current and prevent droop on V_{DD}.

The charge pump's dynamic switching mode can be turned off through the I²C interface. The charge pump can then be forced to output either $\pm(V_{DD}/2)$ or $\pm V_{DD}$ regardless of input signal level.

Class H Operation

A Class H amplifier uses a Class AB output stage with power supplies that are modulated by the output signal. In the case of the MAX97001, two nominal power-supply differentials of 1.8V (+0.9V to -0.9V) and 3.6V (+1.8V to -1.8V) are available from the charge pump. Figure 7 shows the operation of the output voltage dependent power supply.

Low-Power Mode

To minimize power consumption when using the headphone amplifier, enable the low-power mode. In this mode, the headphone mixers and volume control are bypassed and shutdown.

I²C Slave Address

The MAX97001 uses a slave address of 0x9A or 1001101R/W. The address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. Set the read/write bit to 1 to configure the MAX97001 to read mode. Set the read/write bit to 0 to configure the MAX97001 to write mode. The address is the first byte of information sent to the MAX97001 after the START (S) condition.

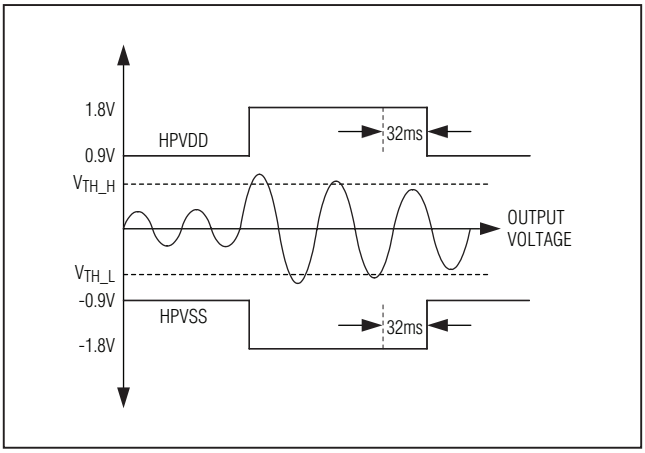


Figure 7. Class H Operation

I²C Registers

Nine internal registers program the MAX97001. Table 1 lists all of the registers, their addresses, and power-on-reset states. Register 0xFF indicates the device revision.

Write zeros to all unused bits in the register table when updating the register, unless otherwise noted. Tables 2–7 describe each bit.

Table 1. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	ADDRESS	DEFAULT	R/W
STATUS											
Input Gain	INADIFF	INBDIFF	PGAINA			PGAINB			0x00	0x00	R/W
Headphone Mixers	HPLMIX				HPRMIX				0x01	0x00	R/W
Speaker Mixer	0	0	0	0	SPKMIX				0x02	0x00	R/W
Headphone Left	$\overline{ZCD}$	$\overline{SLEW}$	HPLM	HPLVOL					0x03	0x00	R/W
Headphone Right	HPGAIN	0	HPRM	HPRVOL					0x04	0x00	R/W
Speaker	FFM	SPKM	SPKVOL						0x05	0x00	R/W
Reserved	0	0	0	0	0	0	0	0	0x06	0x00	R/W
Limiter	THDCLP				0	0	0	THDT1	0x07	0x00	R/W
Power Management	$\overline{SHDN}$	LPMODE		SPKEN	0	HPLEN	HPREN	BYPEN	0x08	0x01	R/W
Charge Pump	0	0	0	0	0	0	CPSEL	FIXED	0x09	0x00	R/W
REVISION ID											
Rev ID	REV								0xFF	0x00	R

Audio Subsystem with Mono Class D Speaker and Class H Headphone Amplifiers

Table 2. Input Register

REGISTER	BIT	NAME	DESCRIPTION
0x00	7	INADIFF	**Input A Differential Mode.** Configures the input A channel as either a mono differential signal (INA = INA2 - INA1) or as a stereo signal (INA1 = left, INA2 = right). 0 = Stereo single-ended 1 = Differential
	6	INBDIFF	**Input B Differential Mode.** Configures the input B channel as either a mono differential signal (INB = INB2 - INB1) or as a stereo signal (INB1 = left, INB2 = right). 0 = Stereo single-ended 1 = Differential
	5	PGAINA	**Input A Preamp Gain.** Set the input gain to maximize output signal level for a given input signal range to improve the SNR of the system. PGAINA = 111 switches to a trimmed 20kΩ feedback resistor for external gain setting.
	4		**VALUE** / **LEVEL (dB)** 000 / -6 001 / -3 010 / 0 011 / 3dB 100 / 6 101 / 9 110 / 18 111 / External
	3		
	2	PGAINB	**Input B Preamp Gain.** Set the input gain to maximize output signal level for a given input signal range to improve the SNR of the system. PGAINB = 111 switches to a trimmed 20kΩ feedback resistor for external gain setting.
	1		**VALUE** / **LEVEL (dB)** 000 / -6 001 / -3 010 / 0 011 / 3 100 / 6 101 / 9 110 / 18 111 / External
	0		

Table 3. Mixer Registers

REGISTER	BIT	NAME	DESCRIPTION
0x01	7	HPLMIX	**Left Headphone Mixer.** Selects which of the four inputs is routed to the left headphone output.
	6		**VALUE** / **INPUT** 0000 — No input xxx1 — INA1 (disabled when INADIFF = 1) xx1x — INA2 (select when INADIFF = 1) x1xx — INB1 (disabled when INBDIFF = 1) 1xxx — INB2 (select when INBDIFF = 1)
	5		
	4		
	3	HPRMIX	**Right Headphone Mixer.** Selects which of the four inputs is routed to the right headphone output.
	2		**VALUE** / **INPUT** 0000 — No input xxx1 — INA1 (disabled when INADIFF = 1) xx1x — INA2 (select when INADIFF = 1) x1xx — INB1 (disabled when INBDIFF = 1) 1xxx — INB2 (select when INBDIFF = 1)
	1		
	0		
0x02	3	SPKMIX	**Speaker Mixer.** Selects which of the four inputs is routed to the speaker output.
	2		**VALUE** / **INPUT** 0000 — No input xxx1 — INA1 (disabled when INADIFF = 1) xx1x — INA2 (select when INADIFF = 1) x1xx — INB1 (disabled when INBDIFF = 1) 1xxx — INB2 (select when INBDIFF = 1)
	1		
	0		