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19-0746; Rev 4; 8/08

2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

General Description

The MAX9775/MAX9776 combine a high-efficiency Class D, stereo/mono audio power amplifier with a mono DirectDrive® receiver amplifier and a stereo DirectDrive headphone amplifier.

Maxim's 3rd-generation, ultra-low-EMI, Class D audio power amplifiers provide Class AB performance with Class D efficiency. The MAX9775/MAX9776 deliver 1.5W per channel into a 4Ω load from a 5V supply and offer efficiencies up to 79%. Active emissions limiting circuitry and spread-spectrum modulation greatly reduce EMI, eliminating the need for output filtering found in traditional Class D devices.

The MAX9775/MAX9776 utilize a fully differential architecture, a full-bridged output, and comprehensive click-and-pop suppression. A 3D stereo enhancement function allows the MAX9775 to widen the stereo sound field immersing the listener in a cleaner, richer sound experience than typically found in portable applications. The devices utilize a flexible, user-defined mixer architecture that includes an input mixer, volume control, and output mixer. All control is done through I²C.

The mono receiver amplifier and stereo headphone amplifier use Maxim's DirectDrive architecture that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors, saving cost, space, and component height.

The MAX9775 is available in a 36-bump WLP (3mm x 3mm) package. The MAX9776 is available in a 32-pin TQFN (5mm x 5mm) or a 36-bump WLP (3mm x 3mm) package. Both devices are specified over the extended -40°C to +85°C temperature range.

Applications

Cell Phones

Portable Multimedia Players

Handheld Gaming Consoles

Features

- ♦ Unique Spread-Spectrum Modulation and Active Emissions Limiting Significantly Reduces EMI
- ♦ 3D Stereo Enhancement (MAX9775 Only)
- ♦ Up to 3 Stereo Inputs
- ♦ 1.5W Stereo Speaker Output (4Ω, V_{DD} = 5V)
- ♦ 50mW Mono Receiver/Stereo Headphone Outputs (32Ω, V_{DD} = 3.3V)
- ♦ High PSRR (68dB at 217Hz)
- ♦ 79% Efficiency (V_{DD} = 3.3V, R_L = 8Ω, P_{OUT} = 470mW)
- ♦ I²C Control—Input Configuration, Volume Control, Output Mode
- ♦ Click-and-Pop Suppression
- ♦ Low Total Harmonic Distortion (0.03% at 1kHz)
- ♦ Current-Limit and Thermal Protection
- ♦ Available in Space-Saving, 36-Bump WLP (3mm x 3mm) and 32-Pin TQFN (5mm x 5mm) Packages

Ordering Information

PART	PIN-PACKAGE	CLASS D AMPLIFIER
MAX9775EBX+T	36 WLP*	Stereo
MAX9776ETJ+	32 TQFN-EP**	Mono
MAX9776EBX+T	36 WLP*	Mono

Note: *All devices are specified over the -40°C to +85°C operating temperature range.*

+Denotes a lead-free/RoHS-compliant package.

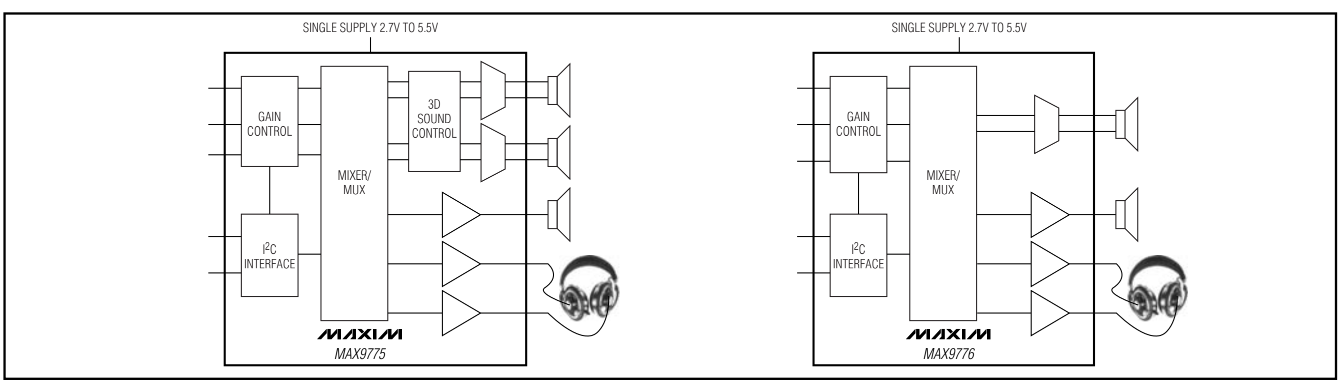
**Four center bumps depopulated.*

***EP = Exposed pad.*

Pin Configurations appear at end of data sheet.

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.

Simplified Block Diagrams



2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND....................6V
PV_{DD} to PGND....................6V
CPV_{DD} to CPGND....................6V
CPV_{SS} to CPGND....................-6V to +0.3V
V_{SS} to CPGND....................-6V to +0.3V
C1N....................(CPV_{SS} - 0.3V) to (CPGND + 0.3V)
C1P....................(CPGND - 0.3V) to (CPV_{DD} + 0.3V)
HPL, HPR to GND....................(CPV_{SS} - 0.3V) to (CPV_{DD} + 0.3V)
GND to PGND and CPGND....................±0.3V
V_{DD} to PV_{DD} and CPV_{DD}....................±0.3V
SDA, SCL to GND....................-0.3V to +6V
All other pins to GND....................-0.3V to (V_{DD} + 0.3V)
Continuous Current In/Out of PV_{DD}, PGND, CPV_{DD}, CPGND, OUT__, HPR, and HPL....................±800mA
Continuous Input Current CPV_{SS}....................260mA
Continuous Input Current (all other pins)....................±20mA
Duration of Short Circuit Between OUT_+ and OUT_-....................Continuous
Duration of HP_, OUT_ Short Circuit to GND or PV_{DD}....................Continuous
Continuous Power Dissipation (T_A = +70°C)
36-Bump (3mm x 3mm) UCSP Multilayer Board (derate 17.0mW/°C above +70°C)....................1360.5mW
32-Pin (5mm x 5mm) TQFN Single-Layer Board (derate 21.3mW/°C above +70°C)....................1702.1mW
32-Pin TQFN Multilayer Board (derate 34.5mW/°C above +70°C)....................2758.6mW
Junction Temperature....................+150°C
Operating Temperature Range....................-40°C to +85°C
Storage Temperature Range....................-65°C to +150°C
Lead Temperature (soldering, 10s)....................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, V_{GND} = V_{PGND} = V_{CPGND} = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL						
Supply Voltage Range	V_{DD}, PV_{DD}, CPV_{DD}	Inferred from PSRR test	2.7		5.5	V
Quiescent Current (Mono)	I_{DD}	Output mode 1, 6, 11 (Rx mode)		6.3	10	mA
		Output mode 4, 9, 14 (HP mode)		8	12.6	
		Output mode 2, 7, 12 (SP mode)		9.5	15	
		Output mode 3, 8, 13 (SP and HP mode)		12.9	18	
Quiescent Current (Stereo)	I_{DD}	Output mode 1, 6, 11 (Rx mode)		7		mA
		Output mode 4, 9, 14 (HP mode)		9		
		Output mode 2, 7, 12 (SP mode)		16.5		
		Output mode 3, 8, 13 (SP and HP mode)		20		
Mute Current	I_{MUTE}	Current in mute (low power)		4.7	10	mA
Shutdown Current	I_{SHDN}	Hard shutdown: $\overline{SHDN}$ = GND		0.1	10	µA
		Soft shutdown: See the *I^2C Interface* section		8.5	15	
Turn-On Time	t_{ON}	Time from shutdown or power-on to full operation		30		ms
Input Resistance	R_{IN}	B and C pair inputs, T_A = +25°C, VOL = max	17.5	28	41.0	kΩ
		A pair inputs, T_A = +25°C, +20dB	3.5	5.5	8.0	kΩ
Common-Mode Rejection Ratio	CMRR	T_A = +25°C, f_{IN} = 1kHz (Note 2)	45	50	60	dB
Input DC Bias Voltage	V_{BIAS}	IN_ inputs	1.12	1.25	1.38	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, V_{GND} = V_{PGND} = V_{CPGND} = 0V, $\overline{SHDN}$ = V_{DD}, I[2]C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SPEAKER AMPLIFIERS							
Output Offset Voltage	V_{OS}	T_A = +25°C			±5.5	±23.5	mV
		T_{MIN} ≤ T_A ≤ T_{MAX}				±40	
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Notes 2, 3)	Into shutdown		-62		dB
			Out of shutdown		-60		
			Into mute		-63		
			Out of mute		-62		
Power-Supply Rejection Ratio (Note 3)	PSRR	T_A = +25°C	V_{DD} = 2.7V to 5.5V	48	70		dB
			f = 217Hz, 100mV_{P-P} ripple		68		
			f = 1kHz, 100mV_{P-P} ripple		60		
			f = 20kHz, 100mV_{P-P} ripple		50		
Output Power (Note 4)	P_{OUT}	THD+N = 1%, T_A = +25°C	R_L = 4Ω, V_{DD} = 5V		1500		mW
			R_L = 8Ω, V_{DD} = 3.3V		450		
			R_L = 8Ω, V_{DD} = 5V		1115		
Current Limit					1.6		A
Total Harmonic Distortion Plus Noise (Note 4)	THD+N	f = 1kHz	R_L = 8Ω, P_{OUT} = 125mW		0.03		%
			R_L = 4Ω, P_{OUT} = 250mW		0.04		
Signal-to-Noise Ratio	SNR	V_{OUT} = 1.8V_{RMS}, R_L = 8Ω, 3D not active (Note 3)	BW = 20Hz to 20kHz		81		dB
			A-weighted		84		
Output Frequency	f_{OSC}	Fixed-frequency modulation			1100		kHz
		Spread-spectrum modulation			1100 ±30		
Efficiency	η	P_{OUT} = 470mW, f = 1kHz both channels driven, L = 68µH in series with 8Ω load			79		%
Gain	A_V				12		dB
Channel-to-Channel Gain Tracking (Note 5)		T_A = +25°C			±1		%
3D Sound Resistors (Note 5)	R_{3D}	Used with 22nF and 2.2nF external capacitors		5	7	9	kΩ
Crosstalk (Notes 4, 5)		L to R, R to L, f = 10kHz, R_L = 8Ω, V_{OUT} = 300mV_{RMS}			73		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, V_{GND} = V_{PGND} = V_{CPGND} = 0V, $\overline{SHDN}$ = V_{DD}, I[2]C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C			±1.8	±5.5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Notes 3, 6)	Into shutdown		-62		dB
			Into mute		-67		
			Out of shutdown		-63		
			Out of mute		-66		
Power-Supply Rejection Ratio (Note 3)	PSRR	T_A = +25°C	V_{DD} = 2.7V to 5.5V	58	80		dB
			f = 217Hz, 100mV_{P-P} ripple		80		
			f = 1kHz, 100mV_{P-P} ripple		70		
			f = 20kHz, 100mV_{P-P} ripple		62		
Output Power	P_{OUT}	T_A = +25°C, THD+N = 1%	R_L = 16Ω		60		mW
			R_L = 32Ω		50		
Gain	A_V				3		dB
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω (V_{OUT} = 800mV_{RMS}, f = 1kHz)			0.03		%
		R_L = 32Ω (V_{OUT} = 800mV_{RMS}, f = 1kHz)			0.024		
Signal-to-Noise Ratio	SNR	R_L = 16Ω, V_{OUT} = 800mV_{RMS} (Note 3)	BW = 20Hz to 20kHz		87		dB
			A-weighted		89		
Slew Rate	SR				0.3		V/µs
Capacitive Drive	C_L				300		pF
HEADPHONE AMPLIFIERS							
Output Offset Voltage	V_{OS}	T_A = +25°C			±1.8	±5.5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Notes 2, 4)	Into shutdown		-61		dB
			Into mute		-65		
			Out of shutdown		-60		
			Out of mute		-64		
ESD Protection		HP_	Contact		±4		kV
			Air		±8		
Power-Supply Rejection Ratio (Note 3)	PSRR	T_A = +25°C	V_{DD} = 2.7V to 5.5V	58	80		dB
			f = 217Hz, 100mV_{P-P} ripple		80		
			f = 1kHz, 100mV_{P-P} ripple		70		
			f = 20kHz, 100mV_{P-P} ripple		62		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, V_{GND} = V_{PGND} = V_{CPGND} = 0V, $\overline{SHDN}$ = V_{DD}, I^2C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power	P_{OUT}	T_A = +25°C, THD+N = 1%	R_L = 16Ω		60		mW
			R_L = 32Ω		50		
Current Limit					170		mA
Gain	A_V				+3		dB
Channel-to-Channel Gain Tracking		T_A = +25°C			±1		%
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω (V_{OUT} = 800mV$_{RMS}$, f = 1kHz)			0.03		%
		R_L = 32Ω (V_{OUT} = 800mV$_{RMS}$, f = 1kHz)			0.024		
Signal-to-Noise Ratio	SNR	R_L = 16Ω, V_{OUT} = 800mV$_{RMS}$	BW = 20Hz to 20kHz		92		dB
			A-weighted		93		
Slew Rate	SR				0.3		V/µs
Capacitive Drive	C_L				300		pF
Crosstalk		L to R, R to L, f = 10kHz, R_L = 16Ω, V_{OUT} = 160mV$_{RMS}$			75		dB
VOLUME CONTROL							
Volume Control		IN+6dB = 0 (minimum gain setting)	HP gain (max)		3		dB
			SP gain (max)		12		
			HP gain (min)		-72		
			SP gain (min)		-63		
		IN+6dB = 1 (maximum gain setting)	HP gain (max)		9		
			SP gain (max)		18		
			HP gain (min)		-61		
			SP gain (min)		-57		
Mono Gain		All outputs	Mono+6dB = 0		0		dB
			Mono+6dB = 1		6		
Input Pair A Control		INA+20dB = 0 (minimum gain setting)			Set by IN+6dB		dB
		INA+20dB = 1 (maximum gain setting)			20		
Mute Attenuation (Minimum Volume)		V_{IN} = 1V$_{RMS}$			80		dB
DIGITAL INPUTS ($\overline{SHDN}$, SDA, SCL)							
Input-Voltage High	V_{IH}			1.4			V
Input-Voltage Low	V_{IL}					0.4	V
Input Hysteresis (SDA, SCL)	V_{HYS}				200		mV

2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, V_{GND} = V_{PGND} = V_{CPGND} = 0V, $\overline{SHDN}$ = V_{DD}, I²C settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise noted. C1 = C2 = C3 = 1µF. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA, SCL Input Capacitance	C_{IN}			10		pF
Input Leakage Current	I_{IN}			0.3	5.0	µA
Pulse Width of Spike Suppressed	t_{SP}			50		ns
DIGITAL OUTPUTS (SDA Open Drain)						
Output Low Voltage SDA	V_{OL}	I_{SINK} = 6mA			0.4	V
Output Fall Time SDA	t_{OF}	$V_{H(MIN)}$ to $V_{L(MAX)}$ bus capacitance = 10pF to 400pF, I_{SINK} = 3mA		250		ns
I²C INTERFACE TIMING (Note 7)						
Serial Clock Frequency	f_{SCL}		DC		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
START Condition Hold	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STA}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0		900	ns
Maximum Receive SCL/SDA Rise Time	t_R				300	ns
Maximum Receive SCL/SDA Fall Time	t_F				300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF

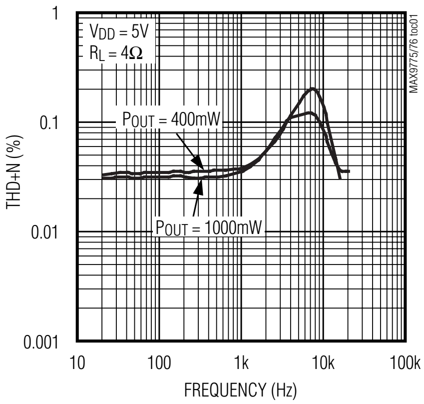
Note 1: All devices are 100% production tested at room temperature. All temperature limits are guaranteed by design.
Note 2: Measured at headphone outputs.
Note 3: Amplifier inputs AC-coupled to GND.
Note 4: Testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 8Ω, L = 68µH; for R_L = 4Ω, L = 47µH.
Note 5: MAX9775 only.
Note 6: Testing performed at room temperature with an 8Ω resistive load in series with a 68µH inductive load connected across BTL outputs for speaker amplifier. Testing performed with a 32Ω resistive load connected between OUT_ and GND for headphone amplifier. Testing performed with 32Ω resistive load connected between OUTRx and GND for mono receiver amplifier. Mode transitions are controlled by I²C.
Note 7: Guaranteed by design.

2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

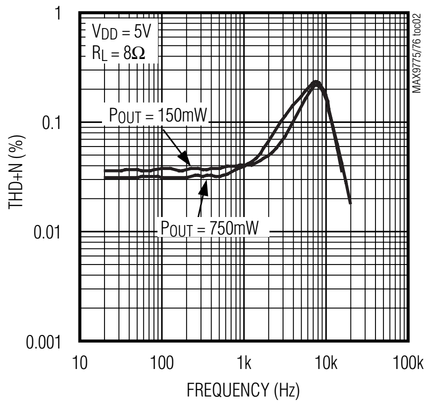
Typical Operating Characteristics

($V_{DD} = PV_{DD} = CPV_{DD} = 3.3V$, GND = PGND = CPGND = 0V, $\overline{SHDN} = V_{DD}$, I²C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

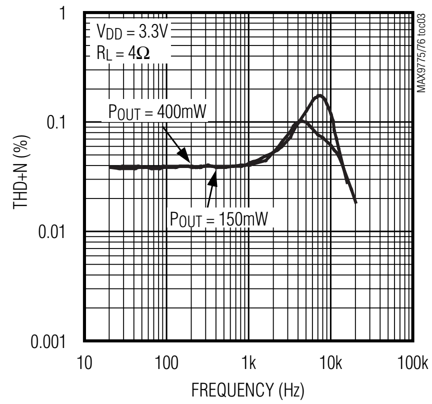
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



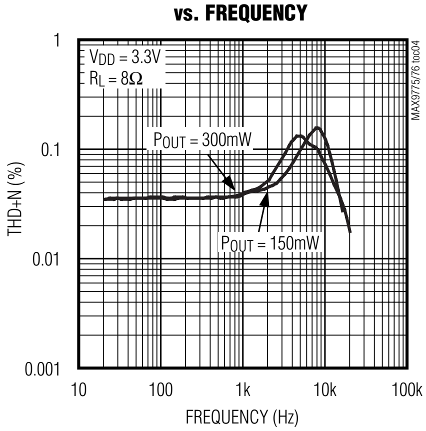
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



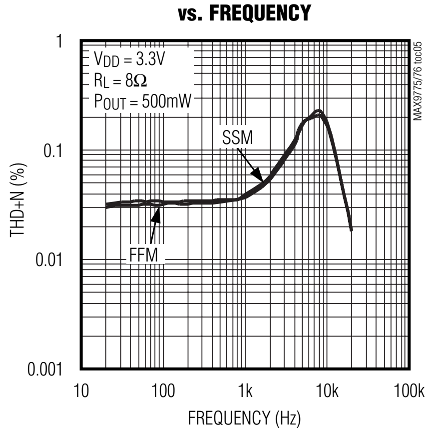
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



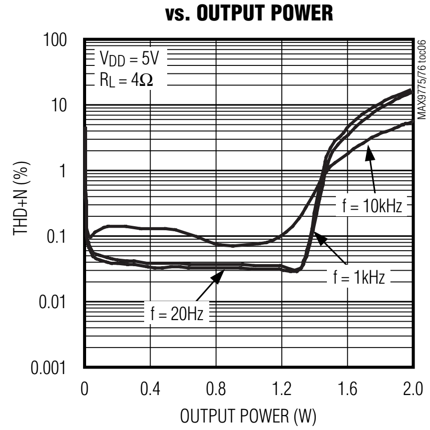
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

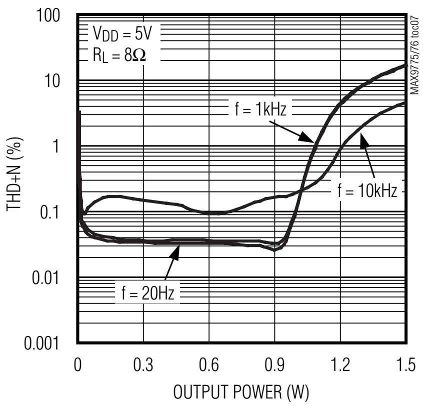


2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

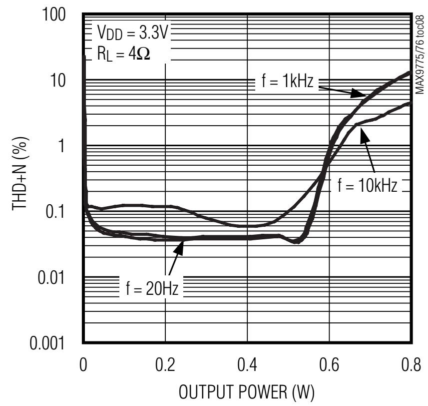
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I[2]C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

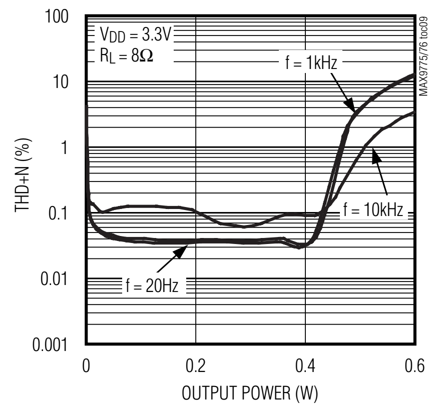
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



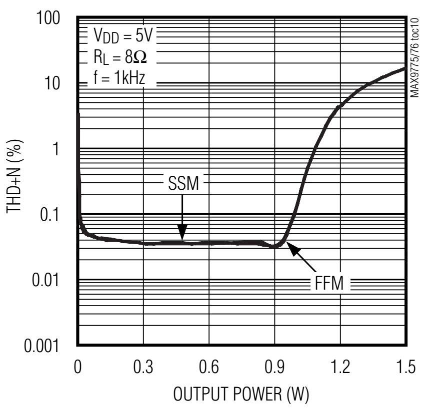
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



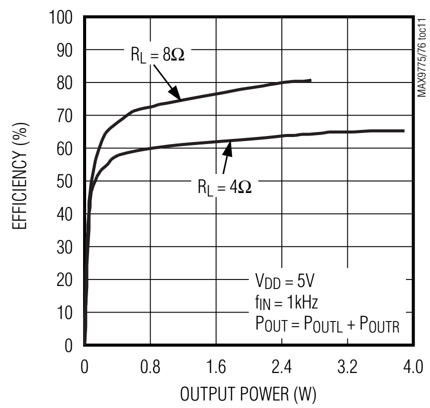
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



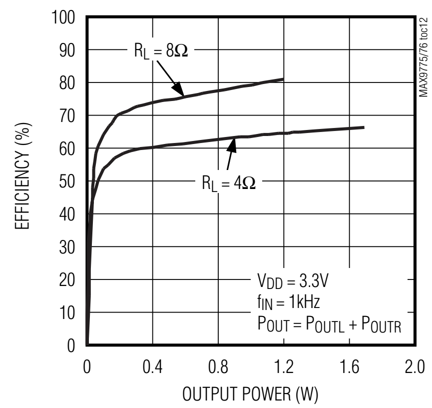
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER

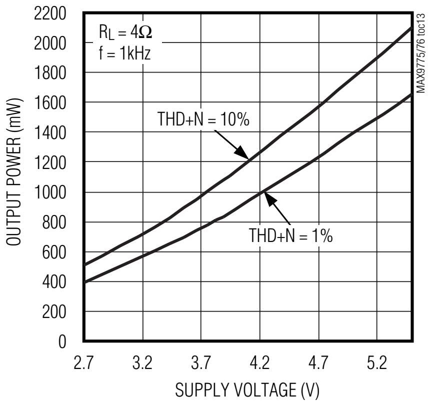


2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

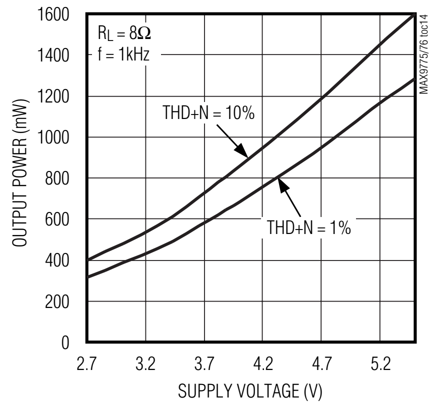
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I²C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

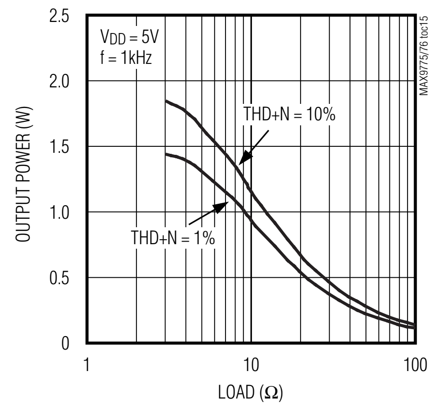
OUTPUT POWER vs. SUPPLY VOLTAGE



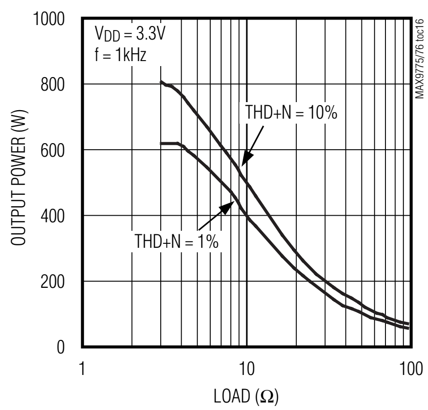
OUTPUT POWER vs. SUPPLY VOLTAGE



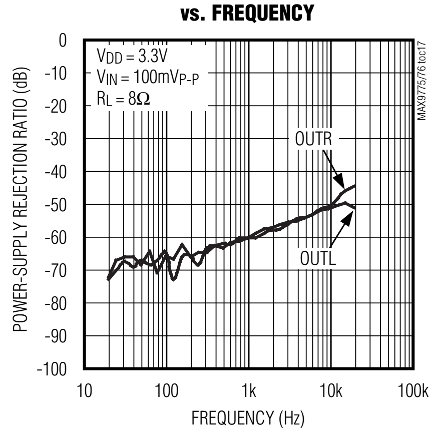
OUTPUT POWER vs. LOAD



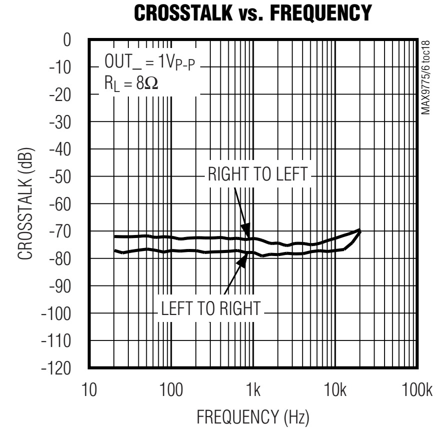
OUTPUT POWER vs. LOAD



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



CROSSTALK vs. FREQUENCY

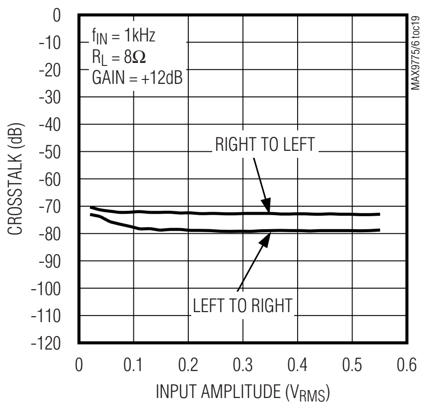


2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

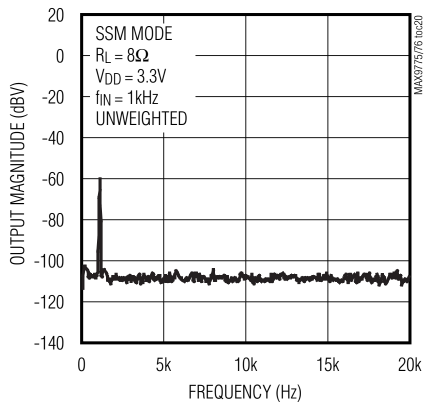
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

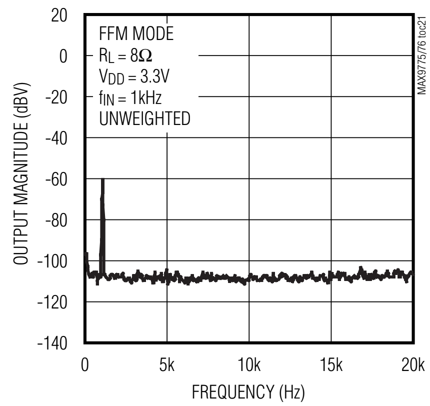
CROSSTALK vs. INPUT AMPLITUDE



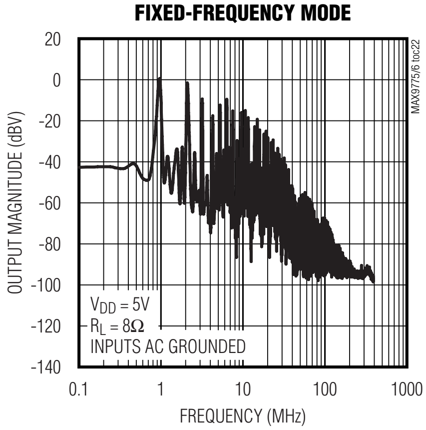
IN-BAND OUTPUT SPECTRUM



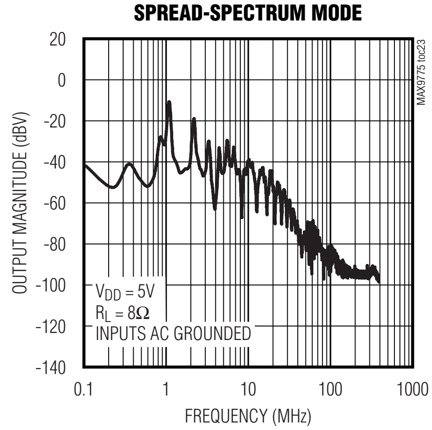
IN-BAND OUTPUT SPECTRUM



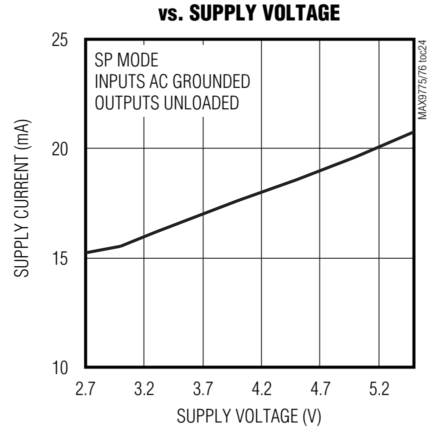
WIDEBAND OUTPUT SPECTRUM FIXED-FREQUENCY MODE



WIDEBAND OUTPUT SPECTRUM SPREAD-SPECTRUM MODE

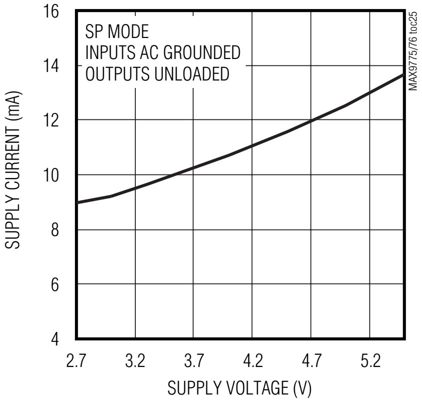


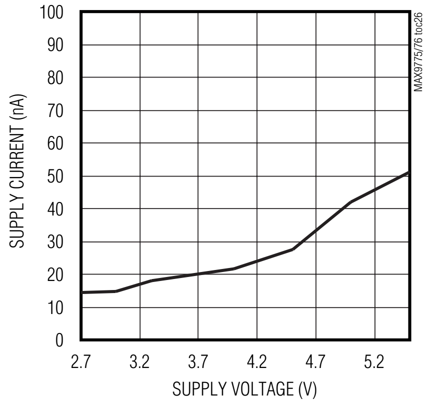
MAX9775 SUPPLY CURRENT vs. SUPPLY VOLTAGE

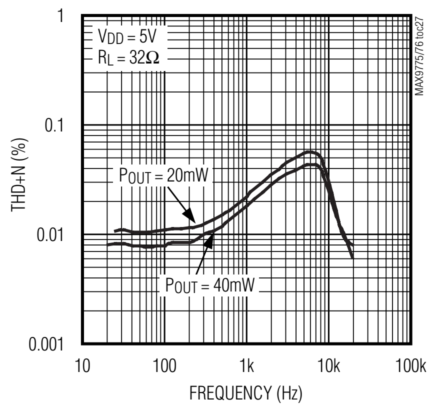


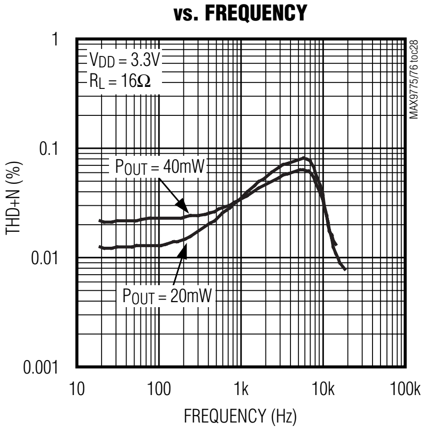
Typical Operating Characteristics (continued)

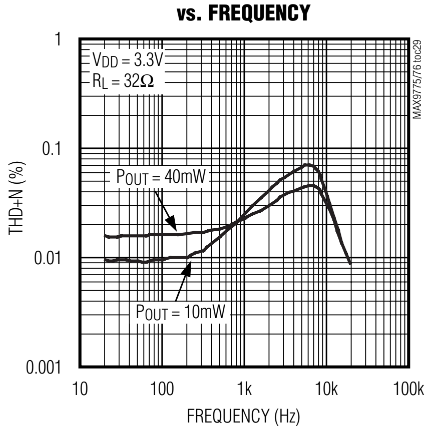
(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I²C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

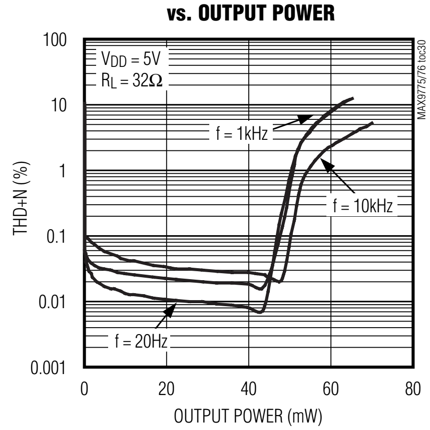










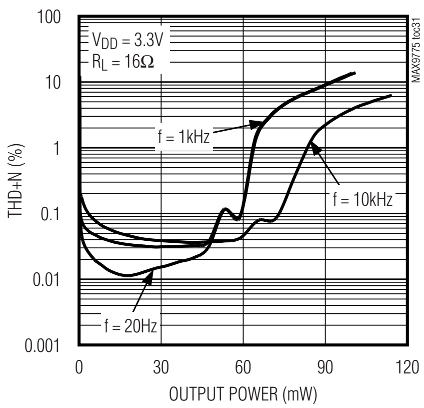


2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

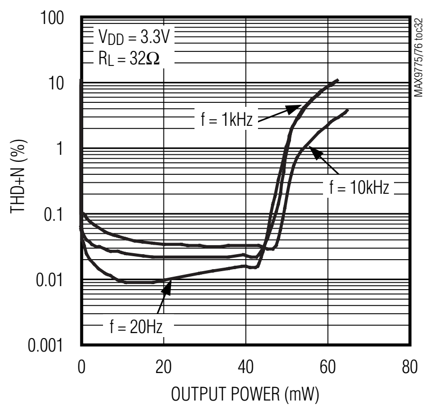
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I²C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

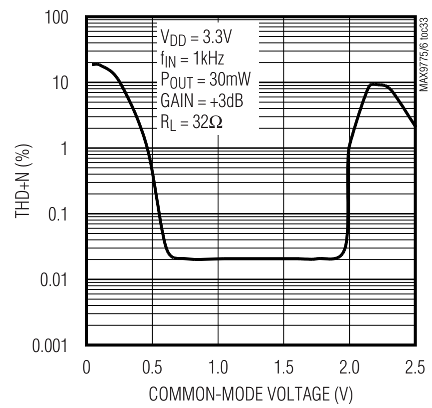
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



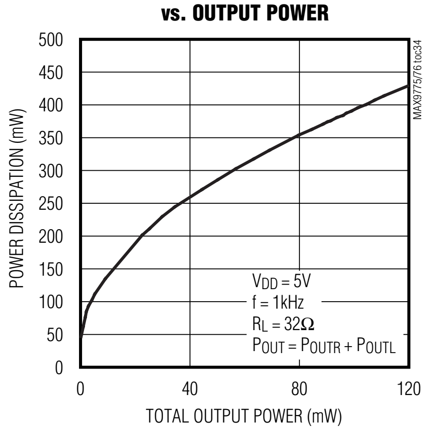
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



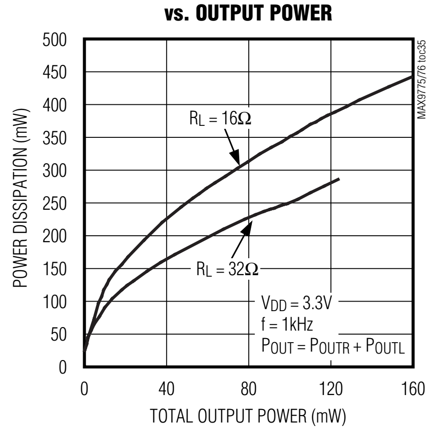
TOTAL HARMONIC DISTORTION PLUS NOISE vs. COMMON-MODE VOLTAGE



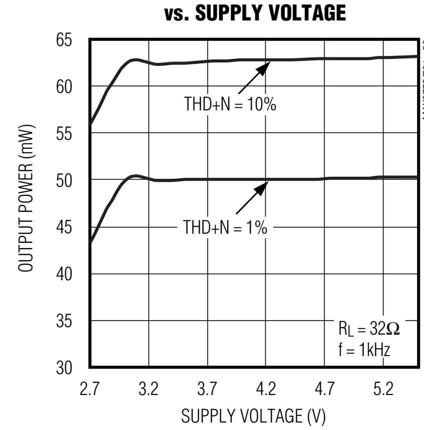
POWER DISSIPATION vs. OUTPUT POWER



POWER DISSIPATION vs. OUTPUT POWER



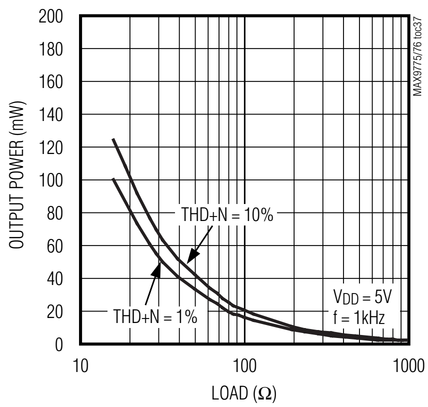
OUTPUT POWER vs. SUPPLY VOLTAGE



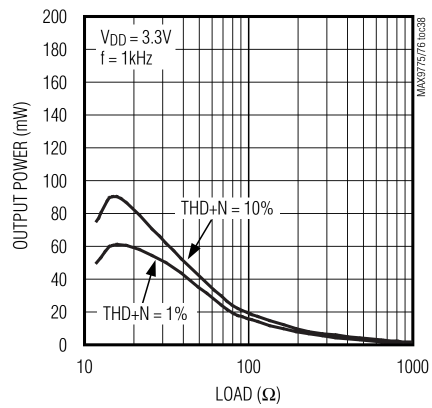
Typical Operating Characteristics (continued)

(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)

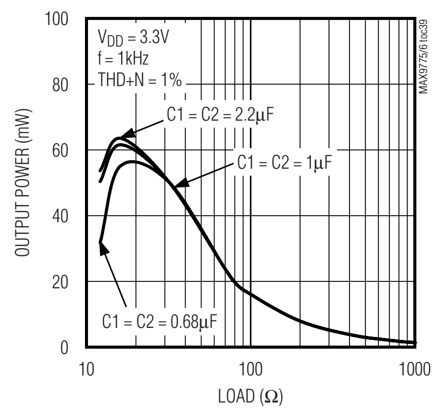
OUTPUT POWER vs. LOAD



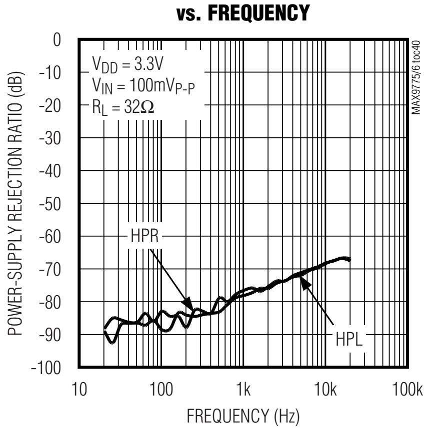
OUTPUT POWER vs. LOAD



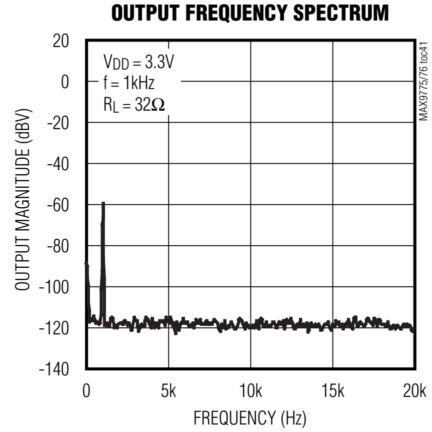
OUTPUT POWER vs. LOAD RESISTANCE AND CHARGE-PUMP CAPACITOR SIZE



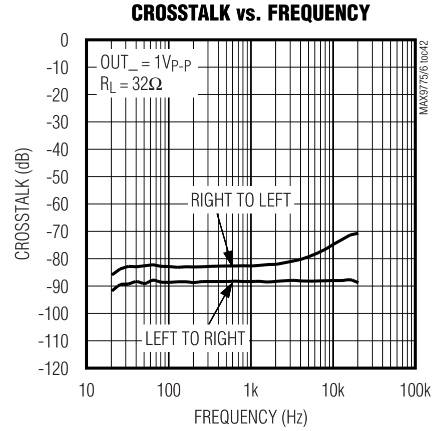
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OUTPUT FREQUENCY SPECTRUM



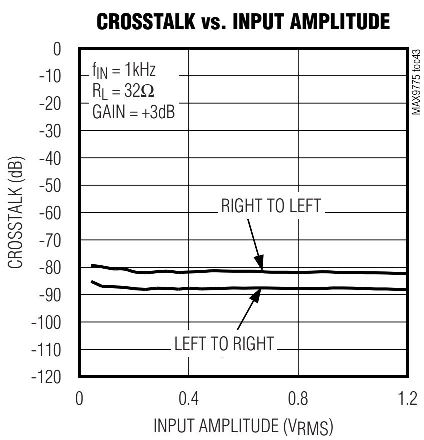
CROSSTALK vs. FREQUENCY

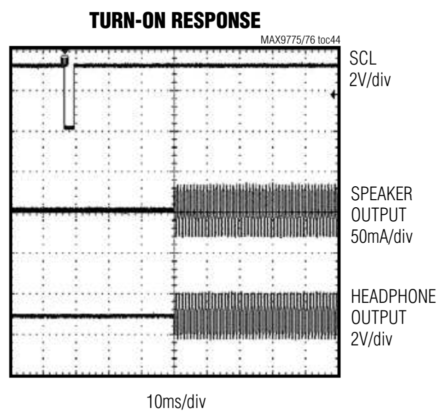


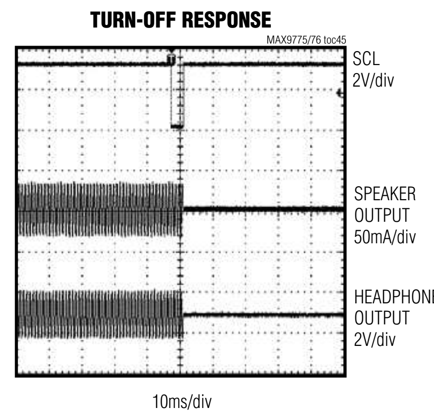
2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

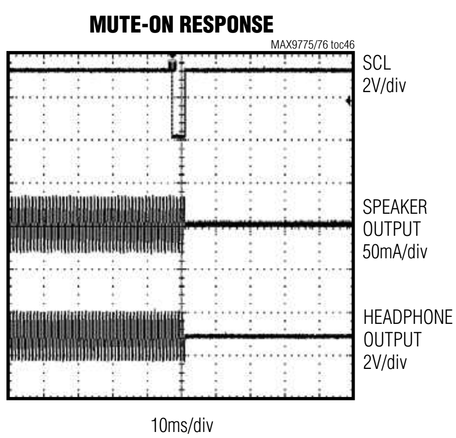
Typical Operating Characteristics (continued)

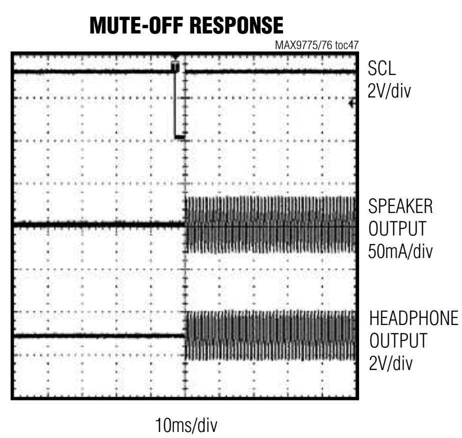
(V_{DD} = PV_{DD} = CPV_{DD} = 3.3V, GND = PGND = CPGND = 0V, $\overline{SHDN}$ = V_{DD}, I^2C default gain settings (INA gain = +20dB, INB gain = INC gain = 0dB, volume setting = 0dB, mono path gain = 0dB, $\overline{SHDN}$ = 1, SSM = 1). Speaker load resistors (R_{LSP}) are terminated between OUT_+ and OUT_-, headphone load resistors are terminated to GND, unless otherwise stated. C1 = C2 = C3 = 1µF. T_A = +25°C, unless otherwise noted.)











Pin Description—MAX9775

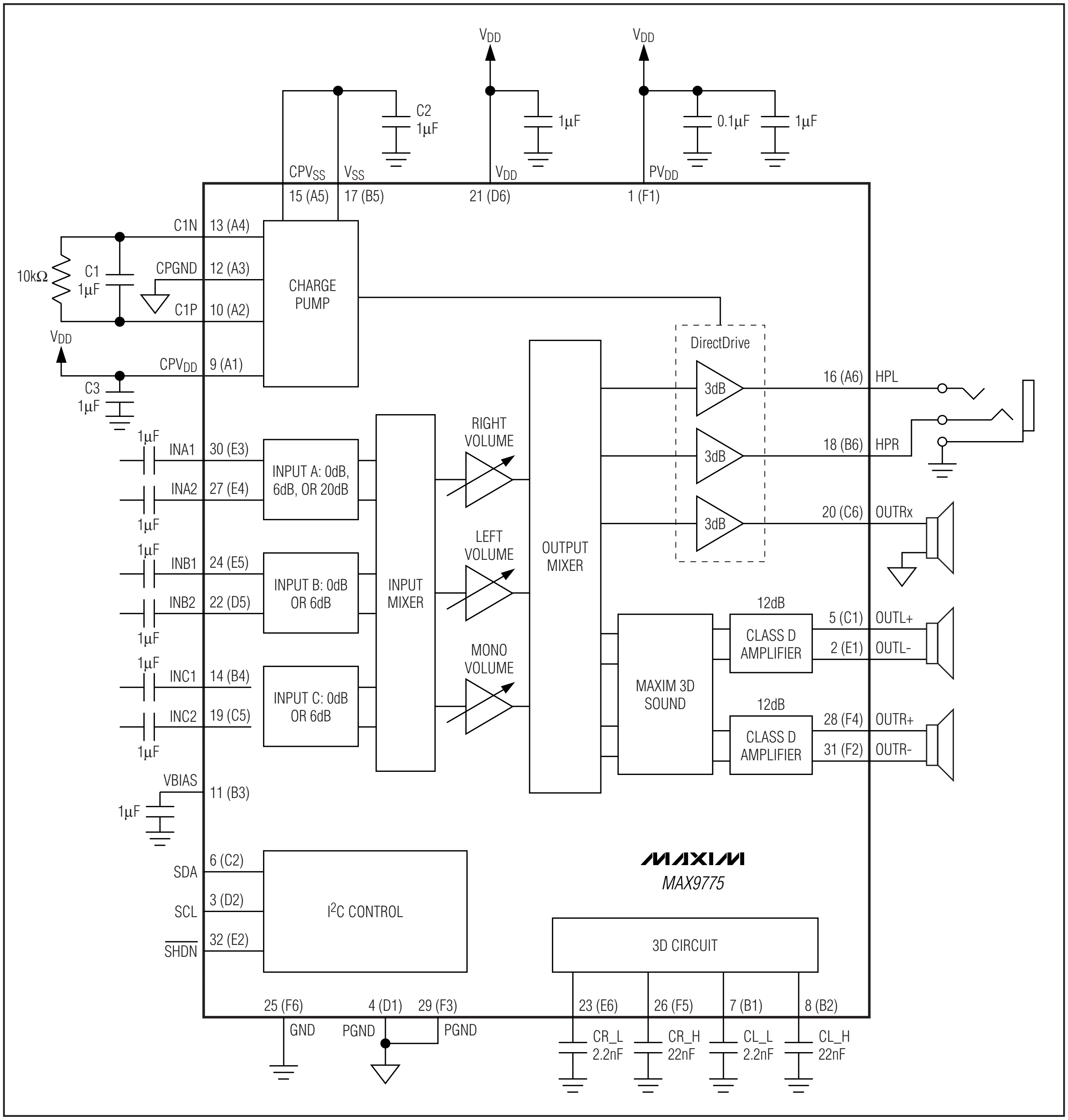
PIN	NAME	FUNCTION
F1	PV_{DD}	Class D Power Supply
E1	OUTL-	Negative Left-Speaker Output
D2	SCL	Serial Clock Input. Connect a 1kΩ pullup resistor from SCL to V_{DD}.
D1, F3	PGND	Power Ground
C1	OUTL+	Positive Left-Speaker Output
C2	SDA	Serial Data Input. Connect a 1kΩ pullup resistor from SDA to V_{DD}.
B1	CL_L	3D External Capacitor 3. Connect a 2.2nF capacitor to GND.
B2	CL_H	3D External Capacitor 4. Connect a 22nF capacitor to GND.
A1	CPV_{DD}	Charge-Pump Power Supply
A2	C1P	Charge-Pump Flying Capacitor Positive Terminal
B3	VBIAS	Common-Mode Bias
A3	CPGND	Charge-Pump GND
A4	C1N	Charge-Pump Flying Capacitor Negative Terminal
B4	INC1	Input C1. Left input or positive input (see Table 5a).
A5	CPV_{SS}	Charge-Pump Output. Connect to V_{SS}.
A6	HPL	Left Headphone Output
B5	V_{SS}	Headphone Amplifier Negative Power Supply. Connect to CPV_{SS}.
B6	HPR	Right Headphone Output
C5	INC2	Input C2. Right input or negative input (see Table 5a).
C6	OUTRx	Mono Receiver Output
D6	V_{DD}	Analog Power Supply
D5	INB2	Input B2. Right input or negative input (see Table 5a).
E6	CR_L	3D External Capacitor 1. Connect a 2.2nF capacitor to GND.
E5	INB1	Input B1. Left input or positive input (see Table 5a).
F6	GND	Analog Ground
F5	CR_H	3D External Capacitor 2. Connect a 22nF capacitor to GND.
E4	INA2	Input A2. Right input or negative input (see Table 5a).
F4	OUTR+	Positive Right Speaker Output
E3	INA1	Input A1. Left input or positive input (see Table 5a).
F2	OUTR-	Negative Right Speaker Output
E2	$\overline{SHDN}$	Active-Low Hardware Shutdown
—	EP	Exposed Pad. The external pad lowers the package's thermal impedance by providing a direct heat conduction path from the die to the PCB. The exposed pad is internally connected to GND. Connect the exposed thermal pad to the GND plane.

2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

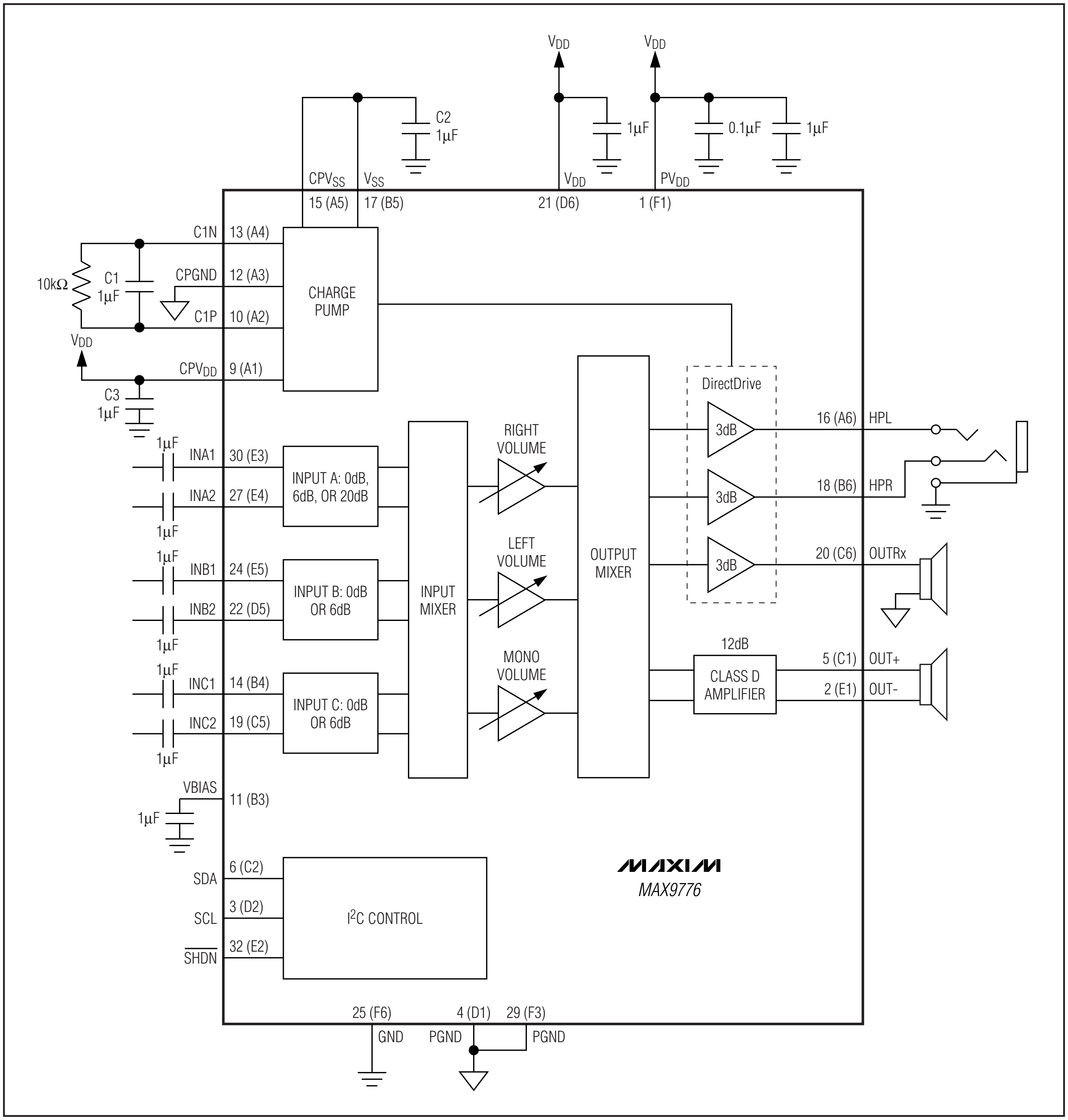
Pin Description—MAX9776

PIN		NAME	FUNCTION
TQFN	UCSP		
1	F1	PV_{DD}	Class D Power Supply
2	E1	OUT-	Negative Left-Speaker Output
3	D2	SCL	Serial Clock Input. Connect a 1kΩ pullup resistor from SCL to V_{DD}.
4, 29	D1, F3	PGND	Power Ground
5	C1	OUT+	Positive Left-Speaker Output
6	C2	SDA	Serial Data Input. Connect a 1kΩ pullup resistor from SDA to V_{DD}.
7, 8, 23, 26, 28, 31	B1, B2, E6, F2, F4, F5	I.C.	Internal Connection. Leave unconnected. This pin is internally connected to the signal path. Do not connect together or to any other pin.
9	A1	CPV_{DD}	Charge-Pump Power Supply
10	A2	C1P	Charge-Pump Flying Capacitor Positive Terminal
11	B3	VBIAS	Common-Mode Bias
12	A3	CPGND	Charge-Pump GND
13	A4	C1N	Charge-Pump Flying Capacitor Negative Terminal
14	B4	INC1	Input C1. Left input or positive input (see Table 5a).
15	A5	CPV_{SS}	Charge-Pump Output. Connect to V_{SS}.
16	A6	HPL	Left Headphone Output
17	B5	V_{SS}	Headphone Amplifier Negative Power Supply. Connect to CPV_{SS}.
18	B6	HPR	Right Headphone Output
19	C5	INC2	Input C2. Right input or negative input (see Table 5a).
20	C6	OUTRx	Mono Receiver Output
21	D6	V_{DD}	Analog Power Supply
22	D5	INB2	Input B2. Right input or negative input (see Table 5a).
24	E5	INB1	Input B1. Left input or positive input (see Table 5a).
25	F6	GND	Analog Ground
27	E4	INA2	Input A2. Right input or negative input (see Table 5a).
30	E3	INA1	Input A1. Left input or positive input (see Table 5a).
32	E2	$\overline{SHDN}$	Active-Low Hardware Shutdown
EP	—	EP	Exposed Pad. The external pad lowers the package's thermal impedance by providing a direct heat conduction path from the die to the PCB. The exposed pad is internally connected to GND. Connect the exposed thermal pad to the GND plane.

Typical Application Circuits



Typical Application Circuits (continued)



Detailed Description

The MAX9775/MAX9776 ultra-low-EMI, filterless, Class D audio power amplifiers feature several improvements to switch-mode amplifier technology. The MAX9775/MAX9776 feature active emissions limiting circuitry to reduce EMI. Zero dead-time technology maintains state-of-the-art efficiency and THD+N performance by allowing the output FETs to switch simultaneously without cross-conduction. A unique filterless modulation scheme and spread-spectrum modulation create compact, flexible, low-noise, efficient audio power amplifiers while occupying minimal board space. The differential input architecture reduces common-mode noise pickup with or without the use of input-coupling capacitors. The MAX9775/MAX9776 can also be configured as single-ended input amplifiers without performance degradation.

The MAX9775/MAX9776 feature three fully differential input pairs (INA_, INB_, INC_) that can be configured as stereo single-ended or mono differential inputs. I^{2}C provides control for input configuration, volume level, and mixer configuration. The MAX9775's 3D enhancement feature widens the stereo sound field to improve stereo imaging when stereo speakers are placed in close proximity.

DirectDrive allows the headphone and mono receiver amplifiers to output ground-referenced signals from a single supply, eliminating the need for large DC-blocking capacitors. Comprehensive click-and-pop suppression minimizes audible transients during the turn-on and turn-off of amplifiers.

Class D Speaker Amplifier

Comparators monitor the audio inputs and compare the complementary input voltages to a sawtooth waveform. The comparators trip when the input magnitude of the sawtooth exceeds their corresponding input voltage. The active emissions limiting circuitry slightly reduces the turn-on rate of the output H-bridge by slew-rate limiting the comparator output pulse. Both comparators reset at a fixed time after the rising edge of the second comparator trip point, generating a minimum-width pulse ($t_{ON(MIN)}$,100ns typ) at the output of the second comparator (Figure 1). As the input voltage increases or decreases, the duration of the pulse at one output increases while the other output pulse duration remains the same. This causes the net voltage across the speaker (V_{OUT+} - V_{OUT-}) to change. The minimum-width pulse helps the devices to achieve high levels of linearity.

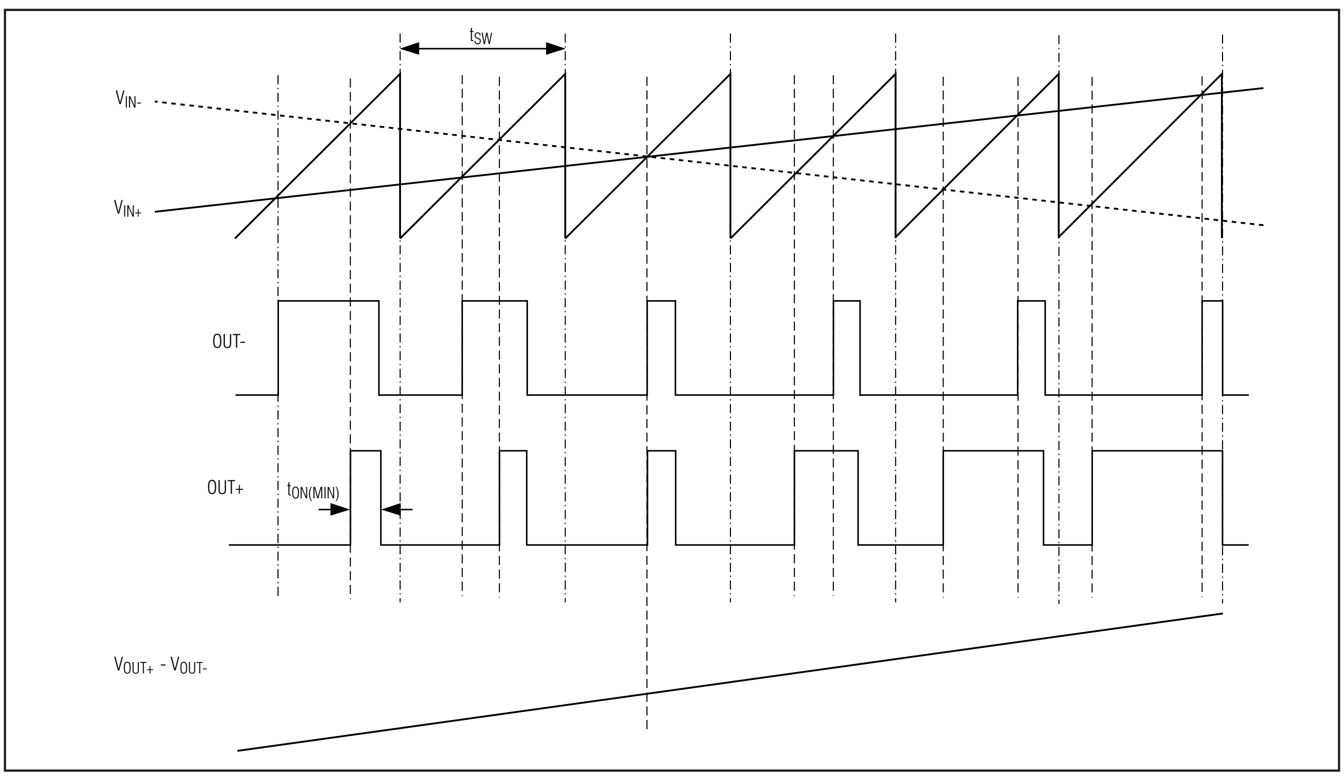


Figure 1. Outputs with an Input Signal Applied

2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

Operating Modes

Fixed-Frequency Modulation

The MAX9775/MAX9776 feature a fixed-frequency modulation mode with a 1.1MHz switching frequency, set through the I^2C interface (Table 2). In fixed-frequency modulation mode, the frequency spectrum of the Class D output consists of the fundamental switching frequency and its associated harmonics (see the Wideband Output Spectrum Fixed-Frequency Mode graph in the *Typical Operating Characteristics*).

Spread-Spectrum Modulation

The MAX9775/MAX9776 feature a unique spread-spectrum modulation that flattens the wideband spectral components. Proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency (see the *Typical Operating Characteristics*). Select spread-spectrum modulation mode through the I^2C interface (Table 2). In spread-spectrum modulation mode, the switching frequency varies randomly by ±30kHz around the center frequency (1.16MHz). The modulation scheme remains the same, but the period of the sawtooth waveform changes from cycle to cycle (Figure 2). Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes (see Figure 3).

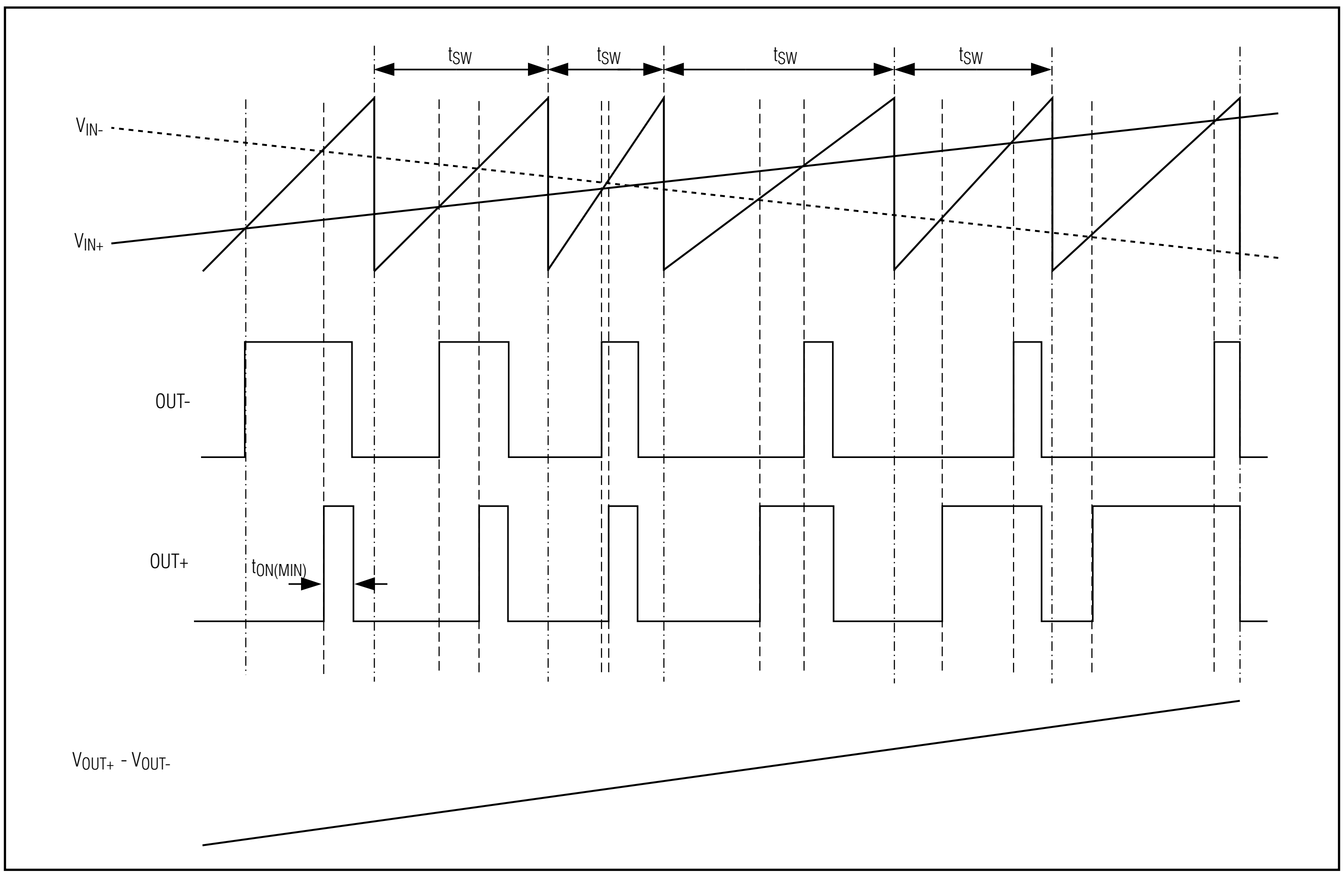


Figure 2. Output with an Input Signal Applied (Spread-Spectrum Modulation Mode)

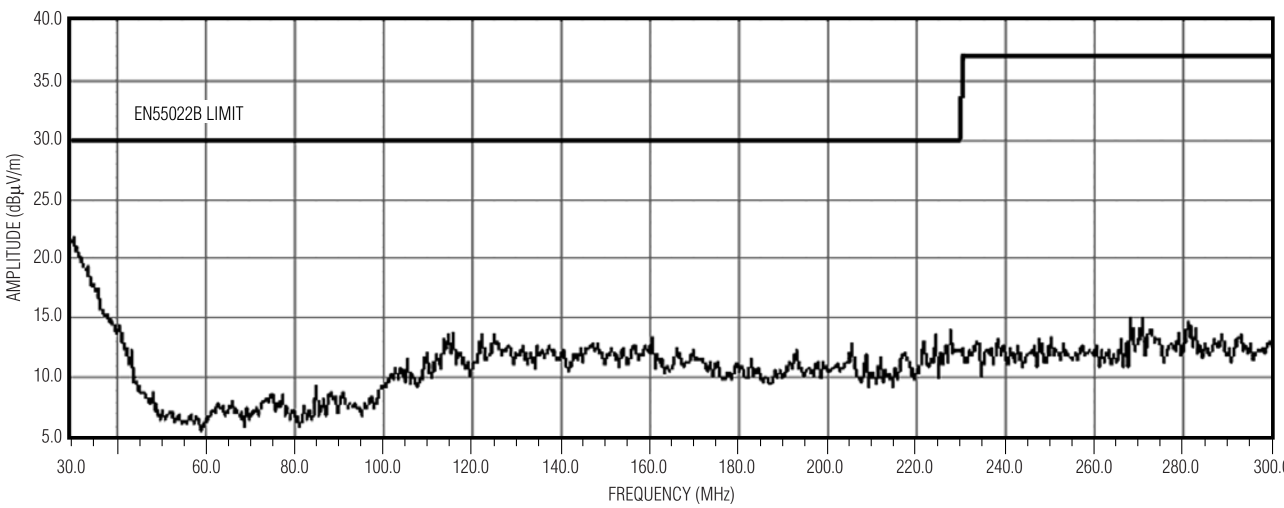


Figure 3. EMI with 76mm of Speaker Cable

2 x 1.5W, Stereo Class D Audio Subsystem with DirectDrive Headphone Amplifier

Filterless Modulation/Common-Mode Idle

The MAX9775/MAX9776 use Maxim's unique modulation scheme that eliminates the LC filter required by traditional Class D amplifiers, improving efficiency, reducing component count, conserving board space and system cost. Conventional Class D amplifiers output a 50% duty-cycle square wave when no signal is present. With no filter, the square wave appears across the load as a DC voltage, resulting in finite load current, increasing power consumption, especially when idling. When no signal is present at the input of the MAX9775/MAX9776, the outputs switch as shown in Figure 4. Because the MAX9775/MAX9776 drive the speaker differentially, the two outputs cancel each other, resulting in no net idle mode voltage across the speaker, minimizing power consumption.

DirectDrive

Traditional single-supply headphone amplifiers have outputs biased at a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the headphone outputs of the MAX9775/MAX9776 to be biased at GND, almost doubling dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220µF, typ) tantalum capacitors, the MAX9775/MAX9776 charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier. See the Output Power vs. Load Resistance and Charge-Pump Capacitor Size graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes. There is a low DC voltage on the amplifier outputs due to amplifier offset. However, the offset of the MAX9775/MAX9776 is typically 1.4mV, which, when combined with a 32Ω load, results in less than 44nA of DC current flow to the headphones.

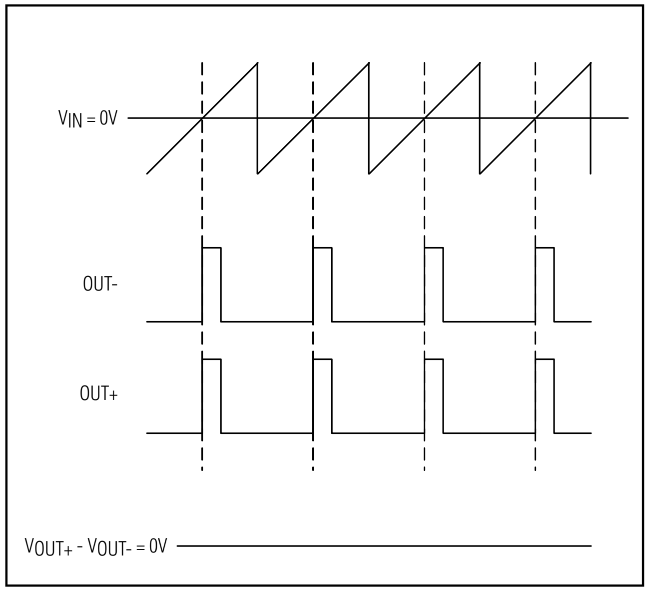


Figure 4. Outputs with No Input Signal

In addition to the cost and size disadvantages of the DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal. Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises some issues:

1) The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design.
2) During an ESD strike, the driver's ESD structures are the only path to system ground. Thus, the amplifier must be able to withstand the full ESD strike.
3) When using the headphone jack as a lineout to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers.

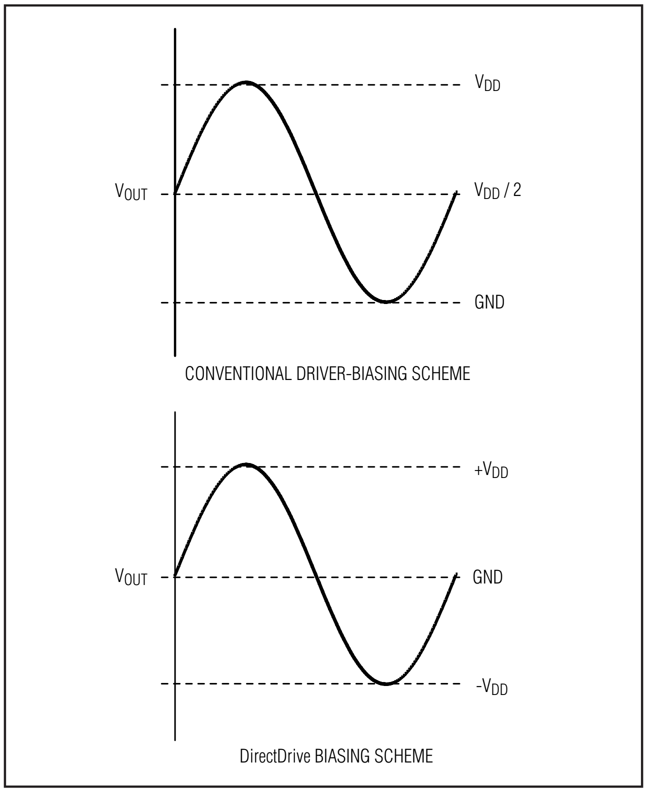


Figure 5. Traditional Amplifier Output vs. MAX9775/MAX9776 DirectDrive Output

Charge Pump

The MAX9775/MAX9776 feature a low-noise charge pump. The switching frequency of the charge pump is half the switching frequency of the Class D amplifier, regardless of the operating mode. The nominal switching frequency is well beyond the audio range, and thus does not interfere with the audio signals, resulting in an SNR of 93dB. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C2 (see the *Typical Application Circuits*). The charge pump is active in both speaker and headphone modes.

3D Enhancement

The MAX9775 features a 3D stereo enhancement function, allowing the MAX9775 to widen the stereo sound field and immerse the listener in a cleaner, richer sound experience. Note the MAX9776, mono Class D speaker amplifier does not feature 3D stereo enhancement.

As stereo speaker applications become more compact, the quality of stereophonic sound is jeopardized.

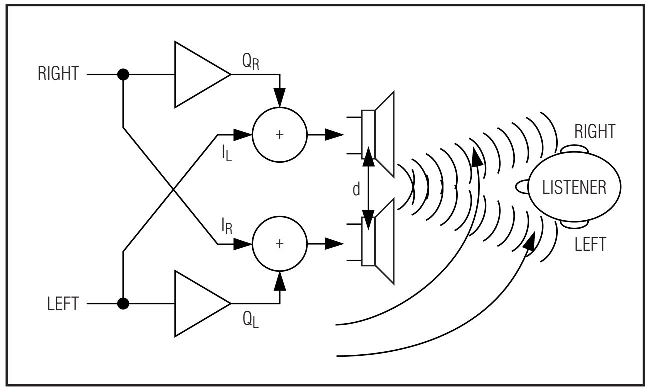


Figure 6. MAX9775 3D Stereo Enhancement

With Maxim's 3D stereo enhancement, it is possible to emulate stereo sound in situations where the speakers must be positioned close together. As shown in Figure 6, wave interference can be used to cancel the left channel in the vicinity of the listener's right ear and vice versa. This technique can yield an apparent separation between the speakers that is a factor of four or greater than the actual physical separation.

The external capacitors CL_L, CL_H, CR_L, and CR_H set the starting and stopping range of the 3D effect. CL_H and CR_H are for the lower limit (in the MAX9775 *Typical Application Circuit*, it is 1kHz), CR_L and CL_L are for the higher limit (10kHz). The internal resistor is typically 7kΩ and the frequencies are calculated as:

$$3D\_START = \frac{1}{2\pi RC}$$

where R = 7kΩ and C = CR_H and CL_H.

$$3D\_STOP = \frac{1}{2\pi RC}$$

where R = 7kΩ and C = CR_L and CL_L.

For example, with CR_L = CL_L = 2.2nF and CR_H = CL_H = 22nF, the 3D start frequency is 1kHz and the 3D stop frequency is 10kHz.

Enabling the 3D sound effect results in an apparent 6dB gain because the internal left and right signals are mixed together. This gain can be nulled by volume adjusting the left and right signals. The volume control can be programmed through the I^2C-compatible interface to compensate for the extra 6dB increase in gain. For example, if the right and left volume controls are set for a maximum gain 0dB (11111 in Table 7, IN+6dB = 0 from Table 10) before the 3D effect is activated, the volume control should be programmed to -6dB (11001 in Table 7) immediately after the 3D effect has been activated.

Signal Path

The audio inputs of the MAX9775/MAX9776—INA, INB, and INC—are preamplified and then mixed by the input mixer to create three internal signals: Left (L), Right (R), and Mono (M). Tables 5a and 5b show how the inputs are mixed to create L, R, and M. These signals are then independently volume adjusted by the L, R, and M volume control and routed to the output mixer. The output mixer mixes the internal L, R, and M signals to create a variety of audio mixes that are output to the headphone speaker and mono receiver amplifiers. Figure 6 shows the signal path that the audio signals take.

Signal amplification takes place in three stages. In the first stage, the inputs (INA, INB, and INC) are preamplified. The amount by which each input is amplified is determined by the bits INA+20dB (B4 in the Input Mode Control Register) and IN+6dB (B3 in the Global Control Register). After preamplification, they are mixed in the Input Mixer to create the internal signals L, R, and M.

In the second stage of amplification, the internal L, R, and M signals are independently volume adjusted.

Finally, each output amplifier has its own internal gain. The speaker, headphone, and mono receiver amplifiers have fixed gains of 12dB, 3dB, and 3dB, respectively.

Current-Limit and Thermal Protection

The MAX9775/MAX9776 feature current limiting and thermal protection to protect the device from short circuits and overcurrent conditions. The headphone amplifier pulses in the event of an overcurrent condition with a pulse every 100µs as long as the condition is present. Should the current still be high, the above cycle is repeated. The speaker amplifier current-limit protection clamps the output current without shutting down the output. This can result in a distorted output. Current is limited to 1.6A in the speaker amplifiers and 170mA in the headphone and mono receiver amplifiers.

The MAX9775/MAX9776 have thermal protection that disables the device at +150°C until the temperature decreases to +120°C.

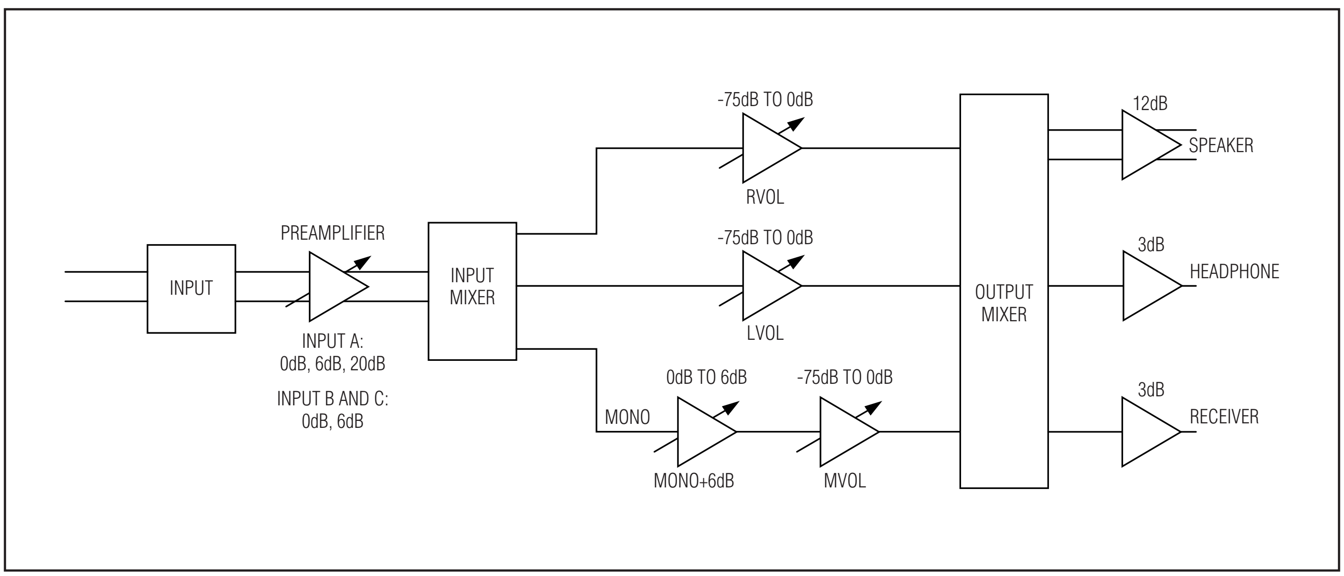


Figure 7. Signal Path

Click-and-Pop Suppression

In conventional single-supply headphone amplifiers, the output-coupling capacitor is a major contributor of audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, during shutdown, the capacitor is discharged to GND. This results in a DC shift across the capacitor, which, in turn, appears as an audible transient at the speaker. Since the MAX9775/MAX9776 headphone amplifier does not require output-coupling capacitors, this problem does not arise.

In most applications, the output of the preamplifier driving the MAX9775/MAX9776 has a DC bias of typically half the supply. During startup, the input-coupling capacitor is charged to the preamplifier's DC bias voltage, resulting in a DC shift across the capacitor and an audible click/pop. An internal delay of 30ms eliminates the click/pop caused by the input filter.

Shutdown

The MAX9775/MAX9776 feature a 0.1µA hard shutdown mode that reduces power consumption to extend battery life and a soft shutdown where current consumption is typically 8.5µA. Hard shutdown is controlled by connecting the $\overline{SHDN}$ pin to GND, disabling the amplifiers, bias circuitry, charge pump, and I²C. In shutdown, the headphone amplifier output impedance is 1.4kΩ and the speaker output impedance is 300kΩ. Similarly, the MAX9775/MAX9776 enter soft-shutdown when the $\overline{SHDN}$ bit = 0 (see Table 2). The I²C interface is active and the contents of the command register are not affected when in soft-shutdown. This allows the master to write to the MAX9775/MAX9776 while in shutdown. The I²C interface is completely disabled in hardware shutdown. When the MAX9775/MAX9776 are re-enabled the default settings are applied (see Table 3).

I²C Interface

The MAX9775/MAX9776 feature an I²C 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9775/MAX9776 and the master at clock rates up to 400kHz. Figure 8 shows the 2-wire interface timing diagram. The MAX9775/MAX9776 are receive-only slave devices relying on the master to generate the SCL signal. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. The MAX9775/MAX9776 cannot write to the SDA bus except to acknowledge the receipt of data from the master. The MAX9775/MAX9776 will not acknowledge a read command from the master.

A master device communicates to the MAX9775/MAX9776 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9775/MAX9776 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9775/MAX9776 SCL line operates as an input only. A pullup resistor (greater than 500Ω) is required on SCL if there are multiple masters on the bus or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9775/MAX9776 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

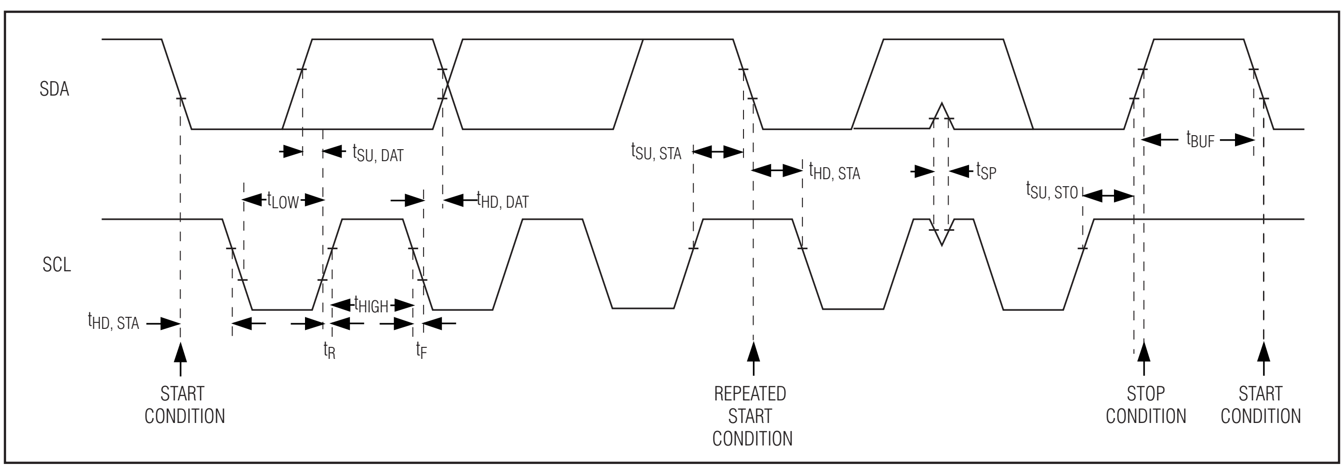


Figure 8. 2-Wire Serial-Interface Timing Diagram