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# MAX98355A/MAX98355B

# PCM Input Class D Audio Power Amplifiers

## General Description

The MAX98355A/MAX98355B are digital pulse-code modulation (PCM) input Class D power amplifiers that provide Class AB audio performance with Class D efficiency. These ICs offer five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) set by a single gain-select input (GAIN).

The digital audio interface is highly flexible with the MAX98355A supporting I$^2$S data and the MAX98355B supporting left-justified data. Both ICs support time division multiplexed (TDM) data. The digital audio interface accepts sample rates ranging from 8kHz to 96kHz for all supported data formats. The ICs can be configured to produce a left channel, right channel, or (left + right)/2 output from the stereo input data. The ICs operate using 16/24/32-bit data for I$^2$S and left justified modes as well as 16-bit data with up to four slots when using TDM mode. The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count of the ICs.

The ICs also feature a very high wideband jitter tolerance (12ns typ) on BCLK and LRCLK to provide robust operation.

Active emissions-limiting, edge-rate limiting, and over-shoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution.

The ICs are available in a 9-pin WLP package (1.345mm x 1.435mm x 0.64mm) and are specified over the -40°C to +85°C temperature range.

## Applications

Cellular Phones

Tablets

Portable Media Players

Notebook Computers
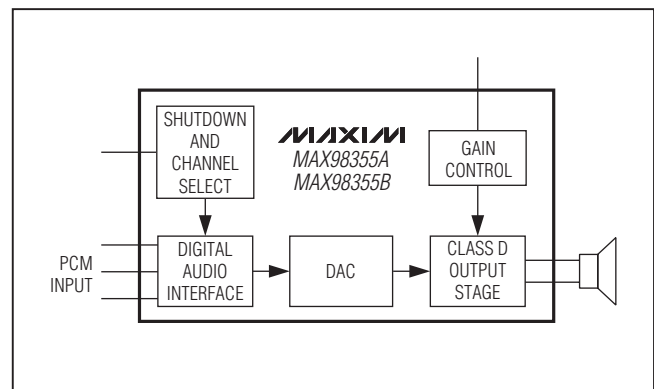
*Ordering Information* **appears at end of data sheet.**

*Functional Diagram* **appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX98355A.related**.*

## Features

♦ **Single-Supply Operation (2.5V to 5.5V)**

♦ **3.2W Output Power into 4Ω at 5V**

♦ **2.2mA Quiescent Current**

♦ **92% Efficiency (R$_L$ = 8Ω, P$_{OUT}$ = 900mW, V$_{DD}$ = 3.7V)**

♦ **25µV$_{RMS}$ Output Noise (A$_V$ = 15dB)**

♦ **Low 0.013% THD+N at 1kHz**

♦ **No MCLK Required**

♦ **Sample Rates of 8kHz to 96kHz**

♦ **Supports Left, Right, or (Left + Right)/2 Outputs**

♦ **Sophisticated Edge Rate Control Enables Filterless Class D Outputs**

♦ **77dB PSRR at 217Hz**

♦ **Low RF Susceptibility Rejects TDMA Noise from GSM Radios**

♦ **Extensive Click-and-Pop Reduction Circuitry**

♦ **Robust Short-Circuit and Thermal Protection**

♦ **Available in Space-Saving Package: 1.345mm x 1.435mm WLP (0.4mm Pitch)**

## Simplified Block Diagram

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.**

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# PCM Input Class D Audio Power Amplifiers

## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$, LRCLK, BCLK, and DIN to GND .....................-0.3V to +6V
All Other Pins to GND .............................. -0.3V to ($V_{DD}$ + 0.3V)
Continuous Current In/Out of $V_{DD}$/GND/OUT_ ................ ±1.6A
Continuous Input Current (all other pins)........................ ±20mA
Duration of OUT_ Short Circuit to GND or $V_{DD}$........Continuous
Duration of OUTP Short to OUTN .............................Continuous

Continuous Power Dissipation ($T_A$ = +70°C)
    WLP (derate 13.7mW/°C above +70°C)...................1096mW
Junction Temperature ....................................................+150°C
Operating Temperature Range .........................-40°C to +85°C
Storage Temperature Range...........................-65°C to +150°C
Soldering Temperature (reflow) ......................................+230°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
    Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..........73°C/W
    Junction-to-Case Thermal Resistance ($\theta_{JC}$) ...............50°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage Range | $V_{DD}$ | Guaranteed by PSSR test | | 2.5 | | 5.5 | V |
| Undervoltage Lockout | UVLO | | | 1.5 | 1.8 | 2.2 | V |
| Quiescent Current | $I_{DD}$ | $T_A$ = +25°C | | | 2.5 | 3.3 | mA |
| | | $T_A$ = +25°C, $V_{DD}$ = 3.7V | | | 2.2 | 2.7 | |
| Shutdown Current | $I_{\overline{SHDN}}$ | $\overline{SD\_MODE}$ = 0V, $T_A$ = +25°C | | | 0.6 | 2 | µA |
| Standby Current | $I_{\overline{STNDBY}}$ | $\overline{SD\_MODE}$ = 1.8V, no BCLK, $T_A$ = +25°C | | | 300 | 400 | µA |
| Turn-On Time | $t_{ON}$ | Time from receipt of first clock cycle to full operation, including 6ms fade-in volume ramp | | | 7 | 7.5 | ms |
| Output Offset Voltage | $V_{OS}$ | $T_A$ = +25°C, gain = 15dB | | | ±0.3 | ±1.5 | mV |
| Click-and-Pop Level | $K_{CP}$ | Peak voltage, $T_A$ = +25°C, A-weighted, 32 samples per second (Note 3) | Into shutdown | | -66 | | dBV |
| | | | Out of shutdown | | -72 | | |
| Power-Supply Rejection Ratio | PSRR | $V_{DD}$ = 2.5V to 5.5V, $T_A$ = +25°C | | 60 | 75 | | dB |
| | | $T_A$ = +25°C (Notes 3, 4) | f = 217Hz, 200m$V_{P-P}$ ripple | | 77 | | |
| | | | f = 10kHz, 200m$V_{P-P}$ ripple | | 60 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Power (Note 3) | $P_{OUT}$ | THD+N 10%, gain = 12dB | $Z_{SPK}$ = 4Ω + 33µH | | 3.2 | | W |
| | | | $Z_{SPK}$ = 8Ω + 68µH | | 1.8 | | |
| | | | $Z_{SPK}$ = 8Ω + 68µH, $V_{DD}$ = 3.7V | | 0.93 | | |
| | | THD+N = 1%, gain = 12dB | $Z_{SPK}$ = 4Ω + 33µH | | 2.5 | | |
| | | | $Z_{SPK}$ = 8Ω + 68µH | | 1.4 | | |
| | | | $Z_{SPK}$ = 8Ω + 68µH, $V_{DD}$ = 3.7V | | 0.77 | | |
| Total Harmonic Distortion + Noise | THD+N | f = 1kHz, $P_{OUT}$ = 1W, $T_A$ = +25°C, $Z_{SPK}$ = 4Ω + 33µH | | | 0.02 | 0.06 | % |
| | | f = 1kHz, $P_{OUT}$ = 0.5W, $T_A$ = +25°C, $Z_{SPK}$ = 8Ω + 68µH | | | 0.013 | | |
| Dynamic Range | DR | A-weighted, $V_{RMS}$ = 2.54V, 24- or 32-bit data | | | 99 | | dB |
| Dynamic Range, High Gain | $DR_{HG}$ | A-weighted, gain = 15dB, $V_{RMS}$ = 4.55V (clipping), 24- or 32-bit data | | | 105 | | dB |
| Output Noise | $V_N$ | A-weighted, 24- or 32-bit data (Note 4) | | | 25 | | $µV_{RMS}$ |
| Output Noise, High Gain | $V_{N\_HG}$ | A-weighted, gain = 15dB, 24- or 32-bit data (Note 4) | | | 25 | | $µV_{RMS}$ |
| Gain (Relative to a 2.1dBV Reference Level) | $A_V$ | GAIN = GND through 100kΩ | | 14.5 | 15 | 15.5 | dB |
| | | GAIN = GND | | 11.5 | 12 | 12.5 | |
| | | GAIN = unconnected | | 8.5 | 9 | 9.5 | |
| | | GAIN = $V_{DD}$ | | 5.5 | 6 | 6.5 | |
| | | GAIN = $V_{DD}$ through 100kΩ | | 2.5 | 3 | 3.5 | |
| Current Limit | $I_{LIM}$ | | | | 2.8 | | A |
| Efficiency | h | $Z_{SPK}$ = 8Ω + 68µH, THD+N = 10%, f = 1kHz, gain = 12dB | | | 92 | | % |
| DAC Gain Error | | | | | 1 | | % |
| Frequency Response | | | | -0.2 | | +0.2 | dB |
| **DAC DIGITAL FILTERS** | | | | | | | |
| **VOICE MODE IIR LOWPASS FILTER (LRCLK < 30kHz)** | | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | | | 0.443 x $f_S$ | | Hz |
| | | -3dB cutoff | | | 0.446 x $f_S$ | | |
| Stopband Cutoff | $f_{SLP}$ | | | | | 0.464 x $f_S$ | Hz |
| Stopband Attenuation | | f > $f_{SLP}$ | | 75 | | | dB |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **AUDIO MODE FIR LOWPASS FILTER (30kHz < LRCLK < 50kHz)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | 0.43 x $f_S$ | | | Hz |
| | | -3dB cutoff | 0.47 x $f_S$ | | | |
| | | -6.02dB cutoff | 0.5 x $f_S$ | | | |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.58 x $f_S$ | Hz |
| Stopband Attenuation | | f > $f_{SLP}$ | 60 | | | dB |
| **AUDIO MODE FIR LOWPASS FILTER (LRCLK > 50kHz)** | | | | | | |
| Passband Cutoff | $f_{PLP}$ | Ripple limit cutoff | 0.24 x $f_S$ | | | Hz |
| | | -3dB cutoff | 0.31 x $f_S$ | | | |
| Stopband Cutoff | $f_{SLP}$ | | | | 0.477 x $f_S$ | Hz |
| Stopband Attenuation | | f < $f_{SLP}$ | 60 | | | dB |
| **DIGITAL AUDIO INTERFACE** | | | | | | |
| LRCLK Range 1 | $f_{S1}$ | | 7.6 | 8 | 8.4 | kHz |
| LRCLK Range 2 | $f_{S2}$ | | 15.2 | 16 | 16.8 | |
| LRCLK Range 3 | $f_{S3}$ | | 30.4 | 48 | 50.4 | |
| LRCLK Range 4 | $f_{S4}$ | | 83.8 | 96 | 100.8 | |
| Resolution | | I²S/left justified mode | | 16/24/32 | | Bits |
| | | TDM mode | | 16 | | |
| BCLK Frequency Range | $f_{BCLK}$ | BCLK must be 32, 48, or 64X of LRCLK | 0.2432 | | 6.4512 | MHz |
| BCLK High Time | $t_{BCLKH}$ | | 40 | | | ns |
| BCLK Low Time | $t_{BCLKL}$ | | 40 | | | ns |
| Maximum Low Frequency BCLK and LRCLK Jitter | | RMS jitter below 40kHz | | 0.5 | | ns |
| Maximum High Frequency BCLK and LRCLK Jitter | | RMS jitter above 40kHz | | 12 | | |
| Input High Voltage | $V_{IH}$ | Digital audio inputs | 1.3 | | | V |
| Input Low Voltage | $V_{IL}$ | Digital audio inputs | | | 0.6 | V |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IH}$, $I_{IL}$ | $V_{IN}$ = 0V, $V_{DD}$ = 5.5V, $T_A$ = +25°C | -1 | | +1 | µA |
| Input Capacitance | $C_{IN}$ | | | 12 | | pF |
| DIN to BCLK Setup Time | $t_{SETUP}$ | | 10 | | | ns |
| LRCLK to BCLK Setup Time | $t_{SYNCSET}$ | | 10 | | | |
| DIN to BCLK Hold Time | $t_{HOLD}$ | | 10 | | | |
| LRCLK to BCLK Hold Time | $t_{SYNCHOLD}$ | | 10 | | | |
| **SD_MODE COMPARATOR TRIP POINTS** | | | | | | |
| B0 | | See SD_MODE and shutdown operation for details | 0.08 | 0.16 | 0.355 | V |
| B1 | | | 0.65 | 0.77 | 0.825 | |
| B2 | | | 1.245 | 1.4 | 1.5 | |
| SD_MODE Pulldown Resistor | $R_{PD}$ | | 92 | 100 | 108 | kΩ |
| **GAIN COMPARATOR TRIP POINTS** | | | | | | |
| | $V_{GAIN}$ | $A_V$ = 3dB gain | 0.65 x $V_{DD}$ | | 0.85 x $V_{DD}$ | V |
| | | $A_V$ = 6dB gain | 0.9 x $V_{DD}$ | | $V_{DD}$ | |
| | | $A_V$ = 9dB gain | 0.4 x $V_{DD}$ | | 0.6 x $V_{DD}$ | |
| | | $A_V$ = 12dB gain | 0 | | 0.1 x $V_{DD}$ | |
| | | $A_V$ = 15dB gain | 0.15 x $V_{DD}$ | | 0.35 x $V_{DD}$ | |

**Note 2:** 100% production tested at $T_A$ = +25°C. Specifications over temperature limits are guaranteed by design.
**Note 3:** Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For $R_L$ = 8Ω, $L_L$ = 68µH. For $R_L$ = 4Ω, $L_L$ = 33µH.
**Note 4:** Digital silence used for input signal.

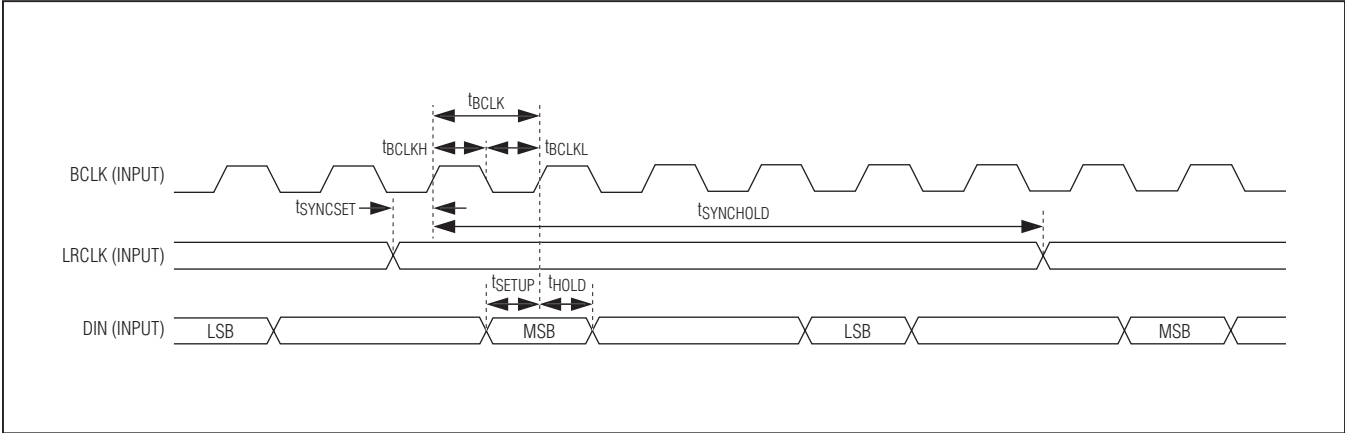# PCM Input Class D Audio Power Amplifiers



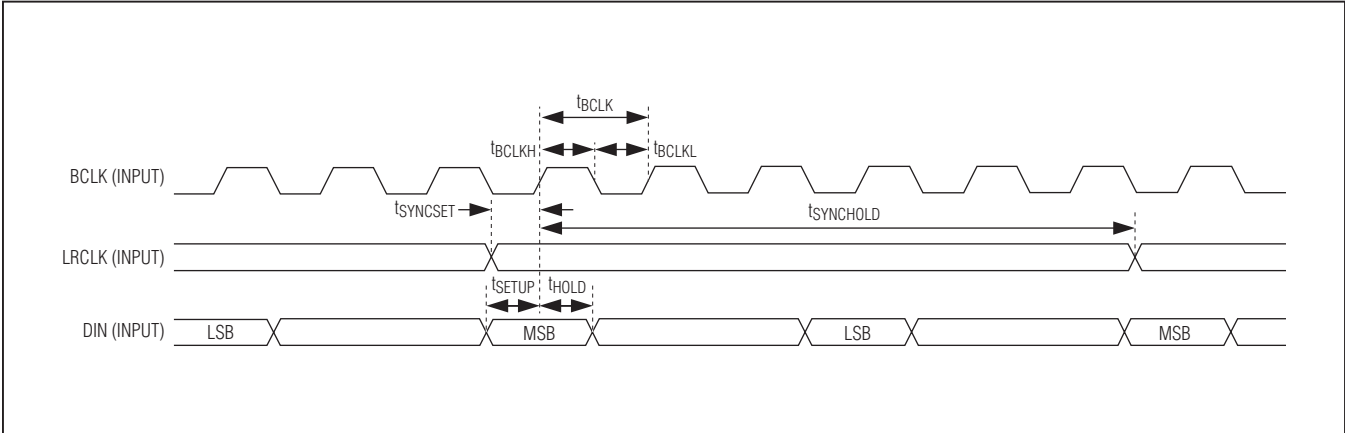Figure 1. I²S Audio Interface Timing Diagram (MAX98355A)



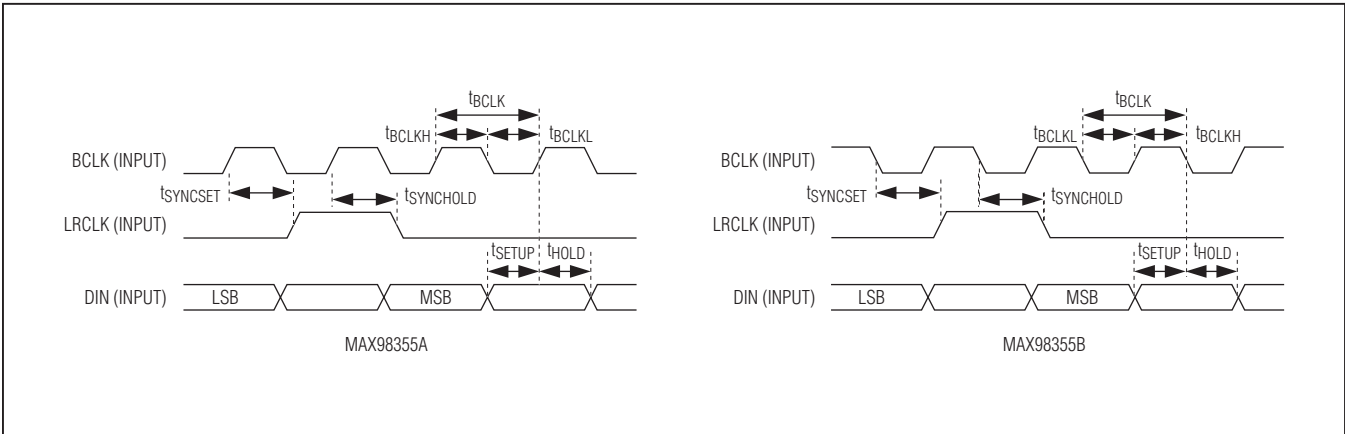Figure 2. Left-Justified Audio Interface Timing Diagram (MAX98355B)



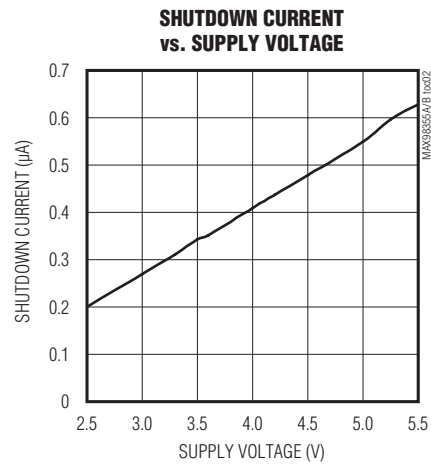Figure 3. TDM Audio Interface Timing Diagram

# PCM Input Class D Audio Power Amplifiers
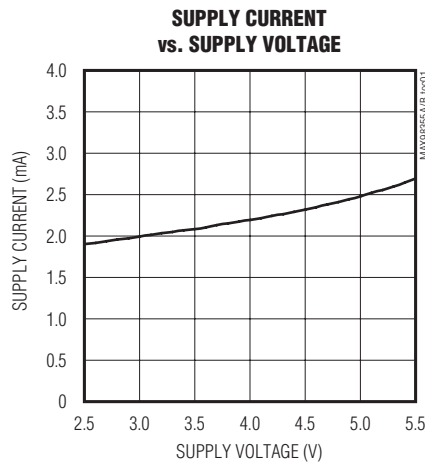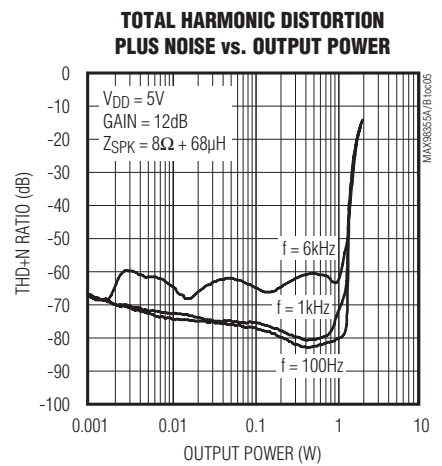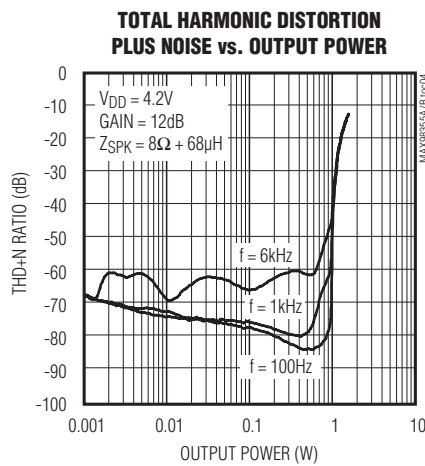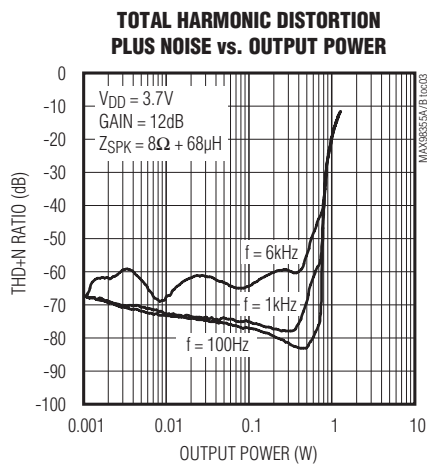
## *Typical Operating Characteristics*

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

### *General*



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE

### *Speaker Amplifier*



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68µH



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68µH



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER
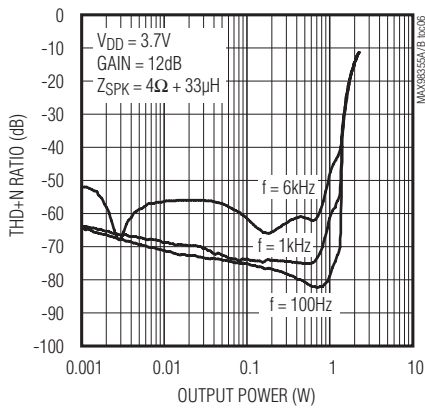
$V_{DD}$ = 5V
GAIN = 12dB
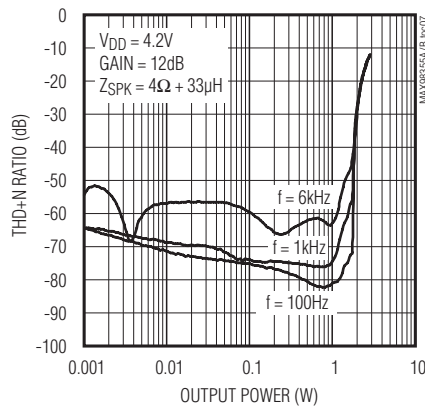$Z_{SPK}$ = 8Ω + 68µH

# PCM Input Class D Audio Power Amplifiers

## *Typical Operating Characteristics (continued)*

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)
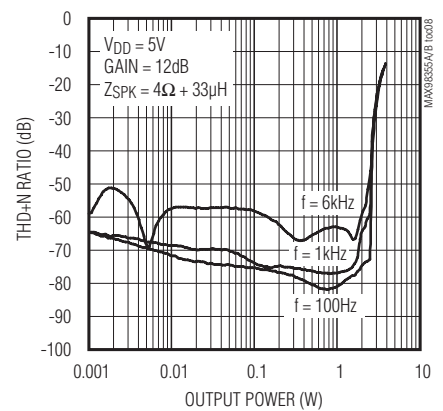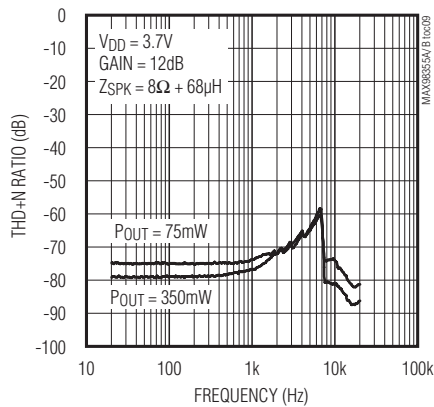
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER**

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33μH

f = 6kHz
f = 1kHz
f = 100Hz

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER**

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33μH

f = 6kHz
f = 1kHz
f = 100Hz

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER**

$V_{DD}$ = 5V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33μH

f = 6kHz
f = 1kHz
f = 100Hz

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68μH

$P_{OUT}$ = 75mW
$P_{OUT}$ = 350mW

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68μH

$P_{OUT}$ = 100mW
$P_{OUT}$ = 500mW

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

$V_{DD}$ = 5V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68μH

$P_{OUT}$ = 150mW
$P_{OUT}$ = 850mW
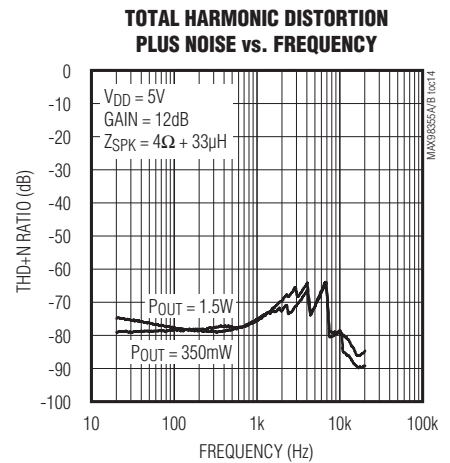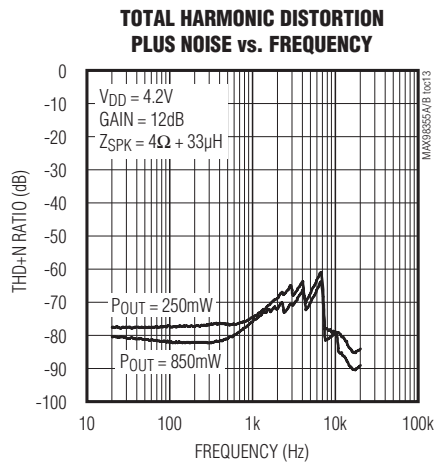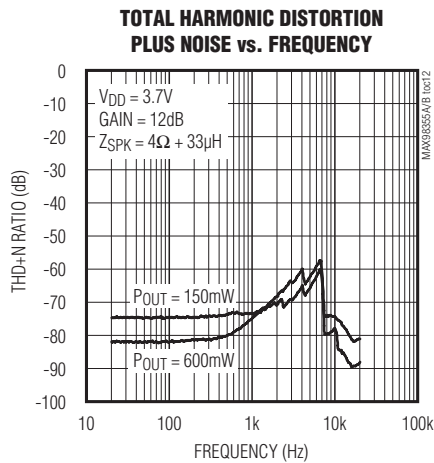
# PCM Input Class D Audio Power Amplifiers

## *Typical Operating Characteristics (continued)*

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH

$P_{OUT}$ = 150mW

$P_{OUT}$ = 600mW

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH

$P_{OUT}$ = 250mW

$P_{OUT}$ = 850mW

**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**

$V_{DD}$ = 5V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH

$P_{OUT}$ = 1.5W

$P_{OUT}$ = 350mW

**OUTPUT POWER vs. LOAD RESISTANCE**

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = $R_{LOAD}$ Ω + 68µH

THD+N = 10%

THD+N = 1%

**OUTPUT POWER vs. LOAD RESISTANCE**

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = $R_{LOAD}$ Ω + 68µH

THD+N = 10%

THD+N = 1%

**OUTPUT POWER vs. LOAD RESISTANCE**

$V_{DD}$ = 5V
GAIN = 12dB
$Z_{SPK}$ = $R_{LOAD}$ Ω + 68µH

THD+N = 10%

THD+N = 1%

# PCM Input Class D Audio Power Amplifiers

## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)
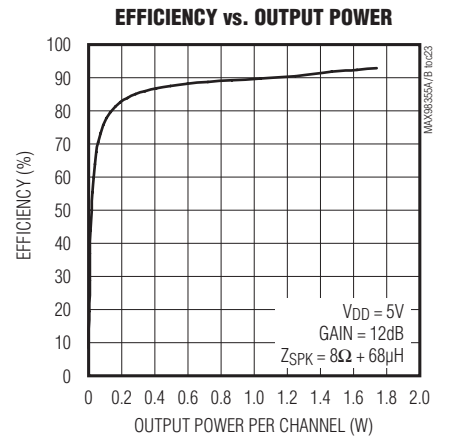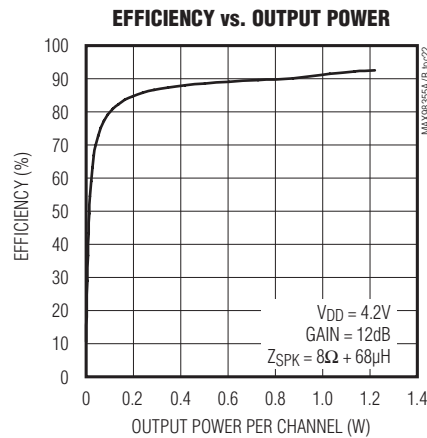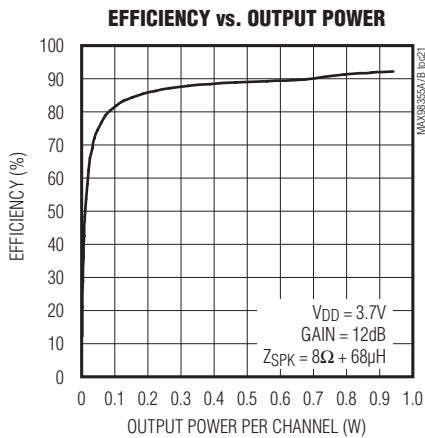
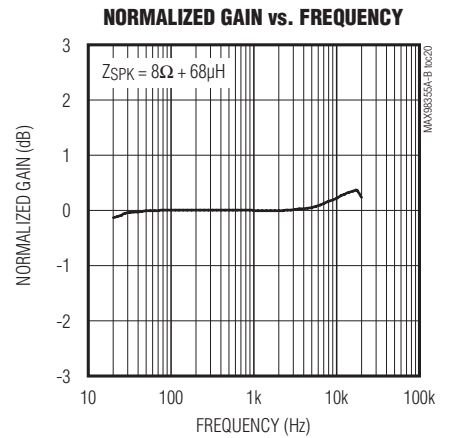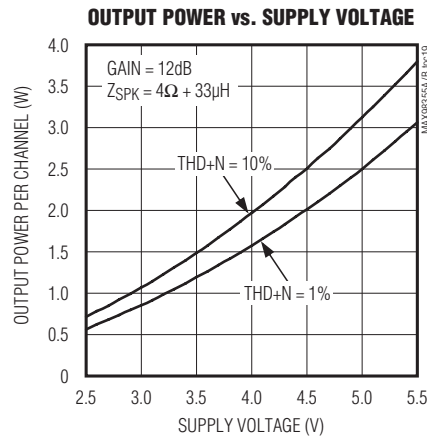**OUTPUT POWER vs. SUPPLY VOLTAGE**

GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68µH

THD+N = 10%

THD+N = 1%

**OUTPUT POWER vs. SUPPLY VOLTAGE**

GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH

THD+N = 10%

THD+N = 1%

**NORMALIZED GAIN vs. FREQUENCY**

$Z_{SPK}$ = 8Ω + 68µH

**EFFICIENCY vs. OUTPUT POWER**

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68µH

**EFFICIENCY vs. OUTPUT POWER**

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68µH

**EFFICIENCY vs. OUTPUT POWER**

$V_{DD}$ = 5V
GAIN = 12dB
$Z_{SPK}$ = 8Ω + 68µH
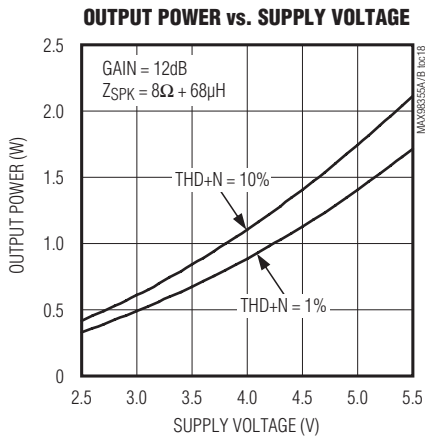
# PCM Input Class D Audio Power Amplifiers

## *Typical Operating Characteristics (continued)*

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)
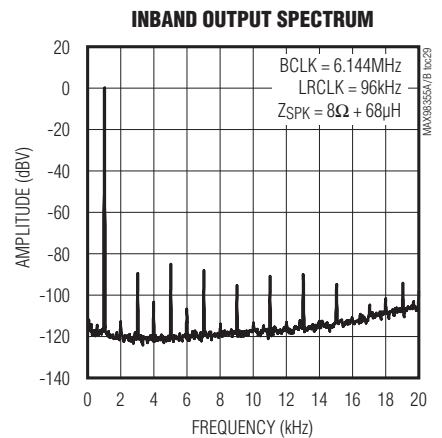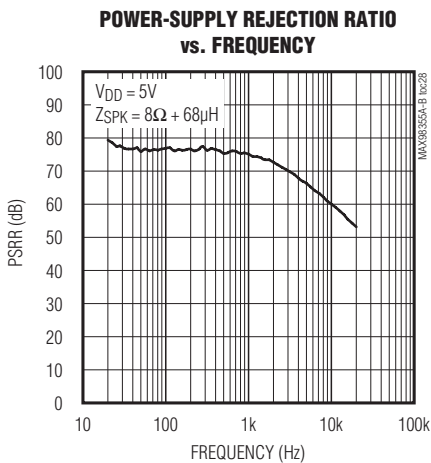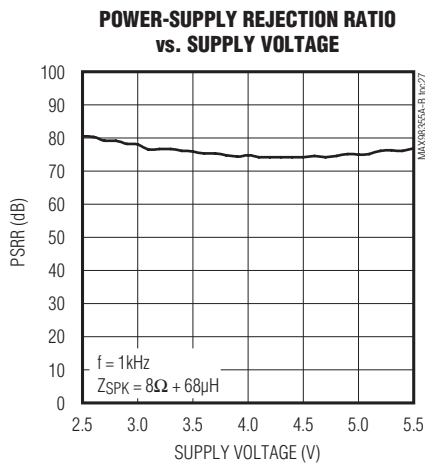


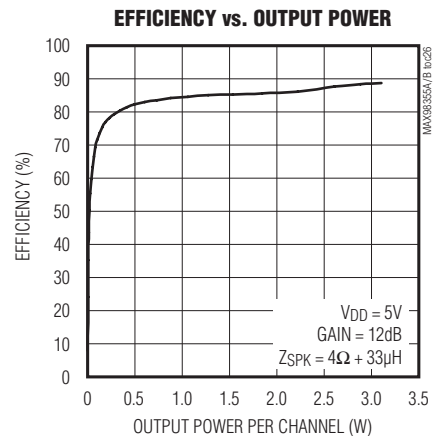EFFICIENCY vs. OUTPUT POWER

$V_{DD}$ = 3.7V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH



EFFICIENCY vs. OUTPUT POWER

$V_{DD}$ = 4.2V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH



EFFICIENCY vs. OUTPUT POWER

$V_{DD}$ = 5V
GAIN = 12dB
$Z_{SPK}$ = 4Ω + 33µH



POWER-SUPPLY REJECTION RATIO
vs. SUPPLY VOLTAGE

f = 1kHz
$Z_{SPK}$ = 8Ω + 68µH



POWER-SUPPLY REJECTION RATIO
vs. FREQUENCY

$V_{DD}$ = 5V
$Z_{SPK}$ = 8Ω + 68µH



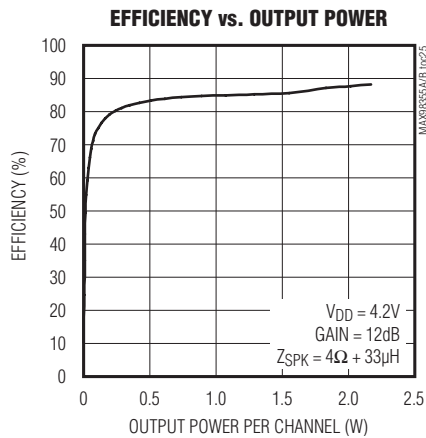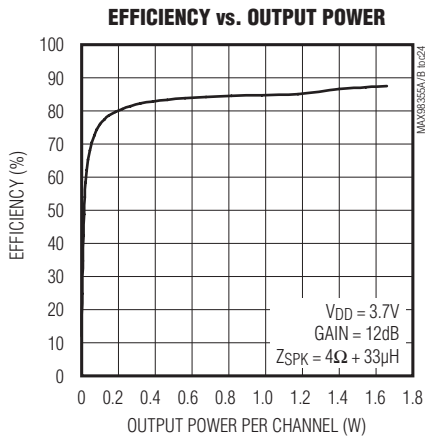INBAND OUTPUT SPECTRUM

BCLK = 6.144MHz
LRCLK = 96kHz
$Z_{SPK}$ = 8Ω + 68µH

# PCM Input Class D Audio Power Amplifiers

## Typical Operating Characteristics (continued)

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)
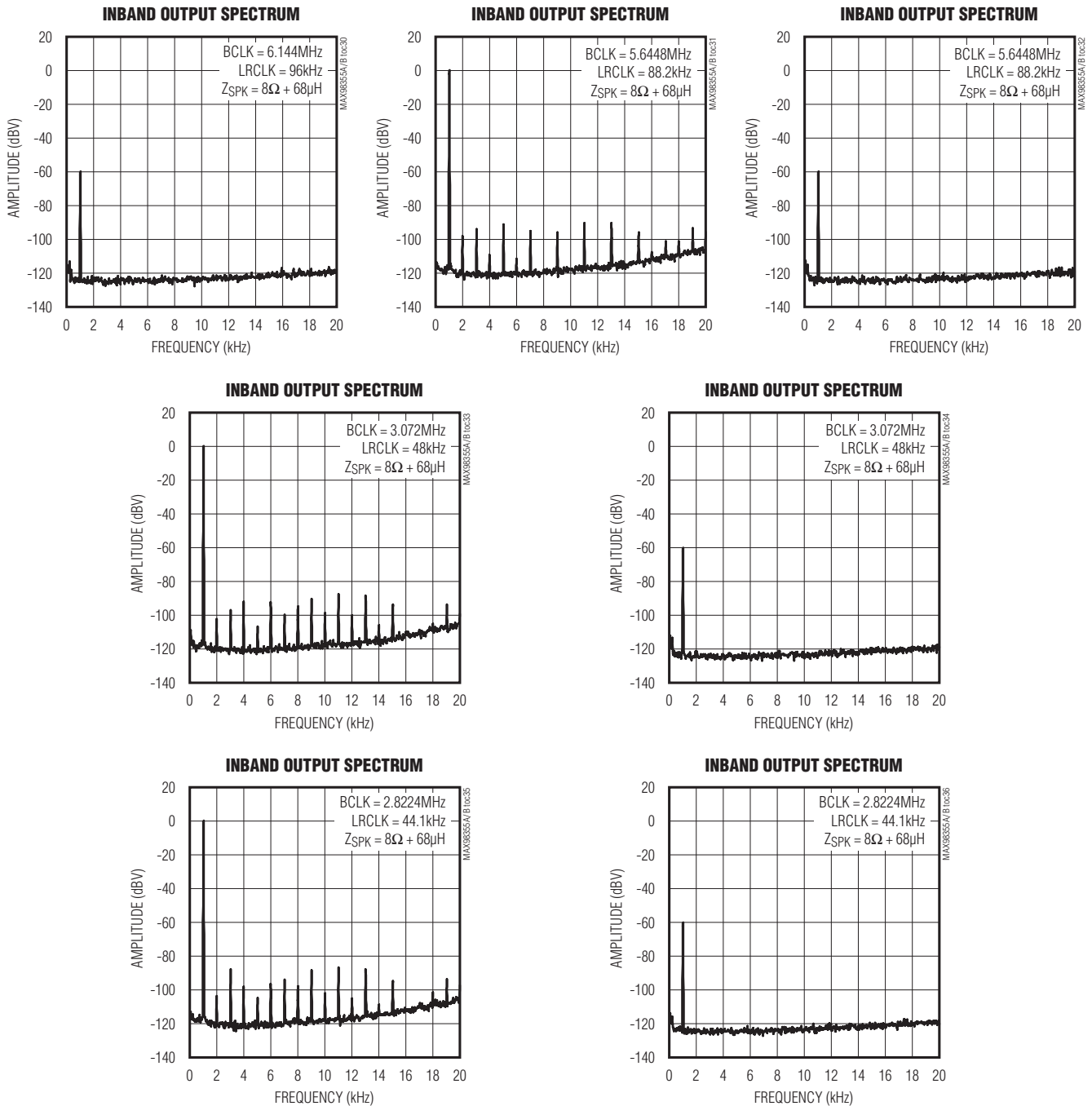
**INBAND OUTPUT SPECTRUM**

BCLK = 6.144MHz
LRCLK = 96kHz
$Z_{SPK}$ = 8Ω + 68µH

**INBAND OUTPUT SPECTRUM**

BCLK = 5.6448MHz
LRCLK = 88.2kHz
$Z_{SPK}$ = 8Ω + 68µH

**INBAND OUTPUT SPECTRUM**

BCLK = 5.6448MHz
LRCLK = 88.2kHz
$Z_{SPK}$ = 8Ω + 68µH

**INBAND OUTPUT SPECTRUM**

BCLK = 3.072MHz
LRCLK = 48kHz
$Z_{SPK}$ = 8Ω + 68µH

**INBAND OUTPUT SPECTRUM**

BCLK = 3.072MHz
LRCLK = 48kHz
$Z_{SPK}$ = 8Ω + 68µH

**INBAND OUTPUT SPECTRUM**

BCLK = 2.8224MHz
LRCLK = 44.1kHz
$Z_{SPK}$ = 8Ω + 68µH

**INBAND OUTPUT SPECTRUM**

BCLK = 2.8224MHz
LRCLK = 44.1kHz
$Z_{SPK}$ = 8Ω + 68µH

# PCM Input Class D Audio Power Amplifiers

## *Typical Operating Characteristics (continued)*

($V_{DD}$ = 5V, $V_{GND}$ = 0V, GAIN = $V_{DD}$ (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads ($Z_{SPK}$) connected between OUTP and OUTN, $Z_{SPK}$ = ∞, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted. Typical values are at $T_A$ = +25°C.)
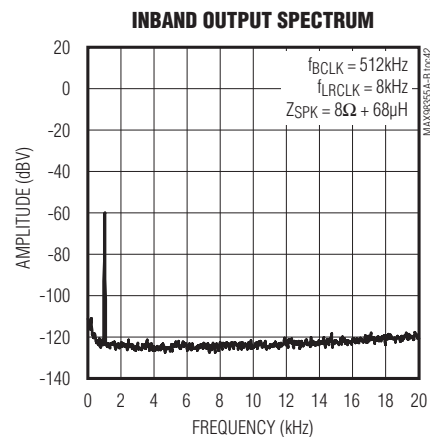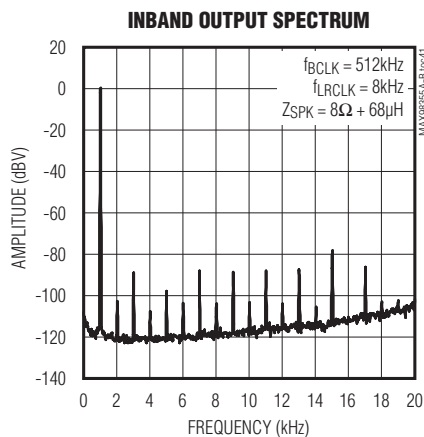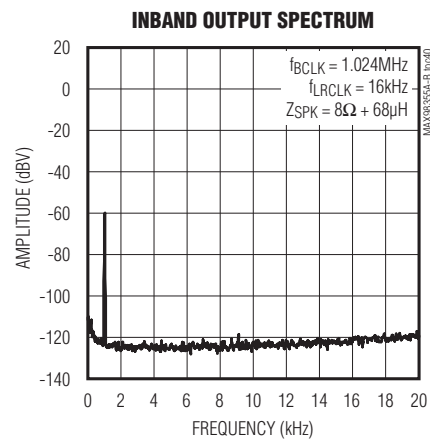


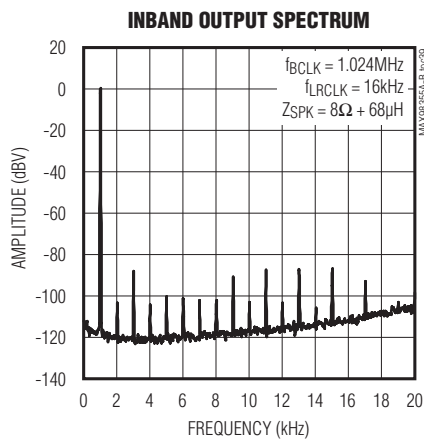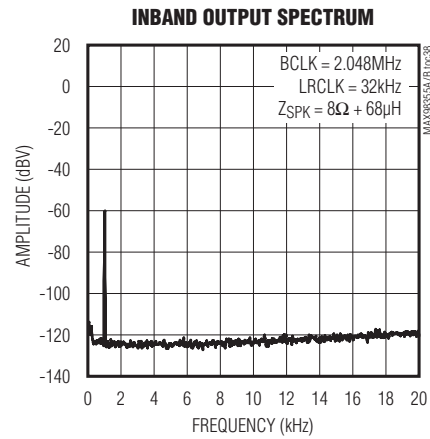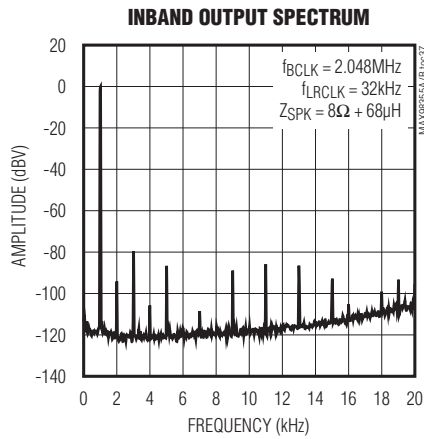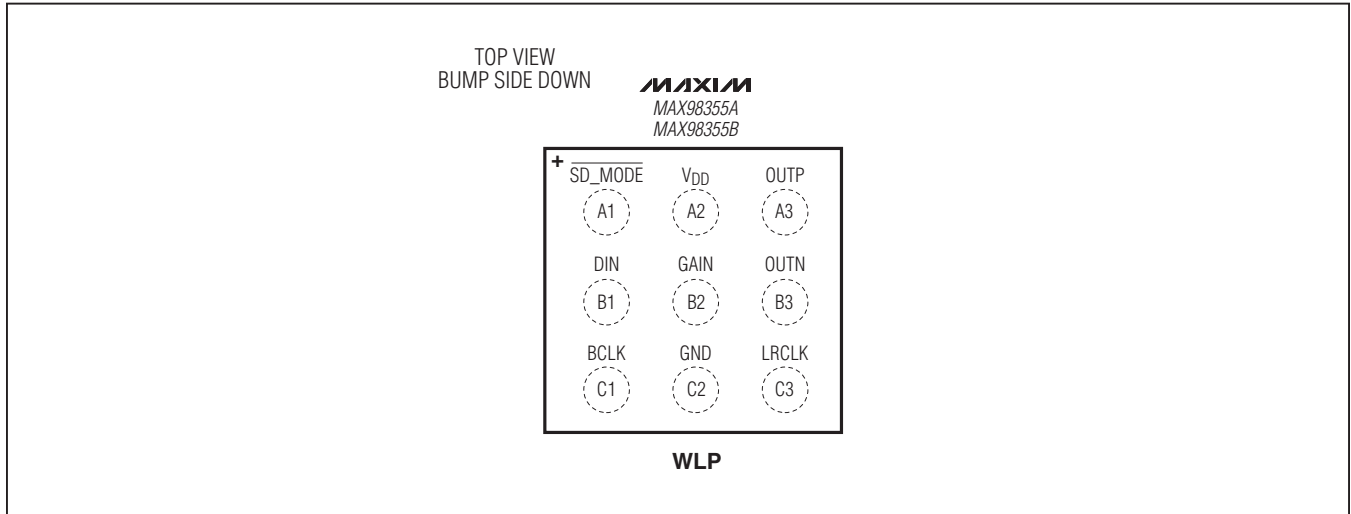INBAND OUTPUT SPECTRUM

$f_{BCLK}$ = 2.048MHz
$f_{LRCLK}$ = 32kHz
$Z_{SPK}$ = 8Ω + 68µH



INBAND OUTPUT SPECTRUM

BCLK = 2.048MHz
LRCLK = 32kHz
$Z_{SPK}$ = 8Ω + 68µH



INBAND OUTPUT SPECTRUM

$f_{BCLK}$ = 1.024MHz
$f_{LRCLK}$ = 16kHz
$Z_{SPK}$ = 8Ω + 68µH



INBAND OUTPUT SPECTRUM

$f_{BCLK}$ = 1.024MHz
$f_{LRCLK}$ = 16kHz
$Z_{SPK}$ = 8Ω + 68µH



INBAND OUTPUT SPECTRUM

$f_{BCLK}$ = 512kHz
$f_{LRCLK}$ = 8kHz
$Z_{SPK}$ = 8Ω + 68µH



INBAND OUTPUT SPECTRUM

$f_{BCLK}$ = 512kHz
$f_{LRCLK}$ = 8kHz
$Z_{SPK}$ = 8Ω + 68µH

# PCM Input Class D Audio Power Amplifiers

TOP VIEW
BUMP SIDE DOWN

**MAXIM**

*MAX98355A*
*MAX98355B*

| + $\overline{\text{SD\_MODE}}$ | $V_{DD}$ | OUTP |
|:---:|:---:|:---:|
| A1 | A2 | A3 |
| DIN | GAIN | OUTN |
| B1 | B2 | B3 |
| BCLK | GND | LRCLK |
| C1 | C2 | C3 |

**WLP**

| PIN | NAME | FUNCTION | |
|:---:|:---:|:---|:---:|
| A1 | $\overline{\text{SD\_MODE}}$ | Shutdown and Channel Select. Determines left, right, or (left + right)/2 mix and also used for shutdown. See Table 5. | |
| A2 | $V_{DD}$ | Power-Supply Input | |
| A3 | OUTP | Positive Speaker Amplifier Output | |
| B1 | DIN | Digital Input Signal | |
| B2 | GAIN | **Amplifier Gain** | |
| | | **Gain Connections** | **Gain (dB)** |
| | | GND through 100kΩ resistor | 15 |
| | | GND | 12 |
| | | Unconnected | 9 |
| | | $V_{DD}$ | 6 |
| | | $V_{DD}$ through 100kΩ resistor | 3 |
| B3 | OUTN | Negative Speaker Amplifier Output | |
| C1 | BCLK | Bit Clock Input Signal. BCLK must be 32, 48, or 64 x LRCLK. Valid frequency range: 256kHz–6.144MHz. | |
| C2 | GND | Ground | |
| C3 | LRCLK | Left/Right Word Clock Input. Valid frequency range: 8kHz–96kHz. | |

# PCM Input Class D Audio Power Amplifiers

## *Detailed Description*

The MAX98355A/MAX98355B are digital PCM input Class D power amplifiers. The MAX98355A accepts standard I2S data through DIN, BCLK, and LRCLK while the MAX98355B accepts left justified data through the same inputs. Both versions can accept 16-bit TDM data with up to four slots. These devices eliminate the need for an external MCLK signal that is typically required for PCM data transmission.

SD_MODE selects which data word is output by the amplifier and is used to put the IC into shutdown. The GAIN pin offers five gain settings and allows the output of the amplifier to be tuned to the appropriate level.

The output stage features low-quiescent current, comprehensive click-and-pop suppression, and excellent RF immunity. The ICs offer Class AB audio performance with Class D efficiency in a minimal board-space solution. The Class D amplifier features spread-spectrum modulation with edge-rate and overshoot control circuitry that offers significant improvements in switch-mode amplifier radiated emissions. The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

### *Digital Audio Interface Modes*

The input stage of the digital audio interface is highly flexible, supporting 8kHz–96kHz sampling rates with 16/24/32-bit resolution for I2S/left justified data as well as up to a 4-slot, 16-bit time division multiplexed (TDM) format (only the first two slots can be selected by the ICs). When LRCLK has a 50% duty cycle the data format is determined by the part number selection (MAX98355A/MAX98355B). When a frame sync pulse is used for the LRCLK the data format is automatically configured in TDM mode. The frame sync pulse indicates the beginning of the first time slot.

### *MCLK Elimination*

The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin-count of the ICs.

### *Jitter Tolerance*

The ICs feature a very high BCLK and LRCLK jitter tolerance of 0.5ns for RMS jitter below 40kHz and 12ns for wideband RMS jitter while maintaining a dynamic range greater than 98dB (Table 1).

### *BCLK Polarity*

When operating in I2S/left justified mode, incoming serial data is always clocked-in on the rising edge of BCLK. In TDM mode, the MAX98355A clocks-in serial data on the rising edge of BCLK while the MAX98355B clocks in serial data on the falling edge of BCLK (Table 2).

### *LRCLK Polarity*

LRCLK specifies whether left-channel data or right-channel data is currently being read by the digital audio interface. The MAX98355A indicates the left channel word when LRCLK is low, and the MAX98355B indicates the left channel word when LRCLK is high (Table 3).

## Table 1. RMS Jitter Tolerance

| FREQUENCY | RMS JITTER TOLERANCE (ns) |
|---|---|
| < 40kHz | 0.5 |
| 40kHz–BCLK | 12 |

## Table 2. BCLK Polarity

| MODE | PART NUMBER | BCLK POLARITY |
|---|---|---|
| I2S/left justified | MAX98355A/MAX98355B | Rising edge |
| TDM | MAX98355A | Rising edge |
| | MAX98355B | Falling edge |

## Table 3. LRCLK Polarity

| PART NUMBER | LRCLK POLARITY (LEFT CHANNEL) |
|---|---|
| MAX98355A | Low |
| MAX98355B | High |

### PCM Timing Characteristics

The MAX98355A follows standard I2S timing by allowing a delay of one BCLK cycle after the LRCLK transition before the beginning of a new data word (Figure 4 and Figure 5). The MAX98355B follows the left justified timing specification by aligning the LRCLK transitions with the beginning of a new data word (Figure 6 and Figure 7).

Figure 8 and Figure 9 show TDM operation, in which a frame-sync pulse is used for LRCLK. In TDM mode, there must be 32, 48, or 64 BCLK cycles per LRCLK. In TDM mode, the IC only accepts 16-bit formatted data and only the first two TDM slots can be selected. However, if the first 16 bits are selected ($\overline{SD\_MODE}$ = logic-high), then the bit-depth or number of channels has no effect as long as there are 32, 48, or 64 BCLK cycles per LRCLK. All extra bits in the frame are ignored (Figure 10 and Figure 11). If the second 16 bits are selected ($\overline{SD\_MODE}$ = logic-high through R$_{SMALL}$), then the TDM data must be 16-bit data and cannot include more than 4 channels (64 BCLK cycles). TDM operation is available in both ICs.
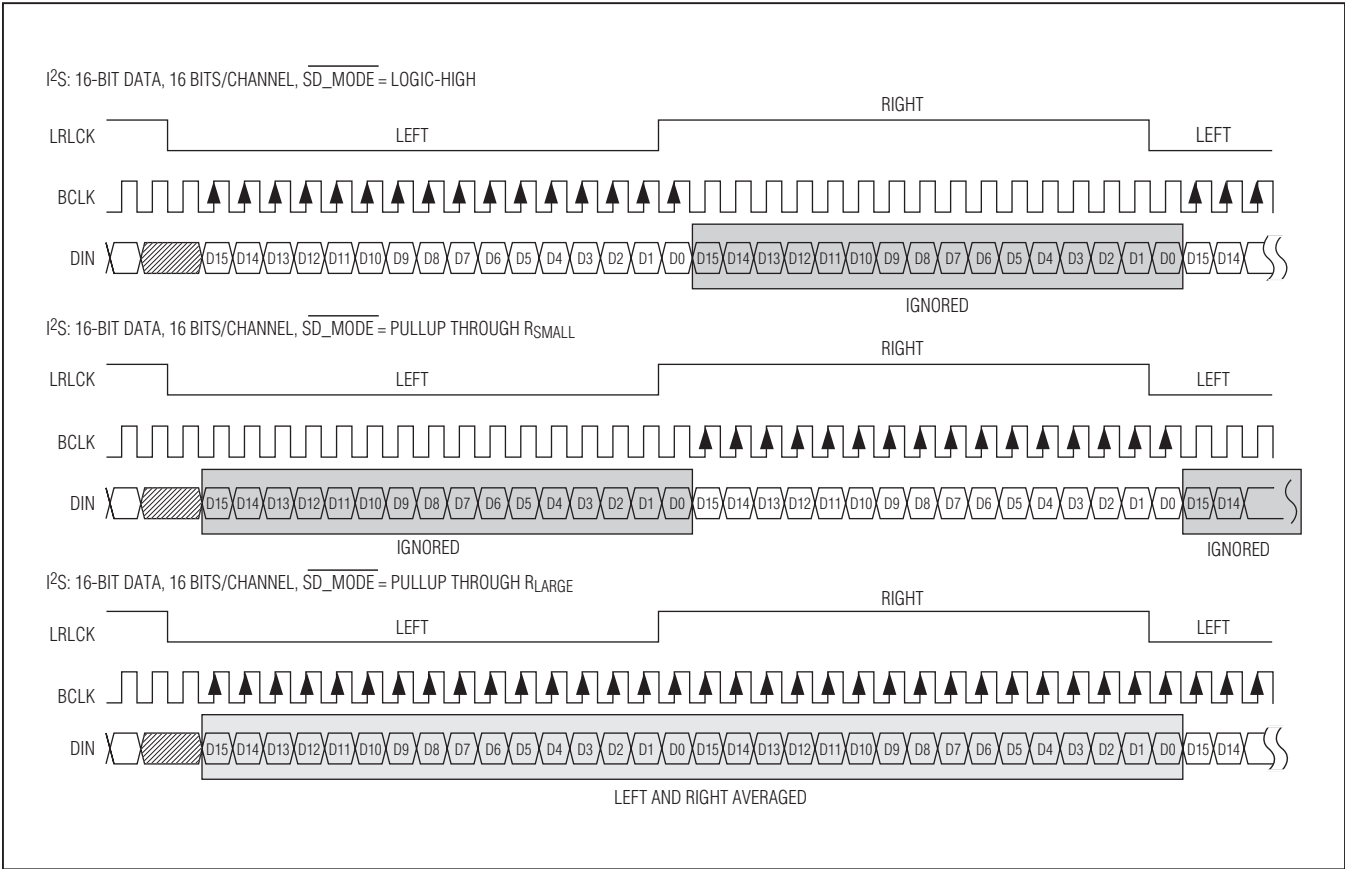


Figure 4. MAX98355A I2S Digital Audio Interface Timing, 16-Bit Resolution

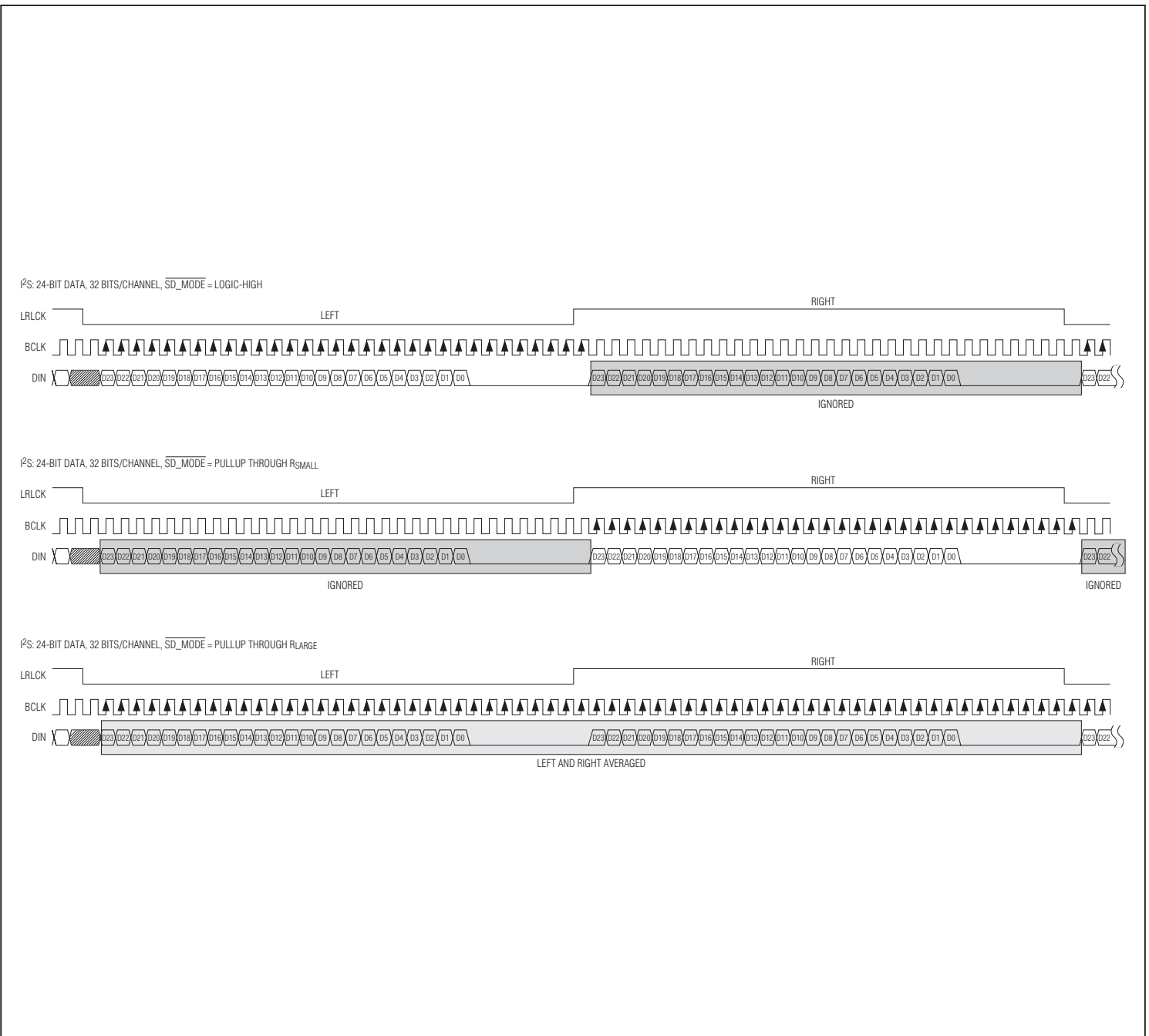**PCM Input Class D Audio Power Amplifiers**

**MAX98355A/MAX98355B**

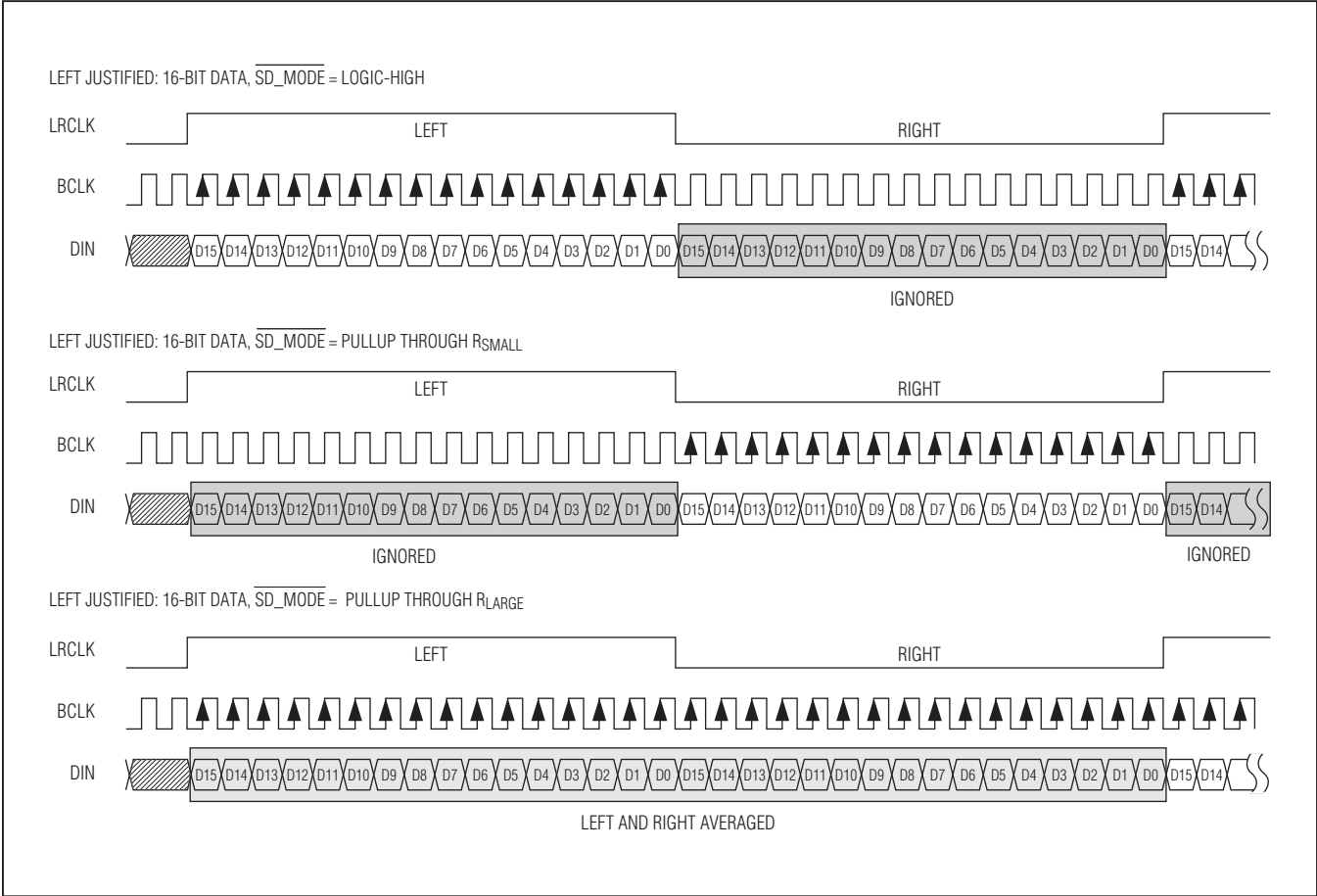Figure 6. MAX98355B Left-Justified Digital Audio Interface Timing, 16-Bit Resolution
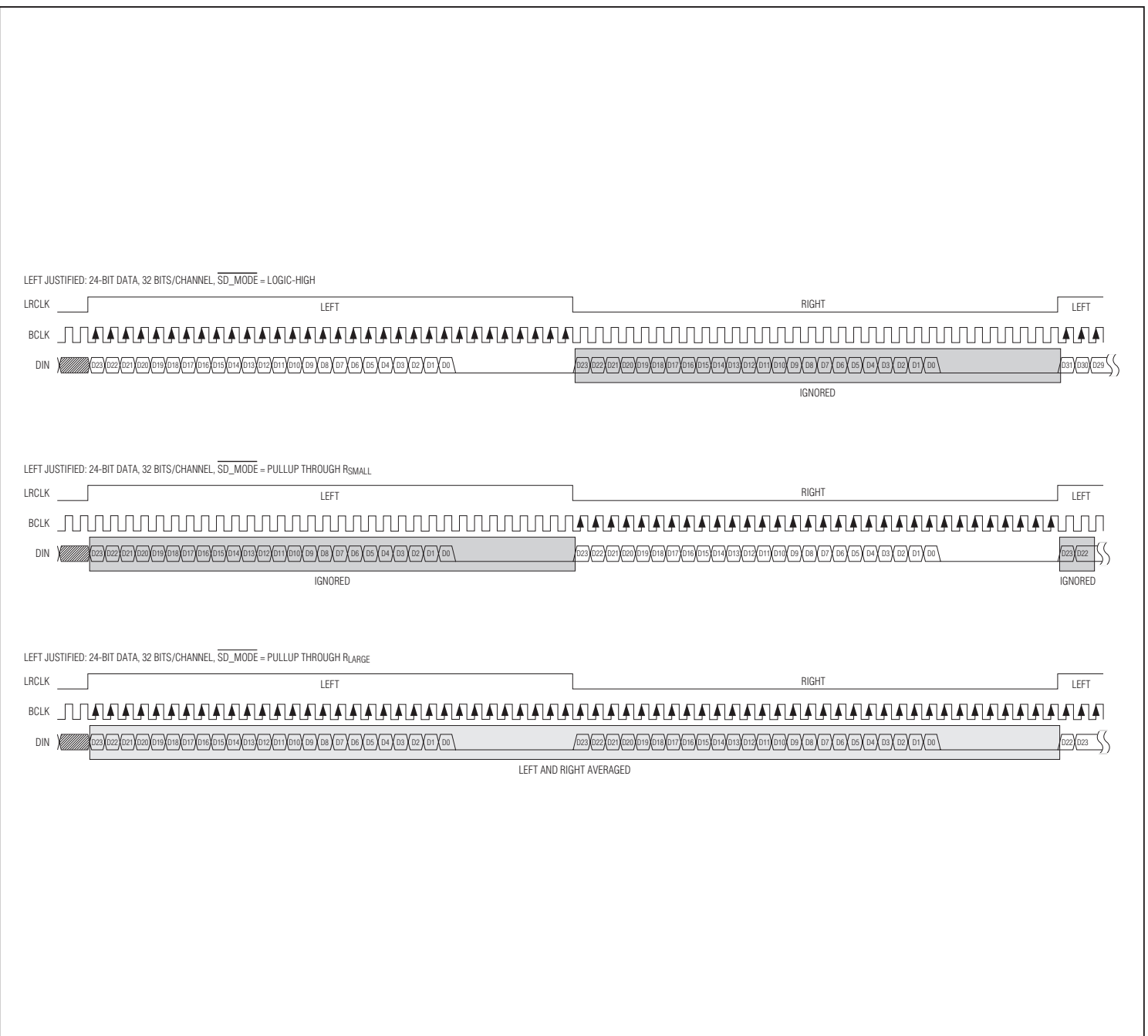
Figure 7. MAX98355B Left-Justified Digital Audio Interface Timing, 24-Bit Resolution

# PCM Input Class D Audio Power Amplifiers



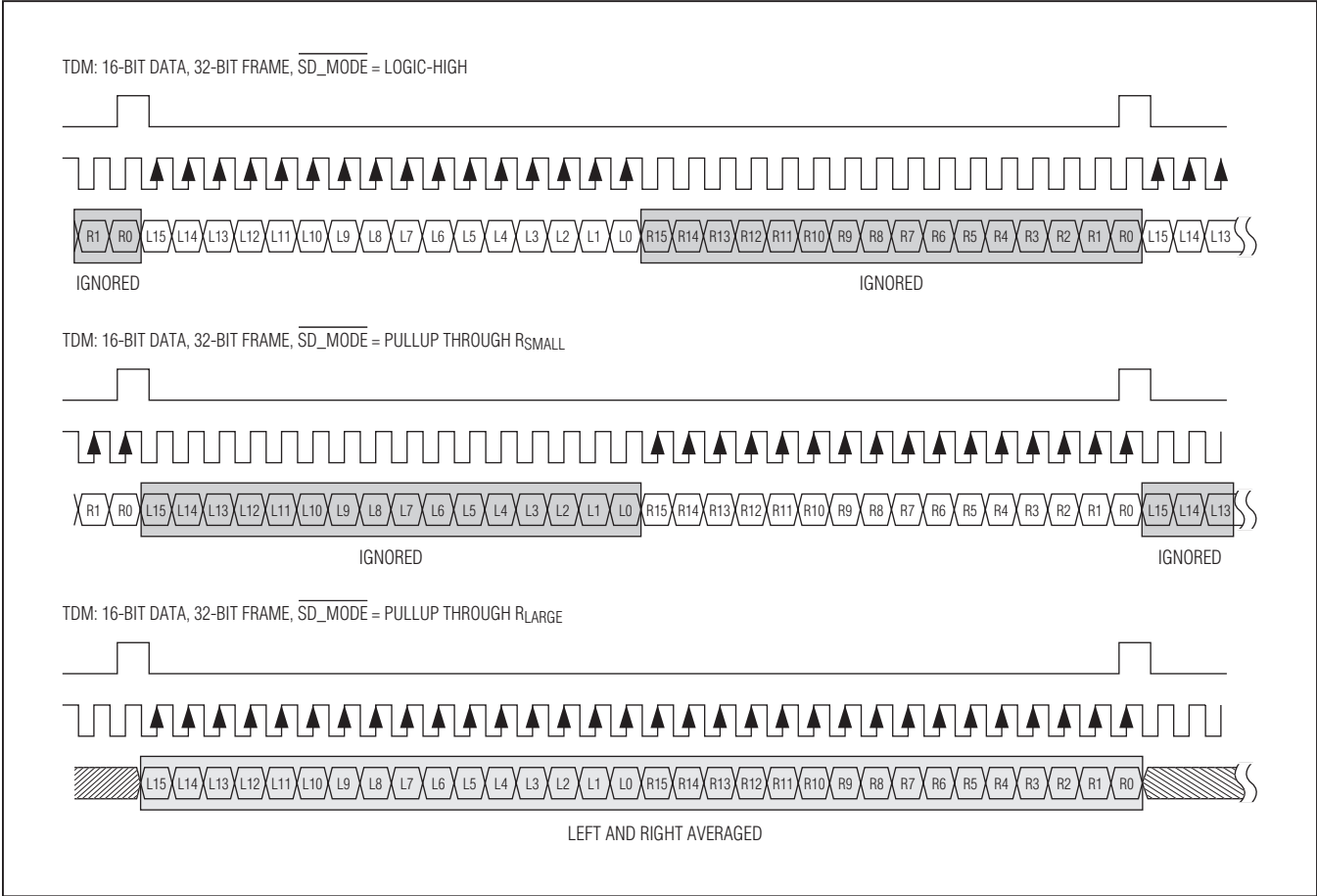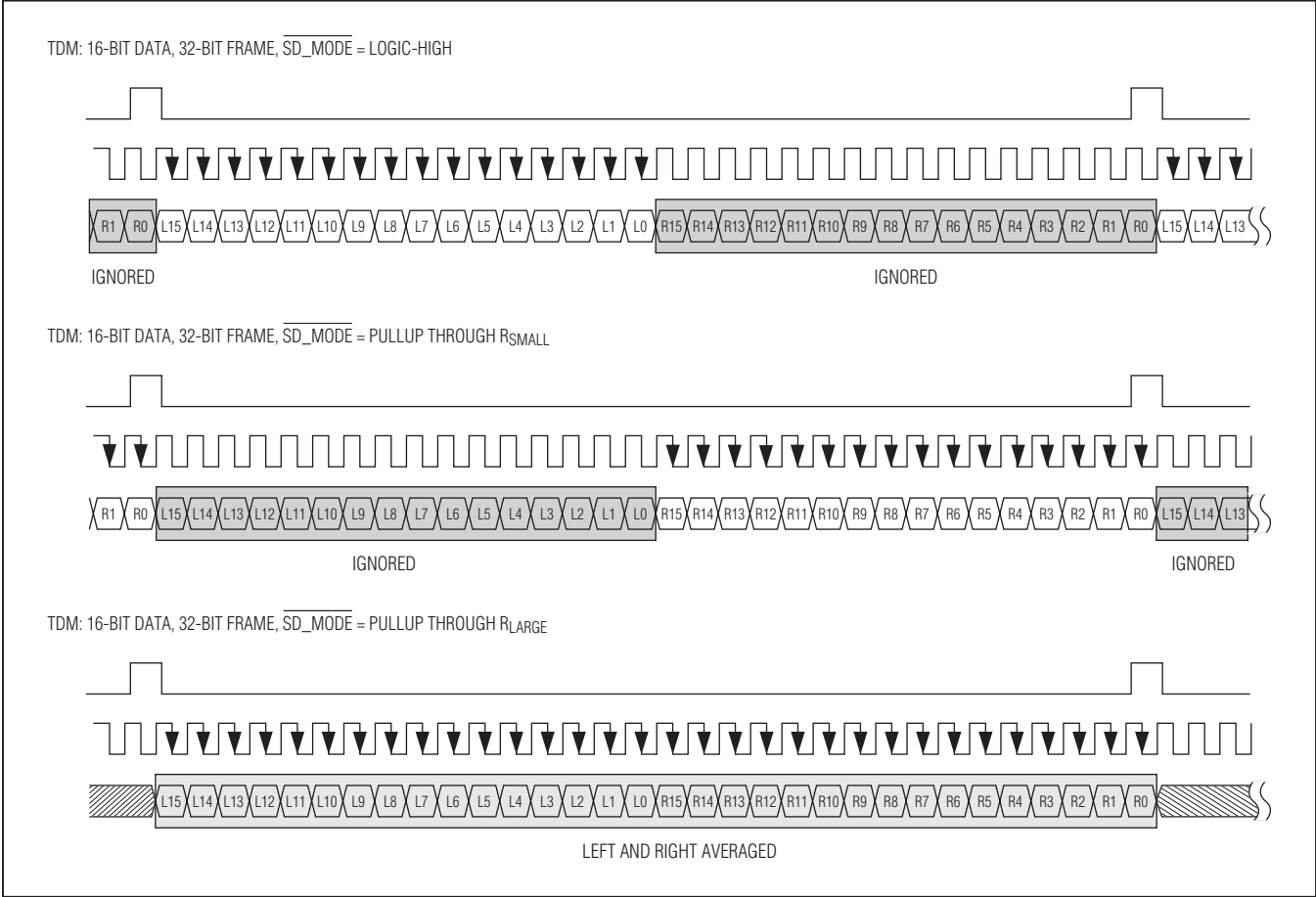Figure 8. MAX98355A TDM Digital Audio Interface Timing

Figure 9. MAX98355B TDM Digital Audio Interface Timing

Figure 10. MAX98355A TDM Digital Audio Interface Timing, Example of Four 16-Bit Slots

TDM: 64-BIT DATA, 64-BIT FRAME, SD_MODE = LOGIC-HIGH

TDM: 64-BIT DATA, 64-BIT FRAME, SD_MODE = PULLUP THROUGH R$_{SMALL}$

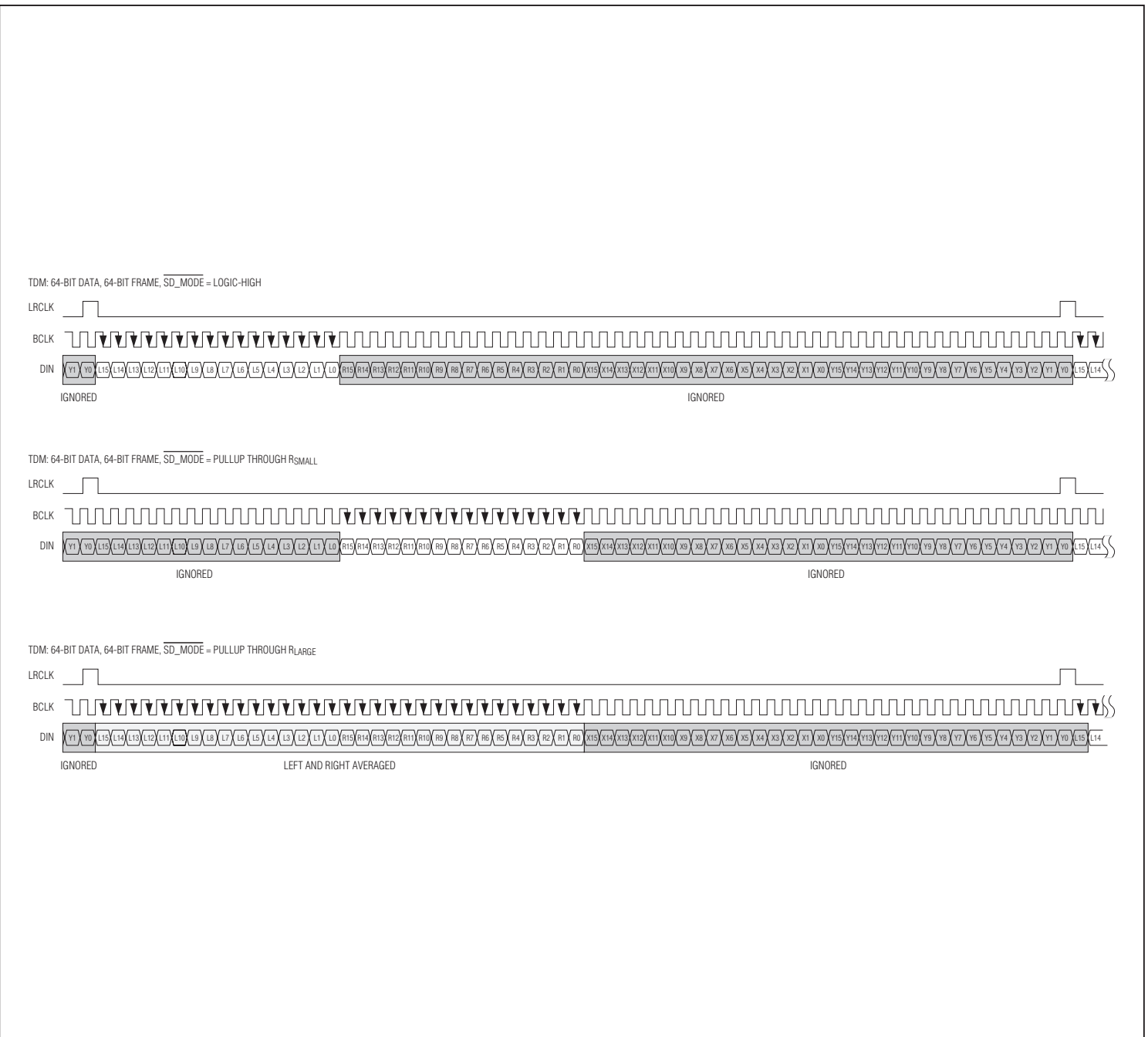TDM: 64-BIT DATA, 64-BIT FRAME, SD_MODE = PULLUP THROUGH R$_{LARGE}$

Figure 11. MAX98355B TDM Digital Audio Interface Timing, Example of Four 16-Bit Slots