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EVALUATION KIT AVAILABLE

MAX98357A/MAX98357B

PCM Input Class D Audio Power Amplifiers

General Description

The MAX98357A/MAX98357B are digital pulse-code modulation (PCM) input Class D power amplifiers that provide Class AB audio performance with Class D efficiency. These ICs offer five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) in I²S/left-justified mode set by a single gain select input and a fixed 12dB gain in TDM mode.

The digital audio interface is highly flexible with the MAX98357A supporting I²S data and the MAX98357B supporting left-justified data. Both ICs support 8 channel time division multiplexed (TDM) data. The digital audio interface accepts specified sample rates between 8kHz and 96kHz for all supported data formats. The ICs can be configured to produce a left channel, right channel, or (left/2 + right/2) output from the stereo input data. The ICs operate using 16/24/32-bit data for I²S and left-justified modes as well as 16-bit or 32-bit data using TDM mode. The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count of the ICs.

The ICs also feature a very high wideband jitter tolerance (12ns typ) on BCLK and LRCLK to provide robust operation.

Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution.

The ICs are available in 9-pin WLP (1.345mm x 1.435mm x 0.64mm) and 16-pin TQFN (3mm x 3mm x 0.75mm) packages and are specified over the -40°C to +85°C temperature range.

Applications

Notebook and Netbook Computers

Cellular Phones

Tablets

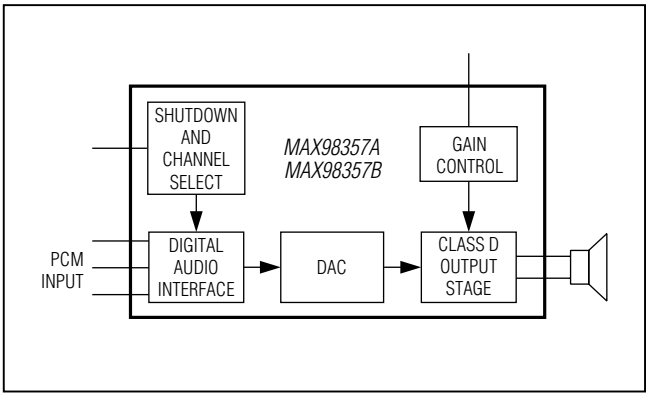
Ordering Information appears at end of data sheet.

Functional Diagram appears at end of data sheet.

Features

- **Single-Supply Operation (2.5V to 5.5V)**
- **3.2W Output Power into 4Ω at 5V**
- **2.4mA Quiescent Current**
- **92% Efficiency (R_L = 8Ω, P_{OUT} = 1W)**
- **25μV_{RMS} Output Noise (A_V = 15dB)**
- **Low 0.015% THD+N at 1kHz**
- **No MCLK Required**
- **Sample Rates of 8kHz to 96kHz**
- **Supports Left, Right, or (Left/2 + Right/2) Output**
- **Sophisticated Edge Rate Control Enables Filterless Class D Outputs**
- **77dB PSRR at 1kHz**
- **Low RF Susceptibility Rejects TDMA Noise from GSM Radios**
- **Extensive Click-and-Pop Reduction Circuitry**
- **Robust Short-Circuit and Thermal Protection**
- **Available in Space-Saving Packages: 1.345mm x 1.435mm WLP (0.4mm Pitch) and 3mm x 3mm TQFN**

Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6779; Rev 8; 6/16

MAX98357A/MAX98357B

PCM Input Class D Audio Power Amplifiers

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ABSOLUTE MAXIMUM RATINGS

V_{DD}, LRCLK, BCLK, and DIN to GND .....-0.3V to +6V
All Other Pins to GND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Current In/Out of V_{DD}/GND/OUT_ ..... ±1.6A
Continuous Input Current (all other pins)..... ±20mA
Duration of OUT_ Short Circuit to GND or V_{DD}.....Continuous
Duration of OUTP Short to OUTN .....Continuous

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 13.7mW/°C above +70°C).....1096mW
TQFN (derate 20.8mW/°C above +70°C).....1666mW
Junction Temperature .....+150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+230°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....73°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....50°C/W

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....48°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = V_{DD}. BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSSR test		2.5		5.5	V
Undervoltage Lockout	UVLO			1.4	1.8	2.3	V
Quiescent Current	I_{DD}	T_A = +25°C			2.75	3.35	mA
		T_A = +25°C, V_{DD} = 3.7V			2.4	2.85	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SD\_MODE}$ = 0V, T_A = +25°C			0.6	2	µA
Standby Current	$I_{\overline{STNDBY}}$	$\overline{SD\_MODE}$ = 1.8V, no BCLK, T_A = +25°C			340	400	µA
Turn-On Time	t_{ON}				7	7.5	ms
Output Offset Voltage	V_{OS}	T_A = +25°C, gain = 15dB			±0.3	±2.5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Note 3)	Into shutdown		-72		dBV
			Out of shutdown		-66		
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.5V, T_A = +25°C		60	75		dB
		T_A = +25°C (Notes 3, 4)	f = 217Hz, 200mV_{P-P} ripple		77		
			f = 10kHz, 200mV_{P-P} ripple		60		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = V_{DD}. BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power (Note 3)	P_{OUT}	THD+N 10%, gain = 12dB	Z_{SPK} = 4Ω + 33µH		3.2		W
			Z_{SPK} = 8Ω + 68µH		1.8		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		0.93		
		THD+N = 1%, gain = 12dB	Z_{SPK} = 4Ω + 33µH		2.5		
			Z_{SPK} = 8Ω + 68µH		1.4		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		0.77		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 1W, T_A = +25°C, Z_{SPK} = 4Ω + 33µH, WLP			0.02	0.06	%
		f = 1kHz, P_{OUT} = 1W, T_A = +25°C, Z_{SPK} = 4Ω + 33µH, TQFN			0.02		
		f = 1kHz, P_{OUT} = 0.5W, T_A = +25°C, Z_{SPK} = 8Ω + 68µH			0.013		
Dynamic Range	DR	A-weighted, V_{RMS} = 2.54V, 24- or 32-bit data			105		dB
Output Noise	V_N	A-weighted, 24- or 32-bit data (Note 4)			25		μV_{RMS}
Gain (Relative to a 2.1dBV Reference Level)	A_V	GAIN_SLOT = GND through 100kΩ		14.4	15	15.6	dB
		GAIN_SLOT = GND		11.4	12	12.6	
		GAIN_SLOT = unconnected		8.4	9	9.6	
		GAIN_SLOT = V_{DD}		5.4	6	6.6	
		GAIN_SLOT = V_{DD} through 100kΩ		2.4	3	3.6	
Current Limit	I_{LIM}				2.8		A
Efficiency	ε	Z_{SPK} = 8Ω + 68µH, THD+N = 10%, f = 1kHz, gain = 12dB			92		%
DAC Gain Error					1		%
Frequency Response				-0.2		+0.2	dB
Class D Switching Frequency	f_{OSC}				330		kHz
Spread-Spectrum Bandwidth					±20		kHz
DAC DIGITAL FILTERS							
VOICE MODE IIR LOWPASS FILTER (LRCLK < 30kHz)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff		0.443 x f_S			Hz
		-3dB cutoff		0.446 x f_S			
Stopband Cutoff	f_{SLP}					0.464 x f_S	Hz
Stopband Attenuation		f > f_{SLP}		75			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD}. BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AUDIO MODE FIR LOWPASS FILTER (30kHz < LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.47 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation		f > f_{SLP}	60			dB
AUDIO MODE FIR LOWPASS FILTER (LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.24 x f_S			Hz
		-3dB cutoff	0.31 x f_S			
Stopband Cutoff	f_{SLP}				0.477 x f_S	Hz
Stopband Attenuation		f < f_{SLP}	60			dB
DIGITAL AUDIO INTERFACE						
LRCLK Range 1	f_{S1}		7.6	8	8.4	kHz
LRCLK Range 2	f_{S2}		15.2	16	16.8	
LRCLK Range 3	f_{S3}		30.4	48	50.4	
LRCLK Range 4	f_{S4}		83.8	96	100.8	
Resolution		I^2S/left justified mode		16/24/32		Bits
		TDM mode		16/32		
BCLK Frequency Range	f_{BCLKH}	BCLK must be 32, 48, or 64X of LRCLK	0.2432		25.804	MHz
BCLK High Time	t_{BCLKH}		15			ns
BCLK Low Time	t_{BCLKL}		15			ns
Maximum Low Frequency BCLK and LRCLK Jitter		RMS jitter below 40kHz		0.5		ns
Maximum High Frequency BCLK and LRCLK Jitter		RMS jitter above 40kHz		12		
Input High Voltage	V_{IH}	Digital audio inputs	1.3			V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD}. BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	Digital audio inputs			0.6	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V, V_{DD} = 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance	C_{IN}			3		pF
DIN to BCLK Setup Time	t_{SETUP}		10			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$		10			ns
DIN to BCLK Hold Time	t_{HOLD}		10			ns
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$		10			ns
$\overline{\text{SD\_MODE}}$ COMPARATOR TRIP POINTS						
B0		See $\overline{\text{SD\_MODE}}$ and shutdown operation for details	0.08	0.16	0.355	V
B1			0.65	0.77	0.825	
B2			1.245	1.4	1.5	
$\overline{\text{SD\_MODE}}$ Pulldown Resistor	R_{PD}		92	100	108	kΩ
GAIN_SLOT COMPARATOR TRIP POINTS						
	V_GAIN_SLOT	A_V = 3dB gain	0.65 x V_{DD}		0.85 x V_{DD}	V
		A_V = 6dB gain	0.9 x V_{DD}		V_{DD}	
		A_V = 9dB gain	0.4 x V_{DD}		0.6 x V_{DD}	
		A_V = 12dB gain	0		0.1 x V_{DD}	
		A_V = 15dB gain	0.15 x V_{DD}		0.35 x V_{DD}	

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 3: Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 8Ω, L_L = 68µH. For R_L = 4Ω, L_L = 33µH.

Note 4: Digital silence used for input signal.

Note 5: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f =20Hz to 20kHz.

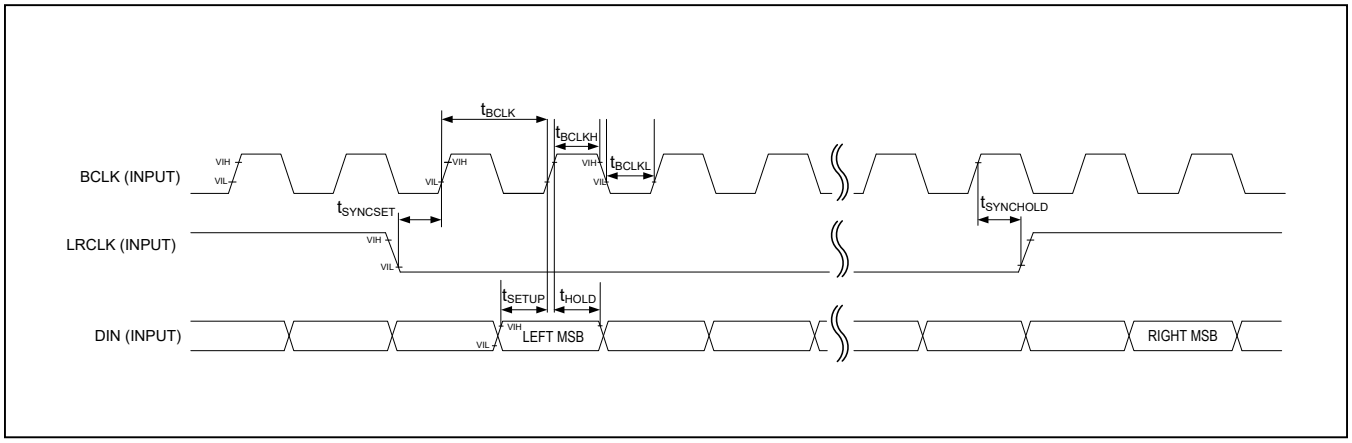


Figure 1. I²S Audio Interface Timing Diagram (MAX98357A)

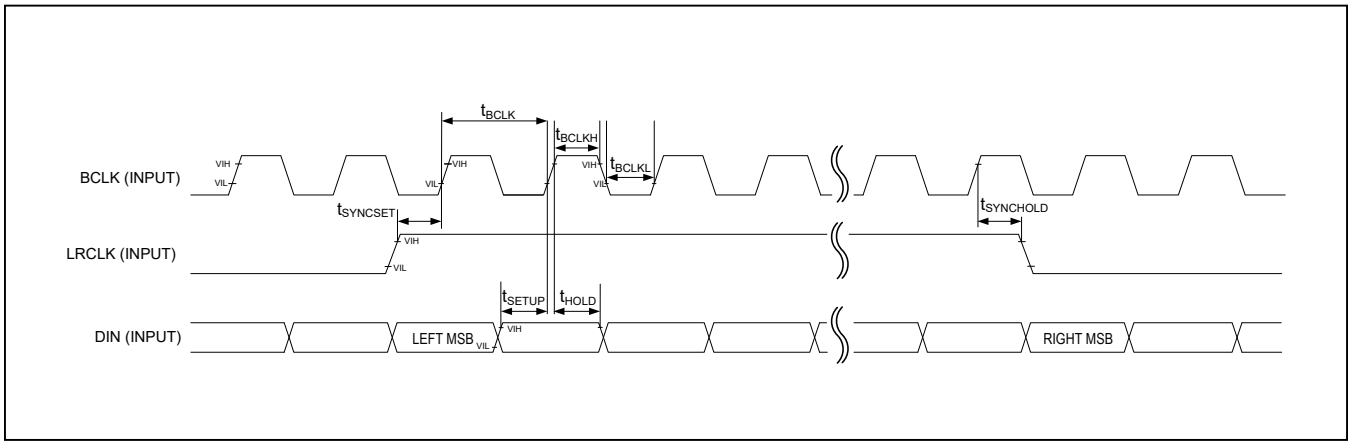


Figure 2. Left-Justified Audio Interface Timing Diagram (MAX98357B)

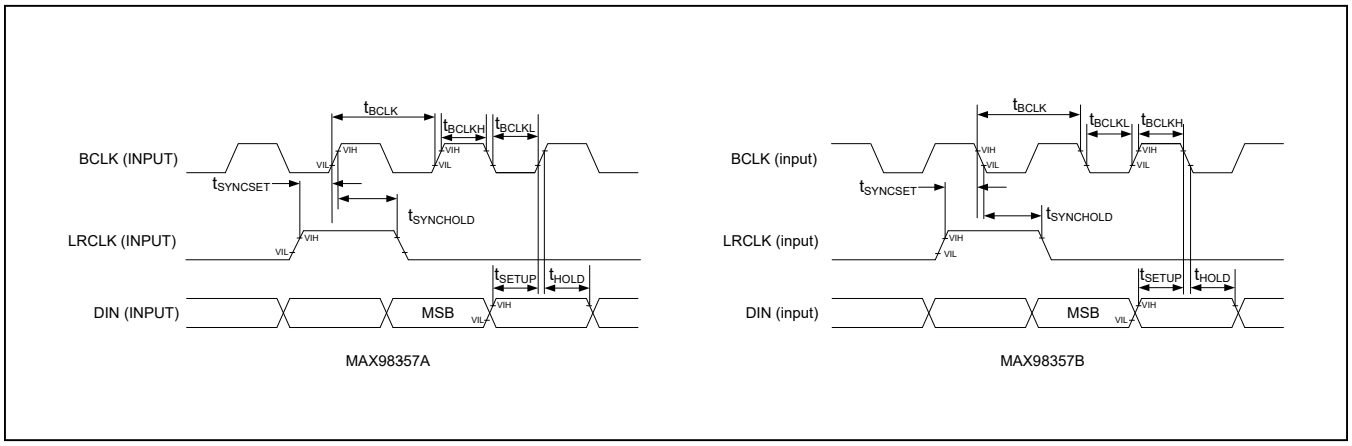
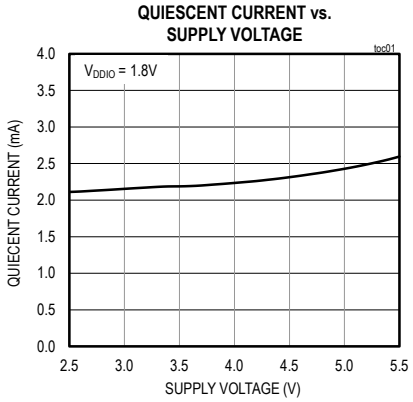
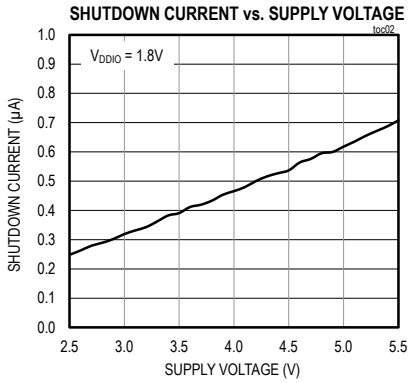


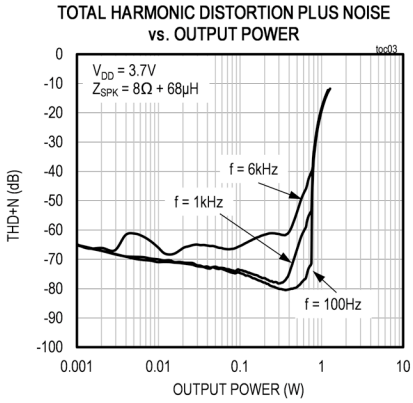
Figure 3. TDM Audio Interface Timing Diagram

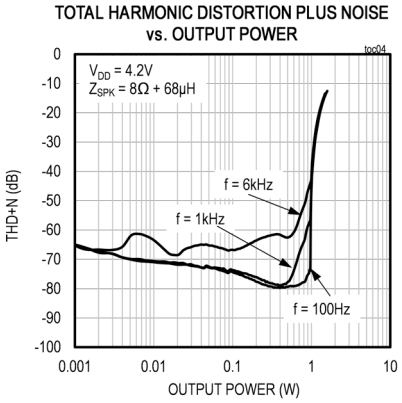
Typical Operating Characteristics

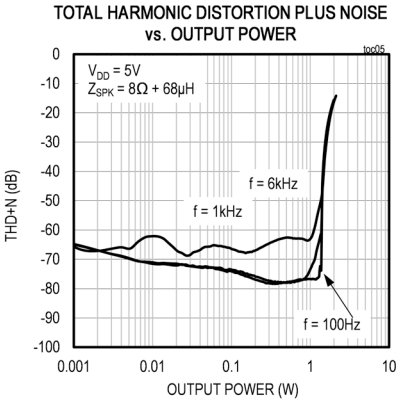
(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = GND (+12dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

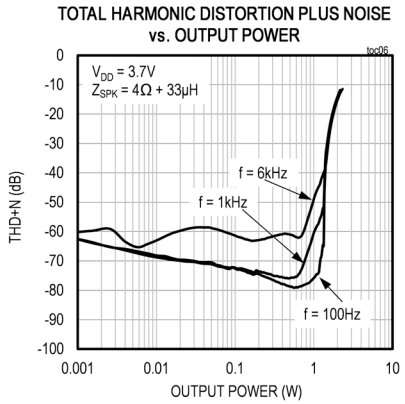


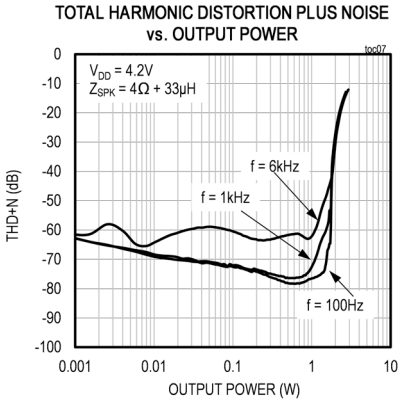


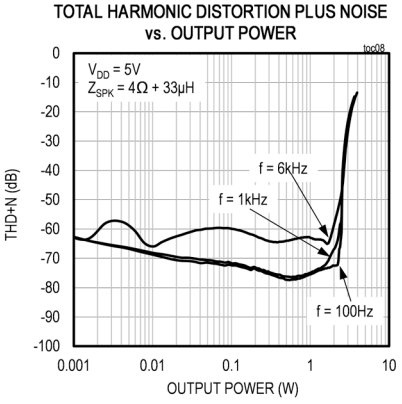








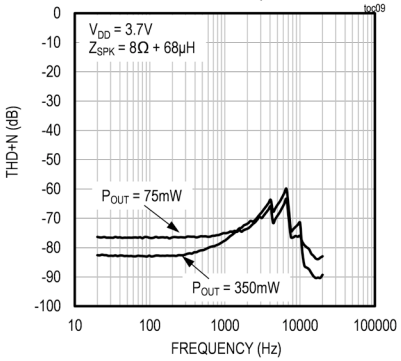




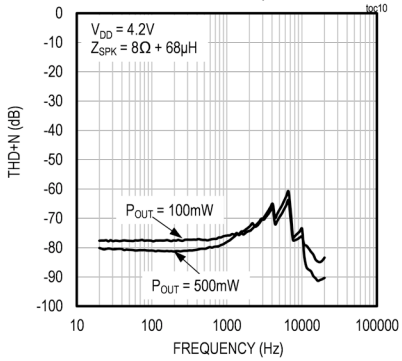
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = GND (+12dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT FREQUENCY



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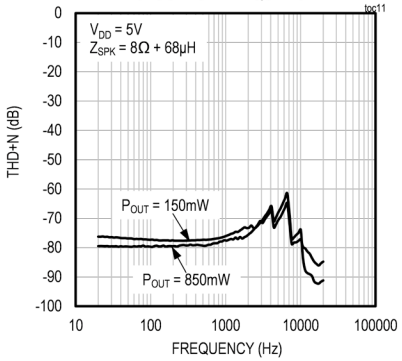

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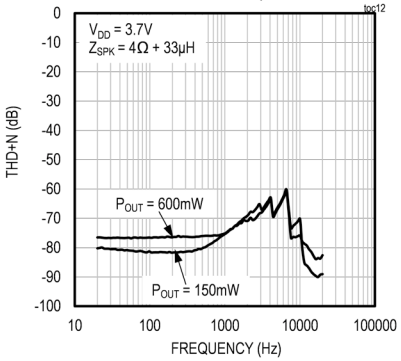

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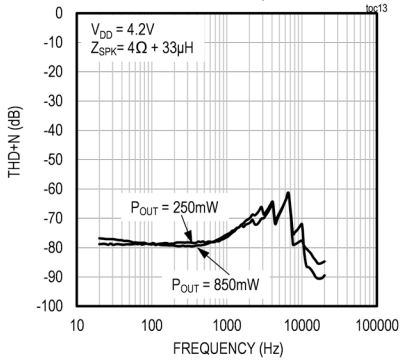

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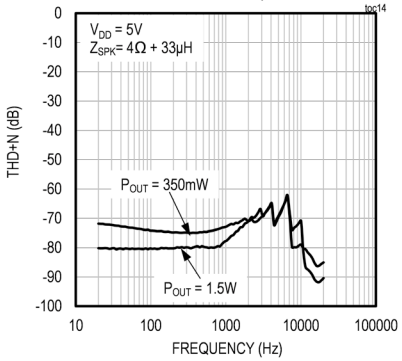
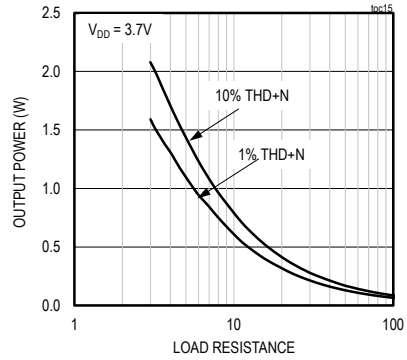


OUTPUT POWER vs. LOAD RESISTANCE



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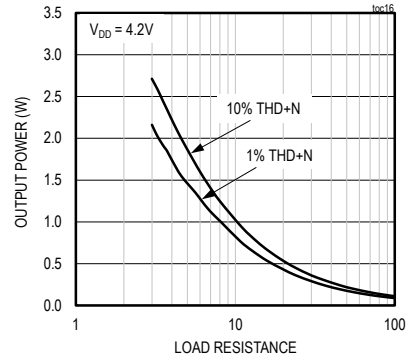
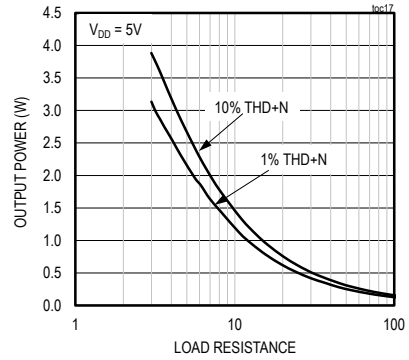
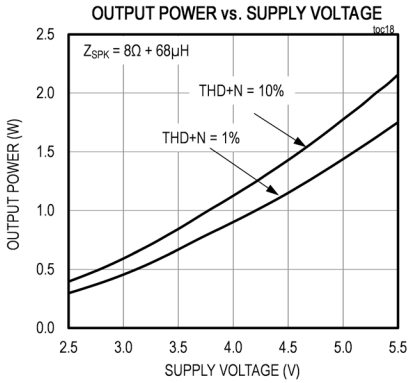


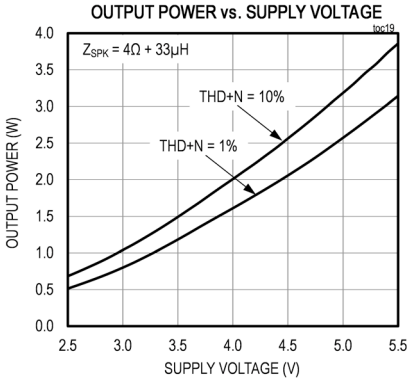
OUTPUT POWER vs. LOAD RESISTANCE

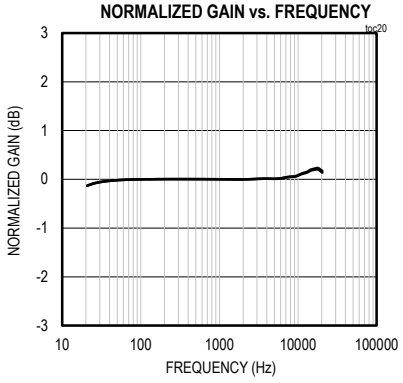


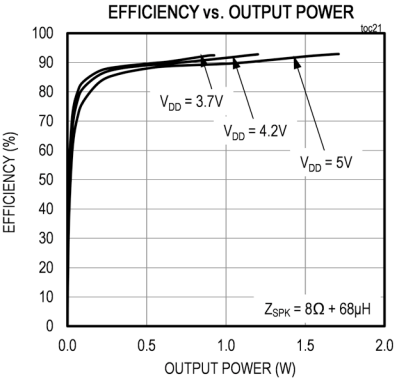
Typical Operating Characteristics (continued)

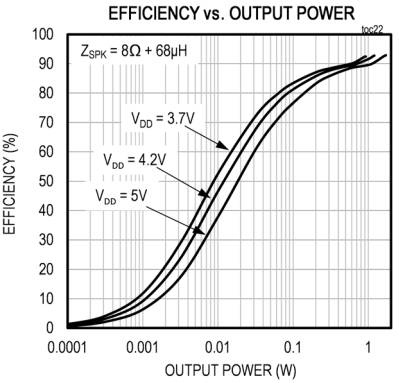
(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = GND (+12dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

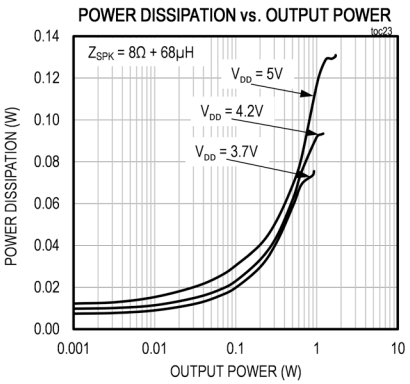


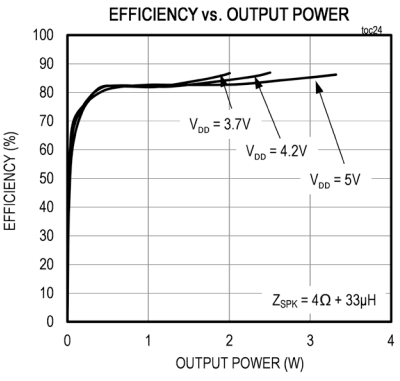


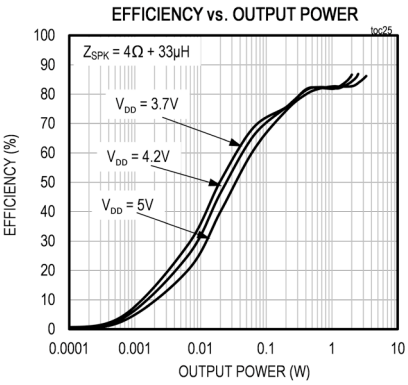


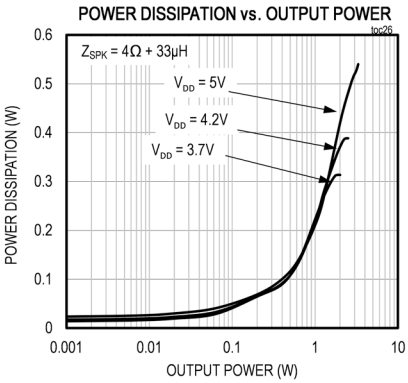








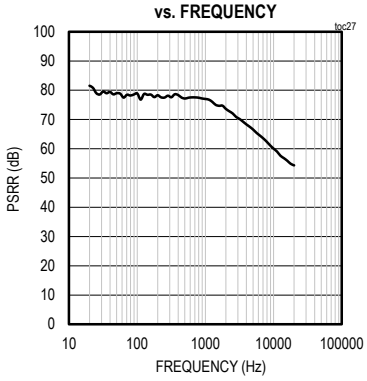




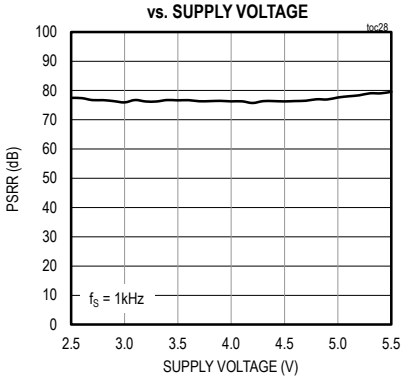
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = GND (+12dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

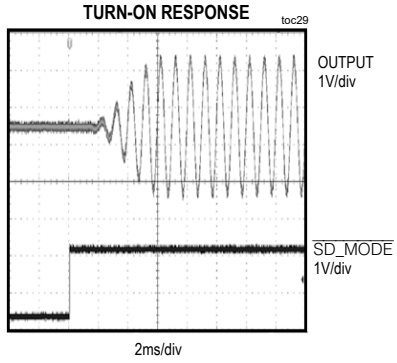
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



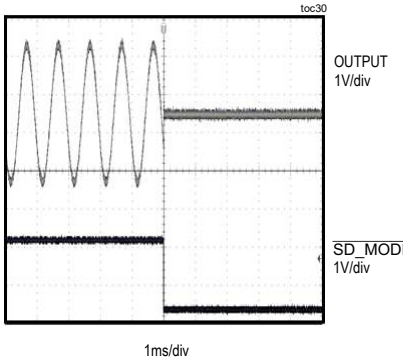
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



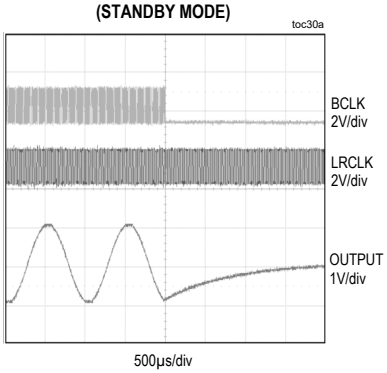
TURN-ON RESPONSE



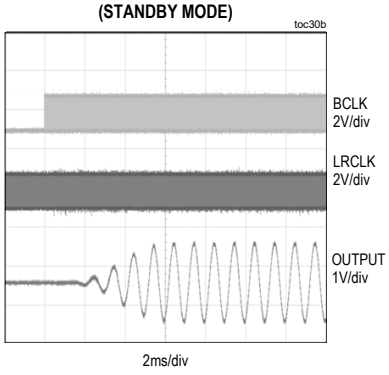
TURN-OFF RESPONSE



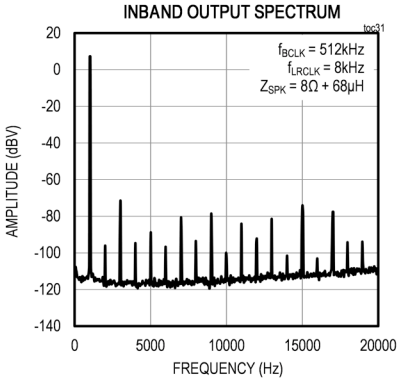
TURN-OFF RESPONSE (STANDBY MODE)



TURN-ON RESPONSE (STANDBY MODE)



INBAND OUTPUT SPECTRUM



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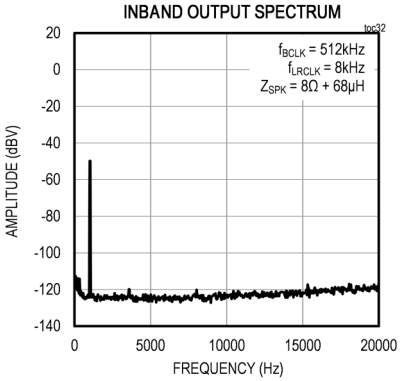
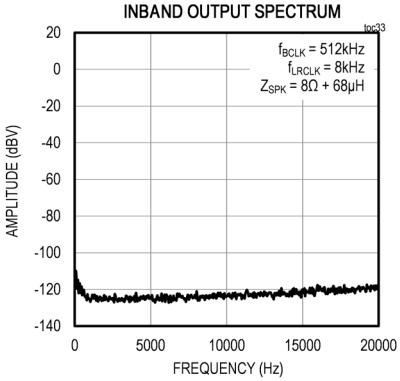
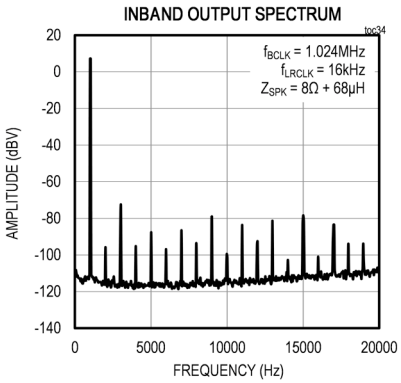


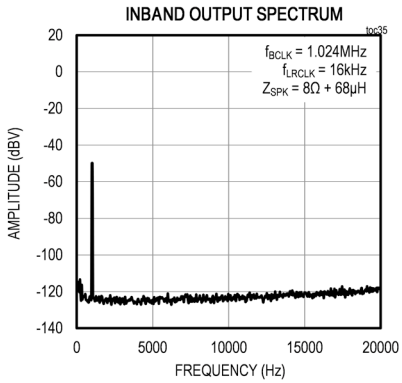
INBAND OUTPUT SPECTRUM

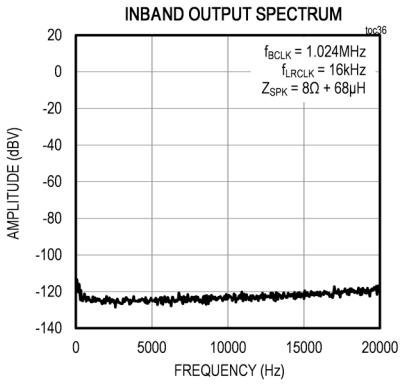


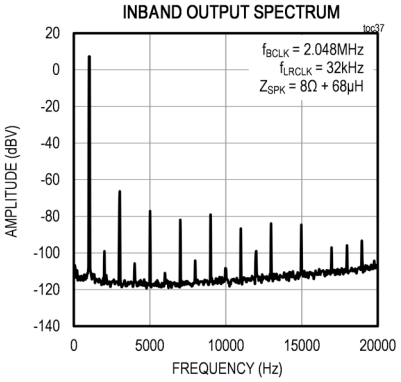
Typical Operating Characteristics (continued)

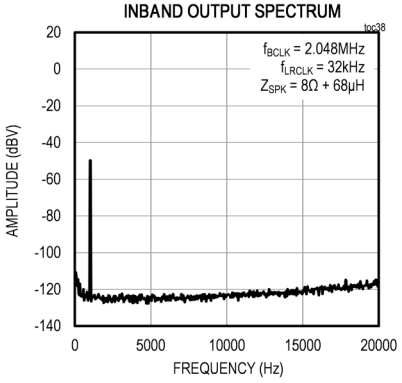
(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = GND (+12dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

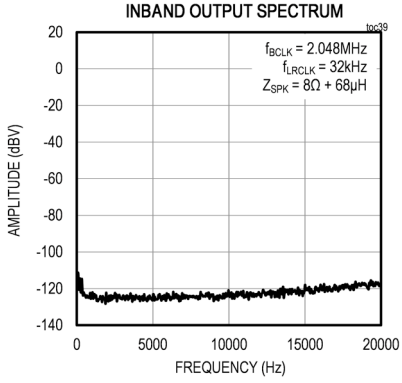


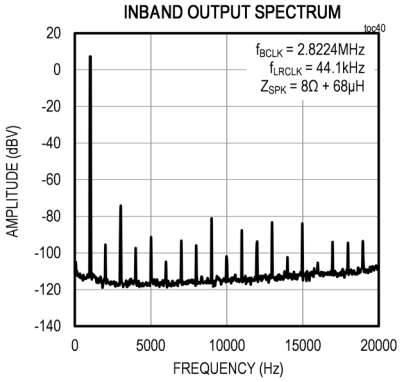


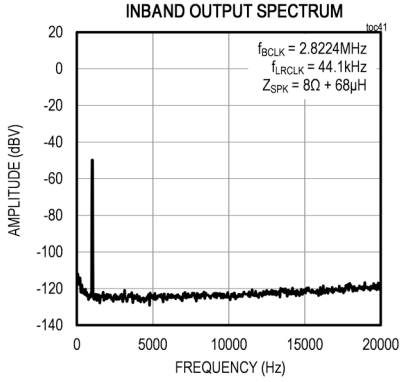


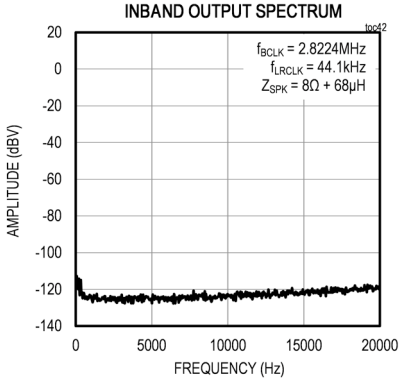






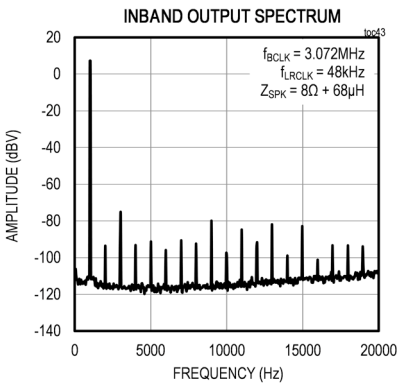


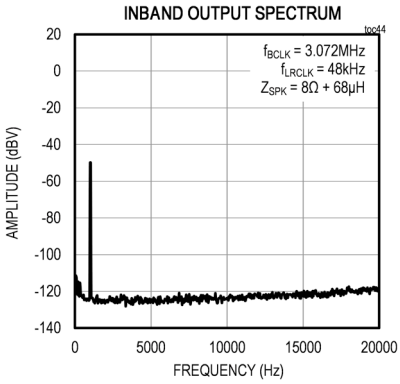


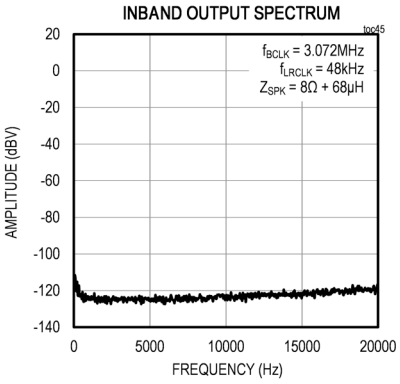


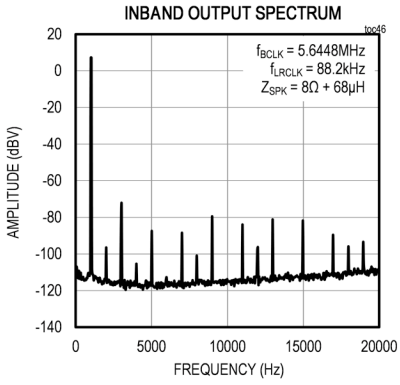
Typical Operating Characteristics (continued)

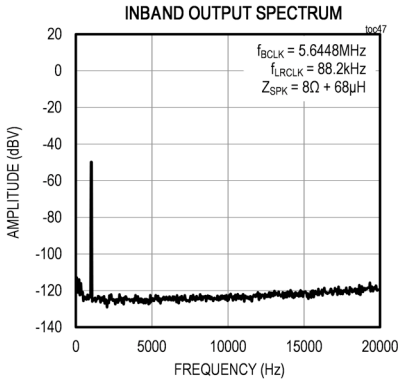
(V_{DD} = 5V, V_{GND} = 0V, GAIN_SLOT = GND (+12dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

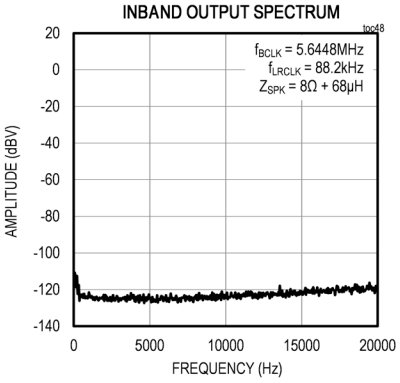


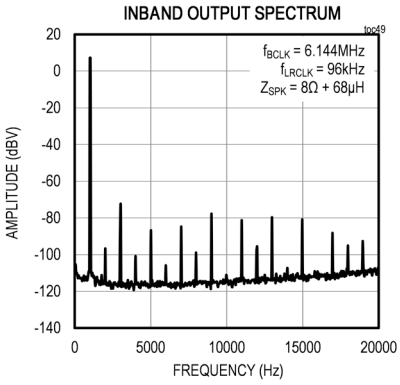


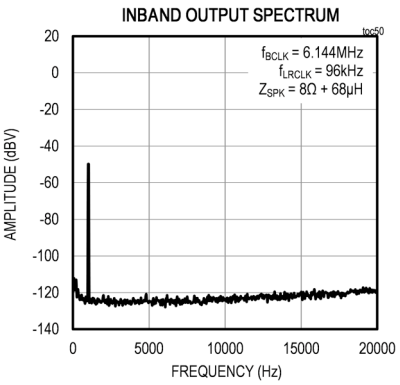


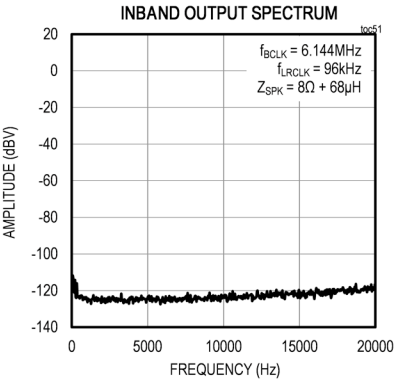




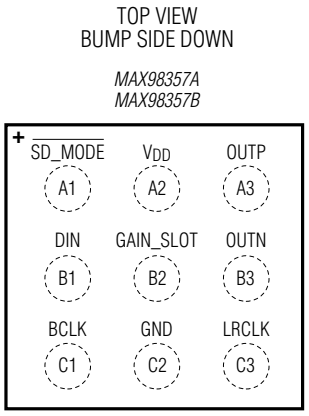




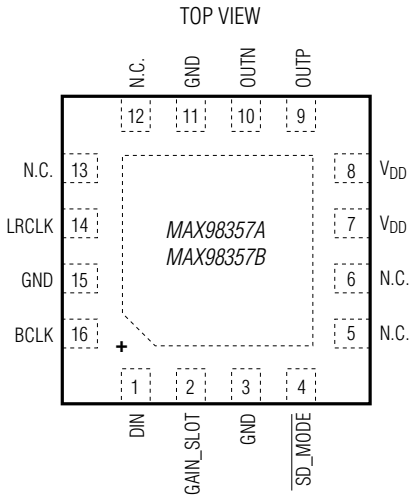




Pin Configurations



WLP



TQFN

Pin Description

PIN		NAME	FUNCTION
WLP	TQFN		
A1	4	$\overline{\text{SD\_MODE}}$	Shutdown and Channel Select. Pull $\overline{\text{SD\_MODE}}$ low to place the device in shutdown. In I²S or LJ mode, $\overline{\text{SD\_MODE}}$ selects the data channel (Table 5). In TDM mode, $\overline{\text{SD\_MODE}}$ and GAIN_SLOT are both used for channel selection (Table 7).
A2	7, 8	V_{DD}	Power-Supply Input
A3	9	OUTP	Positive Speaker Amplifier Output
B1	1	DIN	Digital Input Signal
B2	2	GAIN_ SLOT	Gain and Channel Selection. In I²S and LJ mode determines amplifier output gain (Table 8) In TDM mode, used for channel selection with $\overline{\text{SD\_MODE}}$ (Table 7). In TDM mode, gain is fixed at 12dB.
B3	10	OUTN	Negative Speaker Amplifier Output
C1	16	BCLK	Bit Clock Input
C2	3, 11, 15	GND	Ground
C3	14	LRCLK	Frame Clock. Left/right clock for I²S and LJ mode. Sync clock for TDM mode.
—	5, 6, 12, 13	N.C.	No Connection
—	—	EP	Exposed Pad. The exposed pad is not internally connected. Connect the exposed page to a solid ground plane for thermal dissipation.

Detailed Description

The MAX98357A/MAX98357B are digital PCM input Class D power amplifiers. The MAX98357A accepts standard I²S data through DIN, BCLK, and LRCLK while the MAX98357B accepts left-justified data through the same inputs. Both versions also accept 16-bit or 32-bit TDM data with up to eight slots. The digital audio interface eliminates the need for an external MCLK signal that is typically required for I²S data transmission.

$\overline{\text{SD\_MODE}}$ selects which data word is output by the amplifier and is used to put the ICs into shutdown. These devices offer five gain settings in I²S/left-justified mode and a fixed 12dB gain in TDM mode. Channel selection in TDM mode is set with the combination of SD_MODE and GAIN_SLOT (Table 7).

The MAX98357A/MAX98357B feature low-quiescent current, comprehensive click-and-pop suppression, and excellent RF immunity. The ICs offer Class AB audio performance with Class D efficiency in a minimal board-space solution. The Class D amplifier features spread-spectrum modulation with edge-rate and overshoot control circuitry that offers significant improvements in switch-mode amplifier radiated emissions. The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

Digital Audio Interface Modes

The input stage of the digital audio interface is highly flexible, supporting 8kHz–96kHz sampling rates with 16/24/32-bit resolution for I²S/left justified data as well as up to a 8-slot, 16-bit or 32-bit time division multiplexed (TDM) format. When LRCLK has a 50% duty cycle the data format is determined by the part number selection (MAX98357A/MAX98357B). When a frame sync pulse is used for the LRCLK the data format is automatically configured in TDM mode. The frame sync pulse indicates the beginning of the first time slot.

MCLK Elimination

The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin-count of the ICs.

BCLK Jitter Tolerance

The ICs feature a BCLK jitter tolerance of 0.5ns for RMS jitter below 40kHz and 12ns for wideband RMS jitter while maintaining a dynamic range greater than 98dB (Table 1).

BCLK Polarity

When operating in I²S/left justified mode, incoming serial data is always clocked-in on the rising edge of BCLK. In TDM mode, the MAX98357A clocks-in serial data on the rising edge of BCLK while the MAX98357B clocks in serial data on the falling edge of BCLK (Table 2).

LRCLK Polarity

LRCLK specifies whether left-channel data or right-channel data is currently being read by the digital audio interface. The MAX98357A indicates the left channel word when LRCLK is low, and the MAX98357B indicates the left channel word when LRCLK is high (Table 3).

LRCLK ONLY supports 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz frequencies. LRCLK clocks at 11.025kHz, 12kHz, 22.05kHz and 24kHz are **NOT** supported. Do not remove LRCLK while BCLK is present. Removing LRCLK while BCLK is present can cause unexpected output behavior including a large DC output voltage.

Standby Mode

The ICs automatically enter standby mode when BCLK is removed. If BCLK stops toggling, the ICs automati-

Table 1. RMS Jitter Tolerance

FREQUENCY	RMS JITTER TOLERANCE (ns)
< 40kHz	0.5
40kHz–BCLK	12

Table 2. BCLK Polarity

MODE	PART NUMBER	BCLK POLARITY
I²S	MAX98357A	Rising edge
Left-justified	MAX98357B	Rising edge
TDM	MAX98357A	Rising edge
	MAX98357B	Falling edge

Table 3. LRCLK Polarity

PART NUMBER	LRCLK POLARITY (LEFT CHANNEL)
MAX98357A	Low
MAX98357B	High

cally enter standby mode. In standby mode, the Class D speaker is turned off and the outputs go into a high-impedance state, ensuring that unwanted current is not transferred to the load during this condition. Standby mode has reduced power consumption from normal operation (340µA), but does not reach as low as full shutdown (0.6µA). Standby mode can be used to reduce power consumption when no GPIO us available to pull SD_MODE low.

DAC Digital Filters

The DAC features a digital lowpass filter that is automatically configured for voice playback or music playback based on the sample rate that is used. This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. Table 4 shows the digital filter settings that are automatically selected.

$\overline{\text{SD\_MODE}}$ and Shutdown Operation

The ICs feature a low-power shutdown mode, drawing less than 0.6µA (typ) of supply current. During shutdown, all internal blocks are turned off, including setting the output stage to a high-impedance state. Drive $\overline{\text{SD\_MODE}}$ low to put the ICs into shutdown.

The state of $\overline{\text{SD\_MODE}}$ determines the audio channel that is sent to the amplifier output (Table 5).

Drive $\overline{\text{SD\_MODE}}$ high to select the left word of the stereo input data. Drive $\overline{\text{SD\_MODE}}$ high through a sufficiently small resistor to select the right word of the stereo input data. Drive $\overline{\text{SD\_MODE}}$ high through a sufficiently large resistor to select both the left and right words of the stereo input data (left/2 + right/2). R_{LARGE} and R_{SMALL} are determined by the V_{DDIO} voltage (logic voltage from control interface) that is driving $\overline{\text{SD\_MODE}}$ according to the following two equations:

$$R_{SMALL}\ (k\Omega) = 94.0 \times V_{DDIO} - 100$$

$$R_{LARGE}\ (k\Omega) = 222.2 \times V_{DDIO} - 100$$

When the devices are configured in left-channel mode ($\overline{\text{SD\_MODE}}$ is directly driven to logic-high by the control interface), take care to avoid violating the Absolute Maximum Ratings limits for $\overline{\text{SD\_MODE}}$. Ensuring that V_{DD} is always greater than V_{DDIO} is one way to prevent $\overline{\text{SD\_MODE}}$ from violating the Absolute Maximum Ratings limits. If this is not possible in the application (e.g., if V_{DD} < 3.0V and V_{DDIO} = 3.3V), then it is necessary to add a small resistance (~2kΩ) in series with $\overline{\text{SD\_MODE}}$ to limit the current into the $\overline{\text{SD\_MODE}}$ pin. This is not a concern when using the right channel or (left/2 + right/2) modes.

Figure 4 and Figure 5 show how to connect an external resistor to $\overline{\text{SD\_MODE}}$ when using an open-drain driver or a push-pull driver.

Table 4. Digital Filter Settings

LRCLK FREQUENCY	-3dB CUTOFF FREQUENCY	RIPPLE LIMIT CUTOFF FREQUENCY	STOPBAND CUTOFF FREQUENCY	STOPBAND ATTENUATION (dB)
f_{LRCLK} < 30kHz	0.446 x f_{LRCLK}	0.443 x f_{LRCLK}	0.464 x f_{LRCLK}	75
30kHz < f_{LRCLK} < 50kHz	0.47 x f_{LRCLK}	0.43 x f_{LRCLK}	0.58 x f_{LRCLK}	60
f_{LRCLK} > 50kHz	0.31 x f_{LRCLK}	0.24 x f_{LRCLK}	0.477 x f_{LRCLK}	60

Table 5. $\overline{\text{SD\_MODE}}$ Control

$\overline{\text{SD\_MODE}}$ STATUS		SELECTED CHANNEL
High	$V_{\overline{SD\_MODE}}$ > B2 trip point	Left
Pullup through R_{SMALL}	B2 trip point > $V_{\overline{SD\_MODE}}$ > B1 trip point	Right
Pullup through R_{LARGE}	B1 trip point > $V_{\overline{SD\_MODE}}$ > B0 trip point	(Left/2 + right/2)
Low	B0 trip point > $V_{\overline{SD\_MODE}}$	Shutdown

Table 6. Examples of $\overline{\text{SD\_MODE}}$ Pullup Resistor Values

LOGIC VOLTAGE LEVEL (V_{DDIO}) (V)	R_{SMALL} (kΩ)	R_{LARGE} (kΩ)
1.8	69.8	300
3.3	210.2	634

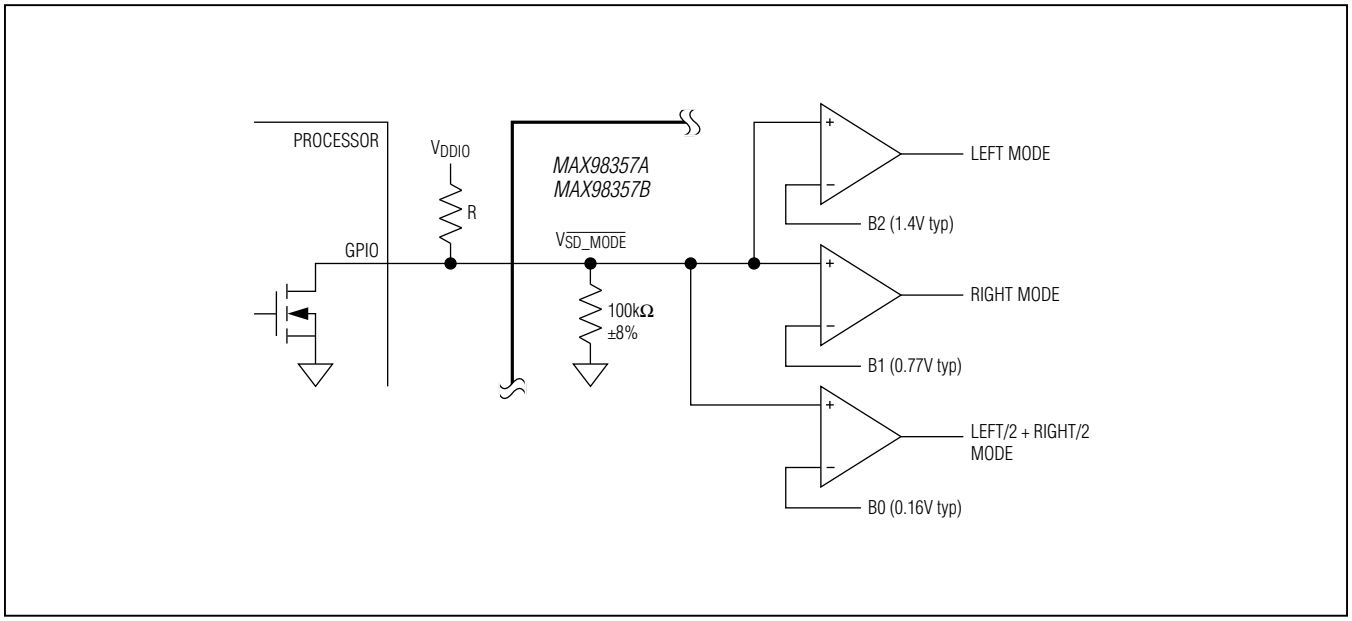


Figure 4. SD_MODE Resistor Connected Using Open-Drain Driver

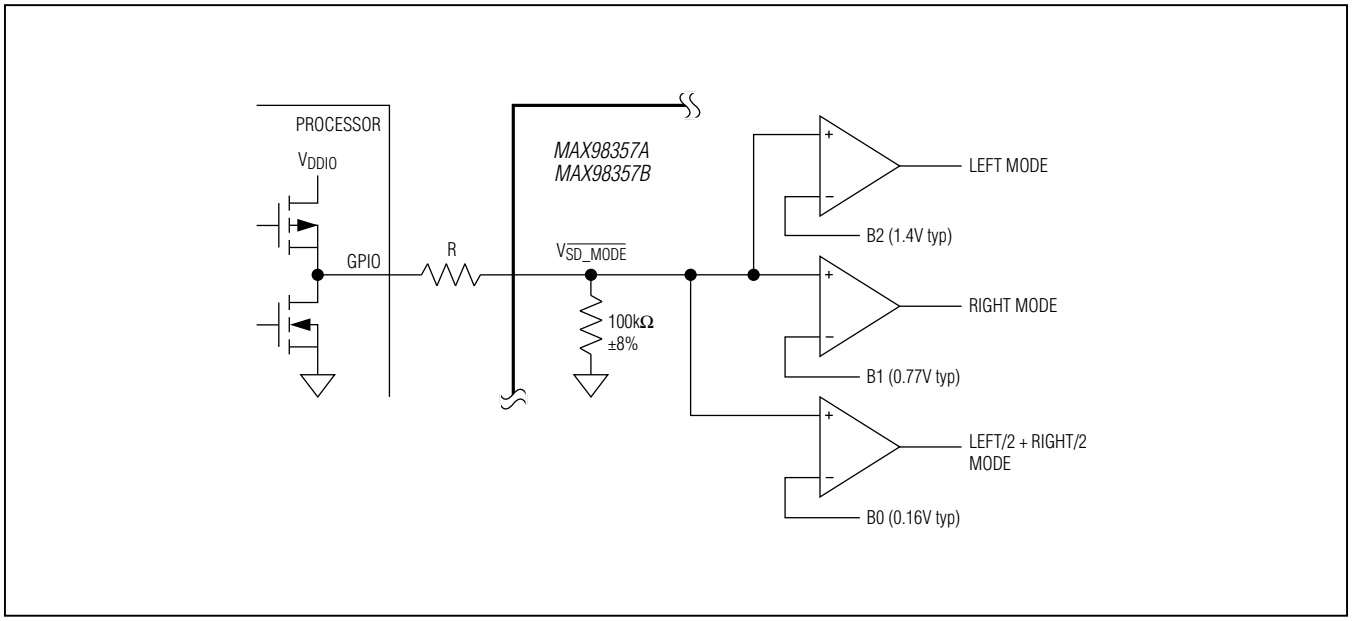


Figure 5. SD_MODE Resistor Connected Using Push-Pull Driver

I²S and Left Justified Mode

The MAX98357A follows standard I²S timing by allowing a delay of one BCLK cycle after the LRCLK transition before the beginning of a new data word (Figure 6 and Figure 7). The MAX98357B follows the left justified timing specification by aligning the LRCLK transitions with the beginning of a new data word (Figure 8 and Figure 9). LRCLK ONLY supports 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz frequencies. LRCLK clocks at 11.025kHz, 12kHz, 22.05kHz and 24kHz are **NOT** supported. Do not remove LRCLK while BLCK is present. Removing LRCLK while BCLK is present can cause unexpected output behavior, including a large DC output voltage.

The digital audio interface output mode is chosen by the voltage at $\overline{SD\_MODE}$. Table 5 shows how the available modes are selected. Trip point B0–B2 are shown the *Electrical Characteristics* in the $\overline{SD\_MODE}$ Comparator Trip Points section. Values for $\overline{SD\_MODE}$ pullup resistors R_{SMALL} and R_{LARGE} are dependent on the voltage level of V_{DDIO}. See Table 6 for pullup resistor values.

TDM Mode

TDM mode is automatically detected by monitoring the short channel sync pulse on LRCLK. The frequency detector circuit detects the bit depth. In TDM mode, the MAX98357A/MAX98357B has a fixed gain of 12dB. GAIN_SLOT and $\overline{SD\_MODE}$ are used to select to which of 8 channels of TDM data the parts respond. Table 7 shows the connections for GAIN_SLOT and $\overline{SD\_MODE}$ for channel selection. The MAX98357A data is valid on the BCLK rising edge. The MAX98357B data is valid on the BCLK falling edge.

Figure 10, Figure 11, Figure 12, and Figure 13 show TDM operation, in which a frame-sync pulse is used for LRCLK. In TDM mode, there must be 128 (16-bit mode) or 256 (32-bit mode) BCLK cycles per frame. In TDM mode, the ICs only accept 16-bit or 32-bit formatted data and any of the 8 TDM slots can be selected.

Table 7. TDM Mode Channel Selection

$\overline{SD\_MODE}$	GAIN_SLOT	CHANNEL	BITS
Low	X	Off	N/A
V_{DD}	GND	0	16/32
V_{DD}	V_{DD} with 0Ω	1	16/32
V_{DD}	Float	2	16/32
V_{DD}	V_{DD} with 100kΩ	3	16/32
V_{DD}	GND with 100kΩ	4	16/32
V_{DD} through R_{LARGE}	GND	5	16/32
V_{DD} through R_{LARGE}	Float	6	16/32
V_{DD} through R_{LARGE}	V_{DD}	7	16/32

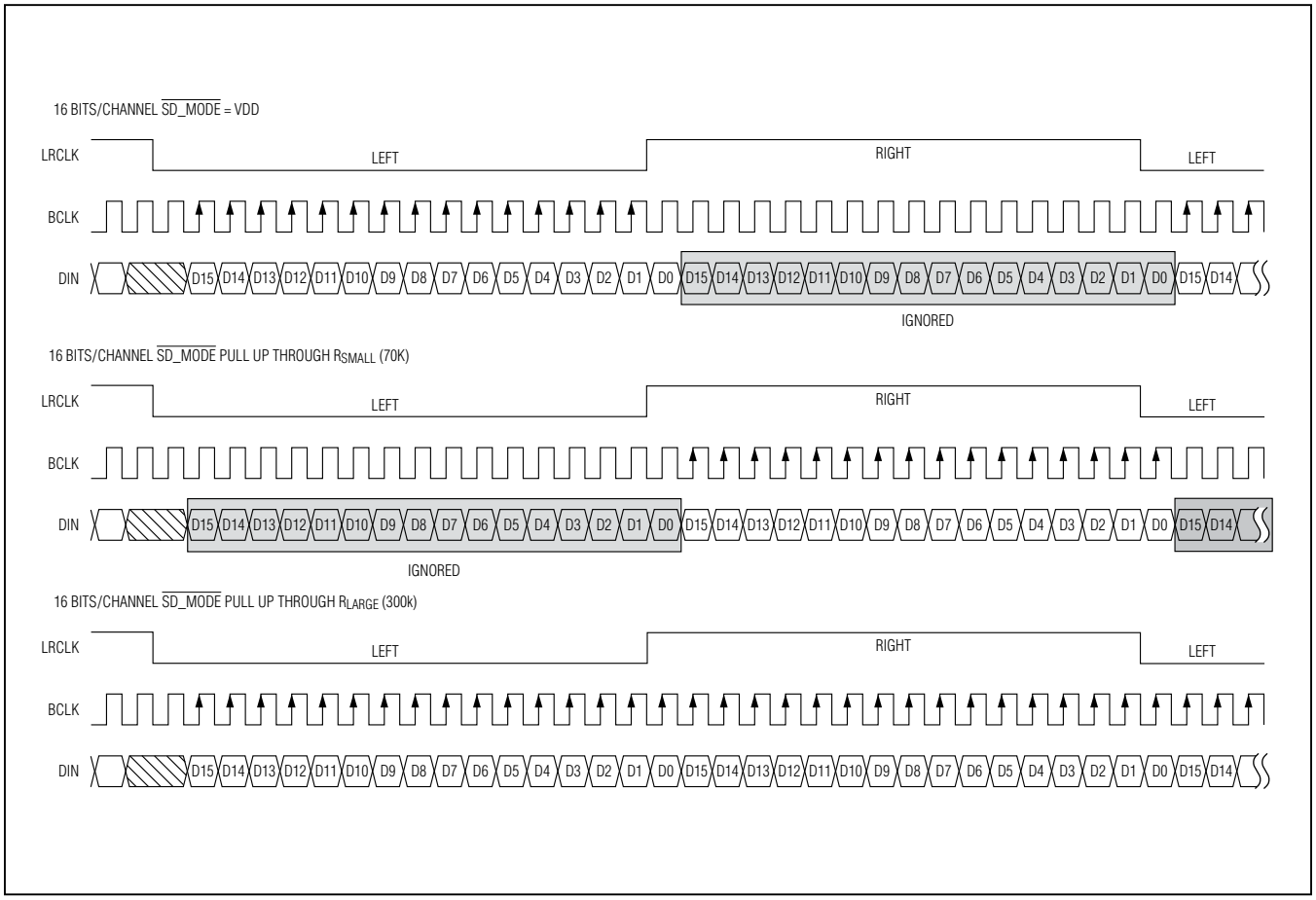


Figure 6. MAX98357A I²S Digital Audio Interface Timing, 16-Bit Resolution

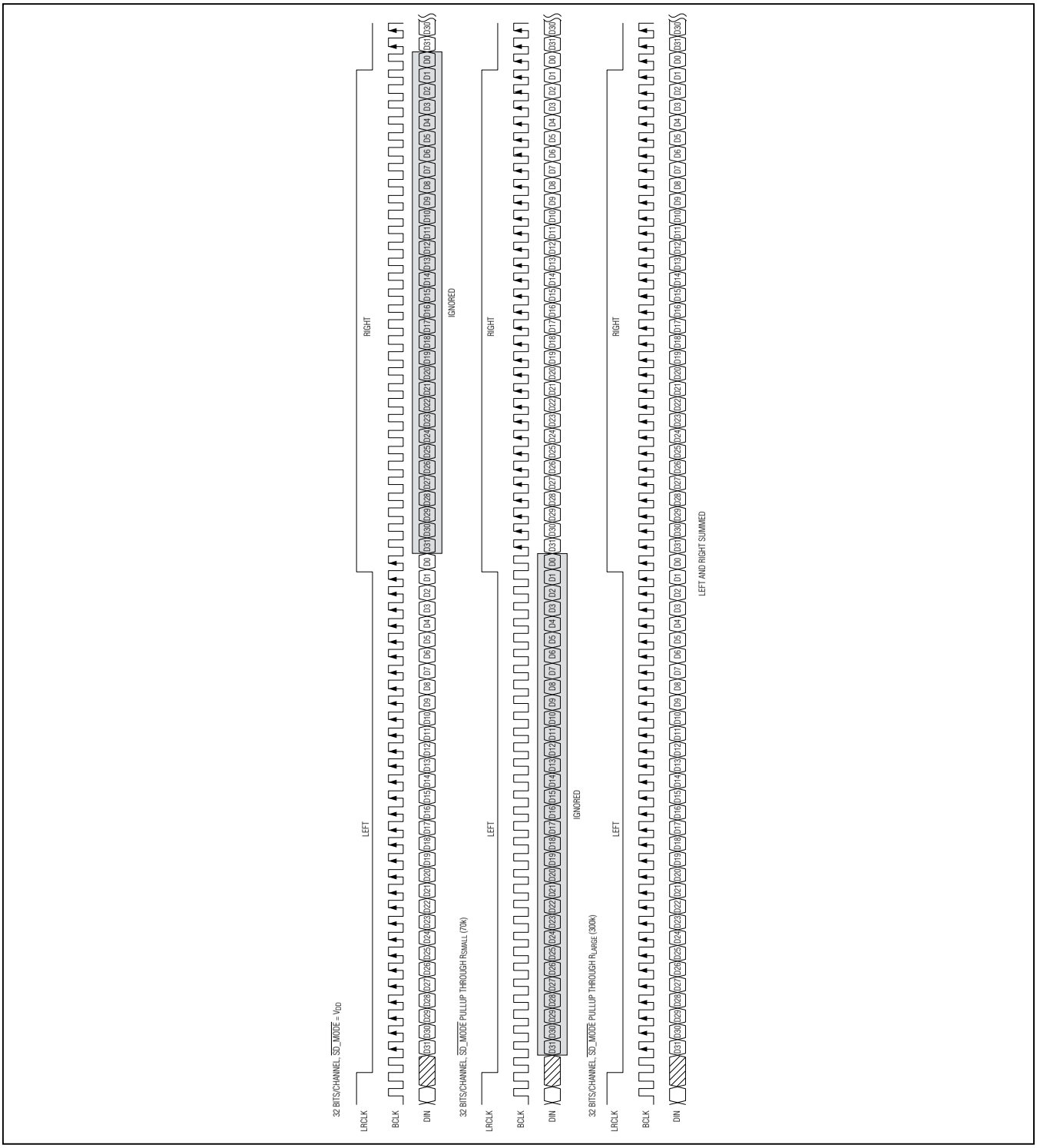


Figure 7. MAX98357A I²S Digital Audio Interface Timing, 32-Bit Resolution

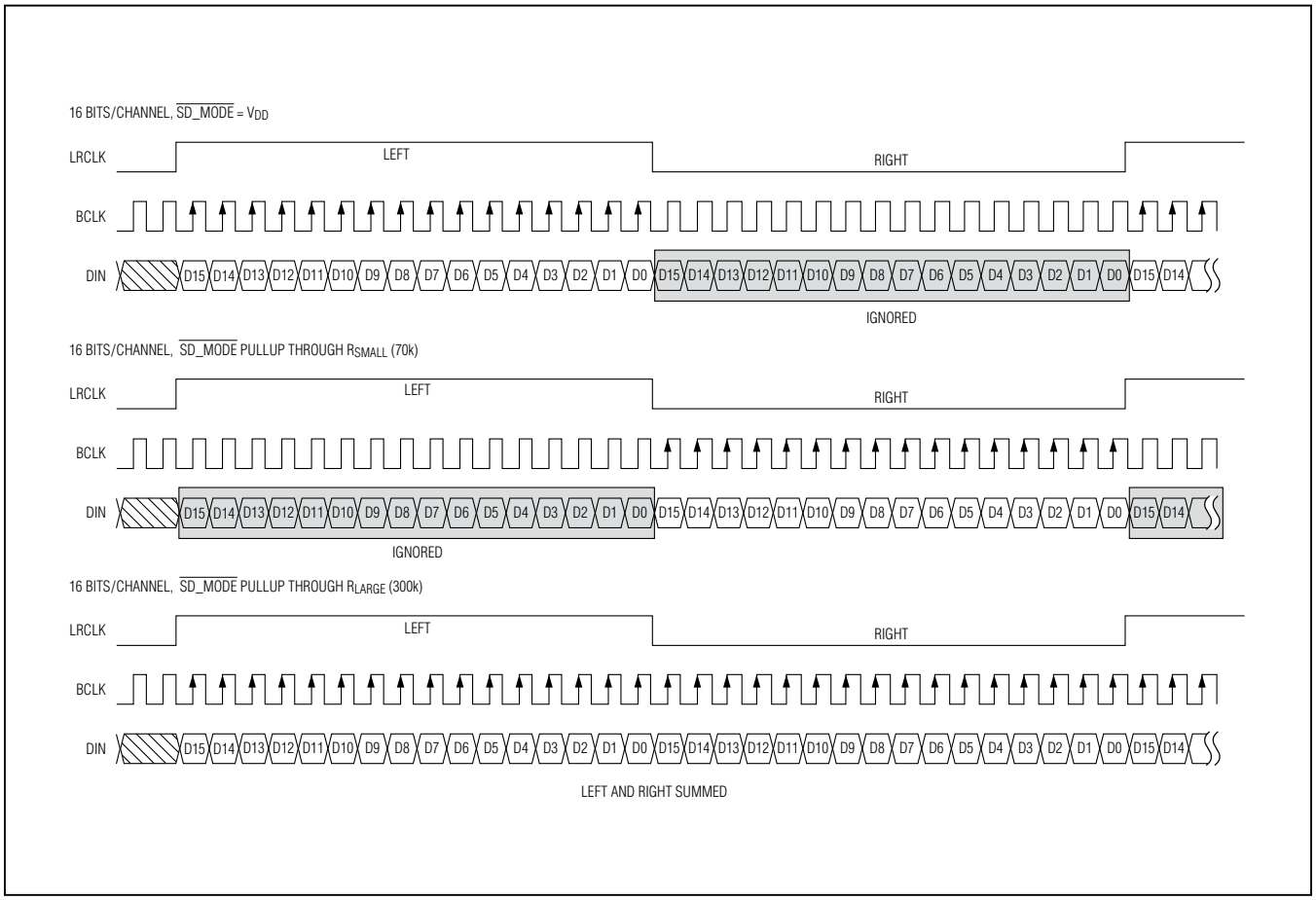


Figure 8. MAX98357B Left-Justified Digital Audio Interface Timing, 16-Bit Resolution

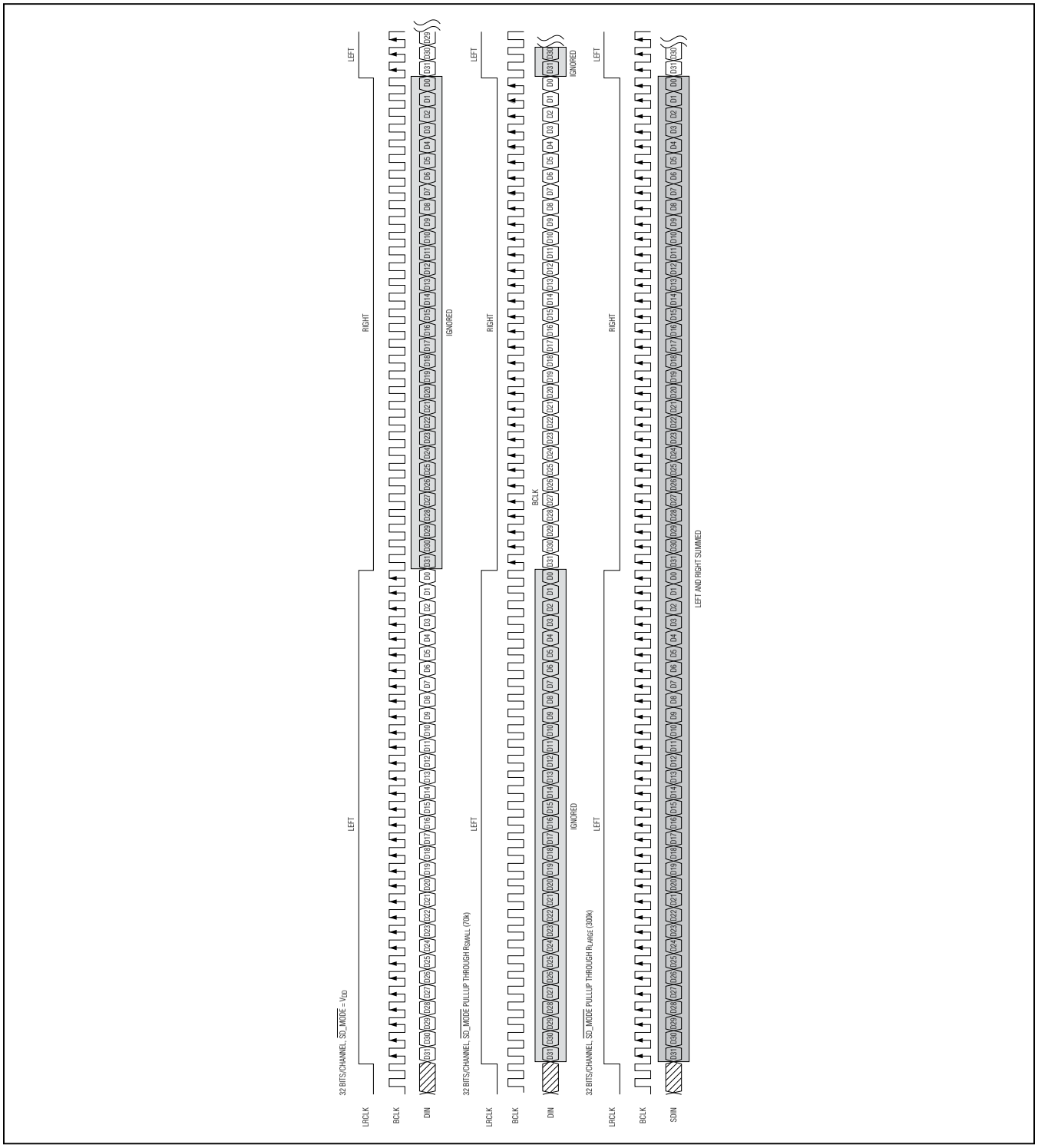


Figure 9. MAX98357B Left-Justified Digital Audio Interface Timing, 32-Bit Resolution

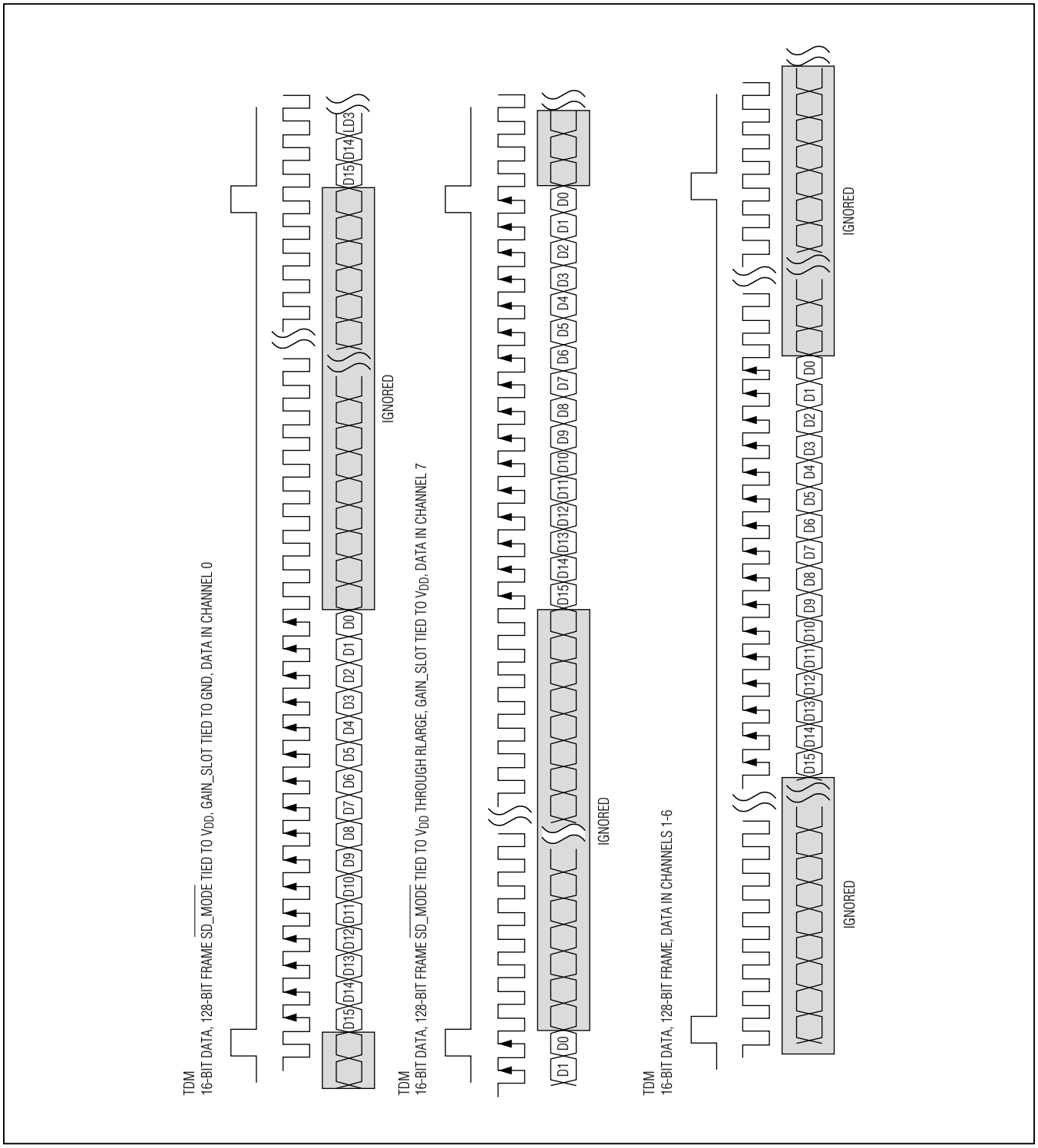


Figure 10. MAX98357A TDM 16-Bit DAI Timing

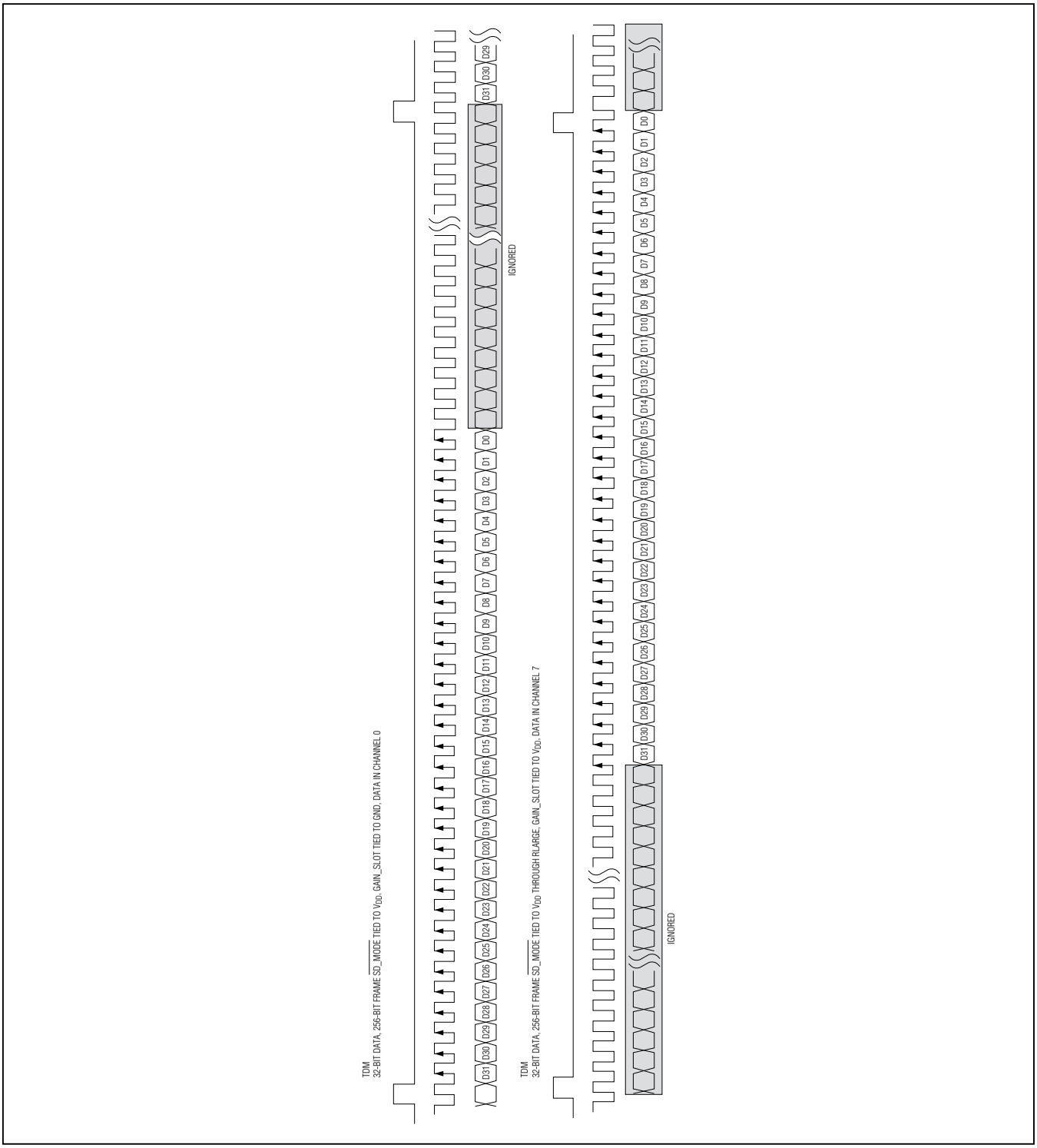


Figure 11. MAX98357A TDM 32-Bit DAI Timing