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MAX98371

Digital Input Class D Speaker Amplifier with Dynamic Headroom Tracking

General Description

The MAX98371 is a high-efficiency, mono Class D audio amplifier featuring dynamic headroom tracking (DHT). DHT automatically optimizes the headroom available to the Class D amplifier as the power supply voltage varies, due to sudden transients and declining battery life to maintain a consistent listening experience. A wide 5.5V to 18V supply range allows the device to reach 19W into an 8Ω load.

The MAX98371's flexible digital audio interface (DAI) supports I²S, left-justified, and TDM formats. The digital audio interface accepts 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz sample rates with 16-/24-/32-bit data supported for all data formats. In TDM mode, the device can support up to 16 channels of audio data. A unique clocking structure eliminates the need for an external MCLK signal that is typically needed for PCM communication. This reduces pin count and simplifies board layout.

Active emissions limiting with edge rate control minimizes EMI, and eliminates the need for output filtering found in traditional Class D devices.

An 8-bit PVDD supply voltage ADC enables the Dynamic Headroom Tracking circuit. DHT optimizes audio program peak behavior as the supply voltage varies and provides flexible user-defined parameters.

Thermal foldback protection ensures robust behavior when the thermal limits of the device are exercised. The circuit can be enabled to automatically reduce the output power above a user specified temperature. This allows for uninterrupted music playback even at high ambient temperatures. Traditional thermal protection is also available in addition to robust overcurrent protection.

All MAX98371 control is performed using a standard 2-wire, I²C interface. One of sixteen slave addresses can be selected through two, four-level address pins. The IC is available in a 0.4mm pitch, 30-bump WLP package. It is specified over the extended, -40°C to +85°C temperature range.

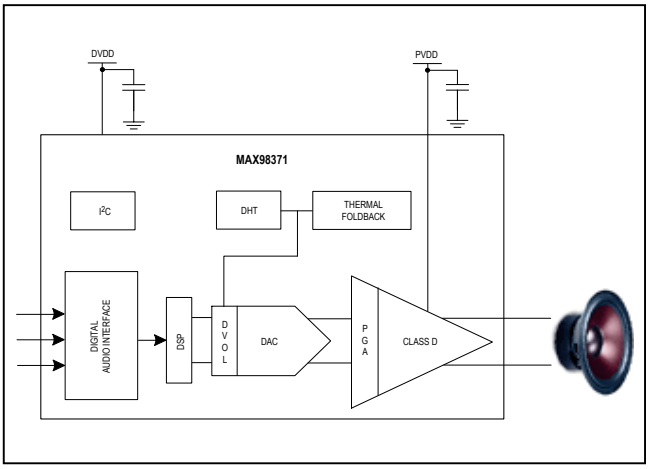
Applications

- Tablets
- Notebook Computers
- Soundbars

Benefits and Features

- Wide Supply Range (5.5V to 18V)
- Dynamic Headroom Tracking Maintains a Consistent Listening Experience
- Integrated Thermal Foldback Allows Robust Operation in a WLP Package
- Remote Output Sensing Allows Up to 20dB THD+N Improvement When Ferrites Are Used
- Class D Edge Rate Control Enables Filterless Operation
- 110dB A-Weighted Dynamic Range
- Output Power at 1% THD+N:
  - 15.7W into 8Ω, V_{PVDD} = 17V
  - 13.2W into 4Ω, V_{PVDD} = 12V
- Output Power at 10% THD+N
  - 19W into 8Ω, V_{PVDD} = 17V
  - 15.8W into 4Ω, V_{PVDD} = 12V
- Speaker Amplifier Efficiency
  - 91% at 10W into 8Ω, V_{PVDD} = 12V
  - 81% at 15W into 4Ω, V_{PVDD} = 12V
- Extensive Click-and-Pop Suppression
- Space Saving, 30-Bump WLP Package (2.1mm x 2.6mm x 0.6mm, 0.4mm Pitch)

Simplified Block Diagram



Ordering Information ***appears at end of data sheet.***

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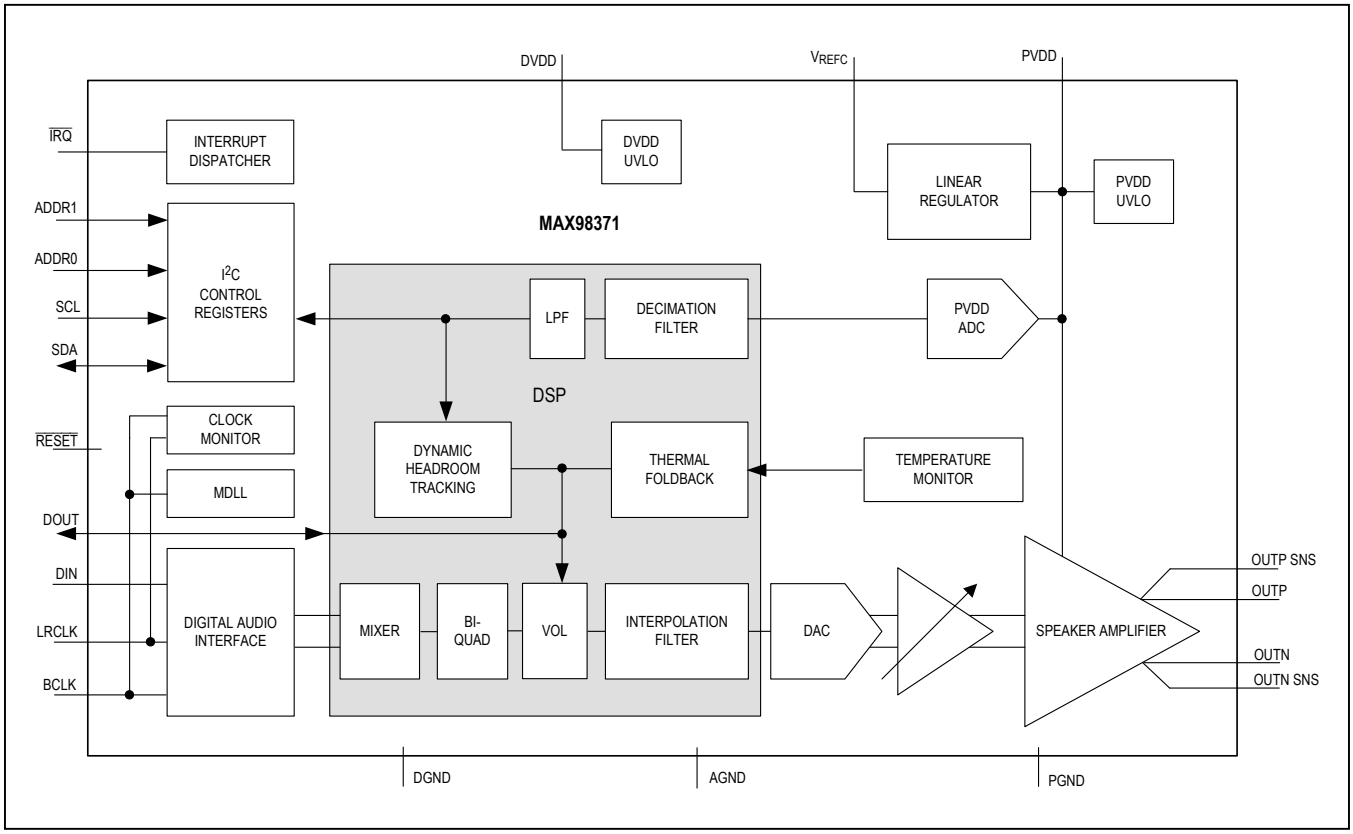


Absolute Maximum Ratings

PVDD to PGND ..... -0.3V to 20V
OUT_ to PGND ..... -0.3V to (V_{PVDD} + 0.3V)
V_{REFC} to AGND ..... -0.3V to 2.2V
DVDD to DGND ..... -0.3V to 2.2V
SDA, SCL, ADDR_, $\overline{IRQ}$ to DGND ..... -0.3V to 2.2V
BCLK, LRCLK, DIN, $\overline{RESET}$ to DGND ..... -0.3V to (V_{DVDD} + 0.3V)
AGND, DGND to PGND ..... -0.1V to 0.1V

Short-Circuit Duration
Between OUTP, OUTN and PGND or PVDD ..... Continuous
Between OUTP and OUTN ..... Continuous
Continuous Power Dissipation (T_A = +70°C) for Multilayer Board (derate 27mW/°C above +70°C) 1.9W
Junction Temperature ..... 150°C
Operating Temperature Range ..... -40°C to 85°C
Storage Temperature Range ..... -65°C to 150°C
Soldering Temperature (reflow) ..... 260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 37°C/W
Junction-to-Board Thermal Resistance (θ_{JB}) ..... 33.4°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{PVDD} = 12V, V_{DVDD} = $\overline{RESET}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Power Supply Voltage Range	V_{PVDD}			5.5		18	V
	V_{DVDD}			1.14		1.98	
VREFC Regulator Output	V_{REFC}				2.0		V
PVDD Under Voltage Lockout	PVDD UVLO			3.65	4.3	4.75	V
DVDD Under Voltage Lockout	DVDD UVLO				0.75		V
Quiescent Current	I_{Q_PVDD}	SPK_SWCLK = 0	472kHz		8.4	12	mA
		SPK_SWCLK = 1	330kHz		7		
Quiescent Current	I_{Q_DVDD}				1.5	2.5	mA
Software Shutdown Supply Current	I_{SHDN_SW}	All DAI pins pulled low, T_A = +25°C	I_{PVDD}			10	µA
			I_{DVDD}			10	
Hardware Shutdown Supply Current	I_{SHDN_HW}	$\overline{RESET}$ =0V, T_A = +25°C	I_{PVDD}			5	µA
			I_{DVDD}			1	
Turn-On Time	t_{ON}	From SW_EN bit set to full operation	Volume ramping disabled		10		ms
			Volume ramping enabled		30		

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Turn-Off Time	t_{OFF}	From SW_EN bit cleared to shutdown	Volume ramping disabled		10		ms
			Volume ramping enabled		30		
DIGITAL FILTER CHARACTERISICS (LRCLK < 50kHz) (Note 5)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff			0.43 x f_S		Hz
		-3dB cutoff			0.47 x f_S		
		-6.02dB cutoff			0.5 x f_S		
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.58 x f_S	Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DIGITAL FILTER CHARACTERISICS (LRCLK > 50kHz) (Note 5)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff			0.24 x f_S		Hz
		-3dB cutoff			0.31 x f_S		
Passband Ripple		f < f_{PLP}		-0.1		+0.1	dB
Stopband Cutoff	f_{SLP}					0.417 x f_S	Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DIGITAL HIGHPASS FILTER CHARACTERISTICS							
DC Attenuation (Note 5)				80			dB
DC Blocking Cutoff Frequency (Note 5)		Across all sample rates	DACHPF = 0x1			2	Hz
Highpass Cutoff Frequency		Across all sample rates	DACHPF = 0x2		50		Hz
			DACHPF = 0x3		100		
			DACHPF = 0x4		200		
			DACHPF = 0x5		400		
			DACHPF = 0x6		800		
SPEAKER AMPLIFIER ELECTRICAL CHARACTERISTICS							
DIGITAL VOLUME CONTROL							
Digital Volume (max)		DVOL[6:0] = 0x00			0		dB
Digital Volume (min)		DVOL[6:0] = 0x7E			-63		dB
Volume Control Step Size					0.5		dB
Output Offset Voltage	VOS	T_A = +25°C			±1	±5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second, digital audio inputs have zero-code input	Into shutdown		-66		dBV
			Out of shutdown		-60		

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
Dynamic Range	DR	V_{PVDD} = 17V, Z_L = 8Ω + 33µH, measured using the EIAJ method, -60dBFS 1kHz output signal, referenced to 1% output power	A-weighted		110		dB
Integrated Output Noise	e_N	Z_L = 8Ω + 33µH	A-weighted		35		μV_{RMS}
			Unweighted		72		
Output Power	P_{OUT}	THD+N ≤ 1%, f = 1kHz	Z_L = 8Ω + 33µH		8.2		W
			Z_L = 8Ω + 33µH, V_{PVDD} = 17V		15.7		
			Z_L = 4Ω + 33µH		13.2		
		THD+N ≤ 10%, f = 1kHz	Z_L = 8Ω + 33µH		10.2		
			Z_L = 8Ω + 33µH, V_{PVDD} = 17V		19		
			Z_L = 4Ω + 33µH		15.8		
Efficiency	η_{SPK}	f = 1kHz	P_{OUT} = 10W, Z_L = 8Ω + 33µH		91		%
			P_{OUT} = 15W, Z_L = 4Ω + 33µH		81		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz	P_{OUT} = 4W, Z_L = 8Ω + 33µH		0.02		%
			P_{OUT} = 8W, Z_L = 4Ω + 33µH		0.03		
		f = Up to 6kHz	P_{OUT} = 4W, Z_L = 8Ω + 33µH		0.1		
			P_{OUT} = 8W, Z_L = 4Ω + 33µH		0.2		
Maximum Frequency Response Deviation		Maximum deviation above and below 1kHz reference			0.2		dB
Gain Error	A_{VERROR}	f =1kHz, V_O = 2.828V_{RMS}		-0.5		+0.5	dB
Maximum Channel-to-Channel Phase Error (Note 3)		Output phase shift between multiple devices from 20Hz to 20kHz, across all sample rates and DAI operating modes			1		deg

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
PVDD Power Supply Rejection Ratio	PSRR		V_{PVDD} = 5.5V to 18V		85		dB
			f = 20Hz to 10kHz, V_{RIPPLE} = 100mV_{P-P}		75		
			f = 10kHz to 20kHz, V_{RIPPLE} = 100mV_{P-P}		60		
DVDD Power Supply Rejection Ratio	PSRR		f = 1kHz, V_{RIPPLE} = 50mV_{P-P}		100		
Output Switching Frequency	f_S	Constant across all sample rates	SPK_SWCLK = 0		472		kHz
			SPK_SWCLK = 1		330		kHz
Output Stage On-Resistance	R_{ON}	PMOS + NMOS			0.425		Ω
Current Limit	I_{LIM}	Z_L = 8Ω + 33µH or Z_L = 4Ω + 33µH		4.5	6.0		A
THERMAL FOLDBACK							
Attack Time					10		µs
Attenuation Slope		THRM_SLOPE[1:0] = 0x0			0.5		dB/°C
		THRM_SLOPE[1:0] = 0x1			1		
		THRM_SLOPE[1:0] = 0x2			2		
Maximum Attenuation					12		dB
Release Time		THRM_REL[1:0] = 0x0			3		ms/dB
		THRM_REL[1:0] = 0x3			300		
THERMAL SHUTDOWN							
Trigger Point		(Note 3)		140	150	160	°C
Hysteresis					20		°C
PVDD ADC ELECTRICAL CHARACTERISTICS							
Resolution					8		Bits
Absolute Error					1.2		LSB
ADC Voltage Range				5.35		18.15	V
ADC Lowpass Filter Cutoff Frequency		-3dB limit			0.0875 x f_S		Hz

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION		MIN	TYP	MAX	UNITS
ADC Lowpass Filter Stopband Frequency		-40dB limit			0.167 x f_S		Hz
ADC Programmable Lowpass Filter		PVDD_ADC_BW[1:0] = 0x1			2		Hz
		PVDD_ADC_BW[1:0] = 0x2			20		
		PVDD_ADC_BW[1:0] = 0x3			200		
DIGITAL I/O CHARACTERISTICS							
DIN, BCLK, LRCLK, ADDR_, $\overline{RESET}$							
Input Voltage High	V_{IH}			0.7 x V_{DVDD}			V
Input Voltage Low	V_{IL}					0.3 x V_{DVDD}	V
Input Leakage Current	I_{IH}, I_{IL}			-1		+1	µA
Input Capacitance	C_{IN}				3		pF
INPUT (SDA, SCL)							
Input Voltage High	V_{IH}			0.7 x V_{DVDD}			V
Input Voltage Low	V_{IL}					0.3 x V_{DVDD}	V
Input Hysteresis	V_{HYS}				200		mV
Input Capacitance	C_{IN}				3		pF
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C, input high		-1		+1	µA
OUTPUT (SDA, $\overline{IRQ}$)							
Output Low Voltage	V_{OL}	I_{SINK} = 3mA				0.4	V
Output Current	I_{OL}				13		mA
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS							
GLOBAL							
LRCLK Frequency Range	f_{LRCLK}	All DAI operating modes		32		96	kHz
Word Length		All DAI operating modes			16		bits
					24		
					32		
BCLK Duty Cycle				45		55	%
Maximum BCLK/LRCLK Input Jitter		Maximum jitter with minimal performance degradation	RMS jitter below 40kHz		0.5		ns
			RMS jitter above 40kHz		0.9		

Electrical Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, C_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
PCM MODE (I^2S, LEFT-JUSTIFIED)						
LRCLK Duty Cycle			45		55	%
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		10			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		10			ns
DIN to BCLK Active Edge Setup Time	t_{SETUP}		10			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		10			ns
BCLK Period (Note 3)	t_{BCLK}		160			ns
BCLK Frequency (Note 3)	f_{BCLK}				6.25	MHz
				f_S x 32		
				f_S x 48		
				f_S x 64		
TDM MODE						
LRCLK Pulse Width	PW_{LRCLK}	Measured in number of BCLK cycles			511	cycles
DIN Frame Delay after LRCLK Edge		Measured in number of BCLK cycles	0		2	cycles
BCLK Period (Note 3)	t_{BCLK}		20			ns
BCLK Frequency (Note 3)	f_{BCLK}	All TDM operating modes			50	MHz

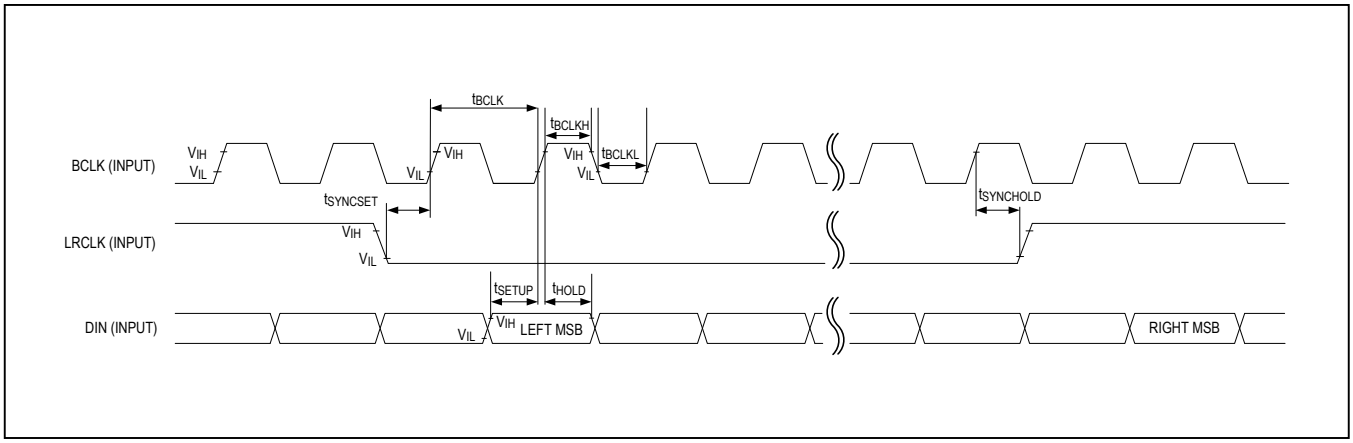


Figure 1. I²S Audio Interface Timing Diagram

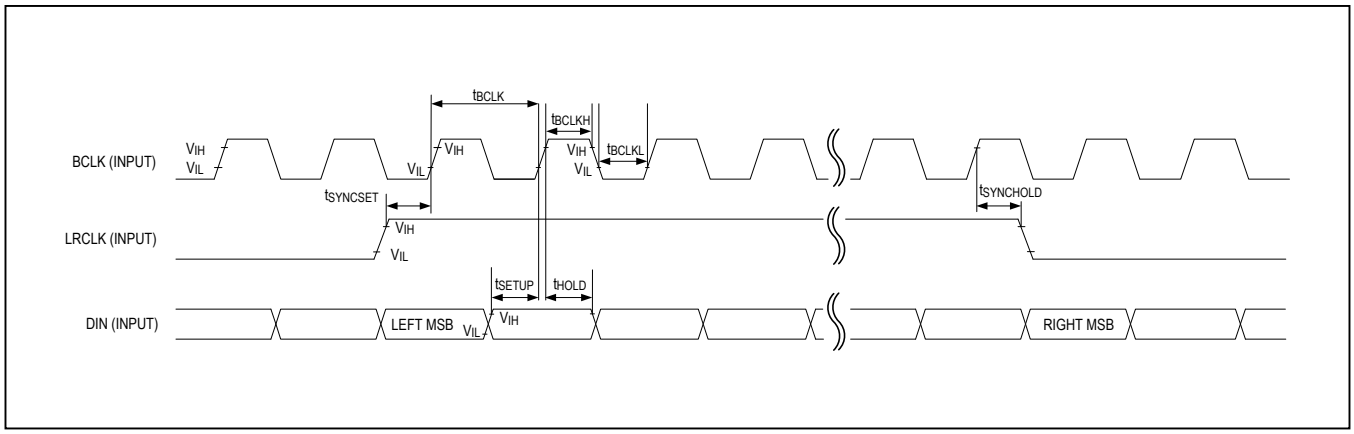


Figure 2. Left-Justified Audio Interface Timing Diagram

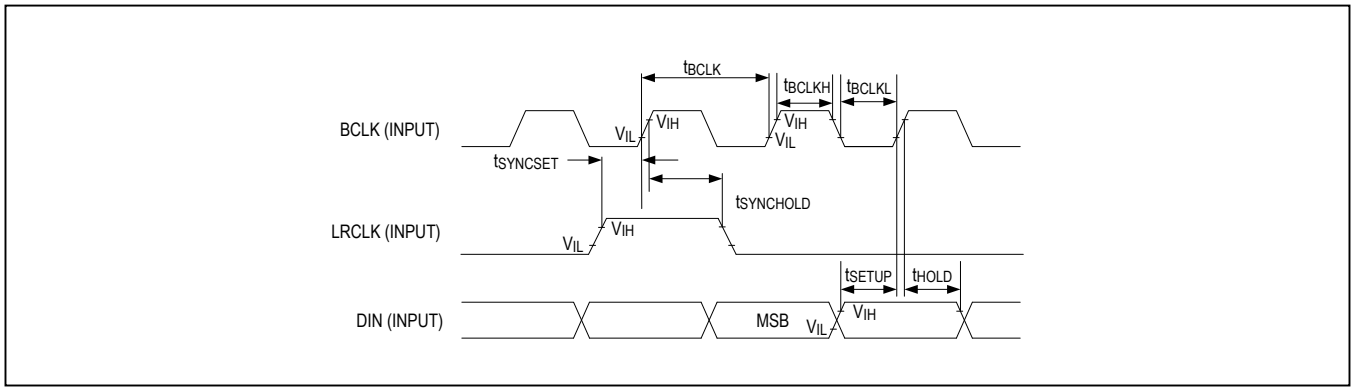


Figure 3.TDM Audio Interface Timing Diagrams

I²C Timing Characteristics

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, CV_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I²C TIMING CHARACTERISTICS						
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$		0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time (Note 4)	t_R		20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time (Note 4)	t_F		20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F		20		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

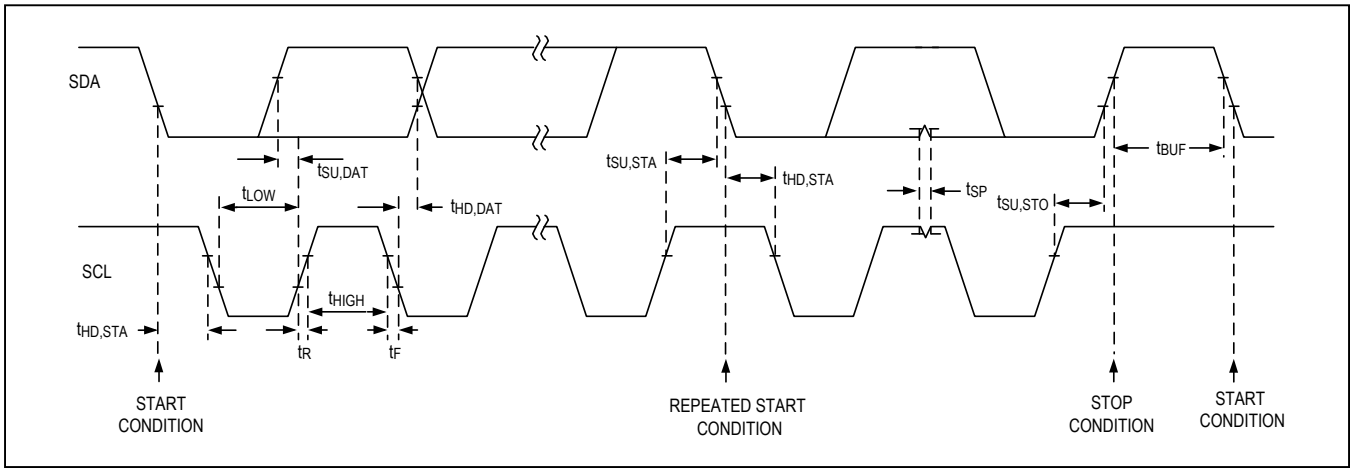


Figure 4. I²C Interface Timing Diagram

Power Consumption

(V_{PVDD} = 12V, V_{DVDD} = $V_{\overline{RESET}}$ = 1.8V, V_{GND} = 0V, C_{PVDD} = 1x 220µF, 2x 10µF, 2x 0.1µF, CV_{REFC} = 1µF, C_{DVDD} = 1µF, Z_{SPK} = open, AC measurement bandwidth 20Hz to 22kHz, f_S = 48kHz, 24-bit data, T_A = T_{MIN} to T_{MAX}, unless, otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

CONDITION	I_{PVDD} (mA)	P_{PVDD} (mW)	I_{DVDD} (mA)	P_{DVDD} (mW)	P_{TOTAL} (mW)
f_{SPK} = 330kHz					
PCM to SPK	7.0	84.0	1.3	2.3	86.3
PCM to SPK, DHT	7.3	88.0	1.8	3.3	91.3
PCM to SPK, LMTR	7.0	84.0	1.8	3.2	87.2
f_{SPK} = 472kHz					
PCM to SPK,	8.4	100.8	1.3	2.3	103.1
PCM to SPK, DHT	8.8	105.6	1.8	3.3	108.9
PCM to SPK, LMTR	8.5	101.5	1.8	3.2	104.7
f_{SPK} = 472kHz AND PVDD = 17V					
PCM to SPK	9.3	157.7	1.3	2.3	160.0
PCM to SPK, DHT	6.6	163.0	1.8	3.3	166.6
PCM to SPK, LMTR	6.0	157.1	1.8	3.2	160.3

Note 2: 100% production tested at T_A = +25C. Specifications over temperature limits are guaranteed by design. Typical values are based on 1 sigma characterization data, unless otherwise noted.

Note 3: Minimums and/or maximum limits shown are design targets and not 100% production tested. Characterization data is provided to validate device performance.

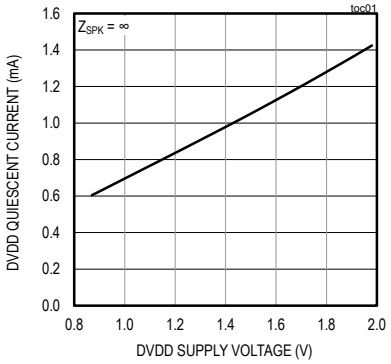
Note 4: C_B in pF.

Note 5: Digital filter performance is invariant over temperature and production tested at T_A = +25C.

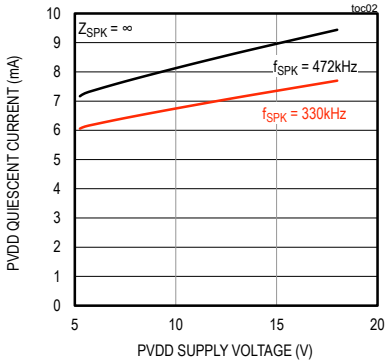
Typical Operating Characteristics

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

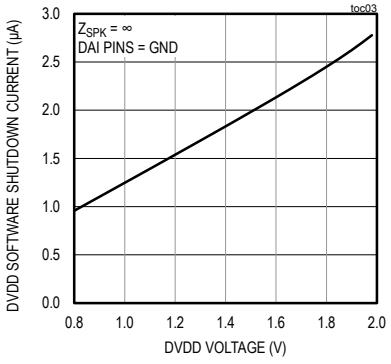
DVDD QUIESCENT CURRENT vs. DVDD VOLTAGE



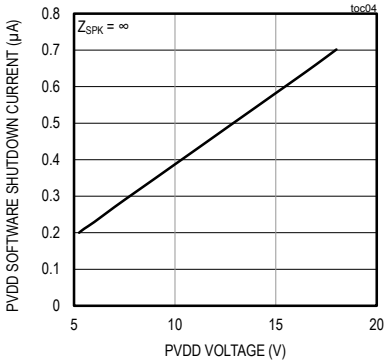
PVDD QUIESCENT CURRENT vs. PVDD VOLTAGE



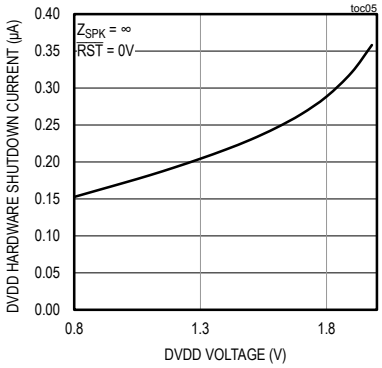
DVDD SOFTWARE SHUTDOWN CURRENT vs. DVDD VOLTAGE



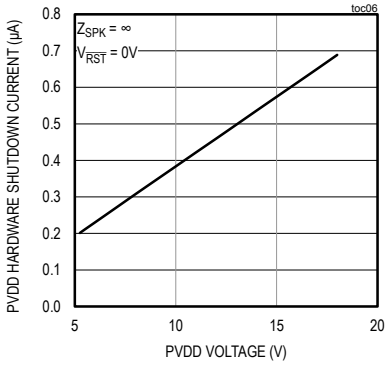
PVDD SOFTWARE SHUTDOWN CURRENT vs. PVDD VOLTAGE



DVDD HARDWARE SHUTDOWN CURRENT vs. DVDD VOLTAGE



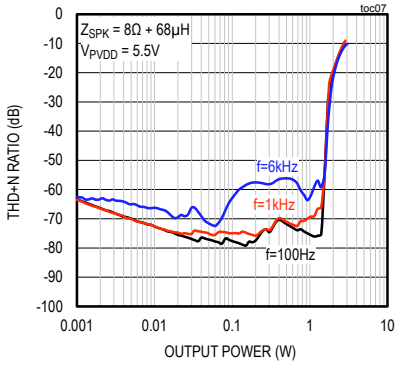
PVDD HARDWARE SHUTDOWN CURRENT vs. PVDD VOLTAGE



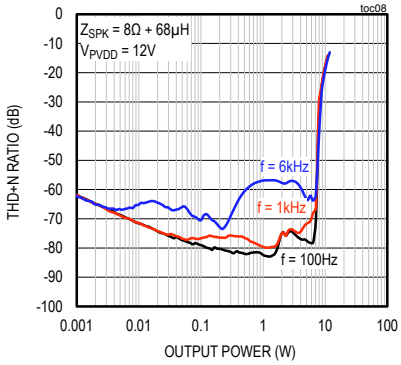
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

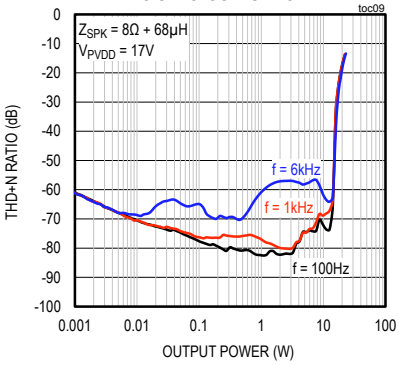
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



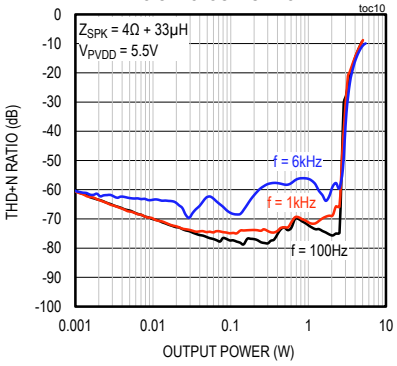
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



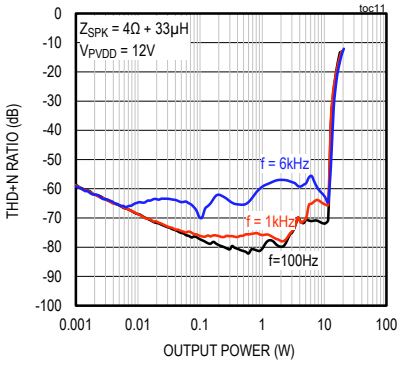
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



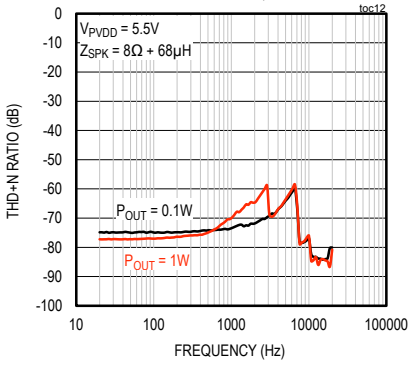
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



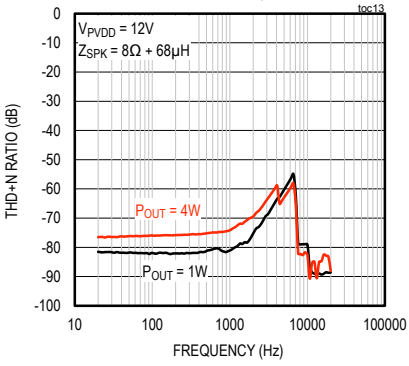
TOTAL HARMONIC DISTORTION + NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



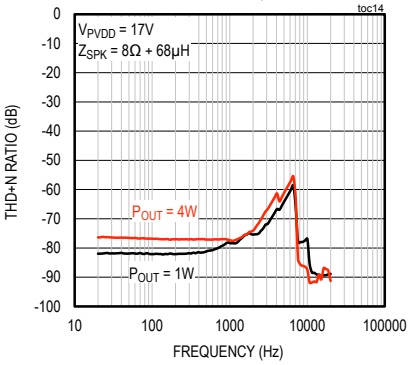
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



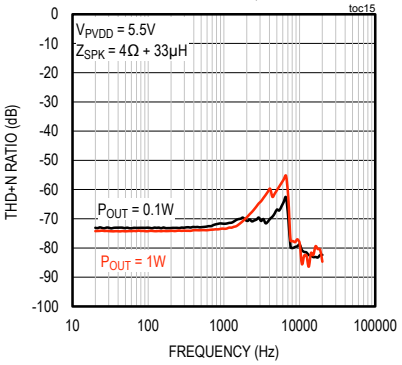
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

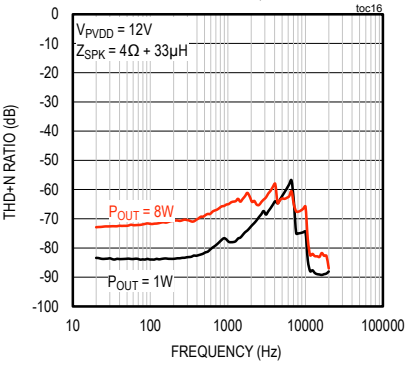
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



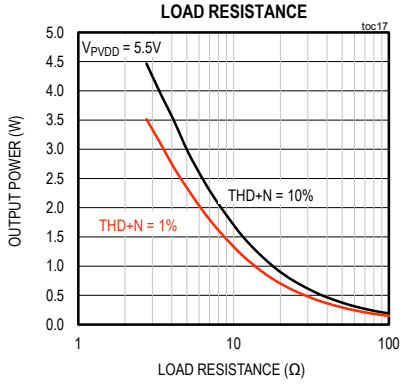
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



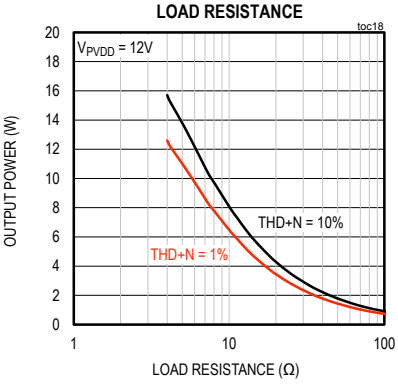
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



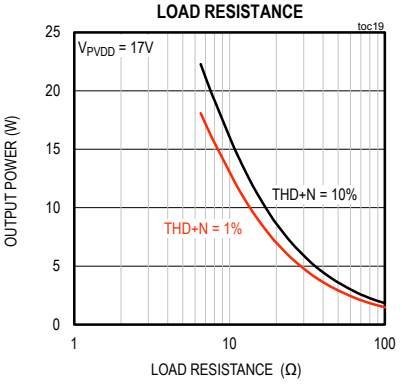
OUTPUT POWER vs. LOAD RESISTANCE



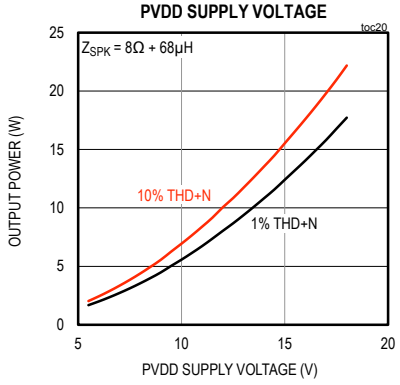
OUTPUT POWER vs. LOAD RESISTANCE



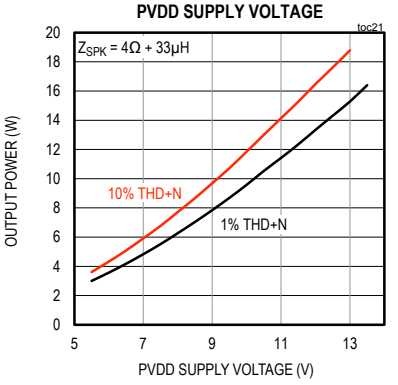
OUTPUT POWER vs. LOAD RESISTANCE



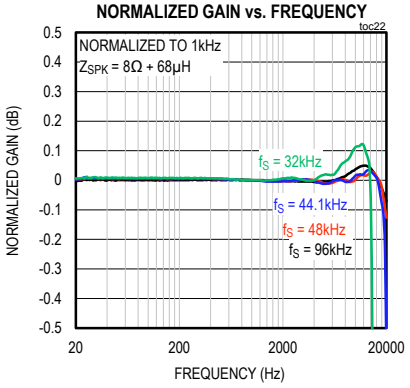
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



OUTPUT POWER vs. PVDD SUPPLY VOLTAGE

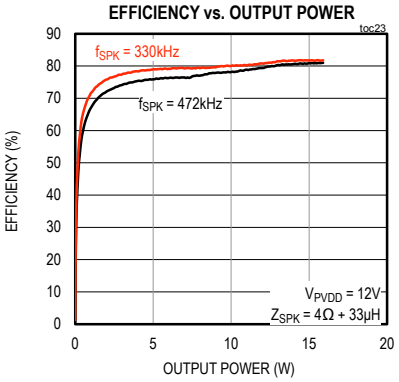


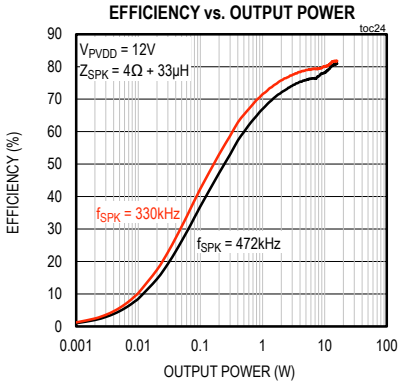
NORMALIZED GAIN vs. FREQUENCY

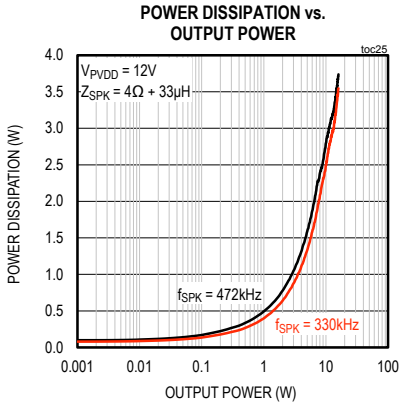


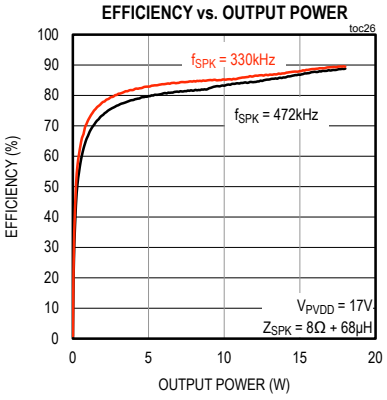
Typical Operating Characteristics (continued)

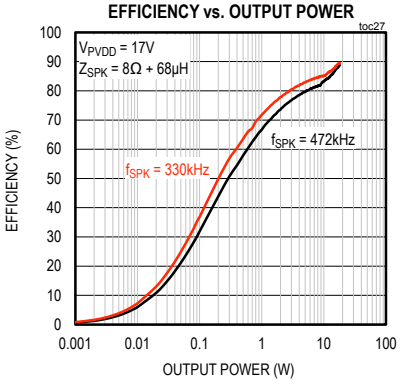
(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

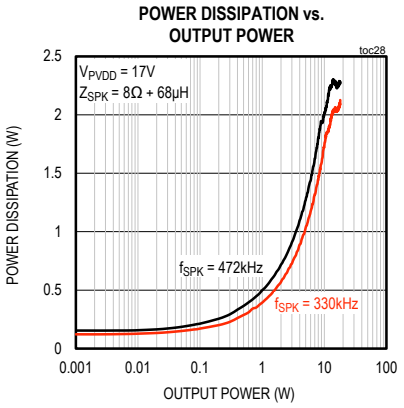


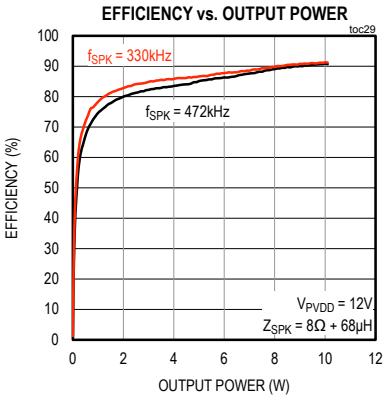


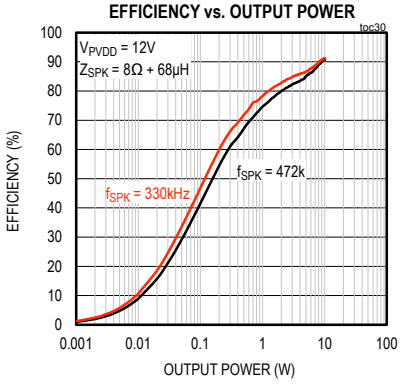


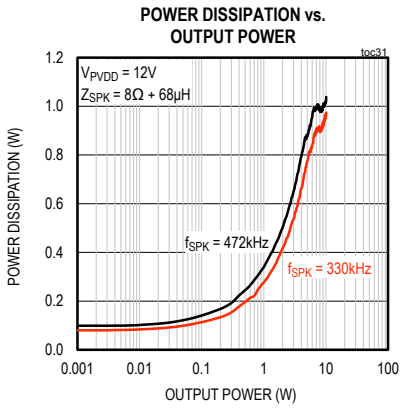








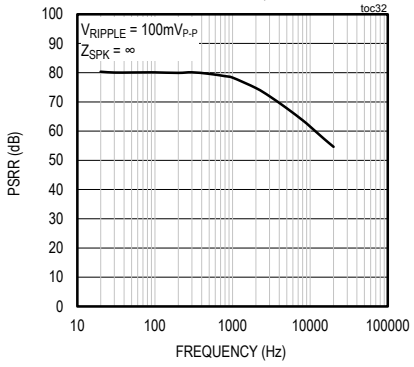




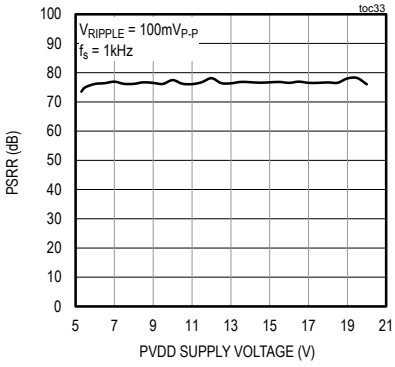
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25˚C.)

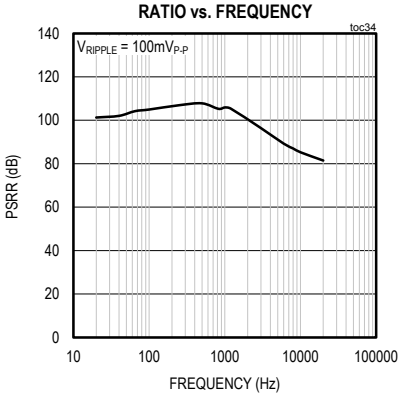
PVDD POWER SUPPLY REJECTION RATIO vs. FREQUENCY



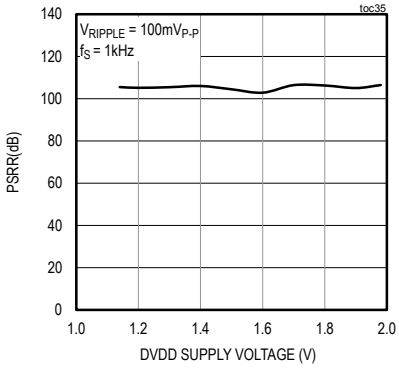
POWER SUPPLY REJECTION RATIO vs. PVDD SUPPLY VOLTAGE



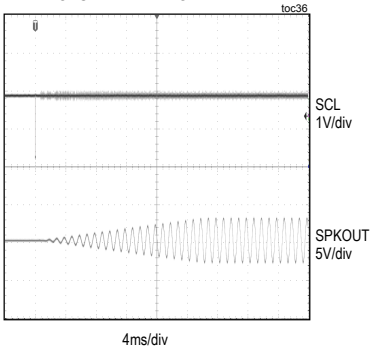
DVDD POWER SUPPLY REJECTION RATIO vs. FREQUENCY



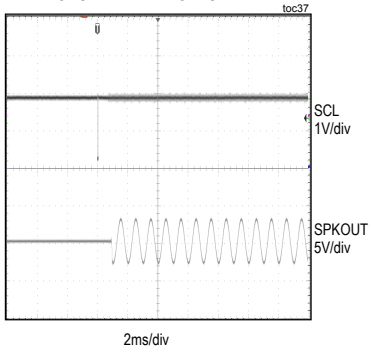
POWER SUPPLY REJECTION RATIO vs. DVDD SUPPLY VOLTAGE



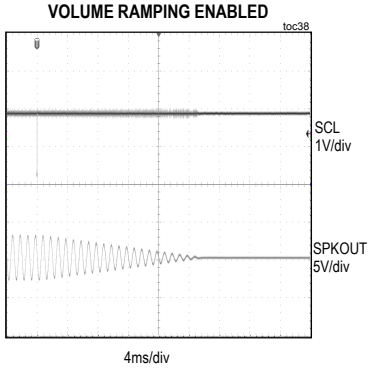
SOFTWARE ENABLE TURN-ON RESPONSE VOLUME RAMPING ENABLED



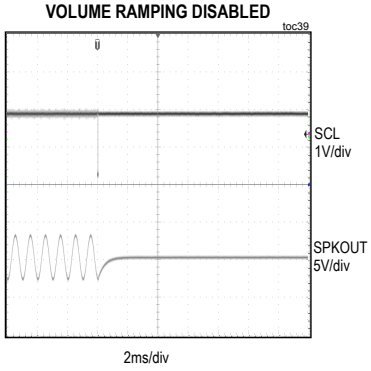
SOFTWARE ENABLE TURN-ON RESPONSE VOLUME RAMPING DISABLED



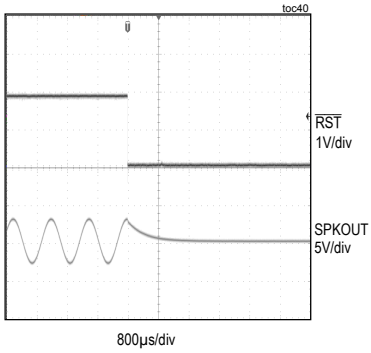
SOFTWARE DISABLE TURN OFF RESPONSE VOLUME RAMPING ENABLED



SOFTWARE DISABLE TURN OFF RESPONSE VOLUME RAMPING DISABLED



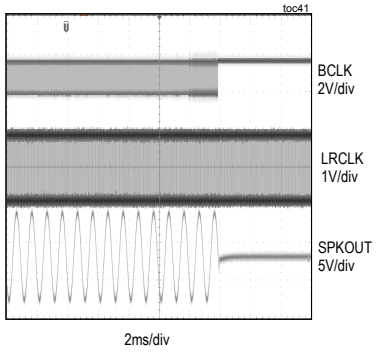
HARDWARE RESET TURN-OFF RESPONSE



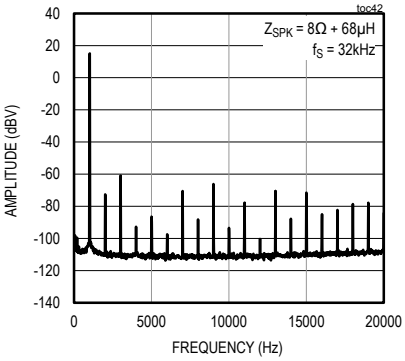
Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

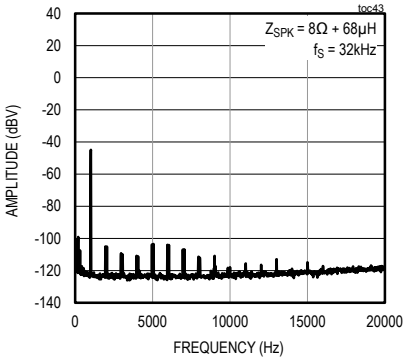
BCLK REMOVAL TURN-OFF RESPONSE



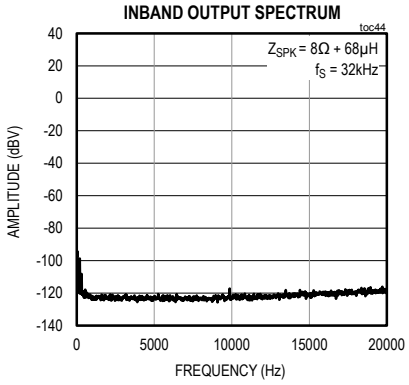
INBAND OUTPUT SPECTRUM



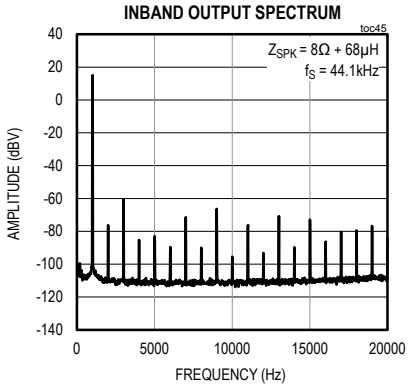
INBAND OUTPUT SPECTRUM



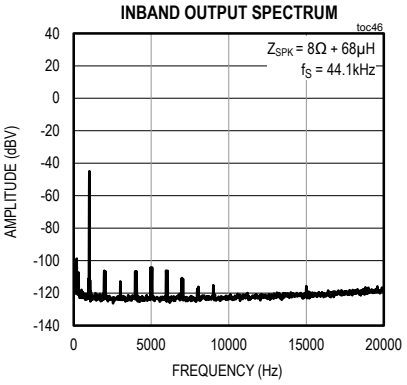
INBAND OUTPUT SPECTRUM



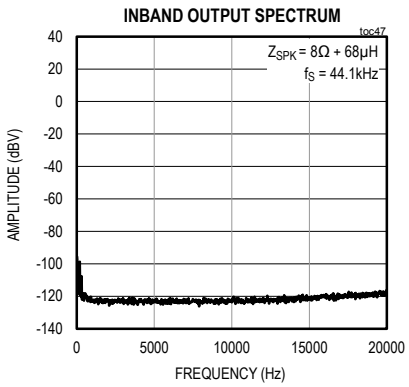
INBAND OUTPUT SPECTRUM



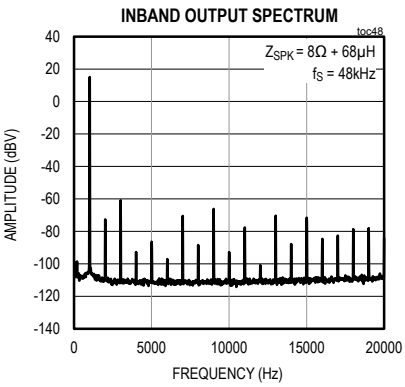
INBAND OUTPUT SPECTRUM



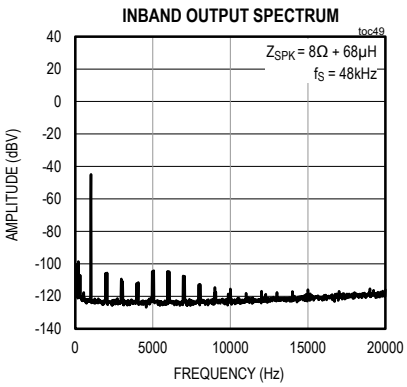
INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM



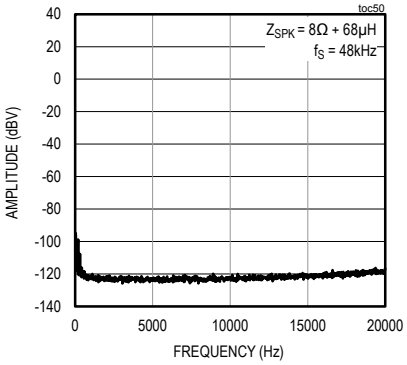
INBAND OUTPUT SPECTRUM



Typical Operating Characteristics (continued)

(V_{PVDD} = 12V, V_{DVDD} = 1.8V, V_{GND} = 0V, SPK_GAIN_MAX = 0x0B (20.5dB), f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25˚C.)

INBAND OUTPUT SPECTRUM



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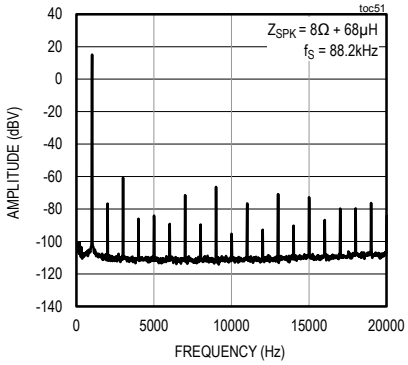
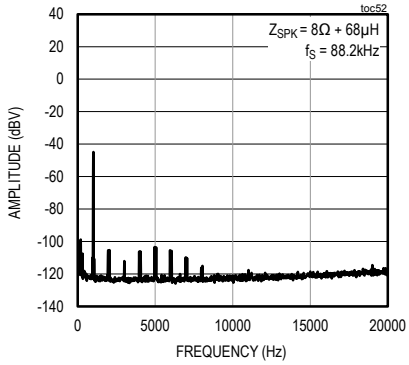
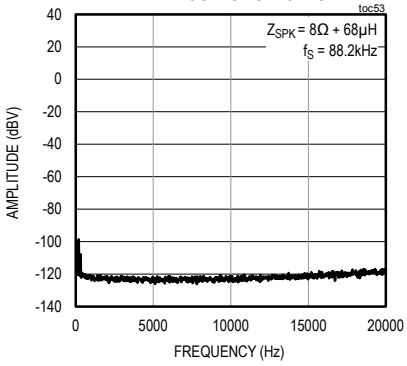


INBAND OUTPUT SPECTRUM



INBAND OUTPUT SPECTRUM



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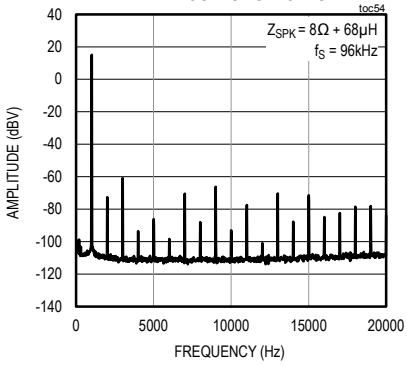

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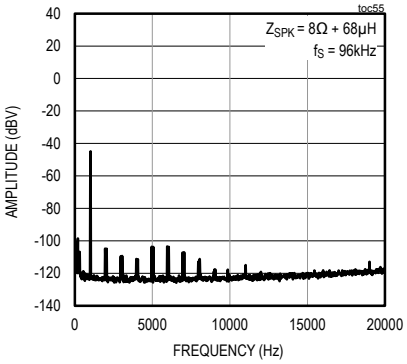
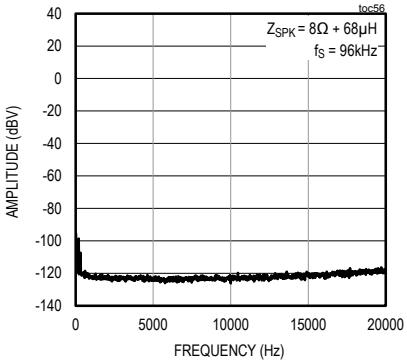
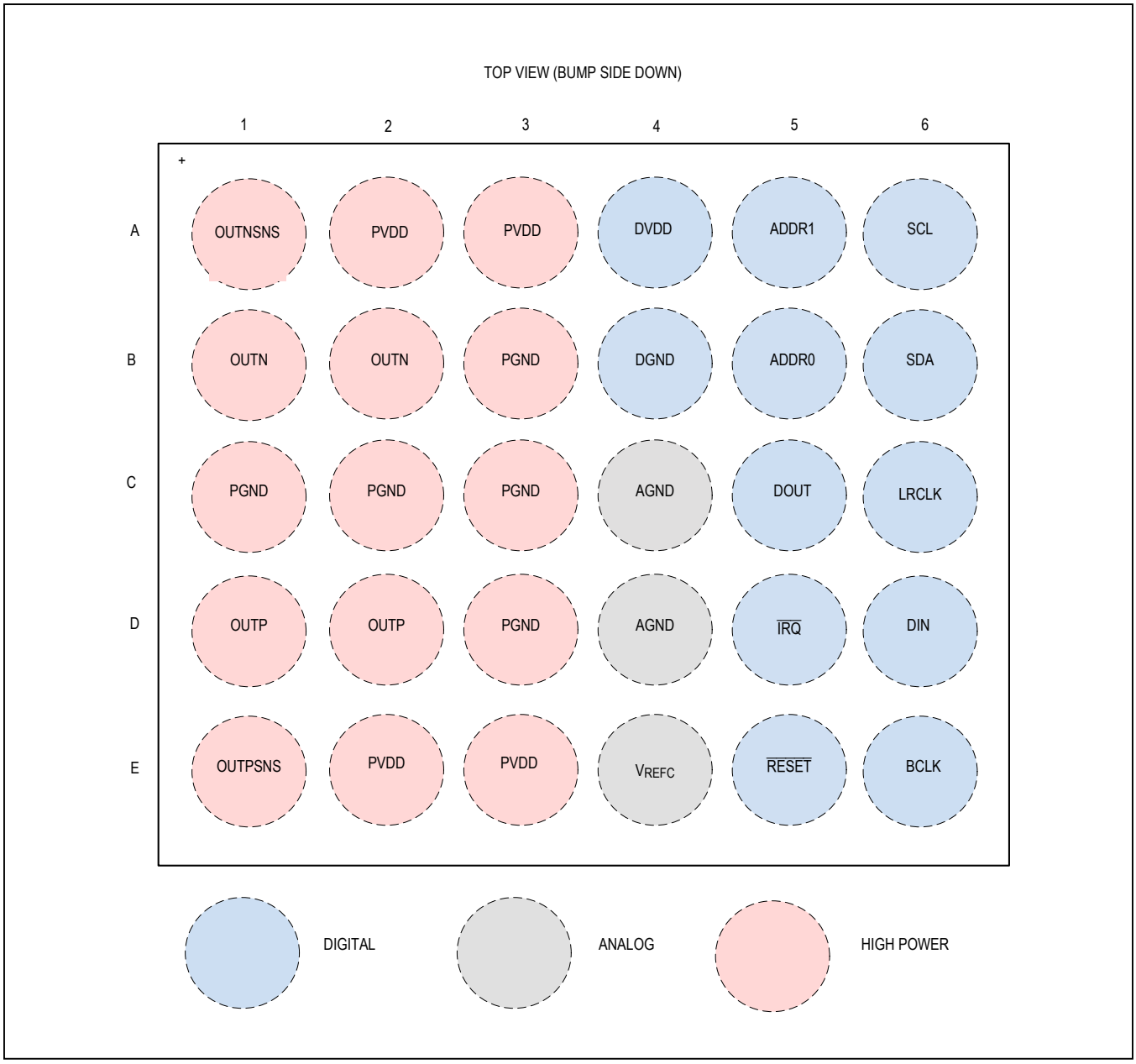


INBAND OUTPUT SPECTRUM



Pin Configuration



Pin Description

BUMP	NAME	SUPPLY RAIL	FUNCTION
A1	OUTNSNS	PVDD	Negative Speaker Amplifier Output Sense. If not used, connect to OUTN.
A2, A3 E2, E3	PVDD	—	Speaker Amplifier Power Supply. Bypass each bump pair to PGND with a 10µF and a 0.1µF, and a single 220µF per device.
A4	DVDD	—	Digital Core, Digital Audio Interface, and I²C Control Power Supply. Bypass to DGND with a 1µF.
A5	ADDR1	DVDD	Four-Level I²C Slave Address Select Input. See the *Slave Address Selection* section for additional information (Table 40).
A6	SCL	DVDD	I²C Control Clock Input
B1, B2	OUTN	PVDD	Negative Speaker Amplifier Output
B3,C1–C3, D3	PGND	—	Speaker Amplifier Ground
B4	DGND	—	Digital Ground
B5	ADDR0	DVDD	Four-Level I²C Slave Address Select Input. See the *Slave Address Selection* section for additional information (Table 40).
B6	SDA	DVDD	I²C Control Data Input/Output
C4, D4	AGND	—	Analog Ground
C5	DOUT	DVDD	Bidirectional ICC Link Data
C6	LRCLK	DVDD	DAI Left/Right Clock Input. LRCLK is the audio sample rate clock and determines whether audio data is routed to the left or right channel. In TDM mode, LRCLK is a frame sync pulse with programmable width.
D1, D2	OUTP	PVDD	Positive Speaker Amplifier Output
D5	$\overline{IRQ}$	DVDD	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to pull low when individual bits in the flag registers change value. Connect a 10kΩ pullup resistor for full output swing.
D6	DIN	DVDD	DAI Audio Data Input
E1	OUTPSNS	PVDD	Positive Speaker Amplifier Output Sense. If not used, connect to OUTP.
E4	V_{REFC}	PVDD	Internal Regulator Decoupling Point. Bypass to AGND with a 1µF.
E5	$\overline{RESET}$	DVDD	Active-Low Hardware Reset. Drive low to place the device into low power reset mode and reset the device registers to their power-on-reset (POR) states.
E6	BCLK	DVDD	DAI Bit Clock Input

Detailed Description

The MAX98371 is a high-efficiency mono Class D audio amplifier that features thermal foldback protection and ADCs for sensing battery supply voltage and onboard temperature.

The MAX98371 can operate over a wide range of supply voltage (PVDD), and has extensive on-board digital signal processing to enable dynamic headroom tracking (DHT). This feature automatically adjusts the output signal to fit into the available supply voltage range. The DHT can be completely bypassed for operation with fixed, regulated supply voltages.

Active emissions limiting edge rate and overshoot control circuitry, together with Class D modulation minimize the electromagnetic interference (EMI) traditionally associated with Class D amplifiers. In systems that use less than 18 inches of speaker cable, an output filter is unnecessary to meet standard EMI limits.

Two ADCs monitor PVDD supply voltage and die temperature. The PVDD supply voltage value can be read using the I²C interface. The temperature ADC can be read back through I²C, however, accurate readings only occur after the die temperature exceeds +100°C.

The DAI supports I²S, left-justified, and TDM formatted data at the following sample rates: 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz. Audio bit depths of 16, 24, and 32 bits are supported for input data. The DAI operates from BCLK to allow the device to function without MCLK.

Thermal foldback allows the device to smoothly attenuate the audio output in an effort to prevent destructive thermal behavior. Above a set threshold, the gain of the replay path reduces at a (user programmable) dB/°C rate to a 12dB maximum attenuation. Thermal monitoring capabilities alert the host when die temperature has triggered the thermal foldback circuit, or is approaching the maximum operating temperature. If maximum die temperature is exceeded, the device shuts down to protect itself. Short-circuit protection ensures that accidental shorts or high-current events do not cause damage to the IC.

Device status is communicated to the host through a hardware interrupt ($\overline{IRQ}$) and status registers accessible through the I²C interface.

The MAX98371 is fully programmable through the I²C interface. ADDR0, ADDR1 connections select one of sixteen I²C slave addresses. Shutdown mode is directly controlled through the I²C interface, or a hardware shutdown can be asserted through the $\overline{RESET}$ pin.

Table 1. MAX98371 Control Register Map

REGISTER DESCRIPTION			REGISTER CONTENTS								POR STATE
ADDR	NAME	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT2	BIT1	BIT 0	
INTERRUPTS											
0x01	INTERRUPT STATUS 0	R	—	—	THRMFB_ STATUS	—	THRM WRN_ STATUS	—	THRM SHDN_ STATUS	—	0x00
0x02	INTERRUPT STATUS 1	R	—	ICCOVC_ STATUS	LMTRACT_ STATUS	INVAL SLOT_ STATUS	DHTACT_ STATUS	SPK CURNT_ STATUS	PVDD OVFL_ STATUS	PVDD UVLO_ STATUS	0x00
0x03	INTERRUPT STATE 0	R	—	—	THRMFB_ END_ STATE	THRMFB_ BGN_ STATE	THRM WRN_END _STATE	THRM WRN_BGN _STATE	THRM SHDN_END _STATE	THRM SHDN_BGN _STATE	0x00
0x04	INTERRUPT STATE 1	R	—	ICCOVC_ STATE	LMTRACT_ STATE	INVAL SLOT_ STATE	DHTACT_ STATE	SPK CURNT_ STATE	PVDD OVFL_ STATE	PVDD UVLO_ STATE	0x00
0x05	INTERRUPT FLAG 0	R/W	—	—	THRMFB_ END_ FLAG	THRMFB_ BGN_ FLAG	THRM WRN_END_ FLAG	THRM WRN_BGN _FLAG	THRM SHDN_ END_ FLAG	THRM SHDN_ BGN_ FLAG	0x00