Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-4573; Rev 2; 6/10

MAXIM

Ultra-Low Power Stereo Audio Codec

General Description

The MAX9867 is an ultra-low power stereo audio codec designed for portable consumer devices such as mobile phones and portable gaming consoles.

The device features stereo differential microphone inputs that can be connected to either analog or digital microphones. The single-ended line inputs, with configurable preamplifier, can be sent to the ADC for record or routed directly to the headphone amplifier for playback. An auxiliary ADC path can be used to track any DC voltage.

The stereo headphone amplifiers support differential, single-ended, and capacitorless output configurations. Using the capacitorless output configuration, the device can output 10mW into 32Ω headphones. Comprehensive click-and-pop circuitry suppresses audible clicks and pops during volume changes and startup or shutdown.

Utilizing Maxim's proprietary digital circuitry, the device can accept any available 10MHz to 60MHz system clock. This architecture eliminates the need for an external PLL and multiple crystal oscillators. The stereo ADC and DAC paths provide user-configurable voiceband or audioband digital filters. Voiceband filters provide extra attenuation at the GSM packet frequency and greater than 70dB stopband attenuation at $f_S/2$.

The MAX9867 operates from a single 1.8V supply, and supports a 1.65V to 3.6V logic level. An I^2C 2-wire serial interface provides control for volume levels, signal mixing, and general operating modes.

The MAX9867 is available in a tiny 2.2mm x 2.7mm, 0.4mm-ball-pitch, WLP package. A 32-pin 5mm x 5mm TQFN package is also available.

Features

- **1.8V Single-Supply Operation**
- **6.7mW Playback Power Consumption**
- **90dB Stereo DAC, 8kHz ≤ f_S ≤ 48kHz**
- **85dB Stereo ADC, 8kHz ≤ f_S ≤ 48kHz**
- **Battery-Measurement Auxiliary ADC**
- **Support for Any Master Clock Between 10MHz to 60MHz**
- **Stereo Digital Microphone Input Support**
- **Stereo Analog Differential Microphone Inputs**
- **Stereo Headphone Amplifiers: Differential, Single-Ended, or Capacitorless**
- **Stereo Line Inputs**
- **Voiceband Filter with a Stopband Attenuation Greater than 70dB**
- **1.65V to 3.6V Digital Interface Supply Voltage**
- **I^2S/TDM-Compatible Digital Audio Bus**
- **30-Bump, 2.2mm x 2.7mm 0.4mm-Pitch WLP**

Applications

Cell Phones
Portable Gaming Devices
Portable Navigation Devices
Portable Multimedia Players
Wireless Headsets

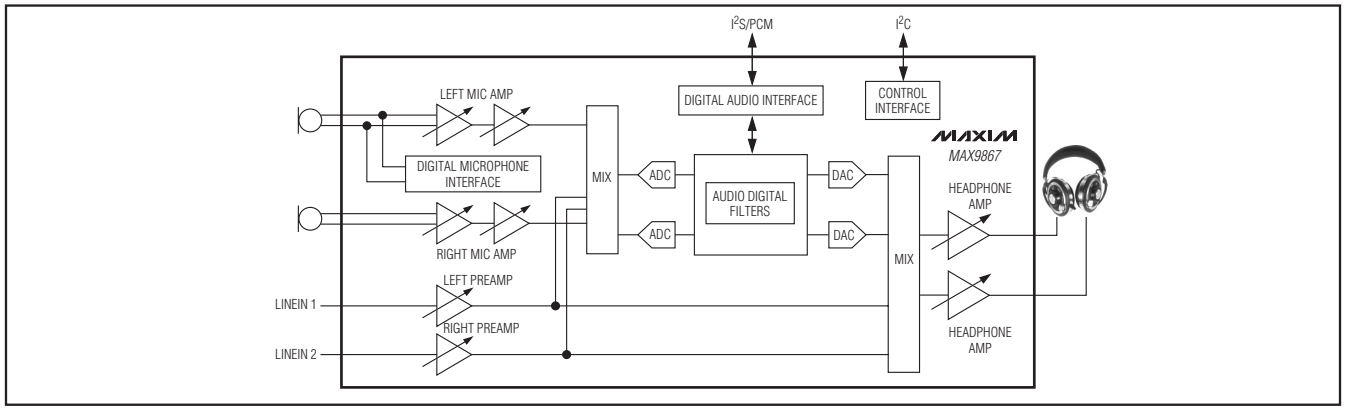
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9867EWV+	-40°C to +85°C	30 WLP
MAX9867ETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Simplified Block Diagram



Ultra-Low Power Stereo Audio Codec

ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND.)
DVDD, AVDD, and PVDD .....-0.3V to +2V
DVDDIO .....-0.3V to +3.6V
DGND and PGND .....-0.1V to +0.1V
PREG, REF, REG, MICBIAS .....-0.3V to (AVDD + 0.3V)
MCLK, LRCLK, BCLK
SDOUT, SDIN .....-0.3V to (DVDDIO + 0.3V)
SDA, SCL, IRQ .....-0.3V to +3.6V
LOUTP, LOUTN, ROUTP,
ROUTN .....(PGND - 0.3V) to (PVDD + 0.3V)
LINL, LINR, JACKSNS/AUX, MICLP/DIGMICDATA,
MICLN/DIGMICCLK, MICRP, MICRN ..-0.3V to (AVDD + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
30-Bump WLP (derate 12.5mW/°C above +70°C) 1000mW
32-Pin TQFN-EP (derate 34.5mW/°C above +70°C) .2759mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
30-Bump WLP .....80°C/W
32-Pin TQFN-EP .....29°C/W
Operating Temp Range .....-40°C to +85°C
Storage Temp Range .....-65°C to +150°C
Lead Temperature (TQFN only, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range		PVDD, DVDD, AVDD		1.65	1.8	1.95	V
		DVDDIO		1.65	1.8	3.6	
Total Supply Current	I_{VDD}	Full-duplex 8kHz mono (voice mode) (Note 3)	Analog (AVDD + PVDD)		4.65	7	mA
			Digital (DVDD + DVDDIO)		0.96	1.5	
		DAC playback 48kHz stereo (audio mode) (Note 3)	Analog (AVDD + PVDD)		3.28	5	
			Digital (DVDD + DVDDIO)		1.40	2	
		Full-duplex 48kHz stereo (audio mode) (Note 3)	Analog (AVDD + PVDD)		8.0	12	
			Digital (DVDD + DVDDIO)		2.0	3	
		Stereo line-in only	Analog (AVDD + PVDD)		3.8	6	
			Digital (DVDD + DVDDIO)		0.004	0.05	
Shutdown Supply Current		T_A = +25°C	Analog (AVDD + PVDD)		1	5	µA
			Digital (DVDD + DVDDIO)		1	5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown to Full Operation		Excludes PLL lock time			10		ms
Soft-Start/-Stop Time					10		ms
DAC (Note 4)							
Dynamic Range (Note 5)	DR	f_S = 48kHz, AV_{VOL} = 0dB, T_A = +25°C	Master or slave mode		90		dB
			Slave mode	84			
Full-Scale Output		V_{OLL}/V_{OLR} = 0x09	Differential mode		1		V_{RMS}
			Capacitorless and single-ended modes		0.56		
Gain Error		DC accuracy, measured with respect to full-scale output			1	5	%
Voice Path Phase Delay	P_{DLY}	f = 1kHz, 0dBFS, HP filter disabled, digital input to analog output	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.59		
Total Harmonic Distortion	THD	MCLK = 12.288MHz, f_S = 48kHz, 0dBFS, measured at headphone outputs			-80		dB
DAC Attenuation Range	AV_{DAC}	DACA = 0xF to 0x0		-15		0	dB
DAC Gain Adjust	AV_{GAIN}	DACG = 00 to 11		0		+18	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	78		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			75		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			62		
DAC VOICE MODE DIGITAL IIR LOWPASS FILTER							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.448 x f_S		Hz
		-3dB cutoff			0.451 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.476 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz		75			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC VOICE MODE DIGITAL 5th ORDER IIR HIGHPASS FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{DHPPB}	DVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		DVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
5th Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable)	f_{DHPSB}	DVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		DVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000		90		dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.47 x f_S		
		-6.02dB cutoff		0.50 x f_S		
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.58 x f_S		Hz
Stopband Attenuation			60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC STEREO AUDIO MODE DIGITAL DC BLOCKING HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1		0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	DVFLT = 0x1		90		dB
ADC (Note 6)						
Dynamic Range (Note 5)	DR	f_S = 8kHz, MODE = 0 (IIR voice)	75	84		dB
		f_S = 8kHz to 48kHz, MODE = 1 (FIR audio)		85		
Full-Scale Input		Differential MIC input or stereo-line inputs, AV_{PRE} = 0dB, AV_{PGAM} = 0dB		1		V_{P-P}
Gain Error (Note 7)		DC accuracy, measured with respect to 80% of full-scale output		1	5	%
Voice Path Phase Delay	P_{DLY}	f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output; f_S = 8kHz		1.2		ms
		f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output; f_S = 16kHz		0.61		
Total Harmonic Distortion	THD	f = 1kHz, f_S = 8kHz, T_A = +25°C, 0dBFS		-81	-70	dB
ADC Level Adjust Range	AV_{ADC}	AVL/AVR = 0xF to 0x0	-12		+3	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	85		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		85		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
ADC VOICE MODE DIGITAL IIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.445 x f_S		Hz
		-3dB cutoff		0.449 x f_S		
Passband Ripple		f < f_{PLP}		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.469 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz	74			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC VOICE MODE DIGITAL 5th ORDER IIR HIGHPASS FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{AHPPB}	AVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		AVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		AVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
ADC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.48 x f_S		
		-6.02dB cutoff		0.5 x f_S		
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.58 x f_S		Hz
Stopband Attenuation		$f > f_{SLP}$, f = 20Hz to 20kHz	60			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC STEREO AUDIO MODE DIGITAL DC BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	AVFLT = 0x1			90		dB
OUTPUT VOLUME CONTROL							
Line Input to Output Volume Control	AV_{VOL}	VOLL/VOLR = 0x00		14.55	14.9	15.15	dB
		VOLL/VOLR = 0x01		14.1	14.4	14.6	
		VOLL/VOLR = 0x02		13.6	13.9	14.1	
		VOLL/VOLR = 0x04		12.6	12.9	13.1	
		VOLL/VOLR = 0x08		9.35	9.9	10.35	
		VOLL/VOLR = 0x10		0.35	0.9	1.35	
		VOLL/VOLR = 0x20		-50.15	-49.2	-48.15	
Output Volume Control Step Size		VOLL/VOLR = 0x00 to 0x06 (+6dB to +3dB)			0.5		dB
		VOLL/VOLR = 0x06 to 0x0F (+3dB to -6dB)			1		
		VOLL/VOLR = 0x0F to 0x17 (-6dB to -22dB)			2		
		VOLL/VOLR = 0x17 to 0x3F (-22dB to mute)			4		
Output Volume Control Mute Attenuation		f = 1kHz			100		dB
HEADPHONE AMPLIFIER (Note 8)							
Output Power per Channel (Differential Mode)	P_{OUT}	f = 1kHz, THD < 1%, T_A = +25°C	R_L = 16Ω	30	52		mW
			R_L = 32Ω		32		
Output Power per Channel (Capacitorless Mode)	P_{OUT}	f = 1kHz, THD < 1%, T_A = +25°C	R_L = 16Ω		19		mW
			R_L = 32Ω	8	10		
Total Harmonic Distortion + Noise (Differential Mode)	THD+N	R_L = 16Ω, P_{OUT} = 25mW, f = 1kHz			-76		dB
		R_L = 32Ω, P_{OUT} = 25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-77	-70	
			MCLK = 12.288MHz, f_S = 48kHz		-80		
Total Harmonic Distortion + Noise (Capacitorless Mode)	THD+N	R_L = 16Ω, P_{OUT} = 6.25mW, f = 1kHz			-72		dB
		R_L = 32Ω, P_{OUT} = 6.25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-74	-65	
			MCLK = 12.288MHz, f_S = 48kHz		-74		
Total Harmonic Distortion + Noise (SE Mode)	THD+N	R_L = 16Ω, P_{OUT} = 6.25mW, f = 1kHz			-74		dB
		R_L = 32Ω, P_{OUT} = 6.25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-74	-65	
			MCLK = 12.288MHz, f_S = 48kHz		-76		
Dynamic Range	DR	AV_{VOL} = +6dB (Notes 5, 7)		76	90		dB

Ultra-Low Power Stereo Audio Codec

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 7)	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	78		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			75		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			62		
Output Offset Voltage	V_{OS}	AV_{VOL} = -84dB differential mode	(LOUTP–LOUTN, ROUTP–ROUTN), T_A = +25°C		±0.2		mV
		AV_{VOL} = -84dB capacitorless mode	(LOUTP–LOUTN, ROUTP–LOUTN), T_A = +25°C		±0.8		
Crosstalk	X_{TALK}	Differential mode, P_{OUT} = 5mW, f = 1kHz			87		dB
		Capacitorless mode, P_{OUT} = 5mW, f = 1kHz	TQFN		55		
			WLP		60		
Capacitive Drive		No sustained oscillations	R_L = 32Ω		500		pF
			R_L = ∞		100		
Click-and-Pop Level (Differential, Capacitorless Modes)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-80		dBV
			Out of shutdown		-69		
Click-and-Pop Level (SE Mode)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-75		dBV
			Out of shutdown		-75		
MICROPHONE AMPLIFIER							
Preamplifier Gain	AV_{PRE}	PALEN/PAREN = 01		-0.5	0	+0.5	dB
		PALEN/PAREN = 10		19.5	20	20.5	
		PALEN/PAREN = 11		29.5	30	30.5	
MIC PGA Gain	AV_{PGAM}	PGAML/PGAMR = 0x1F		-0.6	-0.1	+0.4	dB
		PGAML/PGAMR = 0x00		19.3	19.75	20.3	
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P}, f = 217Hz			50		dB
MIC Input Resistance	R_{IN_MIC}	All gain settings		30	50		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion + Noise	THD+N	AV_{PRE} = 0dB, V_{IN} = $1V_{P-P}$, f = 1kHz		-80		dB
		AV_{PRE} = +30dB, V_{IN} = $32mV_{P-P}$, f = 1kHz, ($1V_{P-P}$ at ADC input)		-67		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	85		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		85		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
MICROPHONE BIAS						
Output Voltage	$V_{MICBIAS}$	V_{AVDD} = 1.8V, I_{LOAD} = 1mA	1.5	1.525	1.55	V
Load Regulation		I_{LOAD} = 1mA to 2mA		0.2	10	V/A
Line Regulation		V_{AVDD} = 1.65V to 1.95V		10		µV/V
Power-Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$		85		dB
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$		81		
Noise Voltage		A-weighted		9.1		$µV_{RMS}$
LINE INPUT						
Full-Scale Input	V_{IN}	AV_{LINE} = 0dB		1.0		V_{P-P}
Line Input Level Adjust Range	AV_{LINE}	LIGL/LIGR = 0xF to 0x0	-6.5		+24.5	dB
Line Input Mute Attenuation		f = 1kHz		100		dB
Input Resistance	R_{IN_LINE}	AV_{LINE} = +24dB	20			kΩ
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $0.1V_{P-P}$, f = 1kHz, differential output		-83		dB
AUXIN INPUT						
Input DC Voltage Range		AUXEN = 1	0		0.738	V
AUXIN Input Resistance	R_{IN}	AUXEN = 1, 0V ≤ AUXIN ≤ 0.738V	10	40		MΩ
JACK SENSE OPERATION						
Threshold	V_{TH}	JDETEN = 1, $\overline{SHDN}$ = 1, JACKSNS	0.92 x MICBIAS	0.95 x MICBIAS	0.98 x MICBIAS	V
		JDETEN = 1, $\overline{SHDN}$ = 0, JACKSNS, LOUTP	AVDD - 0.8	AVDD - 0.4	AVDD - 0.15	
Pullup Current	I_{PU}	JDETEN = 1, $\overline{SHDN}$ = 1, JACKSNS = GND		4		µA
		JDETEN = 1, $\overline{SHDN}$ = 0, JACKSNS = LOUTP = GND		4	20	
Pullup Voltage		JDETEN = 1, JACKSNS, LOUTP		AVDD		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL SIDETONE							
Sidetone Gain Adjust Range	AV_{STGA}	Differential output mode, DVST = 0x1F to 0x01		-60		0	dB
Voice Path Phase Delay	P_{DLY}	MIC input to headphone output, f = 1kHz, HP filter disabled, f_S = 8kHz			2.2		ms
INPUT CLOCK CHARACTERISTICS							
MCLK Input Frequency	f_{MCLK}	For any LRCLK sample rate		10		60	MHz
MCLK Input Duty Cycle		Prescaler = /1 mode		40		60	%
		/2 or /4 modes		30		70	
Maximum MCLK Input Jitter		Maximum allowable RMS for performance limits			100		ps_{RMS}
LRCLK Sample Rate Range				8		48	kHz
LRCLK PLL Lock Time		Any allowable LRCLK and PCLK rate, slave mode	Rapid lock mode		2	7	ms
			Nonrapid lock mode		12	25	
LRCLK Acceptable Jitter for Maintaining PLL Lock		Allowable LRCLK period change from nominal for slave PLL mode at any allowable LRCLK and PCLK rates				±100	ns
LRCLK Average Frequency Error (Master and Slave Modes) (Note 9)		FREQ = 0x8 through 0xF		0		0	%
		PCLK = 192xf_S, 256xf_S, 384xf_S, 512xf_S, 768xf_S, and 1024xf_S		0		0	
		All other modes		-0.025		+0.025	
DIGITAL INPUT (MCLK)							
Input High Voltage	V_{IH}			1.2			V
Input Low Voltage	V_{IL}					0.6	V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C				±1	µA
Input Capacitance					10		pF
DIGITAL INPUTS (SDIN, BCLK, LRCLK)							
Input High Voltage	V_{IH}			0.7 x DVDDIO			V
Input Low Voltage	V_{IL}					0.3 x DVDDIO	V
Input Hysteresis					200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C				±1	µA
Input Capacitance					10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C			±1	µA
Input Capacitance				10		pF
DIGITAL INPUT (DIGMICDATA)						
Input High Voltage	V_{IH}		0.65 x DVDD			V
Input Low Voltage	V_{IL}				0.35 x DVDD	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C			±35	µA
Input Capacitance				10		pF
CMOS DIGITAL OUTPUTS (BCLK, LRCLK, SDOUT)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	DVDDIO - 0.4			V
CMOS DIGITAL OUTPUT (DIGMICCLK)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	DVDD - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Current	I_{OH}	V_{OUT} = V_{DVDD}, T_A = +25°C			1	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.2 x DVDD	V
DIGITAL MICROPHONE TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
DIGMICCLK Divide Ratio	f_{MICCLK}	MICCLK = 00		PCLK/8		MHz
		MICCLK = 01		PCLK/6		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU, MIC}$	Either clock edge	20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD, MIC}$	Either clock edge	0			ns
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Minimum BCLK Cycle Time	t_{BCLKS}	Slave operation		75		ns
	t_{BCLKM}	Master operation		325		ns

Ultra-Low Power Stereo Audio Codec

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

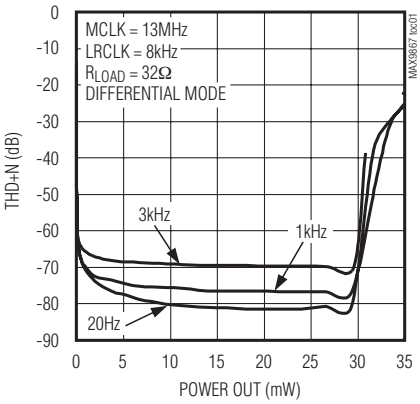
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum BCLK High Time	t_{BCLKH}	Slave operation		30		ns
Minimum BCLK Low Time	t_{BCLKL}	Slave operation		30		ns
BCLK or LRCLK Rise and Fall	t_R, t_F	Master operation, C_L = 15pF		7		ns
SDIN or LRCLK to BCLK Setup Time	t_{SU}		20			ns
SDIN or LRCLK to BCLK Hold Time	t_{HD}		0			ns
SDOUT Delay Time from BCLK Rising Edge	t_{DLY}	C_L = 30pF	0		40	ns
I^2C TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD, STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	$R_{PU, SDA}$ = 475Ω	0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	$R_{PU, SDA}$ = 475Ω (Note 10)	20 + 0.1C_B		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 2: The MAX9867 is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Clocking all zeros into the DAC, master mode, and differential headphone mode.
Note 4: DAC performance measured at the headphone outputs.
Note 5: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f = 20Hz to 20kHz.
Note 6: Performance measured using microphone inputs, unless otherwise stated.
Note 7: Performance measured using line inputs.
Note 8: Performance measured using DAC, unless otherwise stated. LRCLK = 8kHz, unless otherwise stated.
Note 9: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 10: C_B is in pF.

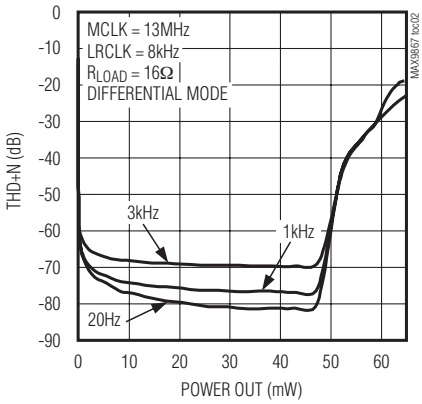
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

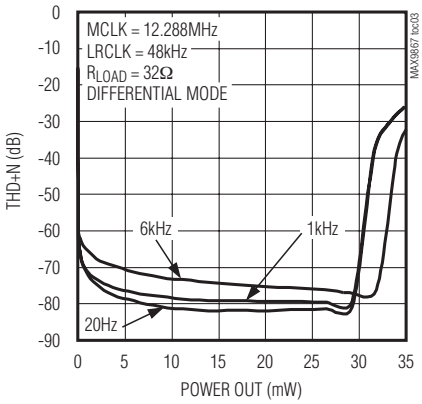
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



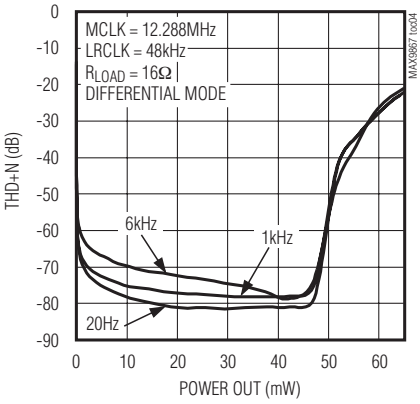
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



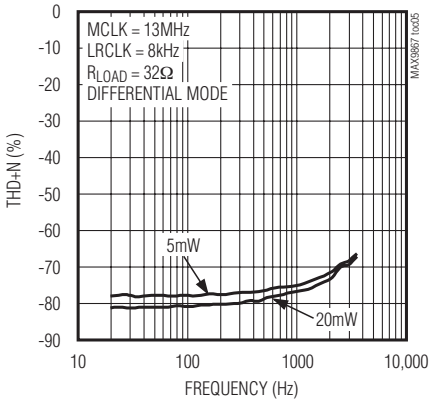
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



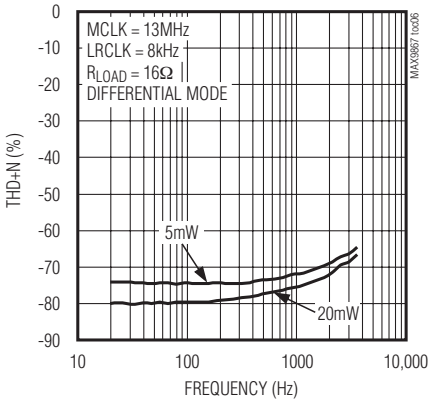
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



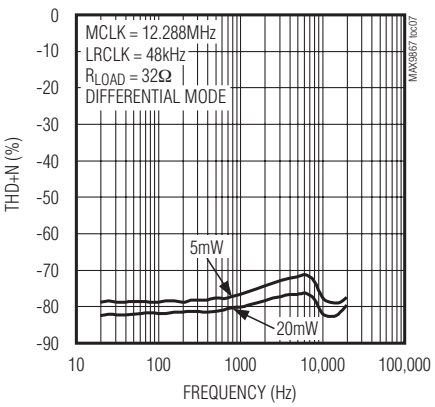
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



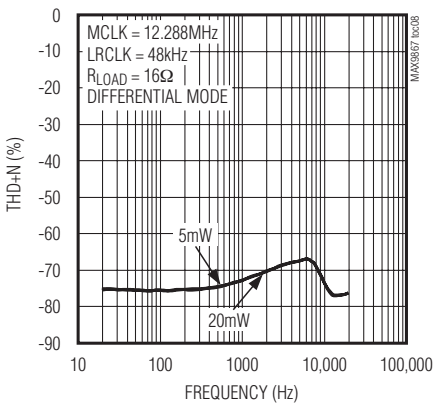
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



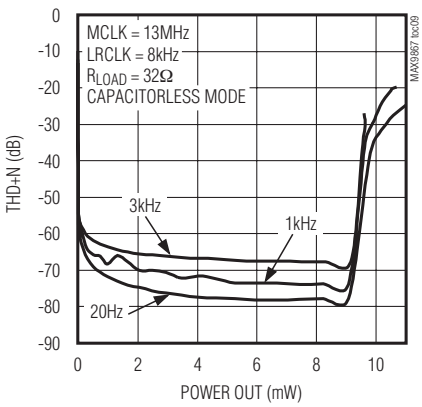
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)

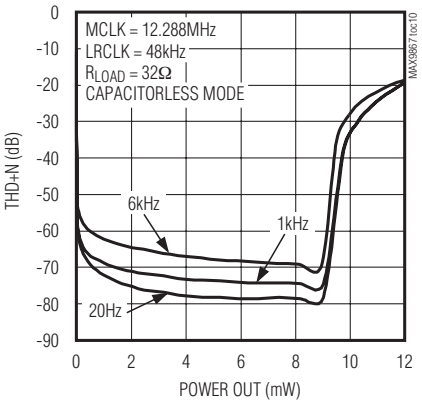


Ultra-Low Power Stereo Audio Codec

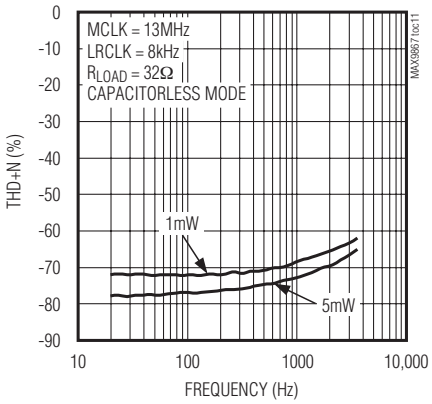
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

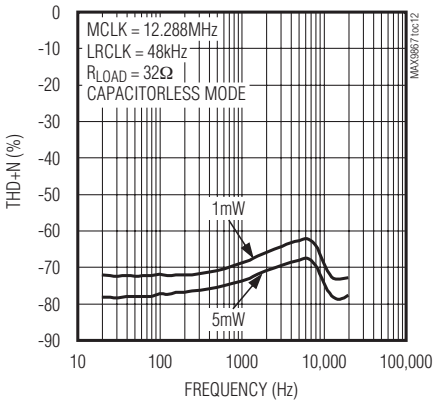
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



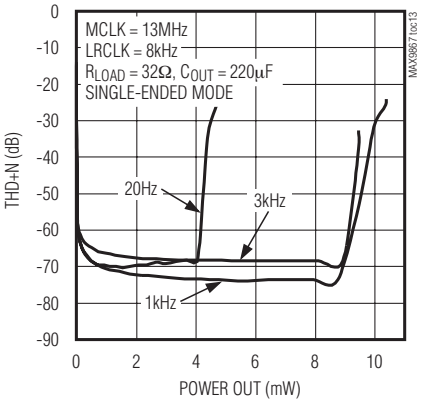
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



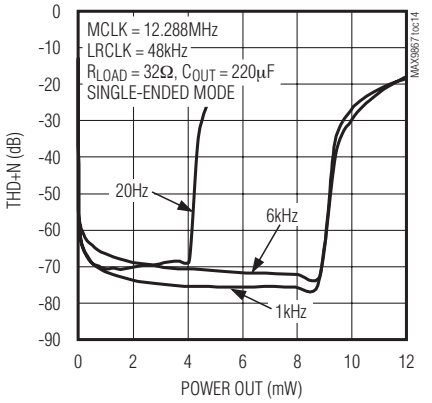
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



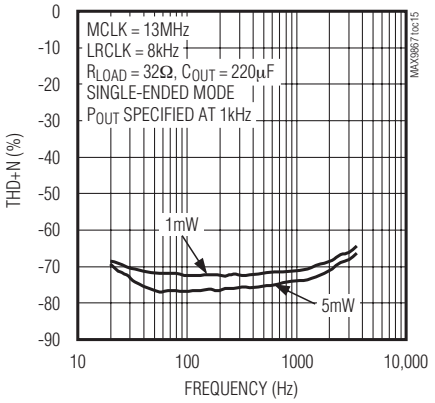
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



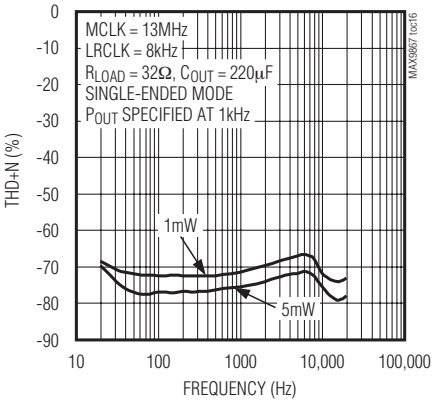
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



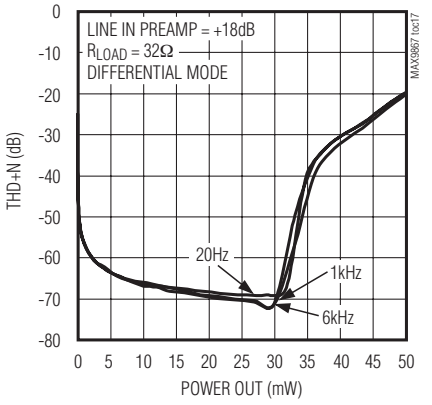
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



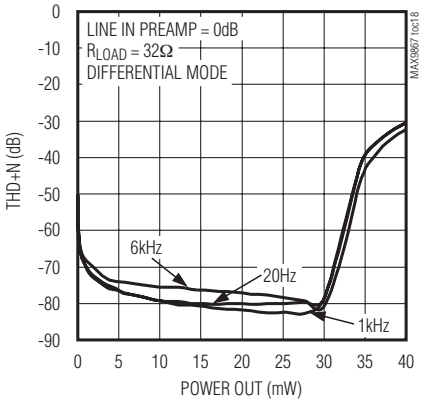
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE IN TO HEADPHONE)



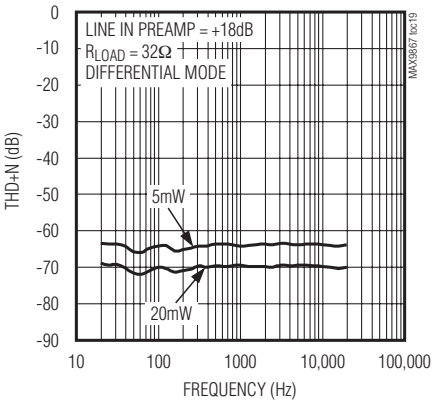
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE IN TO HEADPHONE)



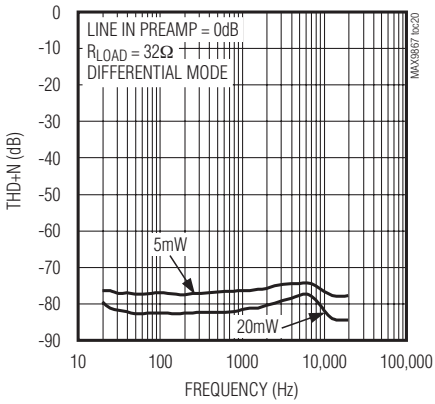
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

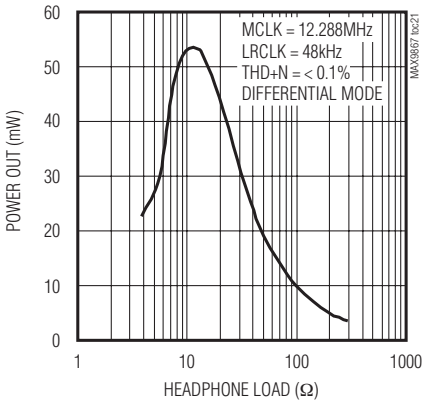
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE IN TO HEADPHONE)



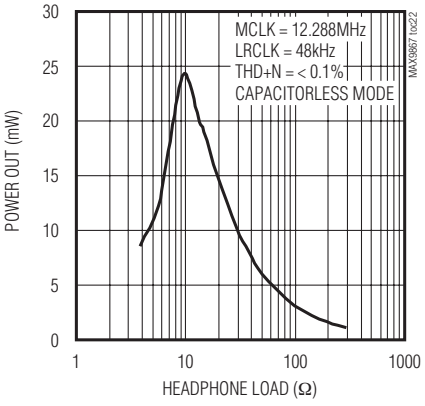
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE IN TO HEADPHONE)



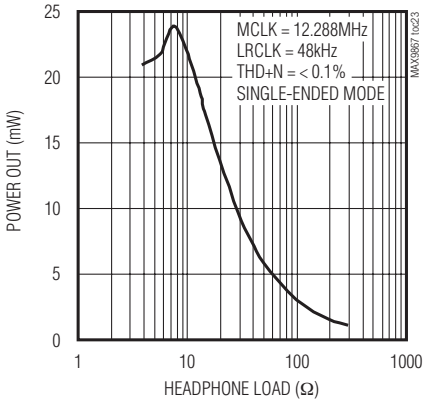
POWER OUT vs. HEADPHONE LOAD



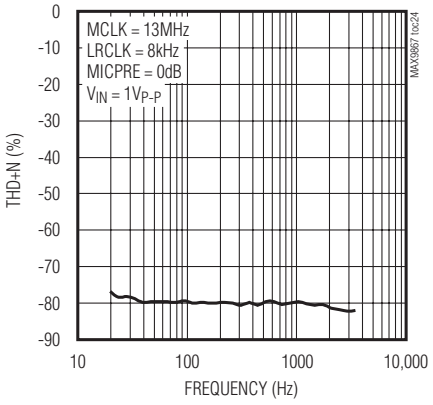
POWER OUT vs. HEADPHONE LOAD



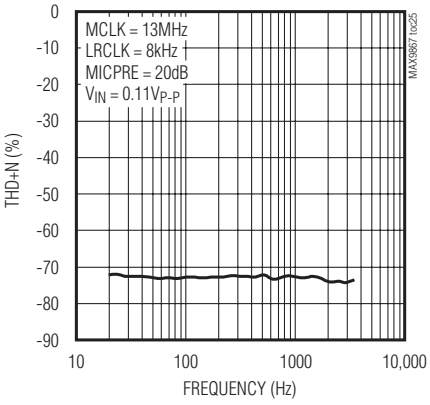
POWER OUT vs. HEADPHONE LOAD



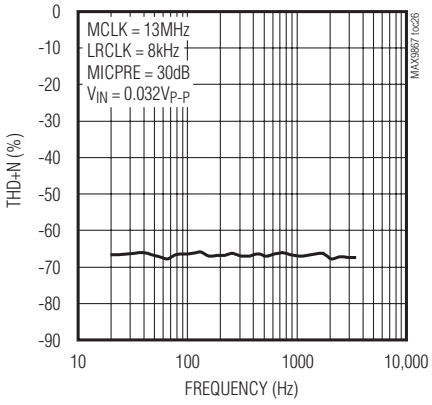
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



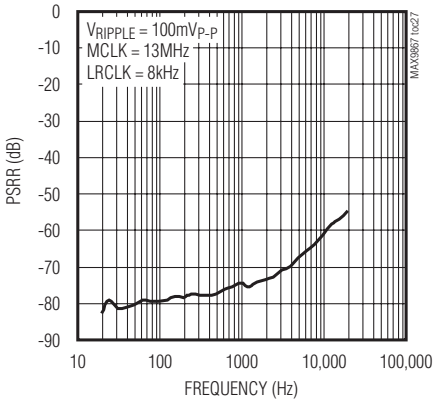
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)

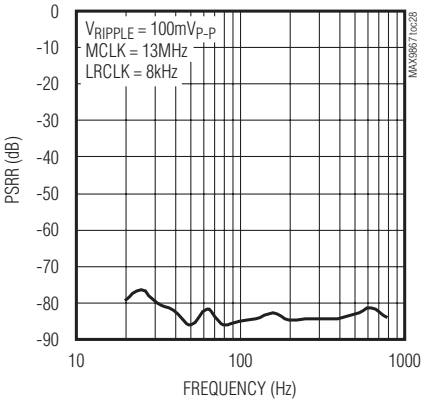


Ultra-Low Power Stereo Audio Codec

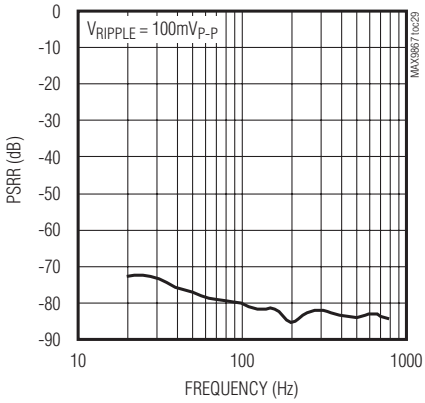
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

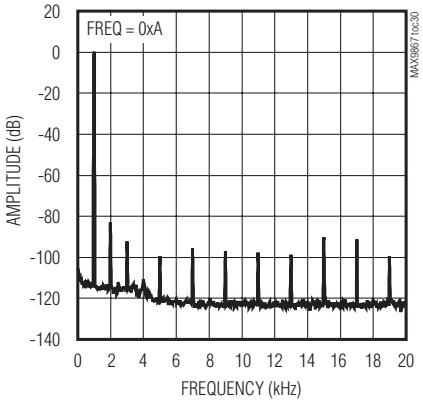
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



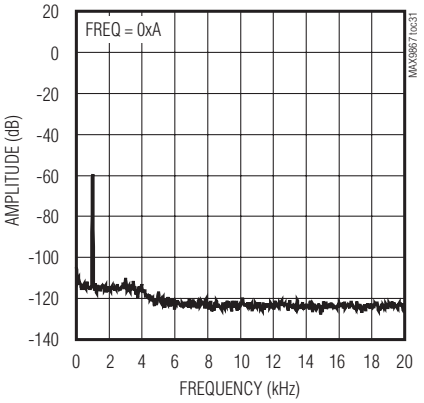
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICBIAS)



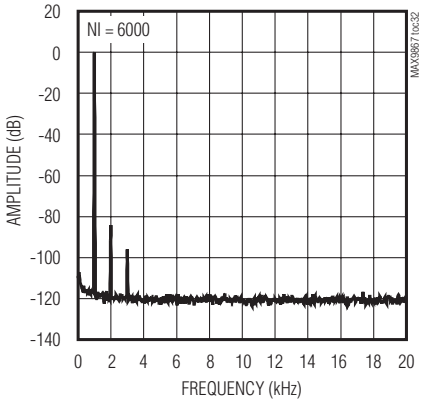
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



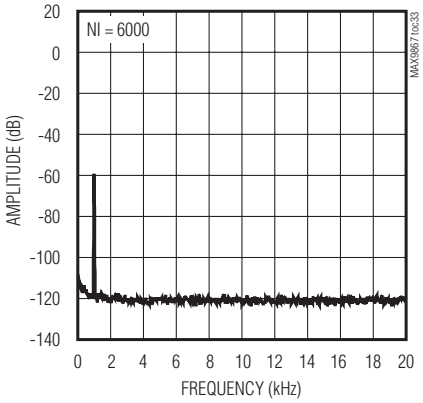
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



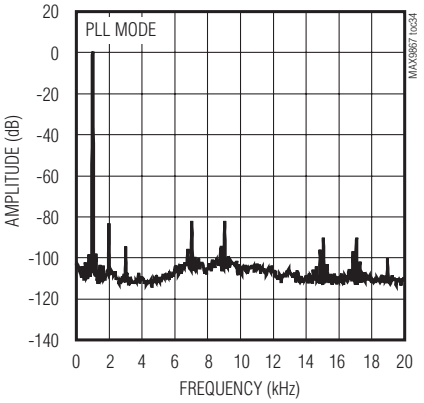
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



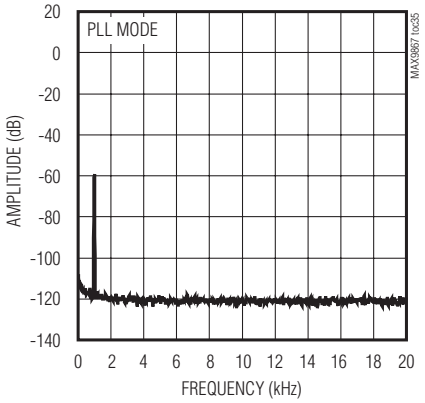
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



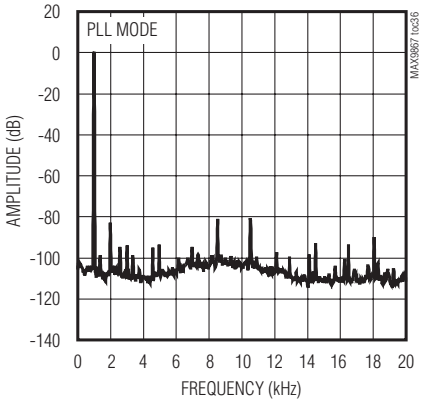
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 48kHz



FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 48kHz



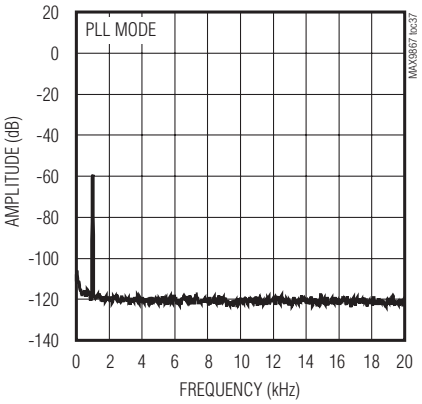
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 44.1kHz



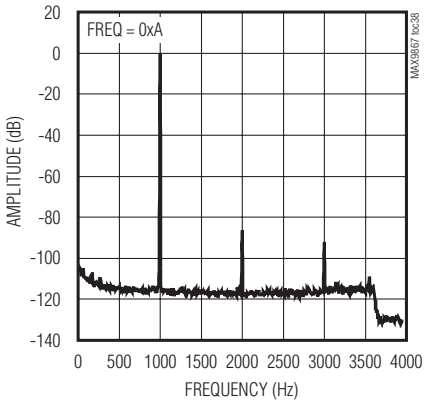
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to $f_S/2$, T_A = +25°C, unless otherwise noted.)

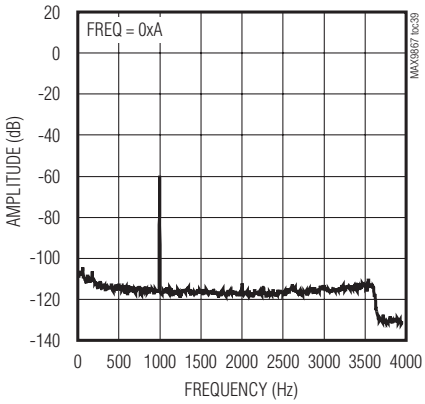
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 44.1kHz



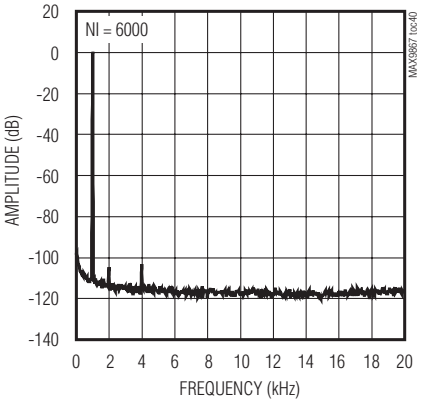
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



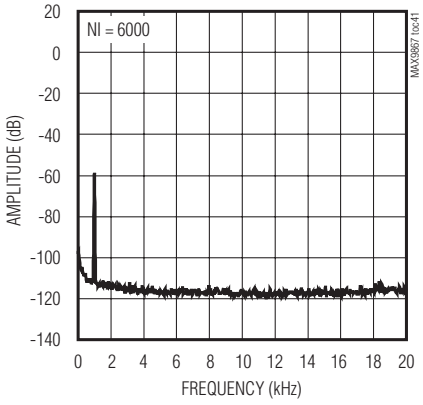
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



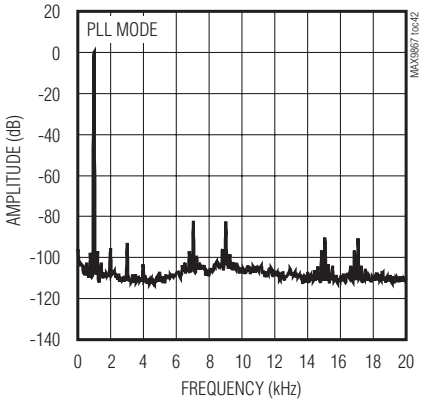
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



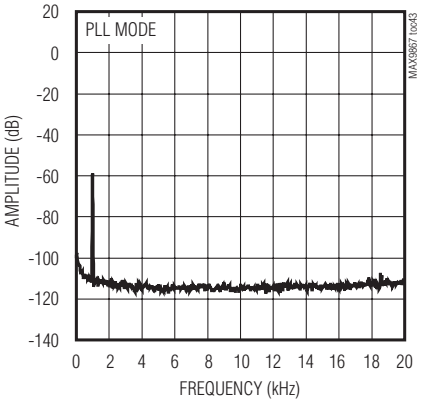
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



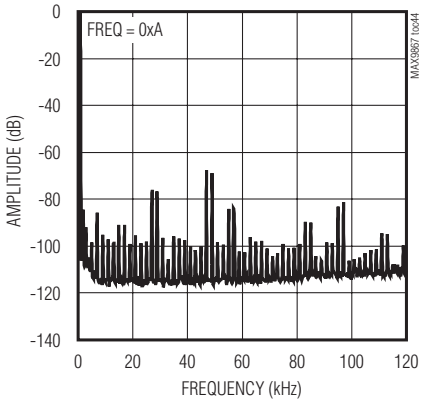
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 13MHz, LRCLK = 48kHz



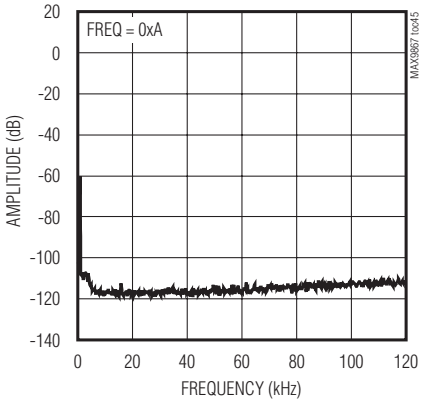
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 13MHz, LRCLK = 48kHz



WIDEBAND FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



WIDEBAND FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz

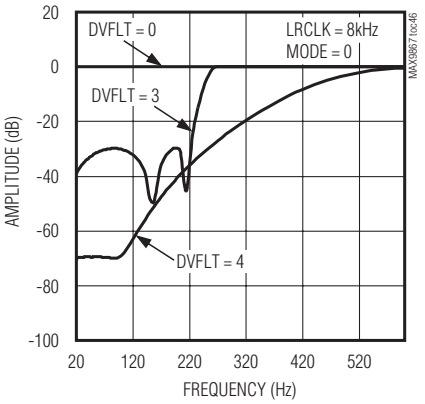


Ultra-Low Power Stereo Audio Codec

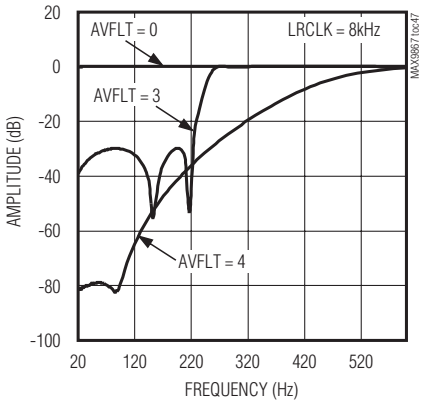
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to $f_S/2$, T_A = +25°C, unless otherwise noted.)

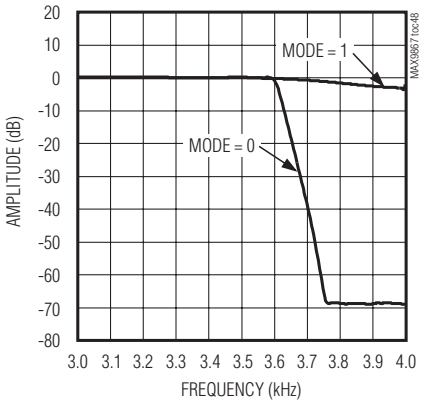
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



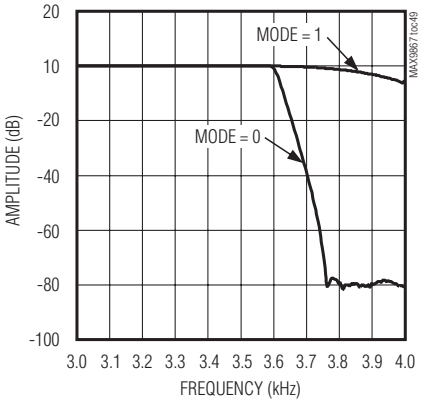
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



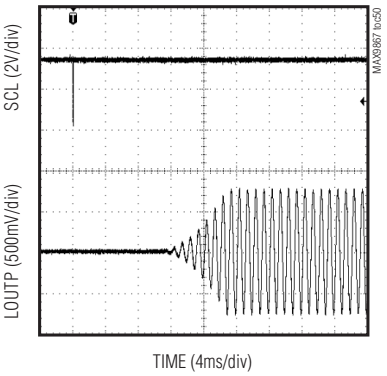
DAC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (8kHz)



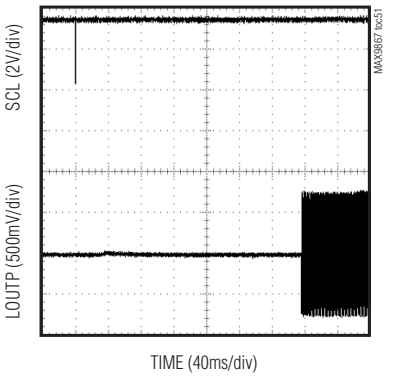
ADC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (8kHz)



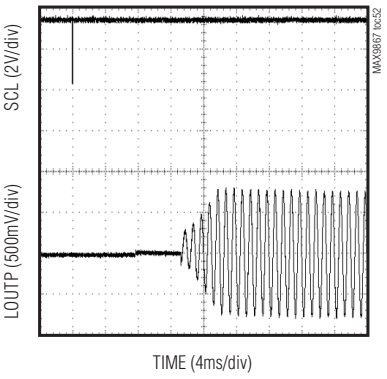
SHUTDOWN TO DAC FULL OPERATION (CAPACITORLESS OR DIFFERENTIAL MODE)



SHUTDOWN TO DAC FULL OPERATION (CLICKLESS SINGLE-ENDED MODE)



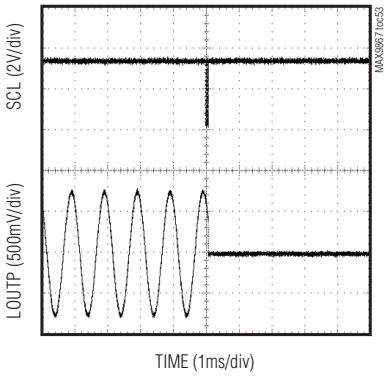
SHUTDOWN TO DAC FULL OPERATION (FAST TURN-ON SINGLE-ENDED MODE)



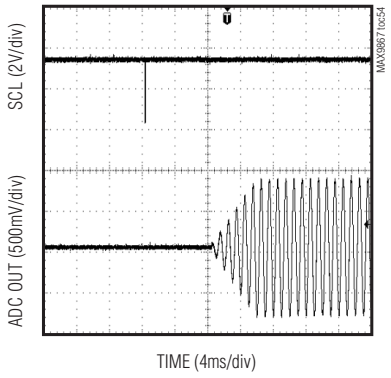
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to $f_S/2$, T_A = +25°C, unless otherwise noted.)

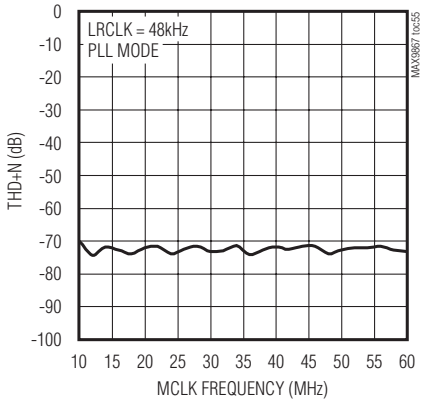
FULL OPERATION TO SHUTDOWN (DAC)



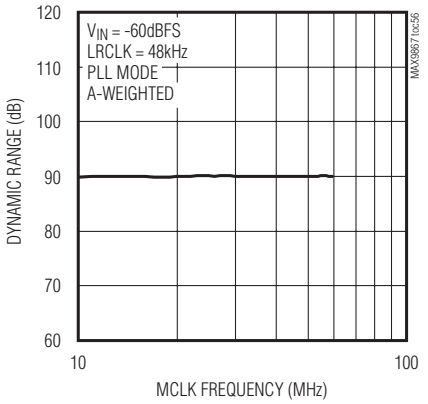
ADC SOFT-START



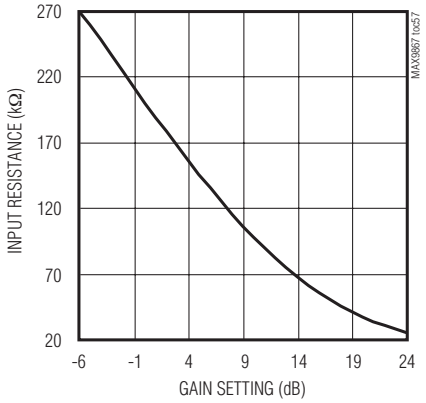
TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS



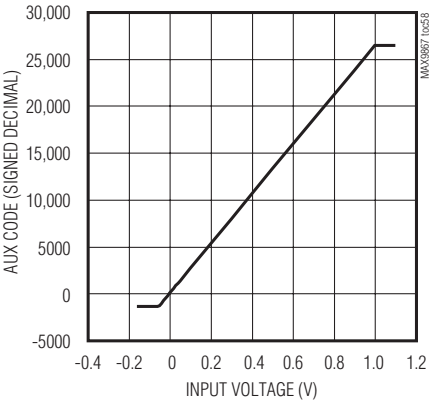
DYNAMIC RANGE vs. MCLK FREQUENCY



LINE INPUT RESISTANCE vs. GAIN SETTING



AUX CODE vs. INPUT VOLTAGE



Ultra-Low Power Stereo Audio Codec

Pin Description

PIN/BUMP		NAME	FUNCTION
TQFN-EP	WLP		
1	A2	DGND	Digital Ground
2	B3	SCL	I²C Serial-Clock Input. Connect a pullup resistor to a 1.7V to 3.3V supply.
3	A3	SDA	I²C Serial-Data Input/Output. Connect a pullup resistor to a 1.7V to 3.3V supply.
4	C3	$\overline{IRQ}$	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to pull low when bits in status register 0x00 are set. Read status register 0x00 to clear $\overline{IRQ}$ once set. Repeat faults have no effect on $\overline{IRQ}$ until it is cleared by reading register 0x00. Connect a 10kΩ pullup resistor to a 1.7V to 3.3V supply.
5	A4	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
6	B4	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor (1.23V nominal).
7	A5	PREG	Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor (1.6V nominal).
8	B5	REG	PREG/2 Voltage Reference. Bypass to AGND with a 1µF capacitor (0.8V nominal).
9	A6	AGND	Analog Ground
10	B6	MICBIAS	Low-Noise Microphone Bias. Connect a 2.2kΩ to 470Ω resistor to the positive output of a microphone (1.525V nominal). Bypass to AGND with a 1µF capacitor.
11	C5	MICLN/ DIGMICCLK	Left Negative Differential Microphone Input or Digital Microphone Clock Output. For analog microphones, AC-couple to the negative output of a microphone with a 1µF capacitor. For digital microphones, connect to the clock input of the microphone.
12	C6	MICLP/ DIGMICDATA	Left Positive Differential Microphone Input or Digital Microphone Data Input. For analog microphones, AC-couple to the positive output of a microphone with a 1µF capacitor. For digital microphones, connect to the data output of the microphone(s). Up to two digital microphones can be connected.
13	C4	MICRP	Right Positive Differential Microphone Input. AC-couple to the positive output of a microphone with a 1µF capacitor.
14	D6	MICRN	Right Negative Differential Microphone Input. AC-couple to the negative output of a microphone with a 1µF capacitor.
15	D5	LINL	Left-Line Input. AC-couple analog audio signal to LINL with a 1µF capacitor.
16	E6	LINR	Right-Line Input. AC-couple analog audio signal to LINR with a 1µF capacitor.
17	D4	JACKSNS/AUX	Jack Sense or Auxiliary ADC Input. When configured for jack detection, JACKSNS detects the presence or absence of a jack. See the *Mode Configuration* section for details. When configured as an auxiliary ADC input, AUX is used to measure DC voltages.
18	E5	PGND	Headphone Power Ground
19	D3	ROUTP	Positive Right-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
20	E4	ROUTN	Negative Right-Channel Headphone Output. Inverting output in differential mode. Leave unconnected in capacitorless and fast turn-on single-ended mode. Bypass with a 1µF capacitor to AGND in clickless, single-ended mode.
21	D2	LOUTN	Negative Left-Channel Headphone Output. Noninverting output in differential mode. Common headphone return in capacitorless mode. Leave unconnected in fast turn-on single-ended mode. Bypass with a 1µF capacitor to AGND in clickless single-ended mode.

Pin Description (continued)

PIN/BUMP		NAME	FUNCTION
TQFN-EP	WLP		
22	E3	LOUTP	Positive Left-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
23	E2	PVDD	Headphone Power Supply. Bypass to PGND with a 1µF capacitor.
24, 25	—	N.C.	No Connection
26	E1	DVDDIO	Digital Audio Interface Power Supply. Bypass to DGND with a 1µF capacitor.
27	D1	SDOUT	Digital Audio Serial-Data ADC Output
28	C2	SDIN	Digital Audio Serial-Data DAC Input
29	C1	LRCLK	Digital Audio Left-Right Clock Input/Output. LRCLK is the audio sample rate clock and determines whether the audio data on SDIN is routed to the left or right channel. In TDM mode, LRCLK is a frame synchronization pulse. LRCLK is an input when the MAX9867 is in slave mode and an output when in master mode.
30	B1	BCLK	Digital Audio Bit Clock Input/Output. BCLK is an input when the MAX9867 is in slave mode and an output when in master mode.
31	B2	MCLK	Master Clock Input. Acceptable input frequency range: 10MHz to 60MHz.
32	A1	DVDD	Digital Power Supply. Supply for the digital circuitry and I^2C interface. Bypass to DGND with a 1µF capacitor.
—	—	EP	Exposed Pad. Connect the exposed thermal pad to AGND.

Detailed Description

The MAX9867 is a low-power stereo audio codec designed for portable applications requiring minimum power consumption.

The stereo playback path accepts digital audio through a flexible interface compatible with I^2S, TDM, and left-justified signals. An oversampling sigma-delta DAC converts the incoming digital data stream to analog audio and outputs the audio through the stereo headphone amplifier. The headphone amplifier can be configured in differential, single-ended, and capacitorless output modes.

The stereo record path has two analog microphone inputs with selectable gain. An integrated microphone bias can be used to power the microphones. The left analog microphone inputs can also accept data from up to two digital microphones. An oversampling sigma-delta ADC converts the microphone signals and outputs the digital bit stream over the digital audio interface.

Integrated digital filtering provides a range of notch and highpass filters for both the playback and record paths to limit undesirable low-frequency signals and GSM transmission noise. The digital filtering provides attenuation of out-of-band energy by over 70dB, eliminating audible aliasing. A digital sidetone function allows audio from the record path to be summed into the playback path after digital filtering.

The MAX9867 also includes two stereo, single-ended line inputs with gain adjustment, which can be recorded by the ADCs and/or output by the headphone amplifiers. An auxiliary ADC accurately measures a DC voltage by utilizing the right audio ADC and reporting the DC voltage through the I^2C interface. A jack detection function allows the detection of headphone, microphone, and headset jacks. Insertion and removal events can be programmed to trigger a hardware interrupt and flag an I^2C register bit.

The MAX9867's flexible clock circuitry utilizes a programmable clock divider and a digital PLL, allowing the DAC and ADC to operate at maximum dynamic range for all combinations of master clock (MCLK) and sample rate (LRCLK) without consuming extra supply current. Any master clock between 10MHz and 60MHz is supported as are all sample rates from 8kHz to 48kHz. Master and slave modes are supported for maximum flexibility.

Ultra-Low Power Stereo Audio Codec

I²C Registers

The MAX9867 audio codec is completely controlled through software using an I²C interface. The power-on default setting is complete shutdown, requiring that the internal registers be programmed to activate the device. See Table 1 for the device's complete register map.

I²C Slave Address

The MAX9867 responds to the slave address 0x30 for all write commands and 0x31 for all read operations.

Table 1. I²C Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
STATUS										
Status (Read Only)	CLD	SLD	ULK	0	0	0	JDET	0	0x00	—
Jack Sense (Read Only)	LSNS	JKSNS	JKMIC	0	0	0	0	0	0x01	—
AUX High (Read Only)	AUX[15:8]								0x02	—
AUX Low (Read Only)	AUX[7:0]								0x03	—
Interrupt Enable	ICLD	ISLD	IULK	0	0	$\overline{\text{SDODLY}}$	IJDET	0	0x04	0x00
CLOCK CONTROL										
System Clock	0	0	PSCLK		FREQ				0x05	0x00
Stereo Audio Clock Control High	PLL	NI[14:8]							0x06	0x00
Stereo Audio Clock Control Low	NI[7:1]							RLK/ NI[0]	0x07	0x00
DIGITAL AUDIO INTERFACE										
Interface Mode	MAS	WCI	BCI	DLY	HIZOFF	TDM	0	0	0x08	0x00
Interface Mode	0	0	0	LVOLFIX	DMONO	BSEL			0x09	0x00
DIGITAL FILTERING										
Codec Filters	MODE	AVFLT			0	DVFLT			0x0A	0x00
LEVEL CONTROL										
Sidetone	DSTS		0	DVST					0x0B	0x00
DAC Level	0	DACM	DACG		DACA				0x0C	0x00
ADC Level	AVL				AVR				0x0D	0x00
Left-Line Input Level	0	LILM	0	0	LIGL				0x0E	0x00
Right-Line Input Level	0	LIRM	0	0	LIGR				0x0F	0x00
Left Volume Control	0	VOLLM	VOLL						0x10	0x00
Right Volume Control	0	VOLRM	VOLR						0x11	0x00
Left Microphone Gain	0	PALEN	PGAML						0x12	0x00
Right Microphone Gain	0	PAREN	PGAMR						0x13	0x00
CONFIGURATION										
ADC Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x14	0x00
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	0	0x15	0x00
Mode	DSLEW	$\overline{\text{VSEN}}$	$\overline{\text{ZDEN}}$	0	JDETEN	HPMODE			0x16	0x00
POWER MANAGEMENT										
System Shutdown	$\overline{\text{SHDN}}$	LNLEN	LNREN	0	DALEN	DAREN	ADLEN	ADREN	0x17	0x00
Revision	REV								0xFF	0x42

Device Status

Status registers 0x00 and 0x01 are read-only registers that report the status of various device functions. The status register bits are cleared upon reading the status register and are set the next time the event occurs. Registers 0x02 and 0x03 report the DC level applied to AUX. See the *ADC* section for more details and Table 2.

Table 2. Status Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Status (Read Only)	CLD	SLD	ULK	0	0	0	JDET	0	0x00
Jack Sense (Read Only)	LSNS	JKSNS	JKMIC	0	0	0	0	0	0x01
AUX High (Read Only)	AUX[15:8]								0x02
AUX Low (Read Only)	AUX[7:0]								0x03

BITS	FUNCTION
CLD	**Clip Detect Flag** Indicates that a signal has reached or exceeded full scale in the ADC or DAC.
SLD	**Slew Level Detect Flag** When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value. SLD is also set when soft-start or stop is complete.
ULK	**Digital PLL Unlock Flag** Indicates that the digital audio PLL has become unlocked and digital signal data is not reliable.
JDET	**Headset Configuration Change Flag** JDET is set whenever there is a change in register 0x01, indicating that the headset configuration has changed.
LSNS	**LOUTP State (Valid if $\overline{SHDN}$ = 0, JDETEN = 1)** LSNS is set when the voltage at LOUTP exceeds AVDD - 0.4V. An internal pullup from AVDD to LOUTP causes this condition whenever there is no load on LOUTP. LSNS is only valid in differential and capacitorless output modes.
JKSNS	**JACKSNS State (Valid if JDETEN = 1)** JKSNS is set when the voltage at JACKSNS exceeds AVDD - 0.4V. An internal pullup from AVDD to JACKSNS causes this condition whenever there is no load on JACKSNS.
JKMIC	**Microphone Detection (Valid if PALEN or PAREN ≠ 00 and JDETEN = 1)** JKMIC is set when JACKSNS exceeds 0.95 x $V_{MICBIAS}$.
AUX	**Auxiliary Input Measurement** AUX is a 16-bit signed two's complement number representing the voltage measured at JACKSNS/AUX. Before reading a value from AUX, set AUXCAP to 1 to ensure a stable reading. After reading the value, set AUXCAP to 0. Use the following formula to convert the AUX value into an equivalent JACKSNS/AUX voltage: $\text{Voltage} = 0.738\text{V} \times \left(\frac{\text{AUX}}{\text{k}} \right)$ k = AUX value when AUXGAIN = 1. See the *ADC* section for complete details.

Ultra-Low Power Stereo Audio Codec

Hardware Interrupts

Hardware interrupts are reported on the open-drain $\overline{IRQ}$ pin. When an interrupt occurs, $\overline{IRQ}$ remains low until the interrupt is serviced by reading the status register 0x00. If a flag is set, it is reported as a hardware interrupt only if the corresponding interrupt enable is set. Each bit enables interrupts for the status flag in the respective bit location in register 0x00. See Table 3.

$\overline{SDODLY}$ is used to control the SDOUT timing. See the *Digital Audio Interface* section for a detailed description.

Clock Control

The MAX9867 can work with a master clock (MCLK) supplied from any system clock within the 10MHz-to-60MHz range. Internally, the MAX9867 requires a 10MHz-to-20MHz clock. A prescaler divides MCLK by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the MAX9867. See Table 4.

The MAX9867 is capable of supporting any sample rate from 8kHz to 48kHz, including all common sample rates (8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, and 48kHz). To accommodate a wide range of system architectures, the MAX9867 supports three main clocking modes:

- **Normal:** This mode uses a 15-bit clock divider coefficient to set the sample rate relative to the prescaled MCLK input (PCLK). This allows high flexibility in both the MCLK and LRCLK frequencies and can be used in either master or slave mode.
- **Exact Integer:** In both master and slave mode, common MCLK frequencies (12MHz, 13MHz, 16MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ bits instead of the NI and PLL control bits.
- **PLL:** When operating in slave mode, a PLL can be enabled to lock onto externally generated LRCLK signals that are not integer related to PCLK. Prior to enabling the interface, program NI to the nearest desired ratio and set the NI[0] = 1 to enable the PLL's rapid lock mode. If NI[0] = 0, then NI is ignored and PLL lock time is slower.

Table 3. Interrupt Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Interrupt Enable	ICLD	ISLD	IULK	0	0	$\overline{SDODLY}$	IJDET	0	0x04

Table 4. Clock Control Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER
System Clock	0	0	PSCLK		FREQ				0x05
Stereo Audio Clock Control High	PLL	NI[14:8]							0x06
Stereo Audio Clock Control Low	NI[7:1]							NI[0]	0x07

BITS	FUNCTION
PSCLK	**MCLK Prescaler** Divides MCLK to generate a PCLK between 10MHz and 20MHz. 00 = Disable clock for low-power shutdown. 01 = Select if MCLK is between 10MHz and 20MHz. 10 = Select if MCLK is between 20MHz and 40MHz. 11 = Select if MCLK is between 40MHz and 60MHz.

Table 4. Clock Control Registers (continued)

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td rowspan="11">FREQ</td><td colspan="4">Exact Integer Modes
Allows integer sampling for specific PCLK (prescaled MCLK) frequencies and 8kHz or 16kHz sample rates.</td></tr>
<tr><td>FREQ[3:0]</td><td>PCLK (MHz)</td><td>LRCLK (kHz)</td><td>PCLK/LRCLK</td></tr>
<tr><td>0x00</td><td colspan="3">Normal or PLL mode</td></tr>
<tr><td>0x1–0x7</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0x8
0x9</td><td>12
12</td><td>8
16</td><td>1500
750</td></tr>
<tr><td>0xA
0xB</td><td>13
13</td><td>8
16</td><td>1625
812.5</td></tr>
<tr><td>0xC
0xD</td><td>16
16</td><td>8
16</td><td>2000
1000</td></tr>
<tr><td>0xE
0xF</td><td>19.2
19.2</td><td>8
16</td><td>2400
1200</td></tr>
<tr><td colspan="4">Modes 0x8–0xF are available in either master or slave mode. In slave mode, if the indicated PCLK/LRCLK ratio cannot be guaranteed, use PLL mode instead.</td></tr>
<tr><td>PLL</td><td colspan="4">PLL Mode Enable
0 = Valid for slave and master mode. The frequency of LRCLK is set by the NI divider bits. In master mode, the MAX9867 generates LRCLK using the specified divide ratio. In slave mode, the MAX9867 expects an LRCLK as specified by the divide ratio.
1 = Valid for slave mode only. A digital PLL locks on to any externally supplied LRCLK signal.

Rapid Lock Mode
To enable rapid lock mode, set NI to the nearest desired ratio and set NI[0] = 1 before enabling the interface.</td></tr>
<tr><td>NI</td><td colspan="4">Normal Mode LRCLK Divider
When PLL = 0, the frequency of LRCLK is determined by NI. See Table 5 for common NI values.

$NI = (65536 \times 96 \times f_{LRCLK})/f_{PCLK}$

f_{LRCLK} = LRCLK frequency
f_{PCLK} = Prescaled MCLK internal clock frequency (PCLK)

LRCLK > 24kHz is only valid for MODE = 0 (stereo audio mode). MODE = 1 (voice mode) requires LRCLK ≤ 24kHz.</td></tr>
</table>

Table 5. Common NI Values

MCLK (MHz)	LRCLK (kHz)						
	PSCLK	**8**	**16**	**24**	**32**	**44.1**	**48**
11.2896	01	0x116A	0x22D4	0x343F	0x45A9	**0x6000**	0x687D
12	01	0x1062	0x20C5	0x3127	0x4189	0x5A51	0x624E
12.288	01	**0x1000**	**0x2000**	**0x3000**	**0x4000**	0x5833	**0x6000**
13	01	0x0F20	0x1E3F	0x2D5F	0x3C7F	0x535F	0x5ABE
19.2	01	0x0A3D	0x147B	0x1EB8	0x28F6	0x3873	0x3D71
24	10	0x1062	0x20C5	0x1893	0x4189	0x5A51	0x624E
26	10	0x0F20	0x1E3F	0x16AF	0x3C7F	0x535F	0x5ABE
27	10	0x0E90	0x1D21	0x15D8	0x3A41	0x5048	0x5762

Note: *Bolded values are exact integers that provide maximum full-scale performance.*