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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-5139; Rev 1; 3/11

EVALUATION KIT AVAILABLE

Low-Power, High-Performance Dual I²S Stereo Audio Codec

MAX9880A

General Description

The MAX9880A is a high-performance, stereo audio codec designed for portable consumer applications such as smartphones and tablets. Operating from a single 1.8V supply to ensure low-power consumption, the MAX9880A offers a variety of input and output configurations for design flexibility. The MAX9880A can be combined with an audio subsystem, such as the MAX9877 or MAX9879, for a complete audio solution for portable applications.

The MAX9880A's stereo differential microphone inputs can support either analog or digital microphones. A stereo single-ended line input, with a configurable preamplifier, can either be recorded by the ADC or routed directly to the headphone or line output amplifiers. The stereo headphone amplifiers can be configured as differential, single ended, or capacitorless. The stereo line outputs have dedicated level adjustment.

There are two digital audio interfaces. The primary interface is intended for voiceband applications, while the secondary interface can be used for high performance stereo audio data. Two digital input streams can be processed simultaneously and both digital interfaces support TDM and I²S data formats.

The flexible clocking circuitry utilizes any available 10MHz to 60MHz system clock, eliminating the need for an external PLL and multiple crystal oscillators. Both the ADC and DAC can be operated synchronously or asynchronously in master or slave mode. The ADC can be operated from 8kHz to 48kHz sample rates, while the DAC can be operated up to 96kHz.

The MAX9880A prevents click and pop during volume changes and during power-up and power-down. Audio quality is further enhanced with user-configurable digital filters for voice and audio data. Voiceband filters provide extra attenuation at the GSM packet frequency and greater than 70dB stopband attenuation at $f_S/2$. An I²C or SPI™ serial interface provides control for volume levels, signal mixing, and general operating modes.

The MAX9880A is available in space-saving, 48-bump, 2.7mm x 3.5mm, 0.4mm-pitch WLP and 48-pin, 6mm x 6mm TQFN packages.

Applications

Cellular Phones

Tablet PCs

Portable Gaming Devices

Portable Multimedia Players

SPI is a trademark of Motorola, Inc.

Features

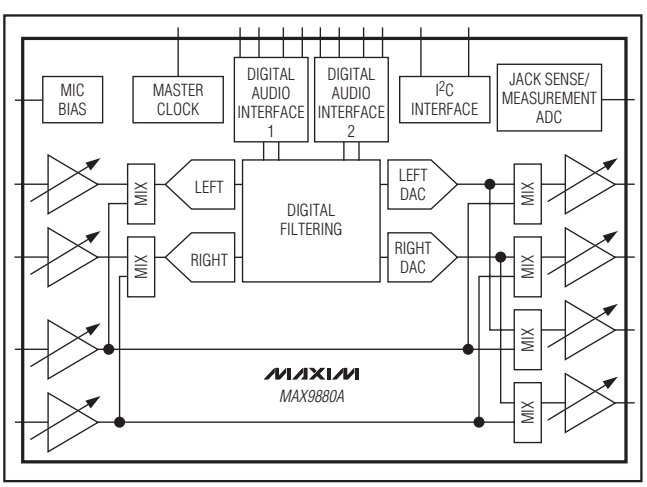
- **1.8V Single-Supply Operation**
- **10.6mW Playback Power Consumption**
- **8kHz to 96kHz Stereo DAC with 96dB Dynamic Range**
- **8kHz to 48kHz Stereo ADC with 82dB Dynamic Range**
- **Support for Any Master Clock Between 10MHz to 60MHz**
- **Stereo Microphone Inputs Support Digital Microphones**
- **Stereo Headphone Amplifiers: Differential (30mW), Single-Ended, or Capacitorless (10mW)**
- **Stereo Line Inputs and Stereo Line Outputs**
- **Voiceband Filters with Stopband Attenuation Greater than 70dB**
- **Battery-Measurement Auxiliary ADC**
- **Comprehensive Headset Detection**
- **Dual I²S- and TDM-Compatible Digital Audio Interfaces**
- **I²C- or SPI-Compatible Control Bus with 3.6V Tolerant Inputs**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9880AEWM+	-40°C to +85°C	48 WLP
MAX9880AETM+	-40°C to +85°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Block Diagram



Functional Diagram/Typical Operating Circuit appears at end of data sheet.

Low-Power, High-Performance Dual I²S Stereo Audio Codec

ABSOLUTE MAXIMUM RATINGS

(Voltages with respect to AGND.)
DVDD, AVDD, PVDD .....-0.3V to +2V
DVDDS1, JACKSNS, MICVDD .....-0.3V to +3.6V
DGND, PGND .....-0.1V to +0.1V
PREG, REF, REG .....-0.3V to (V_{AVDD} + 0.3V)
MICBIAS .....-0.3V to (V_{MICVDD} + 0.3V)
MCLK, LRCLKS1, BCLKS1, SDINS1, SDOUTS1 .....-0.3V to (V_{DVDDS1} + 0.3V)
X1, X2, LRCLKS2, BCLKS2, SDINS2, SDOUTS2, DOUT, MODE .....-0.3V to (V_{DVDD} + 0.3V)
SDA/DIN, SCL/SCLK, $\overline{CS}$, $\overline{IRQ}$ .....-0.3V to +3.6V
LOUTP, LOUTN, ROUTP, ROUTN, LOUTL, LOUTR .....(V_{PGND} - 0.3V) to (V_{PVDD} + 0.3V)
LINL, LINR, MICLP/DIGMICDATA, MICLN/DIGMICCLK, MICRP/SPDMDATA, MICRN/SPDMCLK .....-0.3V to (V_{AVDD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
48-Bump WLP (derate 12.5mW/°C above +70°C) 1000mW
48-Pin TQFN (derate 37mW/°C above +70°C) 2963mW
Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....42°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range		PVDD, DVDD, AVDD		1.65	1.8	1.95	V
		DVDDS1, MICVDD		1.65	1.8	3.6	
Total Supply Current	I_{VDD}	Full-duplex 8kHz mono (Note 3)	Analog (AVDD + PVDD + MICVDD)		5.33	8	mA
			Digital (DVDD + DVDDS1)		1.4	2	
		DAC playback 48kHz stereo (Note 3)	Analog (AVDD + PVDD + MICVDD)		3.5	6	
			Digital (DVDD + DVDDS1)		2.5	4	
		Full-duplex 48kHz stereo (Note 3)	Analog (AVDD + PVDD + MICVDD)		8.4	12	
			Digital (DVDD + DVDDS1)		3.0	5	
		Stereo line-in to line-out only, T_A = +25°C	Analog (AVDD + PVDD + MICVDD)		4.9	8	
			Digital (DVDD + DVDDS1)		0.012	0.05	
Shutdown Supply Current		T_A = +25°C	Analog (AVDD + PVDD + MICVDD)		0.3	2	µA
			Digital (DVDD + DVDDS1)		2.6	8	
Shutdown to Full Operation		Excludes PLL lock time			10		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC (Note 4)							
Dynamic Range (Note 5)	DR	f_S = 48kHz, AV_{VOL} = 0dB, T_A = +25°C	Master or slave mode		96		dB
			Slave mode	88			
Full-Scale Output		Differential mode			1		V_{RMS}
		Capacitorless and single-ended modes			0.56		
Gain Error		DC accuracy, measured with respect to full-scale output			1	5	%
Voice Path Phase Delay	P_{DLY}	1kHz, 0dB input, highpass filter disabled measured from digital input to analog output; MODE = 0 (IIR voice)	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.59		
Total Harmonic Distortion	THD	f_{MCLK} = 12.288MHz, f_S = 48kHz, 0dBFS, measured at headphone outputs			-75		dB
DAC Attenuation Range	AV_{DAC}	VDACA/SDACA = 0xF to 0x0		-15		0	dB
DAC Gain Adjust	AV_{GAIN}	VDACG = 00 to 11		0		+18	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V			85		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			85		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			80		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			74		
DAC VOICE MODE DIGITAL IIR LOWPASS FILTER (6x Interpolation)							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.448 x f_S		Hz
		-3dB cutoff			0.451 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.476 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz		75			dB
DAC VOICE MODE DIGITAL 5th-ORDER IIR HIGHPASS FILTER							
5th-Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{DHPPB}	DVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)			0.0161 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)			0.0312 x f_S		
		DVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)			0.0321 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)			0.0625 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)			0.0042 x f_S		

Low-Power, High-Performance Dual I²S Stereo Audio Codec

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
5th-Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable)	f_{DHPSB}	DVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)			0.0139 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)			0.0156 x f_S		
		DVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)			0.0279 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)			0.0312 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)			0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	DVFLT not equal to 000			90		dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER (DHF = 0 for f_{LRCLK} < 50kHz)							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.43 x f_S		Hz
		-3dB cutoff			0.47 x f_S		
		-6.02dB cutoff			0.50 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz; f = 0.58 f_S to 7.42 f_S			0.58 x f_S		Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER (DHF = 1 for f_{LRCLK} > 50kHz)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff			0.24 x f_S		Hz
		-3dB cutoff			0.33 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f = 0.5 f_S to 3.5 f_S			0.5 x f_S		Hz
Stopband Attenuation		f > f_{SLP}		60			dB
DAC STEREO AUDIO MODE DIGITAL DC-BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1 (DAI1), DCB = 1 (DAI2)			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	DVFLT = 0x1 (DAI1), DCB = 1 (DAI2)			90		dB
ADC (Note 6)							
Dynamic Range (Note 5)	DR	f_S = 8kHz, MODE = 0 (IIR voice), T_A = +25°C		72	82		dB
		f_S = 8kHz to 48kHz, MODE = 1 (FIR audio) (Note 7)			84		
Full-Scale Input		Differential MIC input or stereo line inputs, AV_{PRE} = 0dB, AV_{PGAM} = 0dB			1		V_{P-P}
Gain Error (Note 7)		DC accuracy, measured with respect to 80% of full-scale output			1	5	%
Voice Path Phase Delay		1kHz, 0dB input, highpass filter disabled measured from analog input to digital output; MODE = 0 (IIR voice)	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.61		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	f = 1kHz, f_S = 8kHz, T_A = +25°C, -20dB input		-80	-70	dB
ADC Level Adjust	AV_{ADC}	AVL/AVR = 0xF to 0x0	-12		+3	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred		80		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred		78		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{ADC} = 0dB, input referred		72		
ADC VOICE MODE DIGITAL IIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.445 x f_S		Hz
		-3dB cutoff		0.449 x f_S		
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.469 x f_S		Hz
Stopband Attenuation		$f > f_{SLP}$, f = 20Hz to 20kHz	74			dB
ADC VOICE MODE DIGITAL 5th-ORDER IIR HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		AVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (Elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		AVFLT = 0x3 (Elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
ADC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.48 x f_S		
		-6.02dB cutoff		0.5 x f_S		

Low-Power, High-Performance Dual I²S Stereo Audio Codec

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Passband Ripple		$f < f_{PLP}$			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.58 x f_S		Hz
Stopband Attenuation		$f > f_{SLP}$, f = 20Hz to 20kHz			60		dB
ADC STEREO AUDIO MODE DIGITAL DC-BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	AVFLT = 0x1			90		dB
OUTPUT VOLUME CONTROL							
Output Volume Control (Note 8)		VOLL/VOLR = 0x00		8.1	8.6	9.2	dB
		VOLL/VOLR = 0x01		7.6	8.1	8.6	
		VOLL/VOLR = 0x02		7.1	7.6	8.1	
		VOLL/VOLR = 0x04		6.1	6.6	7.2	
		VOLL/VOLR = 0x08		3.1	3.6	4.3	
		VOLL/VOLR = 0x10		-5.9	-5.4	-4.9	
		VOLL/VOLR = 0x20		-60	-55.1	-52	
		VOLL/VOLR = 0x27		-94	-84	-81	
Output Volume Control Step Size		VOLL/VOLR = 00x00 to 0x06 (+9dB to +6dB)			0.5		dB
		VOLL/VOLR = 00x06 to 0x0F (+6dB to +3dB)			1		
		VOLL/VOLR = 00x0F to 0x17 (-3dB to -19dB)			2		
		VOLL/VOLR = 00x17 to 0x27 (-19dB to -81dB)			4		
Output Volume Control Mute Attenuation		f = 1kHz			100		dB
HEADPHONE AMPLIFIER (Note 9)							
Output Power (Differential Mode)	P_{OUT}	f = 1kHz, 0dBFS input, THD < 1%, T_A = +25°C	R_L = 16Ω	25	48		mW
			R_L = 32Ω		30		
Output Power (Capacitorless Mode)	P_{OUT}	f = 1kHz, 0dBFS input, THD < 1%, T_A = +25°C	R_L = 16Ω		17		mW
			R_L = 32Ω		10		
Total Harmonic Distortion + Noise (Differential Mode)	THD+N	f = 1kHz, -3dBFS input	R_L = 16Ω		-78	-67	dB
			R_L = 32Ω		-79		
Total Harmonic Distortion + Noise (Capacitorless Mode)	THD+N	f = 1kHz, -3dBFS input	R_L = 16Ω		-73	-60	dB
			R_L = 32Ω		-75		
Total Harmonic Distortion + Noise (Single-Ended Mode)	THD+N	f = 1kHz, -3dBFS input	R_L = 16Ω		-70	-60	dB
			R_L = 32Ω		-70		
Dynamic Range (Notes 5, 7)	DR	AV_{VOL} = +6dB		77	90		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 7)	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			80		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			72		
Output Offset Voltage	V_{OS}	AV_{VOL} = -81dB, differential mode	LOUTP to LOUTN, ROUTP to ROUTN, T_A = +25°C		±0.2		mV
		AV_{VOL} = -81dB, capacitorless mode	LOUTP to LOUTN, ROUTP to LOUTN, T_A = +25°C		±0.6		
Crosstalk	XTALK	Differential, P_{OUT} = 5mW, f = 1kHz			90		dB
		Capacitorless mode, P_{OUT} = 5mW, f = 1kHz			45		
Capacitive Drive Capability		No sustained oscillations	R_L = 32Ω		500		pF
			R_L =		100		
Click-and-Pop Level (Differential, Capacitorless Modes)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-70		dBV
			Out of shutdown		-70		
Click-and-Pop Level (Single-Ended Mode)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-70		dBV
			Out of shutdown		-70		
LINE OUTPUTS (Note 7)							
Full-Scale Output					0.5		V_{RMS}
Line Output Level Adjust	AV_{LO}	LOGL/LOGR = 0x00		-0.7	-0.1	+0.6	dB
		LOGL/LOGR = 0x01		-2.6	-2.1	-1.6	
		LOGL/LOGR = 0x02		-4.6	-4.1	-3.6	
		LOGL/LOGR = 0x04		-8.6	-8.1	-7.6	
		LOGL/LOGR = 0x08		-16.6	-16	-15.6	
		LOGL/LOGR = 0x0F		-31.1	-29.9	-29.1	
Line Output Mute Attenuation		f = 1kHz			90		dB
Total Harmonic Distortion + Noise	THD+N	R_L = 1kΩ, f = 1kHz, V_{OUT} = 1.4V_{P-P} (Note 9)			-67	-59	dB
Signal-to-Noise Ratio		R_L = 1kΩ, LINL/LINR = 1µF to GND	20Hz < f < 20kHz		86		dB
			A-weighted		90		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V			46		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			80		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			76		
Capacitive Drive Capability		R_L = 10kΩ, no sustained oscillations			100		pF

Low-Power, High-Performance Dual I²S Stereo Audio Codec

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MICROPHONE AMPLIFIER							
Preamplifier Gain	AV_{PRE}	PALEN/PAREN = 01		-0.5	0	+0.5	dB
		PALEN/PAREN = 10		19.5	20	20.5	
		PALEN/PAREN = 11		29.3	30	30.5	
MIC PGA Gain	AV_{PGAM}	PGAML/PGAMR = 0x1F		-0.5	0	+0.6	dB
		PGAML/PGAMR = 0x00		19.3	19.9	20.4	
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P}, f = 217Hz			50		dB
MIC Input Resistance	RIN_MIC	All gain settings		30	50		kΩ
Total Harmonic Distortion + Noise	THD+N	AV_{PRE} = 0dB V_{IN} = 1V_{P-P}, f = 1kHz, A-weighted			-80		dB
		AV_{PRE} = +30dB V_{IN} = 32mV_{P-P}, f = 1kHz, A-weighted			-65		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred		60	80		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred			80		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred			78		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred			72		
MICROPHONE BIAS							
MICBIAS Output Voltage	$V_{MICBIAS}$	I_{LOAD} = 1mA	V_{MICVDD} = 1.8V, MBIAS = 0	1.48	1.52	1.56	V
			V_{MICVDD} = 3V, MBIAS = 0	2.15	2.2	2.25	
Load Regulation		I_{LOAD} = 1mA to 2mA, MBIAS = 0			0.6	10	V/A
Line Regulation		V_{AVDD} = 1.8V, V_{MICVDD} = 1.65V to 1.95V, MBIAS = 0			1.55		mV/V
Power-Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} = 100mV_{P-P}			100		dB
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}			90		
Noise Voltage		A-weighted			9.5		$µV_{RMS}$
LINE INPUT							
Full-Scale Input	V_{IN}	AV_{LINE} = 0dB			1.0		V_{P-P}
Line Input Level Adjust	AV_{LINE}	LIGL/LIGR = 0x00		22.8	23.9	24.9	dB
		LIGL/LIGR = 0x01		20.7	21.9	22.9	
		LIGL/LIGR = 0x02		18.9	20	20.9	
		LIGL/LIGR = 0x04		14.9	16	16.9	
		LIGL/LIGR = 0x08		6.9	8	8.9	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Line Input Mute Attenuation		f = 1kHz			100		dB
Input Resistance	R_{IN_LINE}	AV_{LINE} = +24dB		20			kΩ
Total Harmonic Distortion + Noise	THD+N	V_{IN} = 0.1V_{P-P}, f = 1kHz			-74		dB
AUXIN INPUT							
Input DC Voltage Range		AUXEN = 1		0		0.738	V
AUXIN Input Resistance	R_{IN}	AUXEN = 1, 0V ≤ V_{AUXIN} ≤ 0.738V		10	40		MΩ
JACK DETECT							
JACKSNS High Threshold	V_{TH1}	$\overline{SHDN}$ = 1		0.92 x $V_{MICBIAS}$	0.95 x $V_{MICBIAS}$	0.98 x $V_{MICBIAS}$	V
		$\overline{SHDN}$ = 0			0.95 x V_{MICVDD}		
JACKSNS Low Threshold	V_{TH2}	$\overline{SHDN}$ = 1		0.06 x $V_{MICBIAS}$	0.10 x $V_{MICBIAS}$	0.17 x $V_{MICBIAS}$	V
		$\overline{SHDN}$ = 0			0.08 x V_{MICVDD}		
JACKSNS Sense Voltage	V_{SENSE}	$\overline{SHDN}$ = 0			V_{MICVDD}		V
JACKSNS Sense Resistance	R_{SENSE}	$\overline{SHDN}$ = 0		1.9	2.3	3.1	kΩ
JACKSNS Deglitch Period	t_{GLITCH}			12		300	ms
Headphone Sense Threshold					8		Ω
1-BIT SPDM OUTPUT							
Dynamic Range (Note 5)	DR	f_S = 48kHz, A-weighted, 20Hz to 20kHz, AV_{VOL} = 0dB; master or slave mode, T_A = +25°C			90		dB
Output Operational Range		0dB signal 1's density		25		75	%
DIGITAL SIDETONE (MODE = 1 IIR Voice Mode Only)							
Sidetone Gain Adjust Range	AV_{STGA}	Differential output mode		-60		0	dB
Voice Path Phase Delay	P_{DLY}	MIC input to headphone output, f = 1kHz, HP filter disabled	f_S = 8kHz		2.2		ms
			f_S = 16kHz		1.1		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT CLOCK CHARACTERISTICS							
MCLK Input Frequency	f_{MCLK}	For any LRCLK sample rate		10		60	MHz
MCLK Input Duty Cycle		Prescaler = /1 mode		40		60	%
		/2 or /4 modes		30		70	
Maximum MCLK Input Jitter		Maximum allowable RMS for performance limits			100		ps
LRCLK Sample Rate (Note 10)		DHF = 0		8		48	kHz
		DHF = 1		48		96	
LRCLK Average Frequency Error (Master and Slave Modes) (Note 11)		FREQ1 mode = 0x8 to 0xF		0		0	%
		PCLK = 192x, 256x, 384x, 512x, 768x, and 1024x		0		0	
		FREQ1 mode = Any clock other than above		-0.025		+0.025	
LRCLK PLL Lock Time		Any allowable LRCLK and PCLK rate, slave mode	Rapid lock mode		2	7	ms
			Nonrapid lock mode		12	25	
LRCLK Acceptable Jitter for Maintaining PLL Lock		Allowable LRCLK period change from nominal for slave PLL mode at any allowable LRCLK and PCLK rates				±100	ns
Soft-Start/Stop Time					10		ms
CRYSTAL OSCILLATOR							
Frequency		Fundamental mode only			12.288		MHz
Maximum Crystal ESR					100		Ω
Input Leakage Current	I_{IH}, I_{IL}	X1, T_A = +25°C		-1		+1	µA
Input Capacitance	C_{X1}, C_{X2}				4		pF
Maximum Load Capacitor	C_{L1}, C_{L2}				45		pF
DIGITAL INPUT (MCLK)							
Input High Voltage	V_{IH}			1.2			V
Input Low Voltage	V_{IL}					0.6	V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C		-1		+1	µA
Input Capacitance					10		pF
DIGITAL INPUTS (SDINS1, BCLKS1, LRCLKS1)							
Input High Voltage	V_{IH}			0.7 x V_{DVDDS1}			V
Input Low Voltage	V_{IL}					0.3 x V_{DVDDS1}	V
Input Hysteresis					200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C		-1		+1	µA
Input Capacitance					10		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL, DIN, SCLK, $\overline{CS}$, MODE, SDINS2, BCLKS2, LRCLKS2)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-1		+1	µA
Input Capacitance				10		pF
DIGITAL INPUTS (DIGMICDATA)						
Input High Voltage	V_{IH}		0.65 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.35 x V_{DVDD}	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C	-35		+35	µA
Input Capacitance				10		pF
CMOS DIGITAL OUTPUTS (BCLKS1, LRCLKS1, SDOUTS1)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	V_{DVDDS1} - 0.4			V
CMOS DIGITAL OUTPUTS (BCLKS2, LRCLKS2, SDOUTS2)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	V_{DVDD} - 0.4			V
CMOS DIGITAL OUTPUTS (DOUT)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA, $\overline{CS}$ = DVDD			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA, $\overline{CS}$ = DVDD	V_{DVDD} - 0.4			V
Output Low Current	I_{OL}	MODE = DVDD, DOUT = 0, T_A = +25°C	-1		+1	µA
Output High Current	I_{OH}	MODE = DVDD, DOUT = DVDD, T_A = +25°C	-1		+1	µA
CMOS DIGITAL OUTPUTS (DIGMICCLK, SPDMDATA, SPDMCLK)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	V_{DVDD} - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Current	I_{OH}	V_{OUT} = V_{DVDD}, T_A = +25°C	-1		+1	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.2 x V_{DVDD}	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL MICROPHONE TIMING CHARACTERISTICS (V_{DVDD} = 1.8V)							
DIGMICCLK Frequency	f_{MICCLK}	f_{MCLK} = 12.288MHz	MICCLK = 00		1.536		MHz
			MICCLK = 01		2.048		
			MICCLK = 10		64f_S		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU, MIC}$	Either clock edge		20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD, MIC}$	Either clock edge		0			ns
SPDM TIMING CHARACTERISTICS							
SPDMCLK Frequency	$f_{SPDMCLK}$	f_{MCLK} = 12.288MHz	SPDMCLK = 00		1.536		MHz
			SPDMCLK = 01		2.048		
			SPDMCLK = 10		3.072		
SPDMCLK to SPDMDATA Delay Time	$t_{DLY,SPDM}$	Rising edge SPDMCLK to right-channel valid SPDMDATA and falling edge SPDMCLK to left-channel valid SPDMDATA	Minimum, f_{MCLK} = 20MHz		15		ns
			Maximum, f_{MCLK} = 10MHz		65		
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (TDM = 0, V_{DVDD} = 1.8V)							
BCLK Cycle Time	t_{BCLKS}			75			ns
BCLK High Time	t_{BCLKH}	T_A = +25°C		30			ns
BCLK Low Time	t_{BCLKL}	T_A = +25°C		30			ns
BCLK or LRCLK Rise and Fall Time	t_R, t_F	Master operation, C_L = 15pF			7		ns
SDIN or LRCLK to BCLK Setup Time	t_{SU}			20			ns
SDIN or LRCLK to BCLK Hold Time	t_{HD}			5			ns
SDOUT Delay Time from BCLK Rising Edge	t_{DLY}	C_L = 30pF		0		40	ns
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (TDM = 1, Figure 3, V_{DVDD} = 1.8V)							
TDM Clock Frequency	1/t_{CLK}	TDM mode (TDM = 1)		128		2048	kHz
TDM Clock Time High	t_{CLKH}	TDM mode (TDM = 1), T_A = +25°C		220			ns
TDM Clock Time Low	t_{CLKL}	TDM mode (TDM = 1), T_A = +25°C		220			ns
TDM Short-Sync Setup Time	$t_{SYNCSET}$	Short TDM mode (TDM = 1, FSW = 0), master mode (MAS = 1)			200		ns
		Short TDM mode (TDM = 1, FSW = 0), slave mode (MAS = 0)		20			

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TDM Short Sync Hold Time	$t_{SYNCHOLD}$	Short TDM mode (TDM = 1, FSW = 0), master mode (MAS = 1)		200		ns
		Short TDM mode (TDM = 1, FSW = 0), slave mode (MAS = 0)	20			
TDM Short Sync Tx Data Delay	t_{SYNCTX}	Short TDM mode (TDM = 1, FSW = 0)		12		ns
TDM Long Sync Start Delay	$t_{CLKSYNC}$	Long TDM mode (TDM = 1, FSW = 1)		3.4		ns
TDM Long Sync End Time Setup	$t_{ENDSYNC}$	Long TDM mode (TDM = 1, FSW = 1)		51		ns
TDM Data Delay from Clock	t_{CLKTX}	TDM mode (TDM = 1)			40	ns
TDM High-Impedance State Setup from Data	t_{HIZOUT}	TDM mode (TDM = 1)		120		ns
TDM Rx Data Setup Time	t_{SETUP}	TDM mode (TDM = 1)	20			ns
TDM Rx Data Hold Time	t_{HOLD}	TDM mode (TDM = 1)	20			ns
I²C TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.6			µs
Data Hold Time	$t_{HD,DAT}$	$R_{PU,SDA}$ = 475Ω	0		900	ns
Data Setup Time	$t_{SU,DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 12)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 12)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	$R_{PU,SDA}$ = 475Ω (Note 12)	20 + 0.1C_B		250	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.6			µs

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ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, differential modes, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns
SPI TIMING CHARACTERISTICS						
Minimum SCLK Clock Period	t_{CP}			40		ns
Minimum SCLK Pulse-Width Low	t_{CL}			18		ns
Minimum SCLK Pulse-Width High	t_{CH}			18		ns
Minimum $\overline{CS}$ Setup Time	t_{CSS}			20		ns
Minimum $\overline{CS}$ Hold Time	t_{CSH}			20		ns
Minimum $\overline{CS}$ Pulse-Width High	t_{CSW}			20		ns
Minimum DIN Setup Time	t_{DS}			5		ns
Minimum DIN Hold Time	t_{DH}			5		ns
Minimum Output Data Propagation Delay	t_{DO}	C_L = 50pF		9		ns
Minimum Output Data Enable Time	t_{DEN}			5		ns
Minimum Output Data Disable Time	t_{DZ}			5		ns

Note 2: The MAX9880A is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 3: Clocking all zeros into the DAC. Master mode. Differential headphone mode.

Note 4: DAC performance measured at headphone outputs.

Note 5: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f = 20Hz to 20kHz.

Note 6: Performance measured using microphone inputs, unless otherwise stated.

Note 7: Performance measured using line inputs.

Note 8: Performance measured using line inputs to line outputs.

Note 9: Performance measured using DAC. f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz, unless otherwise stated.

Note 10: LRCLK can be any rate in the indicated range. Asynchronous or noninteger MCLK/LRCLK ratios can exhibit some full-scale performance degradation compared to synchronous integer-related MCLK/LRCLK ratios.

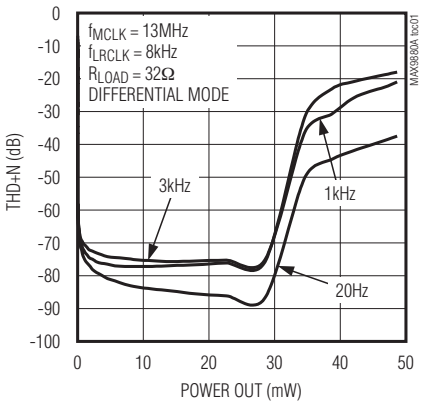
Note 11: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.

Note 12: C_B is in pF.

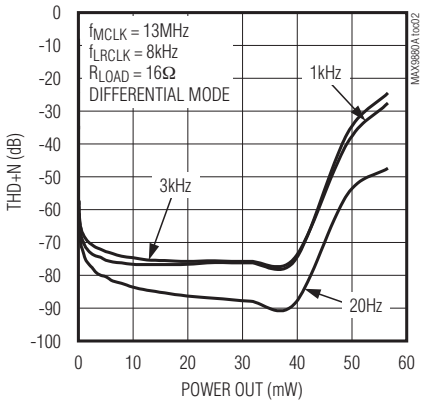
Typical Operating Characteristics

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

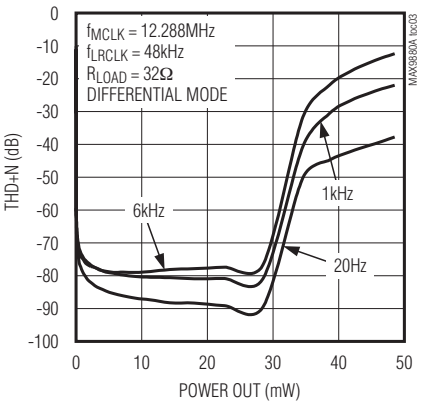
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



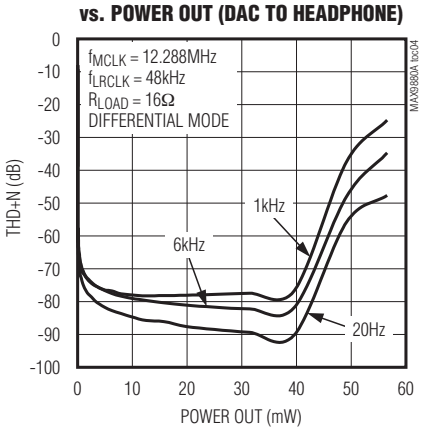
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



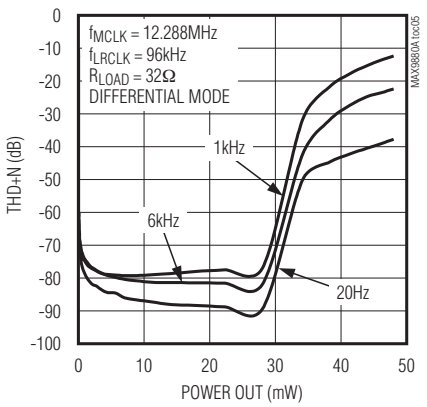
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



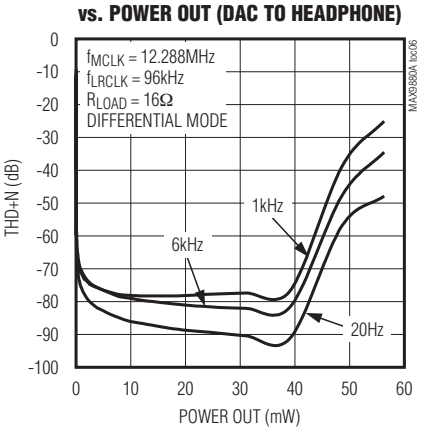
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



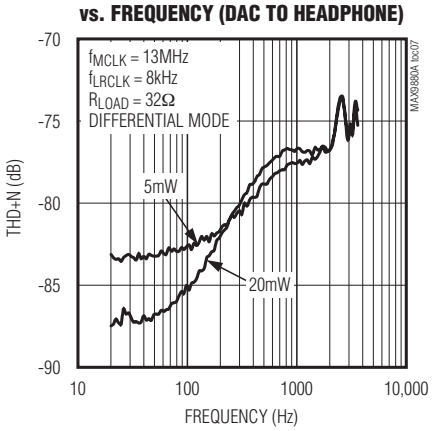
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



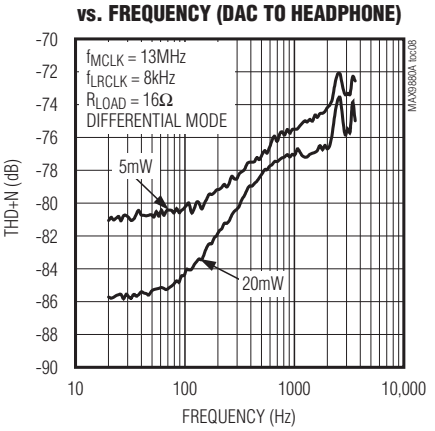
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



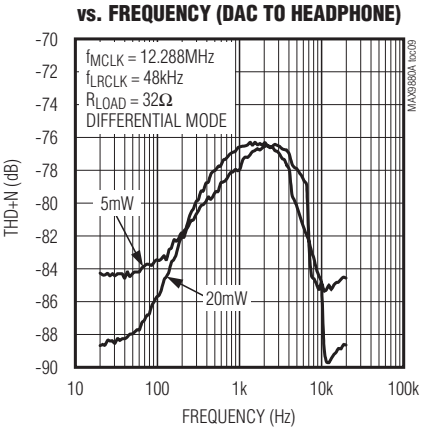
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)

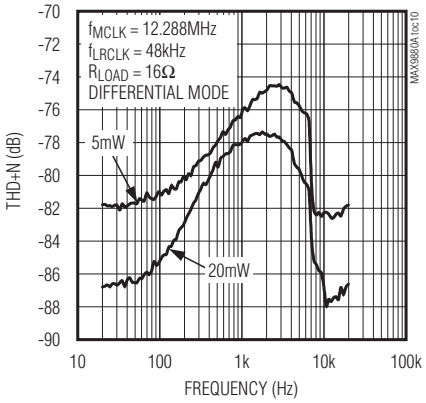


Low-Power, High-Performance Dual I²S Stereo Audio Codec

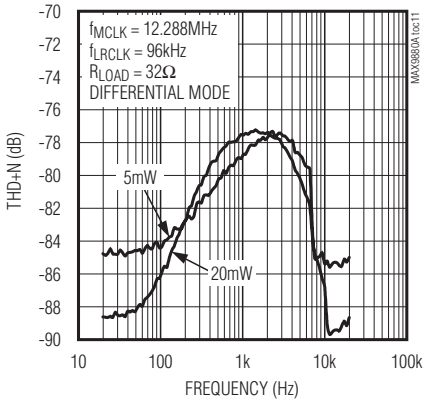
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

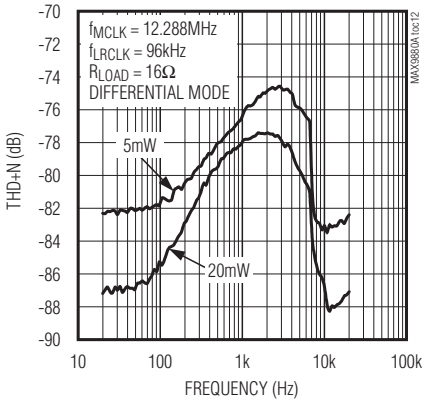
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



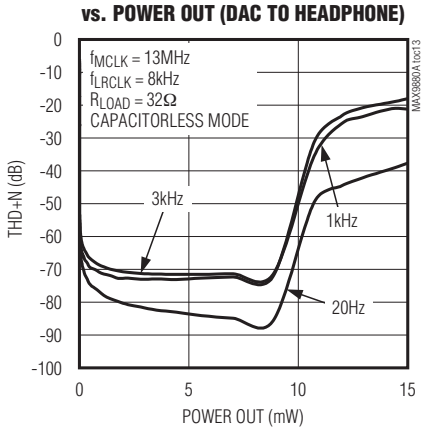
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



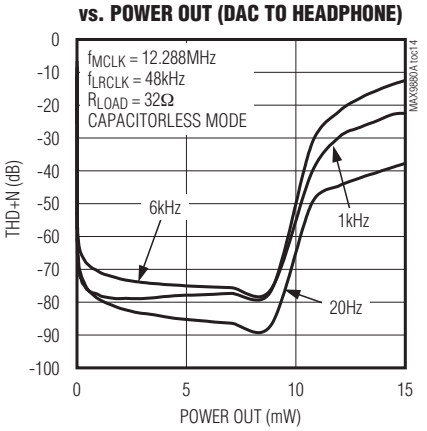
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



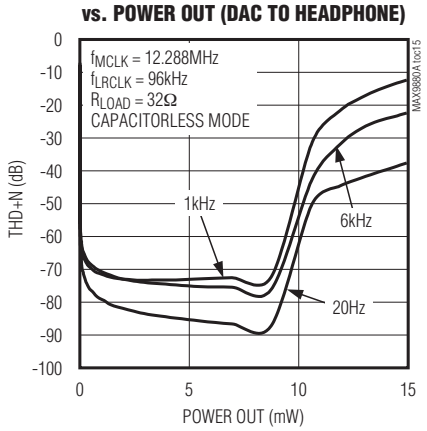
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



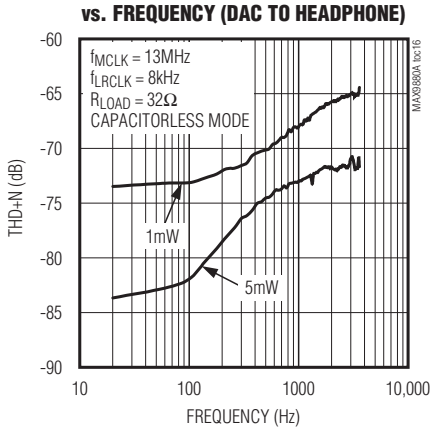
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



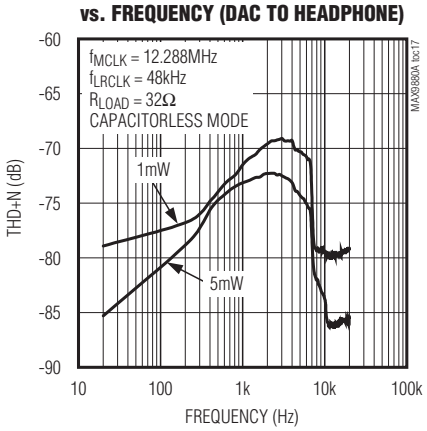
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



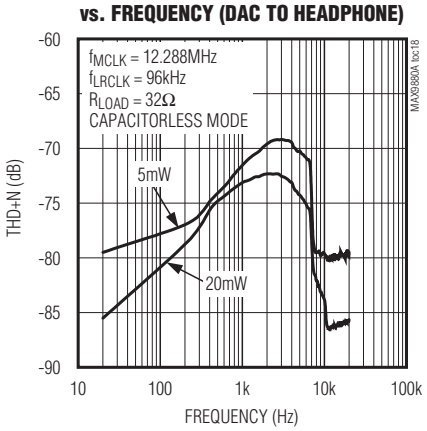
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



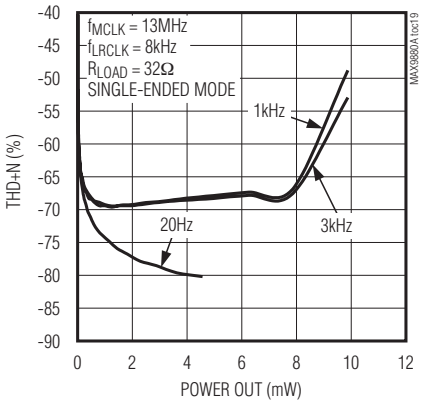
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



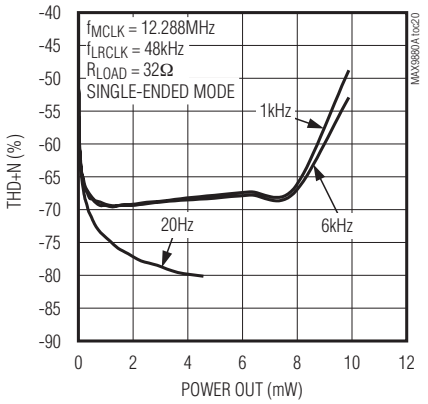
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

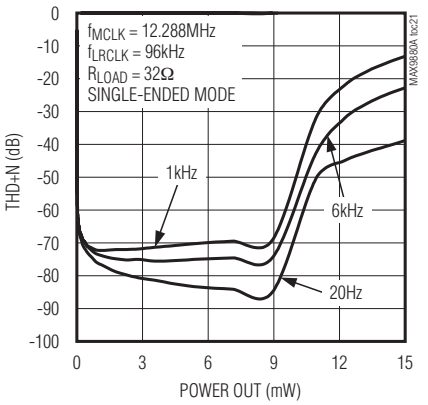
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



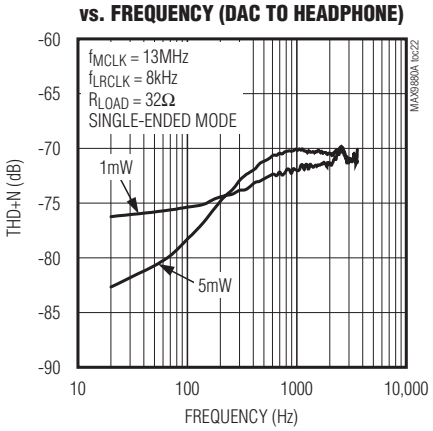
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



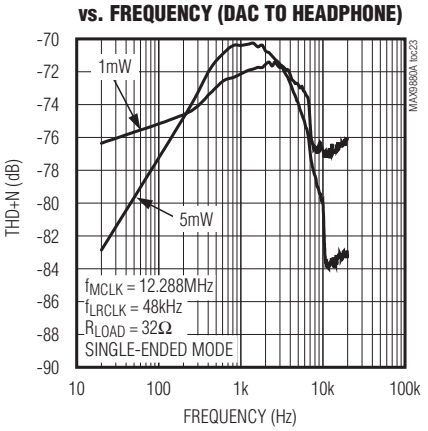
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



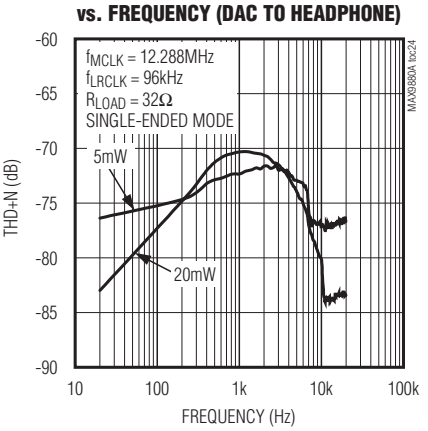
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



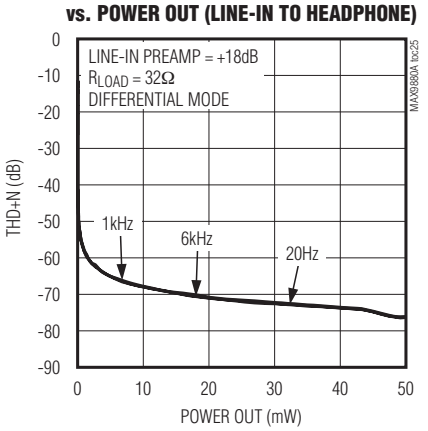
TOTAL HARMONIC DISTORTON + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



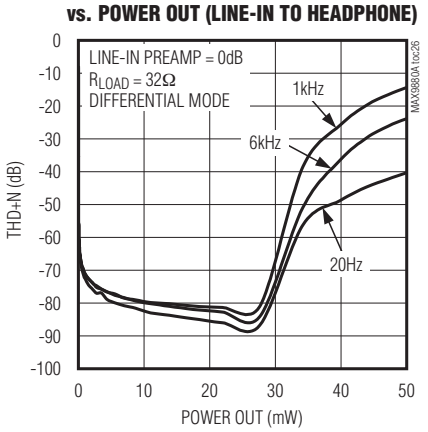
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



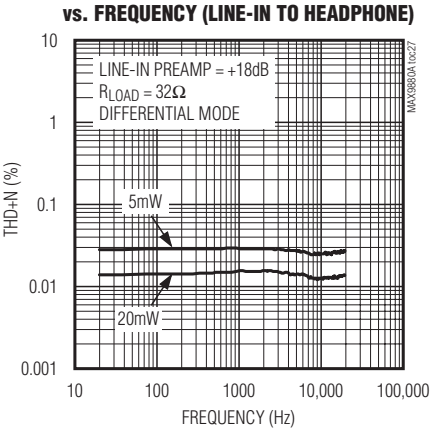
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE-IN TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE-IN TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE-IN TO HEADPHONE)

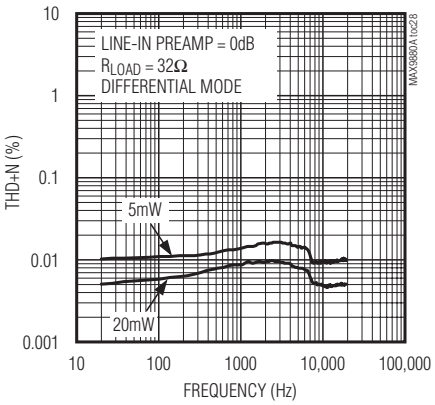


Low-Power, High-Performance Dual I²S Stereo Audio Codec

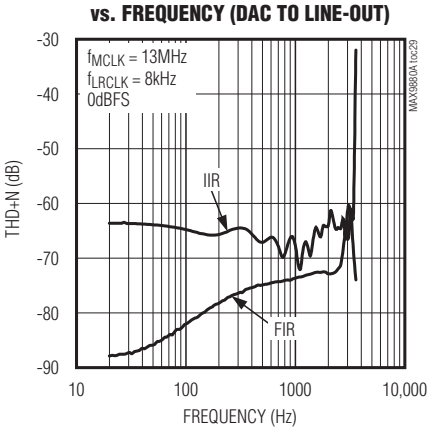
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

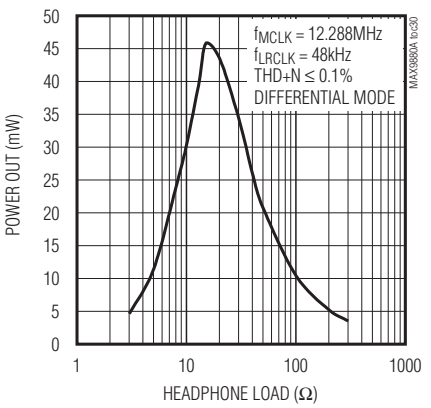
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE-IN TO HEADPHONE)



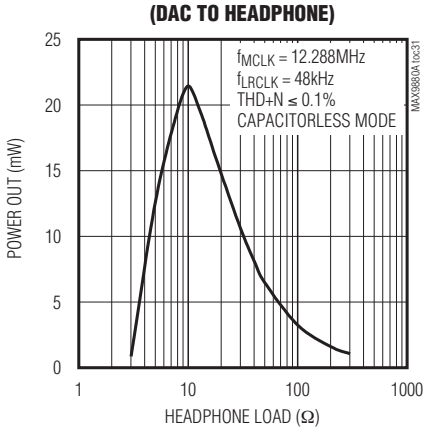
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO LINE-OUT)



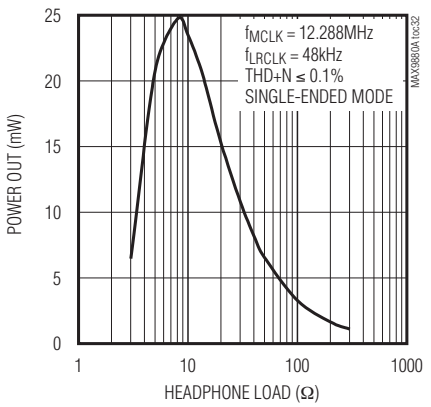
POWER OUT vs. HEADPHONE LOAD



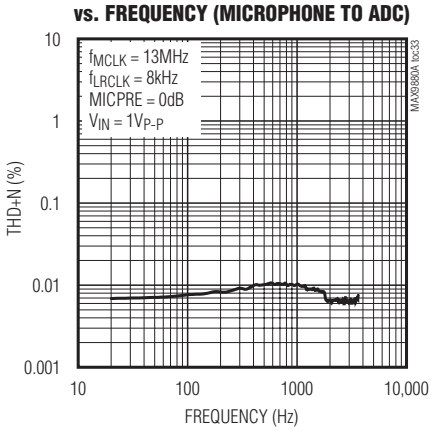
OUTPUT POWER vs. LOAD RESISTANCE (DAC TO HEADPHONE)



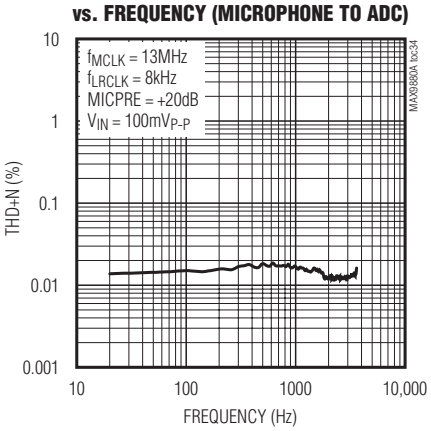
POWER OUT vs. HEADPHONE LOAD



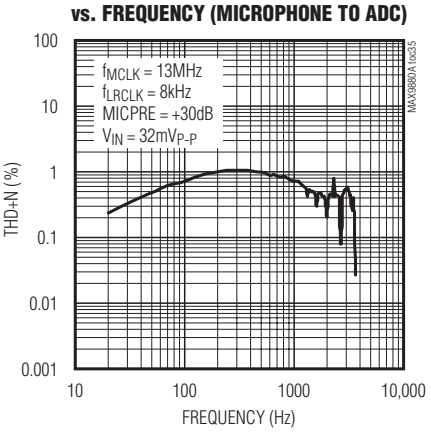
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



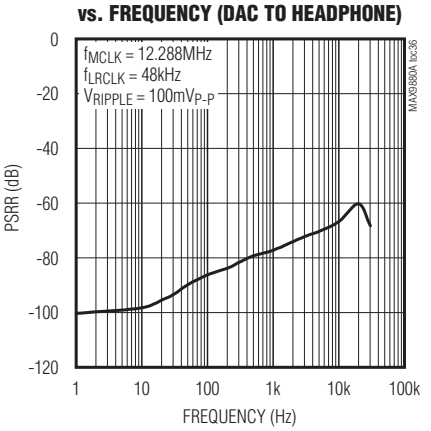
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



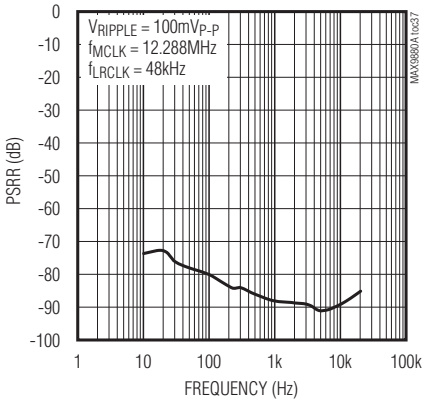
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



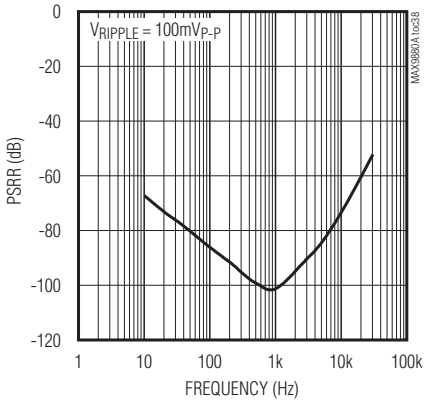
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

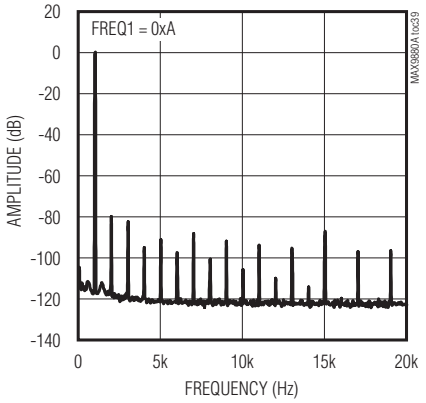
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICROPHONE TO ADC)



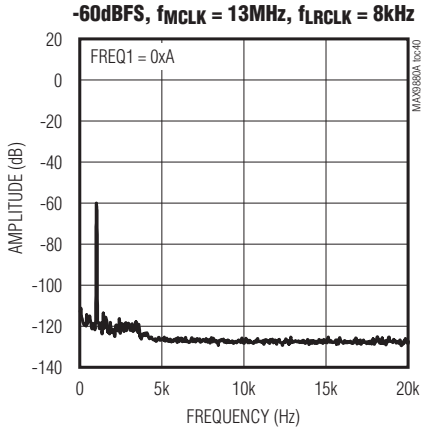
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICBIAS)



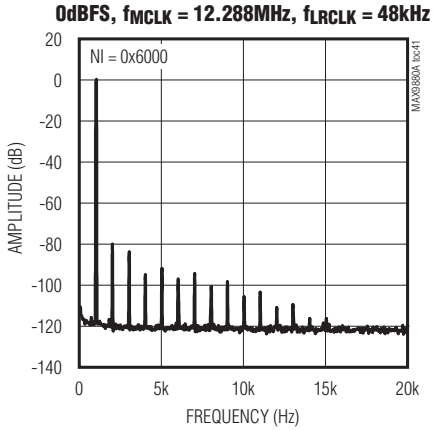
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



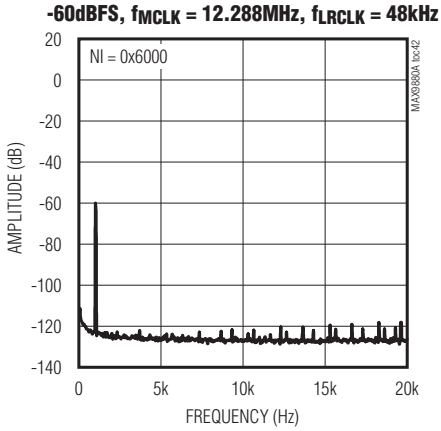
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



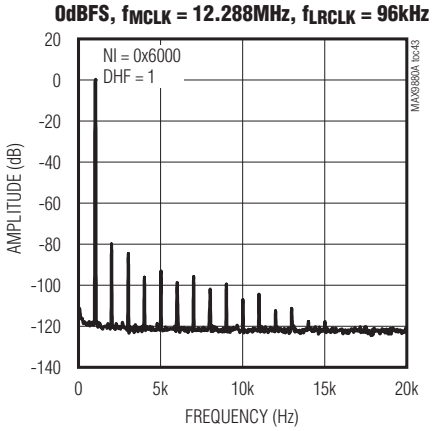
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



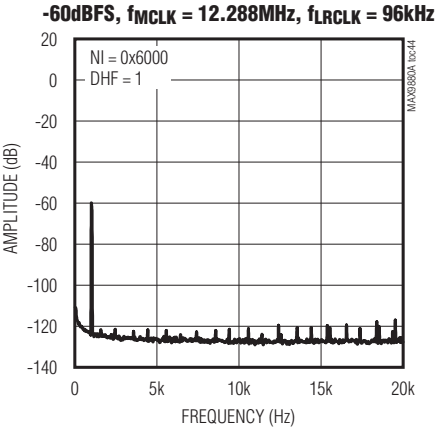
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



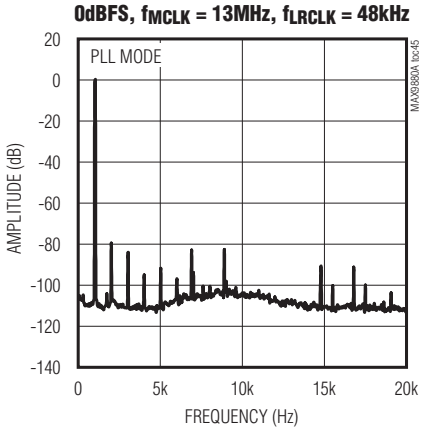
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 96kHz



FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 96kHz



FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



Low-Power, High-Performance Dual I²S Stereo Audio Codec

Typical Operating Characteristics (continued)

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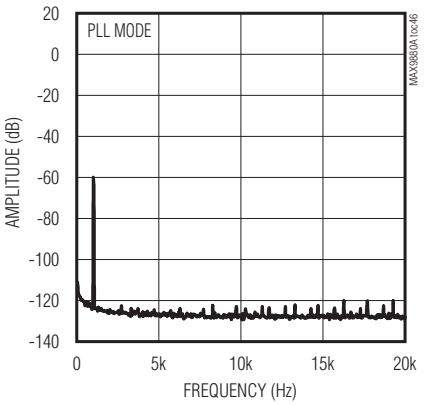
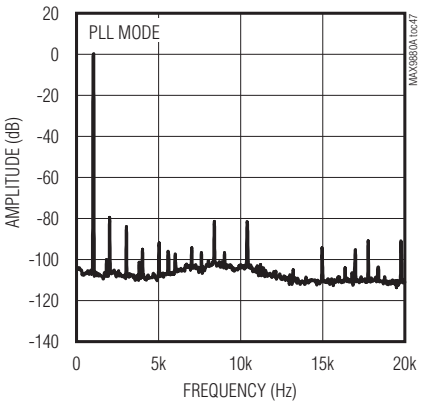
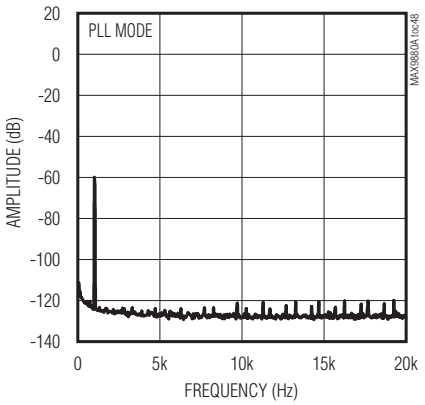
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



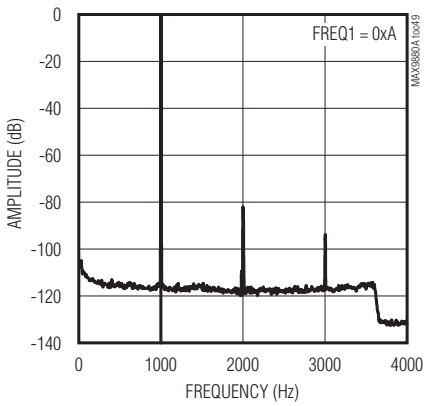
FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 44.1kHz



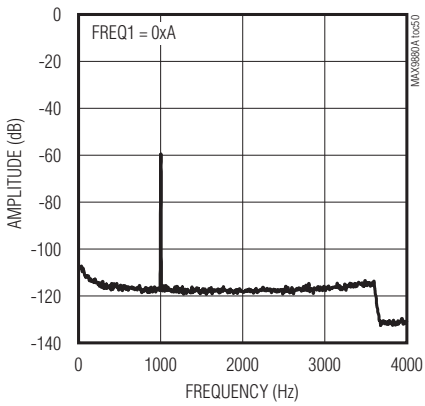
FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 44.1kHz



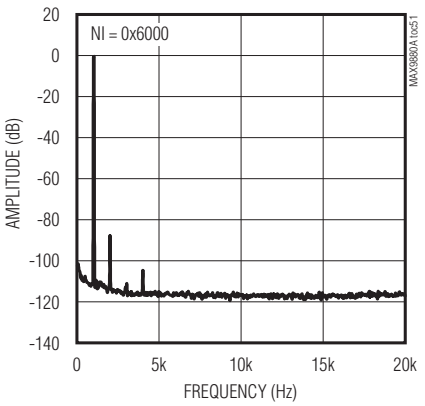
FFT, MICROPHONE TO ADC, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



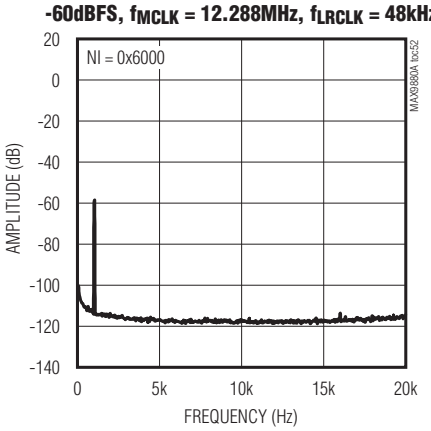
FFT, MICROPHONE TO ADC, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



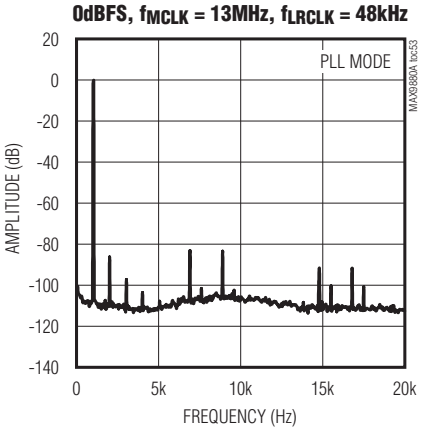
FFT, MICROPHONE TO ADC, 0dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



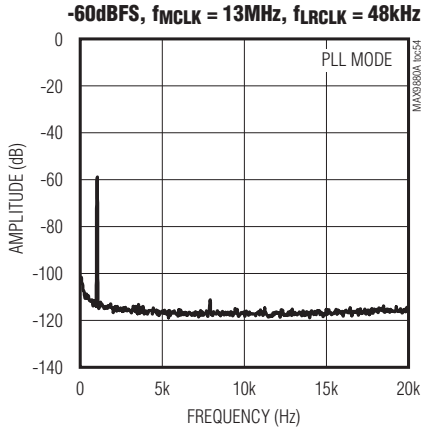
FFT, MICROPHONE TO ADC, -60dBFS, f_{MCLK} = 12.288MHz, f_{LRCLK} = 48kHz



FFT, MICROPHONE TO ADC, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



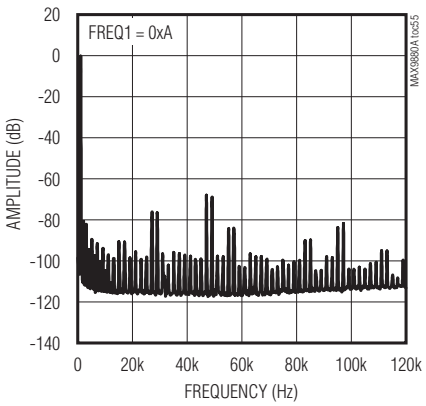
FFT, MICROPHONE TO ADC, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 48kHz



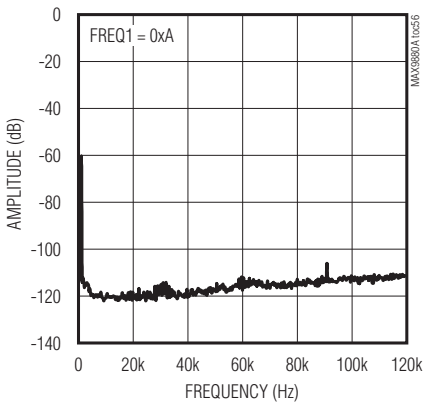
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

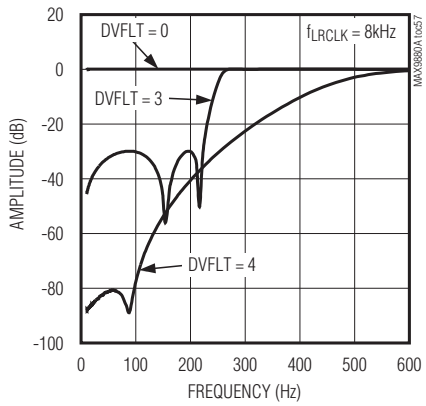
WIDEBAND FFT, DAC TO HEADPHONE, 0dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



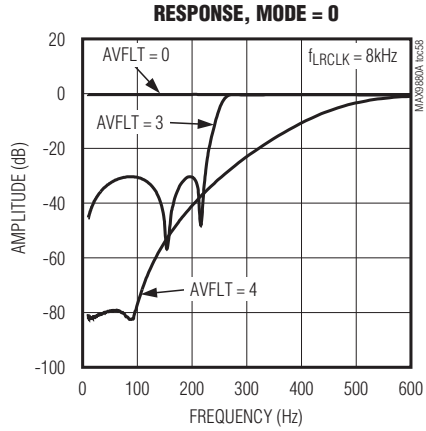
WIDEBAND FFT, DAC TO HEADPHONE, -60dBFS, f_{MCLK} = 13MHz, f_{LRCLK} = 8kHz



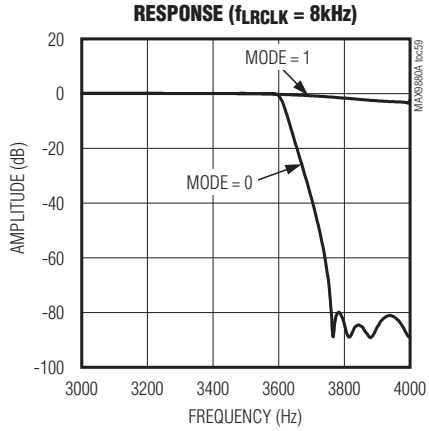
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



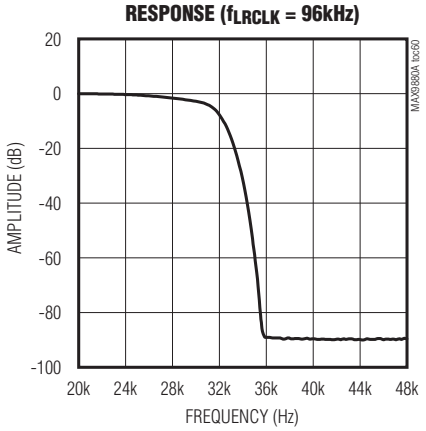
ADC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



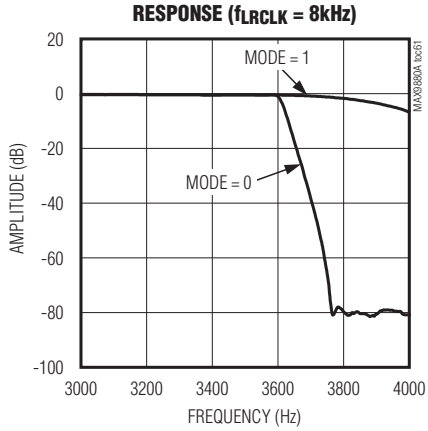
DAC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (f_{LRCLK} = 8kHz)



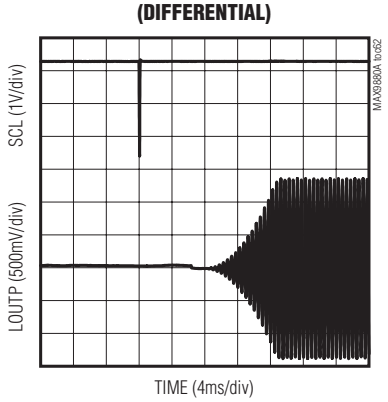
DAC FIR LOWPASS FILTER FREQUENCY RESPONSE (f_{LRCLK} = 96kHz)



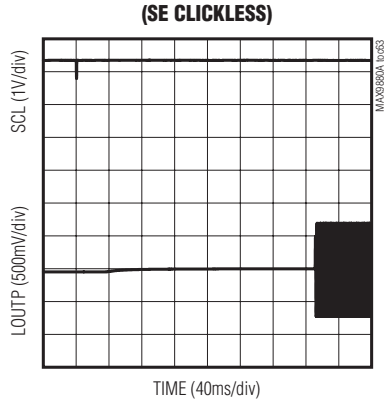
ADC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (f_{LRCLK} = 8kHz)



SHUTDOWN TO FULL OPERATION (DIFFERENTIAL)



SHUTDOWN TO FULL OPERATION (SE CLICKLESS)

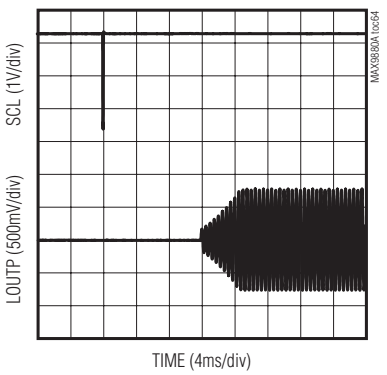


Low-Power, High-Performance Dual I²S Stereo Audio Codec

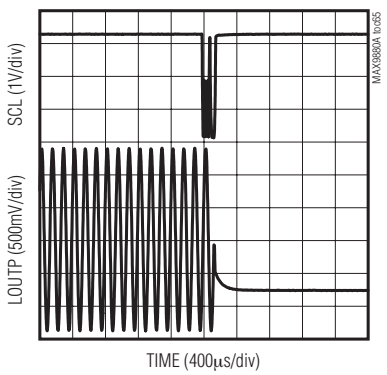
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{MICVDD} = V_{DVDD} = V_{DVDDS1} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, AV_{LO} = 0dB, f_{MCLK} = 13MHz, differential output, unless otherwise noted.)

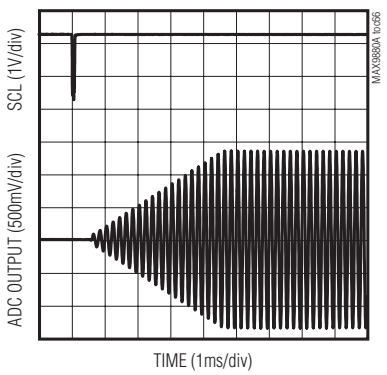
SHUTDOWN TO FULL OPERATION (SE FAST TURN ON)



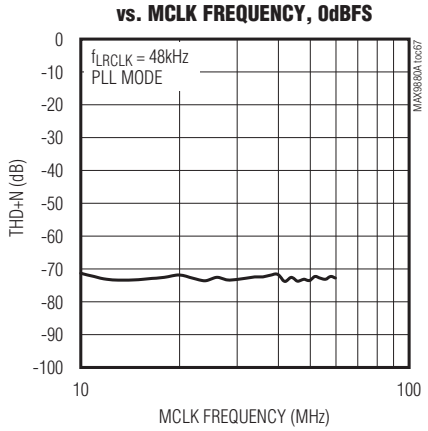
FULL OPERATION TO SHUTDOWN



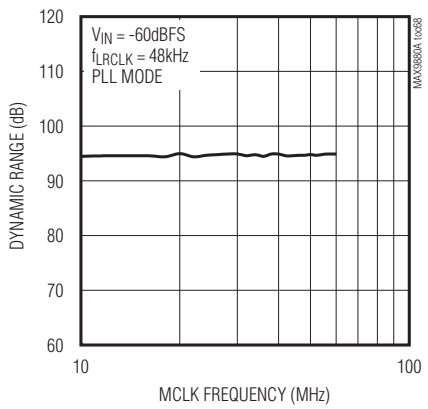
SOFT-START ADC



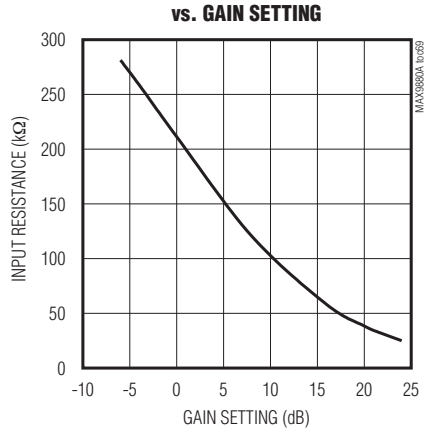
TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS



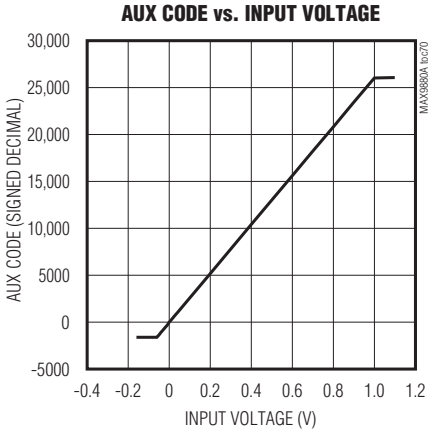
DYNAMIC RANGE vs. MCLK FREQUENCY



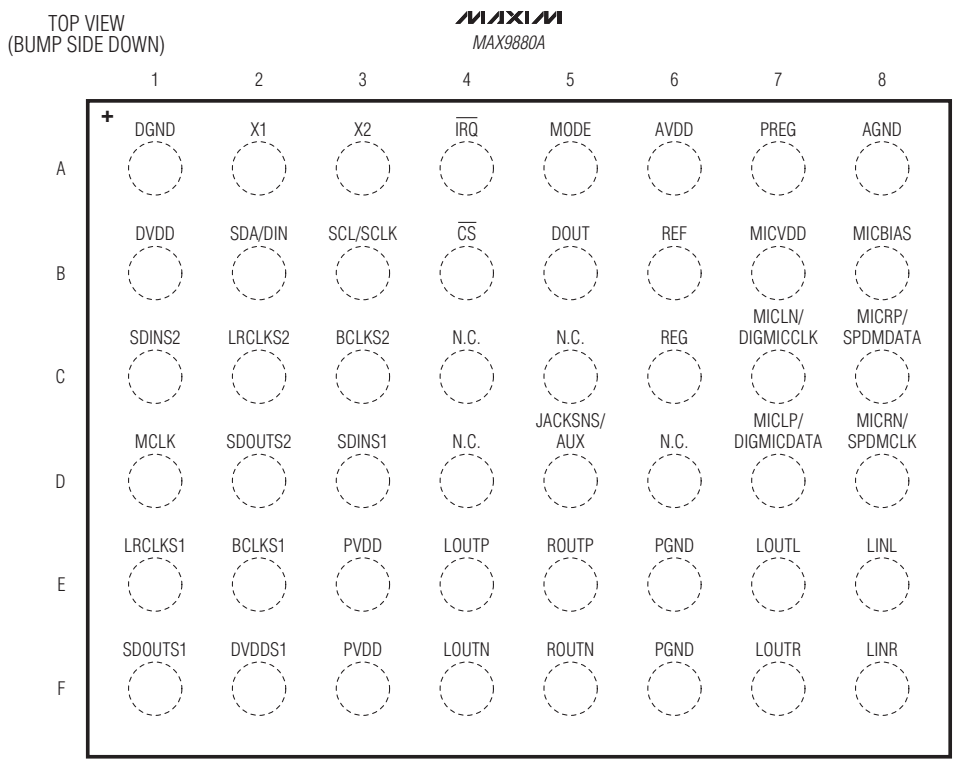
LINE INPUT RESISTANCE vs. GAIN SETTING



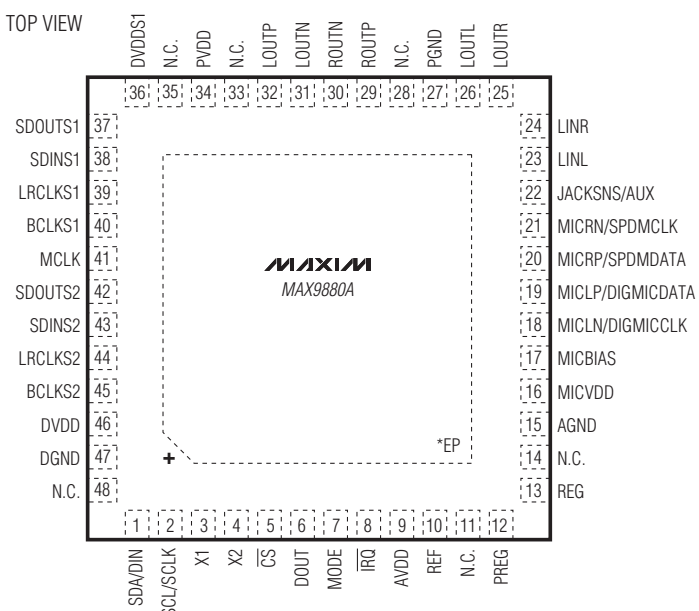
AUX CODE vs. INPUT VOLTAGE



Pin Configurations



WLP



THIN QFN
(6mm × 6mm)

*EP = EXPOSED PAD

Low-Power, High-Performance Dual I²S Stereo Audio Codec

Pin Description

PIN		NAME	FUNCTION
TQFN-EP	WLP		
1	B2	SDA/DIN	I²C Serial-Data Input/Output (MODE = 0). Connect a pullup resistor to DVDD for full output swing. SPI compatible serial-data input (MODE = 1).
2	B3	SCL/SCLK	I²C Serial-Clock Input (MODE = 0). Connect a pullup resistor to DVDD for full output swing. SPI-compatible serial clock input (MODE = 1).
3	A2	X1	Crystal Oscillator Input. Connect load capacitor and one terminal of the crystal to this pin. Acceptable input frequency range: 10MHz to 30MHz.
4	A3	X2	Crystal Oscillator Output. Connect load capacitor and second terminal of the crystal to this pin.
5	B4	$\overline{CS}$	SPI-Compatible, Active-Low Chip-Select Input
6	B5	DOUT	SPI-Compatible Serial-Data Output
7	A5	MODE	I²C/SPI Mode Select Input (MODE = 0 for I²C mode, MODE = 1 for SPI mode)
8	A4	$\overline{IRQ}$	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to go low when bits in the status register 0x00 are set. Read status register 0x00 to clear $\overline{IRQ}$ once set. Repeat faults have no effect on $\overline{IRQ}$ until it is cleared by reading the I²C status register 0x00. Connect a 10kΩ pullup resistor to DVDD for full output swing.
9	A6	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
10	B6	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor (1.23V nominal).
11, 14, 28, 33, 35, 48	C4, D4, C5, D6	N.C.	No Connection. Connect to GND.
12	A7	PREG	Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor (1.6V nominal).
13	C6	REG	PREG/2 Voltage Reference. Bypass to AGND with a 1µF capacitor (0.8V nominal)
15	A8	AGND	Analog Ground
16	B7	MICVDD	Microphone Bias Power Supply. Bypass to AGND with a 1µF capacitor.
17	B8	MICBIAS	Low-Noise Microphone Bias. Connect a 2.2kΩ to 470Ω resistor to the positive output of the microphone. Bypass to AGND with a 1µF capacitor.
18	C7	MICLN/ DIGMICCLK	Left Negative Differential Microphone Input. AC-couple a microphone with a series 1µF capacitor. Also digital microphone clock output. Selectable through I²C.
19	D7	MICLP/ DIGMICDATA	Left Positive Differential Microphone Input. AC-couple a microphone with a series 1µF capacitor. Also digital microphone data input. Selectable through I²C.
20	C8	MICRP/ SPDMDATA	Right Positive Differential Microphone Input or SPDM Data Output. AC-couple a microphone with a series 1µF capacitor. Selectable through I²C.
21	D8	MICRN/ SPDMCLK	Right Negative Differential Microphone Input or SPDM Clock Output. AC-couple a microphone with a series 1µF capacitor. Selectable through I²C.
22	D5	JACKSNS/AUX	Jack Sense. Detects the presence or absence of a jack. See the *Headset Detection* section. When used as an auxiliary ADC input, AUX is used to measure DC voltages.

Pin Description (continued)

PIN		NAME	FUNCTION
TQFN-EP	WLP		
23	E8	LINL	Left-Line Input. AC-couple analog audio signal to LINL with a 1µF capacitor.
24	F8	LINR	Right-Line Input. AC-couple analog audio signal to LINR with a 1µF capacitor.
25	F7	LOUTR	Right-Line Output
26	E7	LOUTL	Left-Line Output
27	E6, F6	PGND	Headphone Power Ground
29	E5	ROUTP	Positive Right-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
30	F5	ROUTN	Negative Right-Channel Headphone Output. Unused in capacitorless and single-ended mode.
31	F4	LOUTN	Negative Left-Channel Headphone Output. Common headphone return in capacitorless mode. Unused in single-ended mode.
32	E4	LOUTP	Positive Left-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
34	E3, F3	PVDD	Headphone Power Supply. Bypass to PGND with a 1µF capacitor.
36	F2	DVDDS1	S1 Digital Audio Interface Power-Supply Input. Bypass to DGND with a 1µF capacitor.
37	F1	SDOUTS1	S1 Digital Audio Serial-Data ADC Output
38	D3	SDINS1	S1 Digital Audio Serial-Data DAC Input
39	E1	LRCLKS1	S1 Digital Audio Left-Right Clock Input/Output. LRCLKS1 is the audio sample rate clock and determines whether the audio data on SDINS1 is routed to the left or right channel. In TDM mode, LRCLKS1 is a frame sync pulse. LRCLKS1 is an input when the MAX9880A is in slave mode and an output when in master mode.
40	E2	BCLKS1	S1 Digital Audio Bit Clock Input/Output. BCLKS1 is an input when the MAX9880A is in slave mode and an output when in master mode.
41	D1	MCLK	Master Clock Input. Acceptable input frequency range: 10MHz to 60MHz.
42	D2	SDOUTS2	S2 Digital Audio Serial-Data ADC Output
43	C1	SDINS2	S2 Digital Audio Serial-Data DAC Input
44	C2	LRCLKS2	S2 Digital Audio Left-Right Clock Input/Output. LRCLKS2 is the audio sample rate clock and determines whether the audio data on SDINS2 is routed to the left or right channel. In TDM mode, LRCLKS2 is a frame sync pulse. LRCLKS2 is an input when the MAX9880A is in slave mode and an output when in master mode.
45	C3	BCLKS2	S2 Digital Audio Bit Clock Input/Output. BCLKS2 is an input when the MAX9880A is in slave mode and an output when in master mode.
46	B1	DVDD	Digital Power Supply. Supply for the digital core and I²C/SPI interface. Bypass to DGND with a 1.0µF capacitor.
47	A1	DGND	Digital Ground
—	—	EP	Exposed Pad. Connect the exposed thermal pad to AGND.