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EVALUATION KIT AVAILABLE

25V Span, 800mA Device Power Supply (DPS)

MAX9959

General Description

The MAX9959 provides all the key features of a device power supply (DPS) common to automatic test equipment (ATE) and other instrumentation. Its small size, high level of integration, and superb flexibility make the MAX9959 ideal and economical for multisite systems requiring many device power supplies.

The MAX9959 has multiple input control voltages that allow independent setting of both the output voltage, and the maximum and minimum (smallest positive or most negative) voltage or current. The MAX9959 is a voltage source when the load current is between the two programmed limits, and transitions gracefully into a precision current source/sink if a programmed current limit is reached. The output features two independently adjustable voltage clamps that limit both the negative and positive output voltage values between levels externally provided.

The MAX9959 can source voltages spanning 25V and can source currents as high as ±800mA. The DPS can support an external buffer for sourcing and sinking higher currents. Multiple MAX9959s can be configured in parallel to load-share, allowing higher output currents with greater flexibility.

The MAX9959 features operation over a wide range of loading conditions. Programmability allows optimizing of settling time, over-/undershoot, and stability. Built-in, configurable, range-change glitch-control circuits minimize output glitches during range transitions.

The MAX9959 offers load regulation of 1mV at 800mA load.

The MAX9959D features an internal 300kΩ sense resistor (R_{FS}), between RCOMF and SENSE. The MAX9959F does not include this sense resistor. Both devices are available in the 100-pin TQFP package with an exposed pad on the top for heat removal.

Applications

Memory Testers

VLSI Testers

System-On-a-Chip Testers

Industrial Systems

Structural Testers

Features

- **25V Span Output Voltage**
- **Programmable Current and Voltage Compliance**
- **Programmable Current Ranges**
  - **±200µA**
  - **±2mA**
  - **±20mA**
  - **±800mA**
- **Load Regulation of 1mV at 800mA**
- **External Buffer Support for Higher Currents**
- **Parallel Multiple Devices for Higher Currents**
- **Programmable Gain Allows a Wide Range of DACs**
- **Device-Under-Test (DUT) Ground Sense**
- **Programmable Compensation for Wide Range of Loads**
- **Integrated Go/No-Go Comparators**
- **IDDQ Test Mode**
- **Range-Change Glitch Control**
- **Compact (14mm x 14mm) Package**
- **3-Wire Compatible Serial Interface**
- **Thermal Warning Flag and Thermal Shutdown**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9959DCCQ	0°C to +70°C	100 TQFP-EPR-IDP*
MAX9959DCCQ+	0°C to +70°C	100 TQFP-EPR-IDP*
MAX9959FCCQ+	0°C to +70°C	100 TQFP-EPR-IDP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EPR = Exposed pad. Inverted die pad.*

Pin Configuration appears at end of data sheet.

25V Span, 800mA Device Power Supply (DPS)

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} .... +31V
V_{CC} to AGND .... +20V
V_{EE} to AGND.. -15V
V_L to DGND .... +6V
AGND to DGND.. -0.5V to +0.5V
Digital Inputs .... -0.3V to (V_L + 0.3V)
All Other Pins .... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
100-Pin TQFP-EPR-IDP (derated at 166.7mW/°C above +70°C).. 13.33W
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow)
Lead(Pb)-Free Packages.. +260°C
Packages Containing Lead(Pb).. +240°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -12V, V_L = +3.3V, T_J = +30°C to +100°C. Typical values are at T_J = +30°C, unless otherwise specified.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE OUTPUT						
Output Voltage Range	V_{DUT}	DUT current below 10% of FSR current	V_{EE} + 2.5		V_{CC} - 2.5	V
		DUT current = +800mA, range A (Note 2)	0		+7	
		DUT current = -800mA, range A (Note 2)	-7		0	
		DUT current at full scale (I_{DUT} = 200µA, 2mA, 20mA, or 200mA)	V_{EE} + 5		V_{CC} - 5	
Output Offset	V_{OS}	V_{IN} = 0V, I_{OUT} = 0A (no load), gain = +1			±25	mV
Output-Voltage Temperature Coefficient	V_{OSTC}			±50		µV/°C
Voltage Gain Error	V_{GE}	Gain = +1			±1.25	%
		Gain = +2			±1.25	
		Gain = +6			±1.25	
		Gain = -1			±1.25	
		Gain = -2			±1.25	
		Gain = -6			±1.25	
Voltage-Gain Temperature Coefficient	V_{GETC}			±5		ppm/°C
Linearity Error	V_{LER}	Gain and offset errors calibrated out; I_{OUT} = 0 for ranges A, C, and D; ±20mA for range B; gain = +1 (Notes 3, 4, 5)			±0.02	%FSR
Off-State Leakage Current	$HIZF_{LK}$	RCOMF = (V_{CC} - 2.5V) to (V_{EE} + 2.5V)	-10		+10	nA
Force-to-Sense Resistor	R_{FS}	"D" option only		300		kΩ
DUT GROUND SENSE						
Voltage Range	ΔV_{DUTGND}	$V_{DUTGSNS}$ - V_{AGND}	±500	±700		mV
LOAD REGULATION (Note 6)						
Voltage	ΔV_{DUT}	Range A, gain = +1, V_{IN} = (V_{CC} - 5V) to (V_{EE} + 5V), ±800mA current load step (Note 5)		±1	±7	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -12V, V_L = +3.3V, T_J = +30°C to +100°C. Typical values are at T_J = +30°C, unless otherwise specified.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT OUTPUT						
Output Current Range	I_{DUT}	Range D, R_D = 5000Ω			±200	µA
		Range C, R_C = 500Ω			±2	mA
		Range B, R_B = 50Ω			±20	
		Range A, R_A = 1.25Ω			±800	
Input Voltage Range Corresponding to the Full-Scale Force Current	V_{INI}	IOSI = AGND	-4		+4	V
		V_{IOSI} = V_{AGND} + 4V	0		+8	
Current-Sense-Amp Offset Voltage Input	V_{IOSI}	Relative to AGND	-0.2		+4.4	V
Output Current Offset	I_{OS}	V_{RCOMF} = 0V (Note 4)		±0.1	±0.5	%FSR
Force-Current Offset Temperature Coefficient	I_{OSTC}			±20		ppm/°C
Gain Error	I_{GE}	V_{RCOMF} = 0V, I_{OUT} = ±FSR			±1.0	%
Forced-Current Gain Temperature Coefficient	I_{GETC}			±20		ppm/°C
Output Over Current-Limit Range (Note 4)	I_{OCL}	Range D, I_{OUT} = ±200µA	±135	±147	±158	%FSR
		Range C, I_{OUT} = ±2mA	±135	±147	±158	
		Range B, I_{OUT} = ±20mA	±135	±147	±158	
		Range A, I_{OUT} = ±800mA	±125	±138	±150	
Linearity Error	I_{LER}	Gain, offset, and CMR errors calibrated out; V_{IOSI} = -0.2V and +4.4V; ranges B, C, and D (Notes 4, 5, 7)			±0.02	%FSR
Rejection of Output Error Due to Common-Mode Load Voltage	CMR_{OER}	Range D, I_{OUT} = 0, V_{RCOMF} = (V_{EE} + 2.5V) and (V_{CC} - 2.5V), measured across R_D		0.001	0.005	%FSR/V
CURRENT MONITOR						
Measured Current Range	I_{DUTM}	Range D		±200		µA
		Range C		±2		mA
		Range B		±20		
		Range A		±800		
Current-Sense-Amp Voltage Range	V_{ISENSE}	IOSI = AGND	-4		+4	V
		V_{IOSI} = V_{AGND} + 4V	0		+8	
Current-Sense-Amp Offset Voltage Input	V_{IOSI}	Relative to AGND	-0.2		+4.4	V
Current-Sense-Amp Offset	I_{MOS}	V_{RCOMF} = 0V (Note 4)		±0.1	±0.5	%FSR
Measured-Current Offset Temperature Coefficient	I_{MOSTC}			±20		ppm/°C
Gain Error	I_{MGE}	V_{RCOMF} = 0V, I_{OUT} = ±FSR			±1	%

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -12V, V_L = +3.3V, T_J = +30°C to +100°C. Typical values are at T_J = +30°C, unless otherwise specified.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Measured-Current Gain Temperature Coefficient	I_{MGETC}			±20		ppm/°C
Linearity Error	I_{MLER}	Gain, offset, and CMR errors calibrated out; V_{IOSI} = -0.2V and +4.4V, range B (Notes 4, 5)			±0.02	%FSR
Rejection of Output Error Due to Common-Mode Load Voltage	CMR_{MOER}	Range D, I_{OUT} = 0A, V_{RCOMF} = (V_{EE} + 2.5V) and (V_{CC} - 2.5V)		0.001	0.005	%FSR/V
VOLTAGE MONITOR						
Measured Output Voltage Range	V_{DUTM}	Gain = +1, IOSV = AGND	V_{EE} + 2.5		V_{CC} - 2.5	V
Voltage-Sense-Amp Offset Voltage Input	V_{IOSV}	Relative to AGND	-0.2		+4.4	V
Voltage-Sense-Amp Offset	V_{DUTMOS}	Gain = +1			±25	mV
Measured Voltage Offset Temperature Coefficient	$V_{DUTMOSTC}$			±10		µV/°C
Voltage-Sense-Amp Gain Error	V_{DUTGE}	Gain = +1			±1	%
		Gain = +1/2			±1	
		Gain = +1/6			±1	
Measured-Voltage Gain Temperature Coefficient	$V_{DUTGETC}$			±10		ppm/°C
Linearity Error	V_{DUTLER}	Gain and offset errors calibrated out, V_{IOSV} = -0.2V and +4.4V, I_{OUT} = 0A, gain = +1, range B (Note 4)			±0.02	%FSR
VOLTAGE/CURRENT CLAMPS (Note 8)						
Input Control Voltage	V_{CLLO}, V_{CLHI}		V_{EE} + 2.3		V_{CC} - 2.3	V
Voltage Clamp Range (Note 9)	VC_{RNG}	DPS output current ≤ 10% of FSR	V_{EE} + 2.5		V_{CC} - 2.5	V
		DPS output current at FSR	V_{EE} + 5		V_{CC} - 5	
Voltage Clamp Gain	VC_{GAIN}			+1		V/V
Voltage Clamp Accuracy (Notes 2, 9)	VC_{ERR}	Range A to D, I_{OUT} ≤ 10% of FSR			±200	mV
		Range A to D, I_{OUT} = ±FSR			±200	
Current Clamp Range	IC_{RNG}	(Note 10)		V_{IOSI} ±1.5 x FSR		V
Current Clamp Gain	IC_{GAIN}			4		V/FSR
Current Clamp Accuracy	IC_{ERR}	Range A, V_{OUT} = ±FSR, I_{OUT} = ±FSR (Notes 2, 10)			±0.15	%FSR
		Range B to D, V_{OUT} = ±FSR, gain and offset errors calibrated out (Note 10)			±0.05	
COMPARATOR INPUTS						
Input Voltage Range	CMP_{IRG}		V_{EE} + 3.5		V_{CC} - 3.5	V
Input Offset Voltage	CMP_{IOS}	V_{ITHHI} = V_{ITHLO} = 0V			±30	mV

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -12V, V_L = +3.3V, T_J = +30°C to +100°C. Typical values are at T_J = +30°C, unless otherwise specified.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATOR OUTPUTS						
Output High Voltage	CMP_{OH}	V_L = 2.375V to 3.3V, R_{PULLUP} = 1kΩ	V_L - 0.2			V
Output Low Voltage	CMP_{OL}	V_L = 2.375V to 3.3V, R_{PULLUP} = 1kΩ			0.4	V
High-Impedance State Leakage Current	CMP_{OLK}			±5		nA
High-Impedance Output Capacitance	CMP_{OC}			1		pF
ANALOG INPUTS						
Input Current	I_{IN}			±5		nA
Input Capacitance	C_{IN}			4		pF
DIGITAL INPUTS						
Input High Voltage	V_{IH}		V_{THR} + 0.15			V
Input Low Voltage	V_{IL}				V_{THR} - 0.15	V
VTHR Input Range	V_{THR}		0.5		V_L - 0.5	V
Input Current	I_{IN}			±25		µA
Input Capacitance	C_{IN}			4		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	V_L = 2.375V to 3.3V, relative to DGND, I_{OUT} = +1.0mA	V_L - 0.25			V
Output Low Voltage	V_{OL}	V_L = 2.375V to 3.3V, relative to DGND, I_{OUT} = -1.0mA			0.2	V
TEMPERATURE SENSOR						
Analog Output Offset	V_{TSNSO}	T_J = +28°C		3.01		V
Analog Output Gain	V_{TSNSG}			10		mV/°C
Digital Output Temperature Threshold	T_{TSNSR}	(Note 11)		+130		°C
Thermal-Shutdown Temperature	T_{SDN}			+140		°C
POWER SUPPLY						
Positive Supply	V_{CC}	(Note 12)	12		18	V
Negative Supply	V_{EE}	(Note 12)	-15		-12	V
Total Supply Voltage	V_{CC} - V_{EE}				+30	V
Logic Supply	V_L		+2.375		+3.300	V
Positive Supply Current	I_{CC}	No load		20	22	mA
Negative Supply Current	I_{EE}	No load		19	21	mA
Analog Ground Current	I_{AGND}	No load		0.8	1.0	mA
Logic Supply Current	I_L	No load, all digital inputs at DGND		7.0	9.0	mA
Digital Ground Current	I_{DGND}	No load, all digital inputs at DGND		7.0	9.0	mA
Power-Supply Rejection Ratio	PSRR	Each supply varied individually from min to max, V_{DUT} = 5.0V		80		dB

25V Span, 800mA Device Power Supply (DPS)

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +12V, V_{EE} = -12V, V_L = +3.3V, C_{C1} = 350pF, C_L = 100pF, C_{MEAS} = 100pF, C_{IMEAS} = 100pF, T_J = +30°C to +100°C. Typical values are at T_J = +35°C, unless otherwise specified.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FORCE VOLTAGE (Notes 13, 14)						
Settling Time	FV_{ST}	Range D = ±200µA, R_L = 35kΩ to AGND		30		µs
		Range C = ±2mA, R_L = 3.5kΩ to AGND		20		
		Range B = ±20mA, R_L = 350Ω to AGND		30	50	
		Range A = ±800mA, R_L = 8.75Ω to AGND		25		
LOAD REGULATION SETTLING TIME (Note 14)						
Settling Time	LR_{ST}	Range A, V_{IN} = ±7V, R_L = 8.75Ω switched between open circuit to AGND, C_L = 10µF		100		µs
FORCE VOLTAGE/MEASURE CURRENT (Notes 13, 14, 15)						
Settling Time	$FVMI_{ST}$	Range D = ±200µA, R_L = 35kΩ to AGND		50		µs
		Range C = ±2mA, R_L = 3.5kΩ to AGND		20		
		Range B = ±20mA, R_L = 350Ω to AGND		25	50	
		Range A = ±800mA, R_L = 8.75Ω to AGND		35		
FORCE CURRENT (Notes 13, 14)						
Settling Time	FI_{ST}	Range D = ±200µA, R_L = 35kΩ to AGND		100		µs
		Range C = ±2mA, R_L = 3.5kΩ to AGND		35		
		Range B = ±20mA, R_L = 350Ω to AGND		25	50	
		Range A = ±800mA, R_L = 8.75Ω to AGND		20		
FORCE CURRENT/MEASURE VOLTAGE (Notes 13, 14, 15)						
Settling Time	$FIMV_{ST}$	Range D = ±200µA, R_L = 35kΩ to AGND		100		µs
		Range C = ±2mA, R_L = 3.5kΩ to AGND		35		
		Range B = ±20mA, R_L = 350Ω to AGND		25	50	
		Range A = ±800mA, R_L = 8.75Ω to AGND		40		
FORCE OUTPUT						
Output Slew Rate	FO_{SLEW}	C_L = 0F (Note 16)	0.7		2.1	V/µs
Stable Load Capacitance Range	FO_{SLC}	(Notes 17, 18)			1000	µF
Output Overshoot	FO_{OSHT}	C_L < 20µF, CB1 = 3nF		0		%
MEASURE OUTPUT						
Stable Load Capacitance Range	MO_{SLC}	(Note 17)			1000	pF
COMPARATORS ($C_{ILIMHI/ILIMLO}$ = 20pF, R_{PULLUP} = 1kΩ) (Note 19)						
Propagation Delay	CMP_{PD}	100mV overdrive, $1V_{P-P}$, measured from input threshold zero crossing to 50% of output voltage		100		ns
Rise Time	CMP_{TR}	20% to 80%		80		ns
Fall Time	CMP_{TF}	20% to 80%		5		ns
Disable True to High Impedance	CMP_{HIZT}	Measured from 50% of digital input voltage to 10% of output voltage		100		ns
Disable False to Active	CMP_{HIZF}	Measured from 50% of digital input voltage to 90% of output voltage		100		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +12V, V_{EE} = -12V, V_L = +3.3V, C_{C1} = 350pF, C_L = 100pF, C_{MEAS} = 100pF, C_{IMEAS} = 100pF, T_J = +30°C to +100°C. Typical values are at T_J = +35°C, unless otherwise specified.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL PORT TIMING CHARACTERISTICS (V_L = 3.0V, C_{DOUT} = 10pF) (Figure 4)						
Serial Clock Frequency	f_{SCLK}				20	MHz
SCLK Pulse-Width High	t_{CH}		12			ns
SCLK Pulse-Width Low	t_{CL}		12			ns
SCLK Fall to DOUT Valid	t_{DO}				25	ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		10			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		22			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}	(Note 17)	0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		5			ns
DIN to SCLK High Setup	t_{DS}		10			ns
DIN to SCLK High Hold	t_{DH}		0			ns
$\overline{CS}$ Pulse-Width High	t_{CSWH}		10			ns
$\overline{CS}$ Pulse-Width Low	t_{CSWL}		10			ns
$\overline{LOAD}$ Pulse-Width Low	t_{CLL}		20			ns
Power-On Reset	POR			50		µs

Note 1: All minimum and maximum test limits are 100% production tested at T_J = +35°C ±15°C at nominal supplies. Specifications over the full operating temperature range are guaranteed by design and characterization.

Note 2: Exercise care not to exceed the maximum power dissipation specifications listed in the *Absolute Maximum Ratings* section. With drive current of ±800mA limit DPS operation to two quadrants (i.e., when sourcing current limit V_{DUT} to below +7V, when sinking current limit V_{DUT} to above -7V). With drive current below ±800mA and four-quadrant operation, limit DPS power dissipation to below the allowed maximum.

Note 3: VIN swept to achieve an output voltage of (V_{EE} + 2.5V) to (V_{CC} - 2.5V), with I_{OUT} = 0.

Note 4: Parameters expressed in terms of %FSR (percent of full-scale range) are as a percent of the end-point-to-end-point range.

Note 5: Case must be maintained to within ±5°C for linearity specifications to apply.

Note 6: Load regulation is defined at a single programmed output voltage (force voltage mode), independent of linearity specification, with a 0 to 100% current step.

Note 7: To maintain linearity, keep the clamps at least 700mV away from V_{RCOMF}.

Note 8: In the force-current and force-voltage modes, the reference-clamping voltage CLH must be greater than 0V, and CLL must be less than 0V. For high clamping accuracy, CLH-CLL is > 1V. To maintain 0.02% force-voltage linearity when the programmable current clamps are enabled, two conditions must be met: 1) CLH and CLL must be set 12.5% FSR higher than the forced current and 2) CLH and CLL must be set such that CLH is ≥ 1.6V + IOSI and CLL is ≤ -1.6V + IOSI (e.g., if driving ±1mA in the 2mA range, the current clamps must be set to a minimum of ±1.5mA, or CLH = 3V, CLL = -3V, and IOSI = 0V).

Note 9: DPS in force current mode.

Note 10: DPS in force voltage mode.

Note 11: The temperature threshold may vary up to ±10°C from the specified threshold.

Note 12: The device operates properly within absolute specifications, for varying supply voltages with equally varying output voltage settings.

Note 13: Settling times are for a full-scale voltage or current step. FV_{ST} measured from VIN to VDUT, $FVMI_{ST}$ from VIN to IMEAS, FI_{ST} from VIN to VDUT, and $FIMV_{ST}$ from VIN to VMEAS.

Note 14: Settling times are to 0.1% of FSR.

Note 15: The actual settling time of the measure path (sense input to measure output) is less than 1µs. However, the RC time constant of the sense resistor and the load capacitance causes a longer overall settling time of VDUT. This settling time is a function of the current range resistor.

Note 16: Slew rate is measured from the 20% to 80% points.

Note 17: Guaranteed by design and characterization.

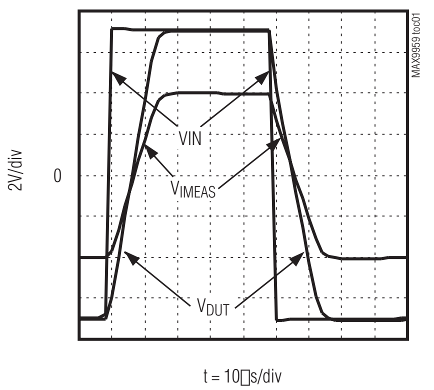
Note 18: Range A.

Note 19: The propagation delay time is measured by holding the current constant, and transitioning ITHHI or ITHLO.

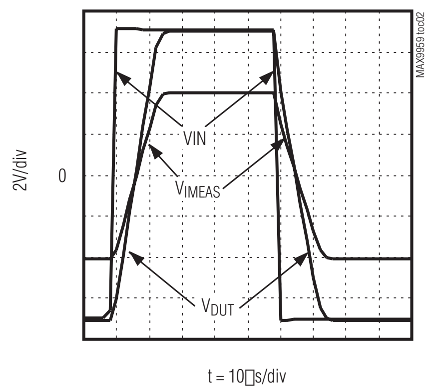
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

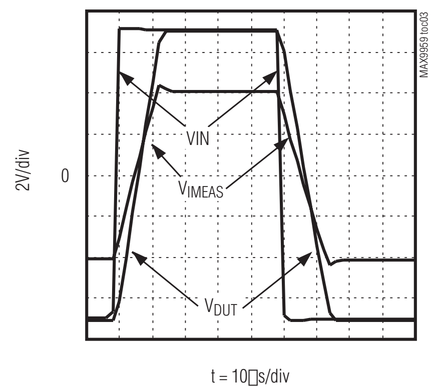
TRANSIENT RESPONSE FVMI MODE, RANGE A



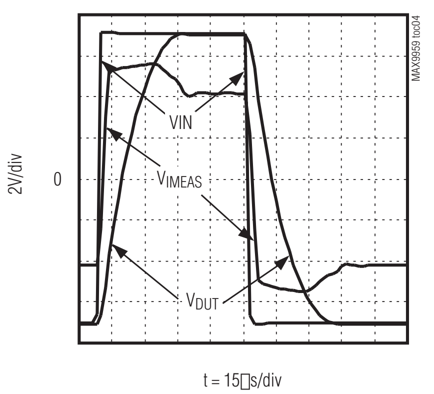
TRANSIENT RESPONSE FVMI MODE, RANGE B



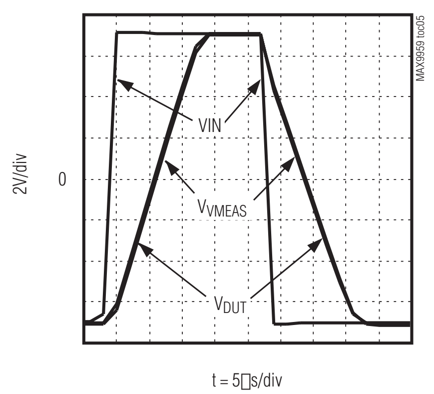
TRANSIENT RESPONSE FVMI MODE, RANGE C



TRANSIENT RESPONSE FVMI MODE, RANGE D



TRANSIENT RESPONSE FVMV MODE, RANGE C



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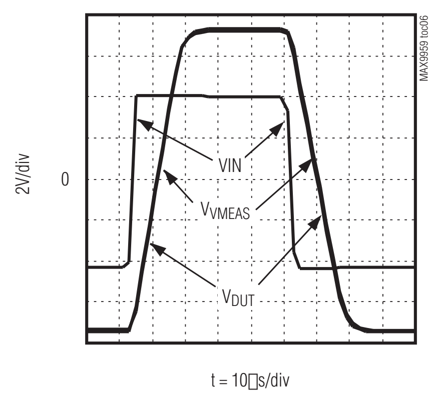
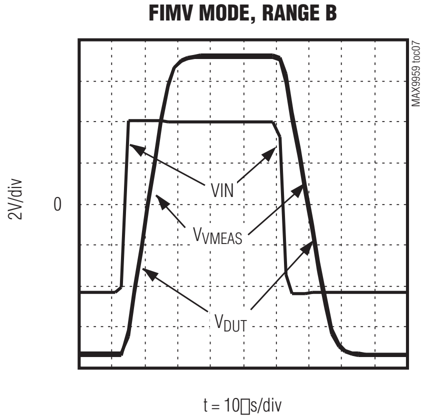
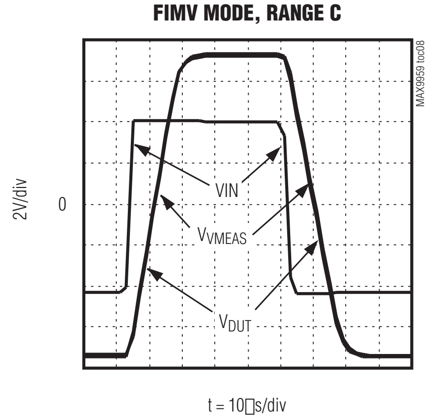


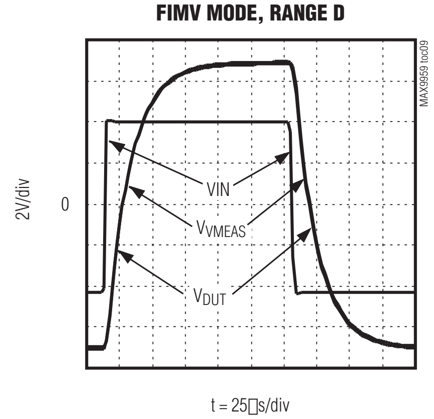
TRANSIENT RESPONSE FIMV MODE, RANGE B



TRANSIENT RESPONSE FIMV MODE, RANGE C



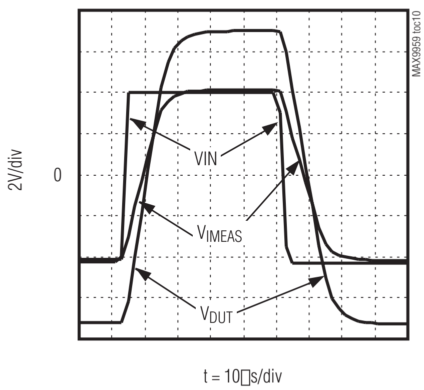
TRANSIENT RESPONSE FIMV MODE, RANGE D



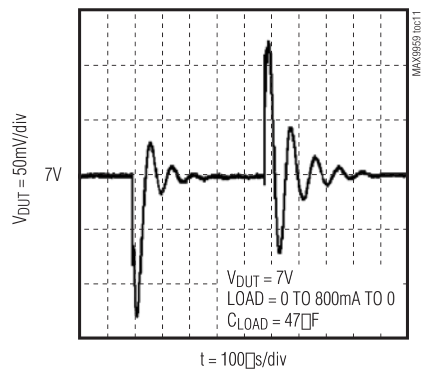
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

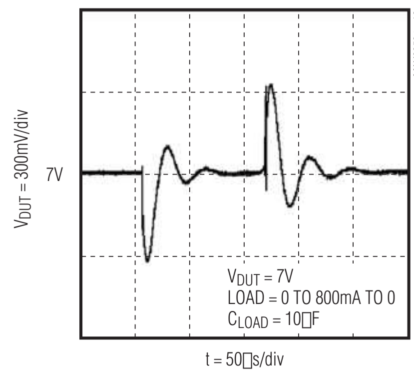
TRANSIENT RESPONSE FIMI MODE, RANGE C



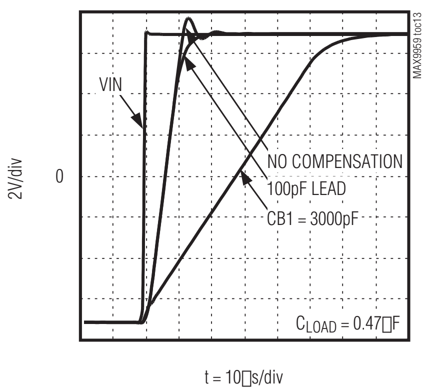
LOAD REGULATION TRANSIENT RECOVERY



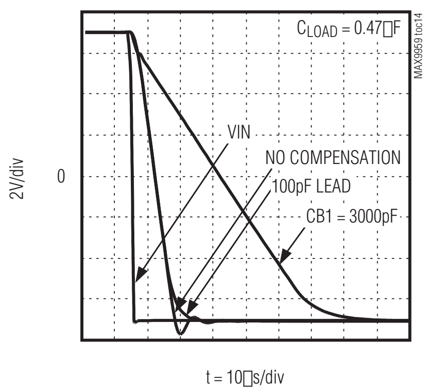
LOAD REGULATION TRANSIENT RECOVERY



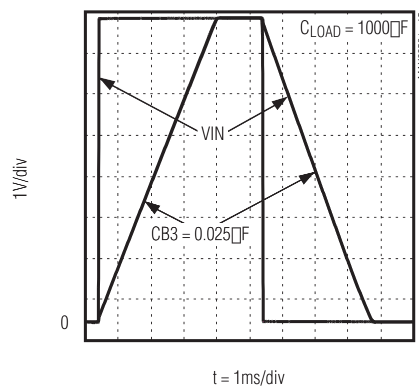
RESPONSE TO CAPACITIVE LOAD RISING EDGE



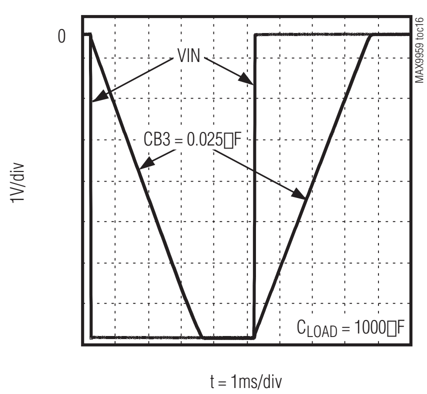
RESPONSE TO CAPACITIVE LOAD FALLING EDGE



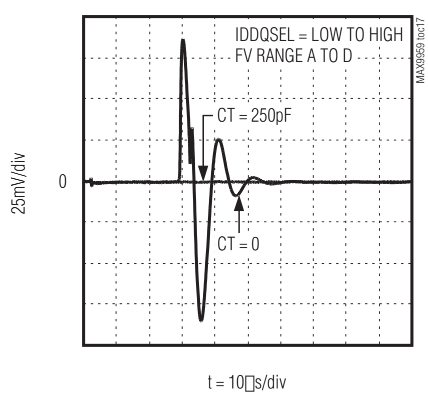
RESPONSE TO CAPACITIVE LOAD POSITIVE SIGNAL



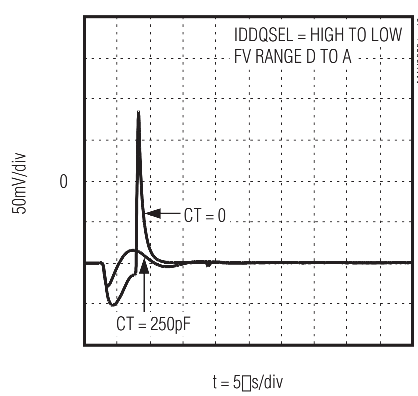
RESPONSE TO CAPACITIVE LOAD NEGATIVE SIGNAL



RANGE-CHANGE GLITCH



RANGE-CHANGE GLITCH



Pin Description

PIN	NAME	FUNCTION
1–8	RA	Range A Outputs. Connect together and to a range-setting resistor.
9	BIFRCA	Positive Current-Sense-Amplifier Input. Used in range A to provide a Kelvin connection to range-setting resistor.
10	RB	Range B Output. Connect to a range-setting resistor.
11	BIFRCB	Positive Current-Sense-Amplifier Input. Used in range B to provide a Kelvin connection to range-setting resistor.
12	RC	Range C Output. Connect to a range-setting resistor.
13	RD	Range D Output. Connect to a range-setting resistor.
14	RCOMF	Sense Resistors Kelvin Connection. The Kelvin connection for the sense resistors that connect to the DUT. RCOMF provides a feedback point for current sensing.
15	SENSE	Sense Input. Kelvin connection to the DUT. Provides the feedback signal for FVMI and the measured signal for FIMV.
16	DUTGSNS	DUT Ground Sense. In force voltage mode, senses the error between AGND and DUTGND and adjusts the output voltage to achieve the desired voltage drop across the DUT with respect to DUTGND.
17, 18, 25, 49, 77–84, 93, 99	V_{CC}	Positive Analog Supply
19, 20, 26, 50, 76, 85–92, 95, 100	V_{EE}	Negative Analog Supply
21	VRXP	Positive Current-Sense-Amplifier Input. Used in the external range to provide a Kelvin connection to the range-setting resistor.
22	VRXM	Negative Current-Sense-Amplifier Input. Used in the external range to provide a Kelvin connection to the range-setting resistor.
23	CT1	Range-Change Glitch-Control Capacitor Connection. Connect optional capacitor from CT1 to DGND.
24	CT2	Range-Change Glitch-Control Capacitor Connection. Connect optional capacitor from CT2 to DGND.
27, 28, 45–48, 96, 97, 98	N.C.	No Connection. Make no connection to these pins.
29, 38, 44	DGND	Digital Ground
30	$\overline{\text{HIZMP}}$	High-Impedance Control Input. Places current and voltage measure outputs into a high-impedance state.
31	IDDQSEL	IDDQ Test Select. In FV mode, switches between the programmed current range and range D, the lowest current range.
32	DIN	Data Input. Serial interface data input.
33	$\overline{\text{LOAD}}$	Load Data Input. A falling edge at $\overline{\text{LOAD}}$ transfers data from the input registers to the DPS registers.
34	SCLK	Serial Clock Input. Serial interface clock.
35	$\overline{\text{CS}}$	Chip-Select Input
36	VTHR	Threshold Voltage Input. Sets the input logic threshold level of all digital inputs. Defaults to 1/2 V_L if unconnected.
37	V_L	Logic Power Supply

Pin Description (continued)

PIN	NAME	FUNCTION
39	DOUT	Data Output. Serial interface data output.
40	EXTSEL	External Select Output. Selects the external range.
41	$\overline{HITEMP}$	High Temperature Indicator Output. Open-collector output goes low when the temperature of the die is above the specified safe operating temperature.
42	ILIMLO	Low Current-Limit Output. A sensed current below the ITHLO level forces the ILIMLO output low. ILIMLO is an open-drain output.
43	ILIMHI	High Current-Limit Output. A sensed current above the ITHHI level forces the ILIMHI output low. ILIMHI is an open-drain output.
51	ITHLO	Low Current-Limit Input. Voltage input that sets the lower threshold for the sense current comparator.
52	ITHHI	High Current-Limit Input. Voltage input that sets the upper threshold for the sense current comparator.
53	IOSI	Current-Sense Offset Voltage Input. Voltage input that sets an offset voltage for the current-sense amplifier in either FI or MI mode.
54	IOSV	Measure Offset Voltage Input. Voltage input that sets an offset voltage for the measure voltage amplifier.
55	VINS	Forced-Current Input. Voltage input that sets the forced current in FI slave mode.
56	VIN	Forced-Current/Voltage Input. Voltage input that sets the forced current in FI mode or forced voltage in FV mode.
57	AGND	Analog Ground
58	CLL	Compliance Low Input. Voltage input that sets the low-side voltage/current compliance.
59	CLH	Compliance High Input. Voltage input that sets the high-side voltage/current compliance.
60	IPAR	Current-Controlled Proportional Voltage Output. IPAR outputs a voltage that is proportional to the DUT current. Used to slave additional parallel DPSs to provide increased output current.
61	IMEAS	Current-Controlled Proportional Voltage Output. IMEAS outputs a voltage that is proportional to the DUT current. High impedance when $\overline{HIZMP}$ is forced low.
62	VMEAS	Voltage-Controlled Proportional Voltage Output. VMEAS outputs a voltage equal to 1x, 1/2x, or 1/6x the voltage present at SENSE. High impedance when $\overline{HIZMP}$ is forced low.
63	TEMP	Temperature Monitor Output. TEMP outputs a voltage proportional to die temperature of 10mV/K.
64	CBC	CB Common. Common point for bypass capacitor connections CB1, CB2, and CB3.
65	CB1	Bypass Capacitor 1. Compensation capacitor 1 connection.
66	CB2	Bypass Capacitor 2. Compensation capacitor 2 connection.
67	CB3	Bypass Capacitor 3. Compensation capacitor 3 connection.
68	CC1	Main Compensation Capacitor. Compensation capacitor connection 1.
69	CC2	Main Compensation Capacitor. Compensation capacitor connection 2.
70	CCHL	Clamp Compensation Capacitor Common. Common connection for CCL and CCH.
71	CCH	High Clamp Compensation Capacitor. High-side voltage clamp compensation capacitor connection.
72	CCL	Low Clamp Compensation Capacitor. Low-side voltage clamp compensation capacitor connection.
73	SAMPO	Lead Compensation Capacitor Common. Common connection for CCOMP1 and CCOMP2.
74	CCOMP1	Compensation Capacitor 1. Lead compensation capacitor 1 connection.
75	CCOMP2	Compensation Capacitor 2. Lead compensation capacitor 2 connection.
94	AMPOUT	Main Amplifier Output. Drives the external buffer when in external range mode.
—	EP	Exposed pad. Internally connected to V_{EE}. Connect to a large V_{EE} power plane or heatsink to maximize thermal performance. Not intended as an electrical connection point.

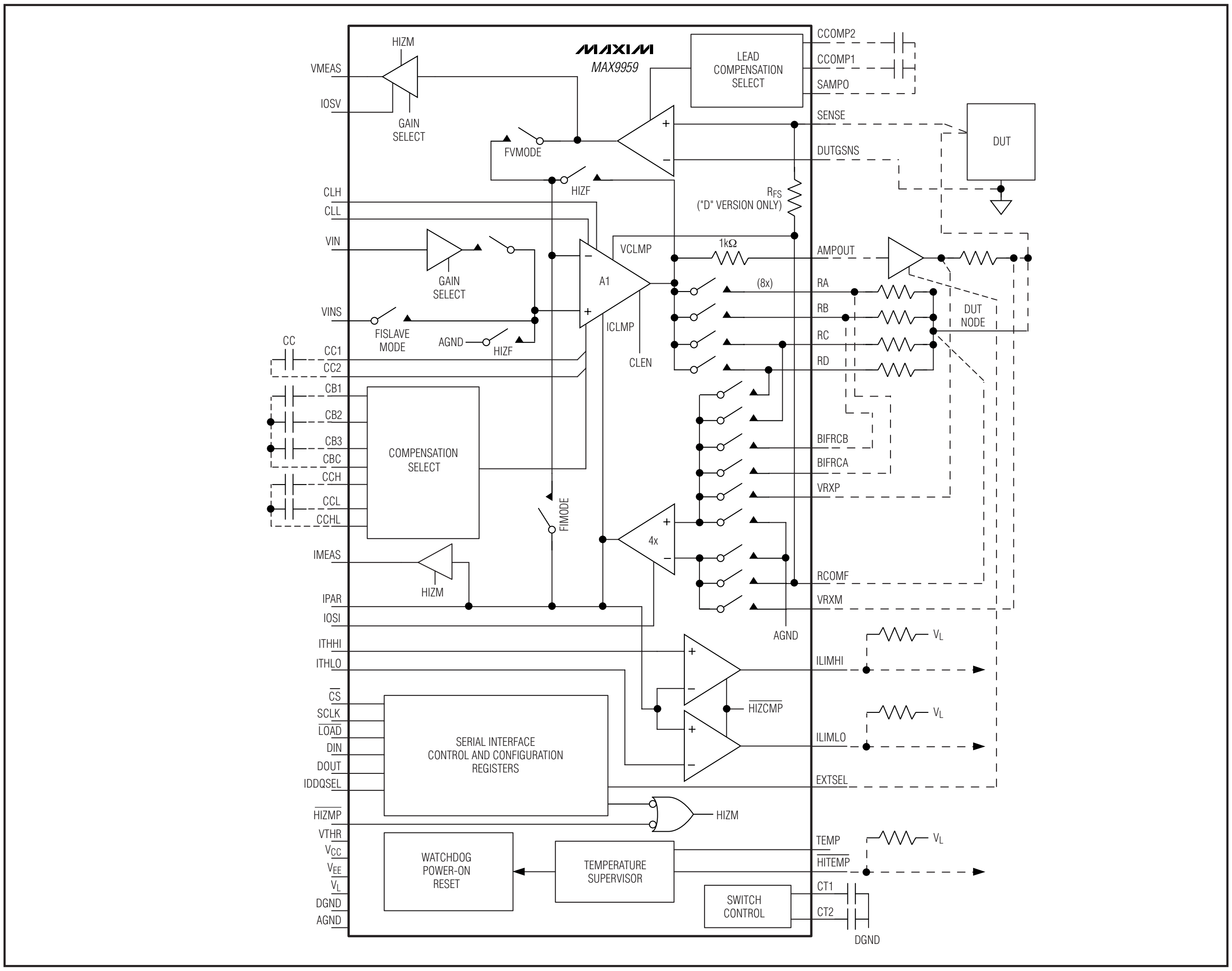


Figure 1. Functional Diagram

Detailed Description

The MAX9959 device power supply (DPS) is a voltage source when the load current is between the two programmed limits and transitions gracefully into a precision current source/sink if a programmed current limit is reached. It provides voltage-control inputs that allow independent setting of the output voltage, the maximum voltage (current), and the minimum (smallest positive or most negative) voltage (current), and it can source voltages over a span of 25V at up to ±800mA of current. For currents less than ±200mA, the MAX9959 provides full four-quadrant operation. It supports the addition of an external buffer for sourcing and sinking higher currents, and multiple MAX9959s can be paralleled to load-share, thus realizing higher total current capability with greater flexibility. Additionally, the output features two independently adjustable clamps that limit both the negative and positive output voltages or currents to externally provided limits. It offers voltage and current measurement outputs, a window comparator for go/no-go testing, a temperature monitor, a high-temperature warning flag, and a high-temperature shutdown.

The MAX9959D features an internal 300kΩ sense resistor, R_{FS}, between RCOMF and SENSE. The MAX9959F version does not include this sense resistor.

Analog Signal Polarities

In force-voltage mode the output voltage (SENSE/RCOMF in Figure 1, the *Functional Diagram*) is proportional to the input control voltage and determined by the choice of one of three +/- gain settings controlled through the serial interface.

In force-current mode, the output current is proportional to the input control voltage and behaves according to the formula:

$$I_{OUT} = \frac{V_{IN}}{4R_{SENSE}}$$

Positive current is defined as flowing out of the MAX9959 DPS.

In high-impedance mode, outputs RA, RB, RC, and RD are high impedance.

Current-Sense-Amplifier Offset Voltage Input

The current-sense amplifier monitors the voltage across the output resistors connected to RA, RB, RC, and RD in Figure 1. The current-sense offset voltage input, IOSI, introduces an offset to the current-sense amplifier. When IOSI is zero relative to AGND, the nominal output voltage range of the current-sense amplifier, corresponding to a +/- full-scale output current, is -4V to +4V. Voltage applied to IOSI adds directly to this output voltage. For example, if +4V is applied to IOSI, the voltage range corresponding to +/- full-scale current becomes 0 to +8V, within the range allowed by the power-supply rails.

Measure Voltage-Sense-Amplifier Offset Voltage Input

The measure voltage-sense amplifier monitors the output voltage of the MAX9959. The measure offset voltage input, IOSV, introduces an offset to the measure voltage amplifier. Voltage applied to IOSV adds directly to this output voltage.

External Mode Support

The MAX9959 includes resources to drive an external amplifier to provide a current range beyond the highest range (or below the lowest current range) included within the device. A voltage output, AMPOUT, is provided for the input of the external amplifier, and a digital output, EXTSEL, goes high to activate the external amplifier. Feedback inputs VRXP and VRXM connect across the external amplifier's current-sense resistor. The external amplifier must have a high-impedance output when not selected (EXTSEL = low), if connected as shown in Figure 1.

Parallel DPS Operation

The MAX9959 allows multiple devices to be configured in parallel to increase the available DUT drive current. One DPS must be configured as the master (in FV mode), and the parallel devices must be configured as slaves (in FI slave mode). The connection between the master and slaves is made using the IPAR output and VINS input. IPAR outputs a voltage that is proportional to the DUT current and VINS provides a proportional force-current/voltage input. Up to 16 MAX9959s can be placed in parallel.

Voltage Clamps

Internal programmable voltage clamps limit the output voltage to the programmed values when in FI mode. Set the clamp voltage limits with inputs CLH and CLL. The clamps handle the full ±800mA and are triggered by the voltage at RCOMF independent of the voltage at SENSE. Clamp enable bit, CLEN, in the serial control word, enables the voltage clamps.

Current Limit

Programmable and default current limits are available at the output in the FI and FV modes. When programmable current compliance is enabled, the DPS output current limits at the preprogrammed setting for each current range. When the current limit is disabled, the DPS output current limits at the default value, 147% FSR (typ), of the selected current ranges for range B, C, and D. In range A, under FI or FV conditions, the DPS output current limits at 138% FSR (typ). For currents within each selected range, the FV output behaves as a constant voltage source. When the default or programmed current compliance limits are reached, the DPS transitions to constant current mode.

Current-Limit Flags

The MAX9959 can flag currents within user-specified limits. This allows fast go/no-go testing in production environments. The window comparator continuously monitors the load current and compares it to inputs ITHHI and ITHLO. The comparator outputs are open collector and can be made high impedance with the serial interface.

Measure Amplifier High-Impedance Modes

Measure outputs VMEAS and IMEAS can be placed in a high-impedance state with logic input $\overline{\text{HIZMP}}$ or serial interface bit $\overline{\text{HIZMS}}$. This allows busing of the measure outputs with other DPS measure outputs.

Ground and DUT Ground Sense

Two ground connections, AGND (analog ground) and DGND (digital ground), are both local grounds. Connect these grounds together on the printed circuit board (PCB). DUT ground-sense input, DUTGSNS, allows sensing with respect to the DUT in force voltage mode.

Short-Circuit Protection

RA, RB, RC, RD, AMPOUT, and SENSE withstand a short to any voltage between and including the supply rails.

Temperature Sensor and Over-Temperature Protection

The MAX9959 outputs a voltage proportional to its die temperature, at TEMP, of 10mV/K (or 10mV/°C) with the nominal output voltage being 3.43V at 343K (+70°C). If the temperature of the die enters the range of +120°C to +140°C, the open-collector output $\overline{\text{HITEMP}}$ goes low. If the die temperature exceeds +140°C, the temperature sensor issues a power-on reset, placing the DPS into its high-impedance state. A reduction in temperature after a temperature-initiated reset does not return the DPS to its original operating state; reprogramming is required.

Mode and Range-Change Transients

Glitch minimization measures in the MAX9959 employ make-before-break switching and internal clamps to reduce output glitches. To guarantee minimum glitches between range changes, change between adjacent ranges, e.g., RA to RB, RD to RC. Do not switch to another range until the present range-change operation has been completed. In addition to the make-before-break measures, connections CT1 and CT2 are provided for optional capacitors that control the edge rate of the gate drive to the range-change switches. Two capacitors of 150pF each provide a reasonable balance between glitch control and range-change transition time.

DUT Voltage Swing vs. DUT Current and Power-Supply Voltages

The DUT voltage that the MAX9959 can deliver is limited by two main and two lesser factors:

1) The 2.5V overhead from each supply rail required by the amplifiers and other on-chip circuitry.
2) The voltage drop across the sense resistor and internal circuitry in series with the sense resistor. At full current the combined voltage drop is 2.5V, 1V across the resistor and 1.5V across the switches. This voltage is not all in addition to the overhead requirement. There is some overlap of the two effects; see Figure 2.
3) Variations in the system power-supply voltages.
4) Variations between the ground voltage of the device-under-test and AGND.

Neglecting the effects of items 3 and 4, the output capabilities of the DPS are demonstrated by Figure 2.

Figure 2 shows that for zero DUT current, the DUT voltage swing is from (V_{EE} + 2.5V) to (V_{CC} - 2.5V). For positive DUT currents, the maximum voltage drops off linearly until it reaches V_{CC} - 5V at full current. Similarly for negative DUT currents, the magnitude of the negative voltage drops off linearly until it reaches V_{EE} + 5V.

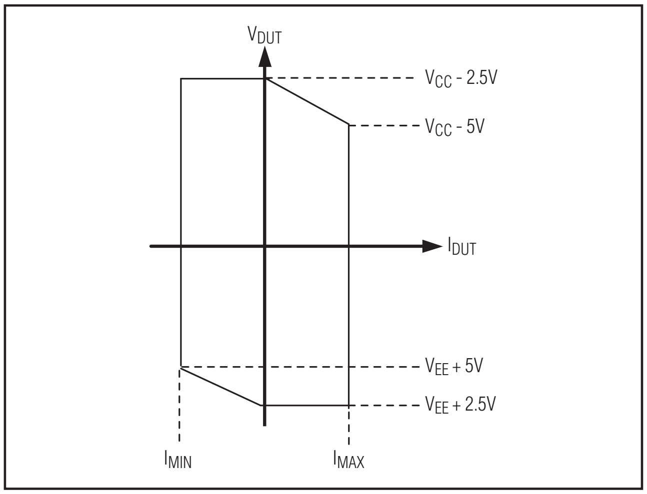


Figure 2. Output Swing

When the DPS is driving more than ±200mA output current, the power dissipated by the DPS must be limited to below the power limit of the package (see the *Absolute Maximum Ratings* and Note 2). For example, when the DPS is driving ±800mA in range A, the V_{CC} supply must not exceed +12V, and the V_{EE} supply must not exceed -12V. When the DPS is sourcing current, the DUT node must not be driven below zero volts. When the DPS is sinking current, the DUT node must not be driven above zero volts (two-quadrant operation). When operating below ±800mA, four-quadrant operation may be possible depending on the power dissipation of the DPS. Power dissipation analysis must consider variations in the power-supply voltage and the voltage difference between the device-under-test ground and the DPS AGND (items 3 and 4 above).

Since the maximum output voltage range is relative to the supply voltage, any decrease in a supply voltage from nominal proportionally decreases the range. The maximum output voltage range is also reduced by the difference between the DUT ground and the analog ground potentials (DUTGSNS - AGND). Note that within these limitations, the forced DUT voltage is equal to DUT ground plus the input control voltage. Similarly, when measuring a voltage, the measured voltage is equal to the difference between the DUT voltage and DUT ground.

Configuration and Control

Configuration of the MAX9959 is achieved through the serial interface, and through the dedicated logic-control inputs HIZMP, LOAD, and IDDQSEL.

The serial interface has a shift register, an input register, and a DPS register (Figure 3). Serial data do not directly affect the DPS until the data reach the DPS register. Control of data flow to the DPS register is through two control bits (A0 and C0) and logic input LOAD. LOAD asynchronously transfers data from the input register into the DPS register. If LOAD is held low when data are latched into the input register, then the data transfer directly (transparently) into the DPS register. This allows changing the state of the DPS coincident with the end of serial-port data communication, or asynchronously with respect to serial-port communications. Asynchronous update using LOAD facilitates simultaneous updates of multiple daisy-chained DPS devices.

DPS Data Control Bits

An 18-bit word programs the MAX9959. Table 1 outlines the 18-bit control word structure.

Serial Interface Data Flow Control Bits

Bits 0 and 1 (C0 and A0) specify if and how data transfers from the shift register to the input and DPS registers. The specified actions shown in Table 2 occur when CS goes high (Figures 5 and 6).

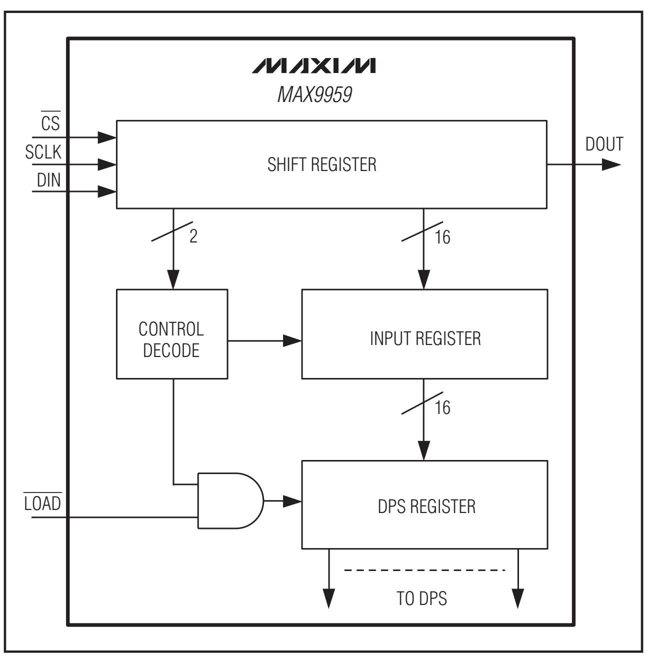


Figure 3. DPS Serial Port Block Diagram

When A0 = C0 = 0 (NOP), data move through the shift register to DOUT without change in mode or operation. This is useful when daisy-chaining devices to shift operational data through a number of devices to a specific device without altering some or all the device's operational data. To update multiple daisy-chained devices simultaneously use A0 = 1 and C0 = 0 to load the input register of the devices to be updated and activate LOAD after CS goes high (Figure 5). If LOAD is held low while CS is raised, data latched to the input register are also latched to the DPS register, independent of the state of C0.

Table 1. Data Control Bits and Bit Order

DATA BIT	NAME	FUNCTION
17	FMODE	Mode Select
16	G2	Gain and Polarity Select
15	G1	
14	G0	
13	RS2	Range Select
12	RS1	
11	RS0	
10	CLEN	Clamp Enable
9	RESERV	Reserved. Set this bit to zero.
8	HIZFRC	Force High-Impedance Select
7	HIZMS	Measure High-Impedance Select
6	HIZCMP	Comparator High-Impedance Select
5	LCOMP1	Compensation Select
4	LCOMP0	
3	BCOMP1	
2	BCOMP0	
1	A0	Serial Interface Data Flow Control
0	C0	

Table 2. Serial Interface Data Flow Control Bits

DATA BITS		OPERATION
A0 (D1)	C0 (D0)	
0	0	NOP: Input and DPS registers remain unchanged
0	1	Load DPS register from input register
1	0	Load input register from shift register
1	1	Load input register and DPS register from shift register

"Quick Load" Using Chip Select

Latching data from the input register to the DPS register under standard operation of the MAX9959 requires an additional command, and/or use of $\overline{LOAD}$. An alternative "shortcut" is to take $\overline{CS}$ low, satisfy the minimum $\overline{CS}$ low pulse-width specification, and then return it high without any coincident clock activity. Data in the input register are latched to the DPS register on the rising edge of $\overline{CS}$.

Programmable Analog Modes

Current Range Selection

Bits D11 to D13 of the control word (RS0, RS1, and RS2) control the full-scale current range for either FI (force current) or MI (measure current) mode. Nominal current monitor resistor values and current ranges are listed in Table 3.

Table 3. Range Select Bits and Nominal Sense Resistor Values

DATA BITS			RANGE	MAXIMUM CURRENT	NOMINAL SENSE RESISTOR VALUE (Ω)
RS2 (D13)	RS1 (D12)	RS0 (D11)			
0	0	0	D	±200µA	5000
0	0	1	C	±2mA	500
0	1	0	B	±20mA	50
0	1	1	A	±800mA	1.25
1	X	X	External	—	—

X = Don't care.

VIN and Measure Voltage, Variable-Gain Amplifier Selection

Bits D14 to D16 of the control word (G0, G1, and G2) control the gain and polarity of the variable-gain amplifiers (VGAs). These bits also control the gain of the measure amplifier, allowing a 1:1 input-to-output voltage transfer function when in the FVMV mode. The settings are detailed in Table 4.

Table 4. VGA Gain and Polarity Select Bits

DATA BITS*			VIN VGA	MEASURE VOLTAGE VGA
G2 (D16)	G1 (D15)	G0 (D14)		
0	0	0	+1	+1
0	0	1	+2	+1/2
0	1	0	+6	+1/6
1	0	0	-1	+1
1	0	1	-2	+1/2
1	1	0	-6	+1/6

**States 011 and 111 are unused.*

Mode Selection

Bits D8 and D17 in the control word ($\overline{HIZFRC}$ and FMODE) select the mode of operation of the MAX9959, indicated in Table 5. FMODE selects whether the DPS forces a voltage or a current. $\overline{HIZFRC}$ determines if the driver amplifier is placed in a high-output-impedance state, or if VINS is selected as the input to the amplifier (FI slave mode).

Table 5. DPS Mode Select Bits

DATA BITS		DPS MODE	AMP INPUT	OUTPUTS RA, RB, RC, AND RD
$\overline{HIZFRC}$ (D8)	FMODE (D17)			
0	0	High Impedance	AGND	High Impedance
0	1	FI Slave	VINS	Current
1	0	FV	VIN	Voltage
1	1	FI	VIN	Current

In FV and FI modes, IMEAS and VMEAS outputs provide measurement of the DUT sense voltage or current, allowing flexible modes of operation beyond the traditional force-voltage/measure-current (FVMI) and force-current/measure-voltage (FIMV) modes. The modes supported are:

FVMI: Force-voltage/measure-current

FIMV: Force-current/measure-voltage

FVMV: Force-voltage/measure-voltage

FIMI: Force-current/measure-current

FNMV: Force-nothing/measure-voltage

In the FV or FI modes, VIN is selected to control the forced voltage or forced current. In the FI slave mode, VINS is selected. This allows connecting a master DPS to its slaves without using external relays.

Digital Interface Operation

A 3-wire SPI™/QSPI™/MICROWIRE™-compatible serial interface is used for command and control of the MAX9959. The serial interface operates with clock speeds up to 20MHz. Additionally, a few logic inputs control special functions, sometimes working with the serial interface control data, sometimes overriding it.

Logic Inputs and Shared Control Functions

Control of the measure output high-impedance state is shared between the $\overline{HIZMS}$ bit (D7) and the logic input $\overline{HIZMP}$. Data transfer operations from the input shift register to the two internal control registers, input and DPS, are shared between the control word's A0 and C0 bits, and logic input $\overline{LOAD}$ (see the *Configuration and Control* section).

Digital Inputs

Digital inputs SCLK, DIN, $\overline{CS}$, $\overline{LOAD}$, $\overline{HIZMP}$, and IDDQSEL incorporate hysteresis to mitigate noise and to provide compatibility with opto-isolators. Voltage threshold levels for digital inputs are determined by VTHR, and default to 1/2 V_L if VTHR is left unconnected.

Digital Output (DOUT)

When the input data register is full, the data become available at DOUT in a first-in-first-out fashion, allowing multiple devices to be daisy-chained. Data at DOUT follow DIN with a delay of 18 clock cycles per chained unit. The digital output is clocked on the falling edge of the input clock, allowing daisy-chained devices to use the same clock signal.

Serial-Port Timing

Timing of the serial port is detailed in timing Figures 4, 5, and 6, and in the serial port timing characteristics section of the *AC Electrical Characteristics* table.

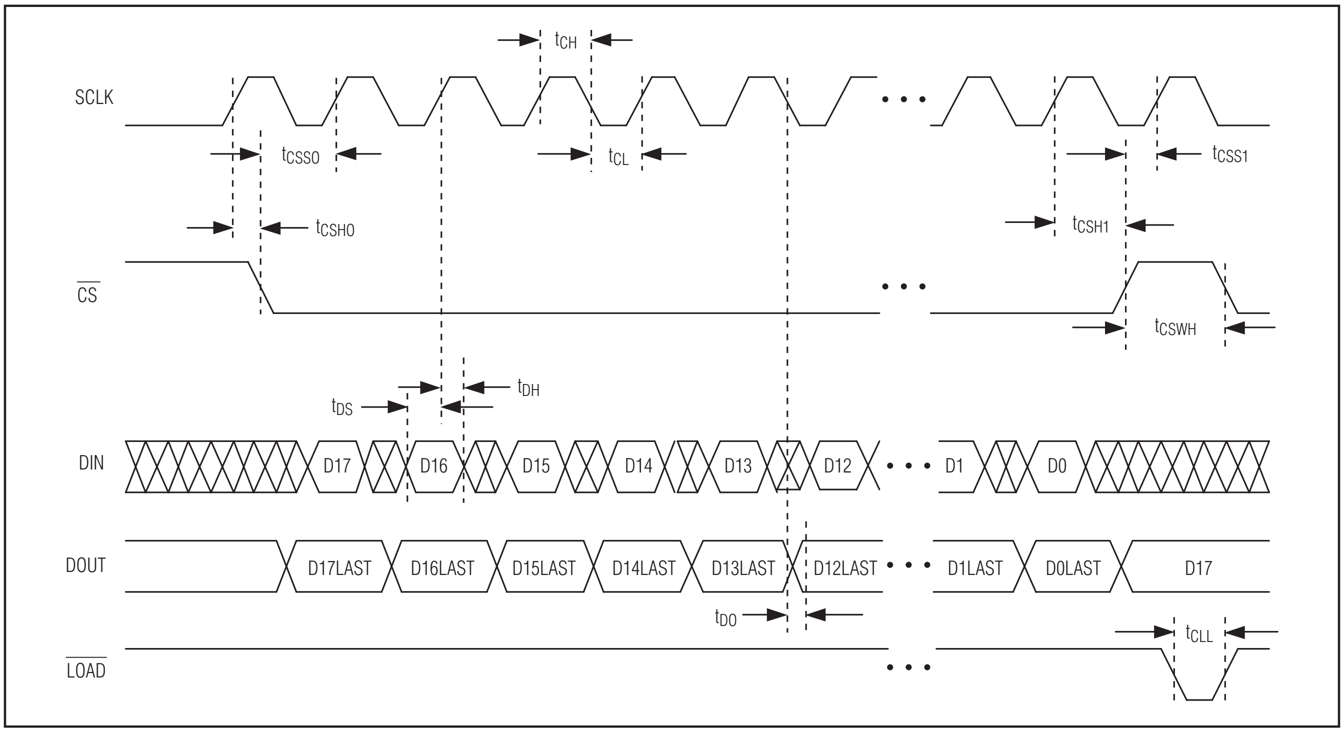


Figure 4. Serial Interface Timing

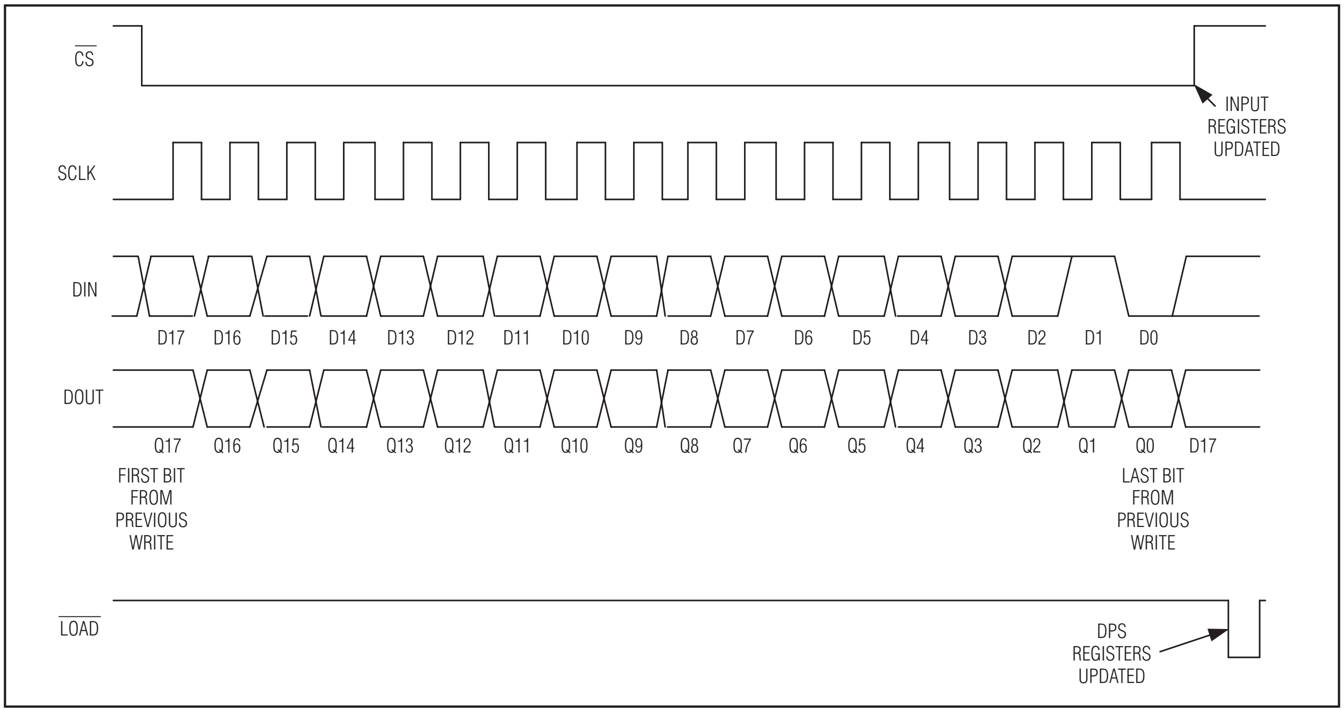


Figure 5. Serial Interface Timing with Asynchronous Loading of the DPS Register

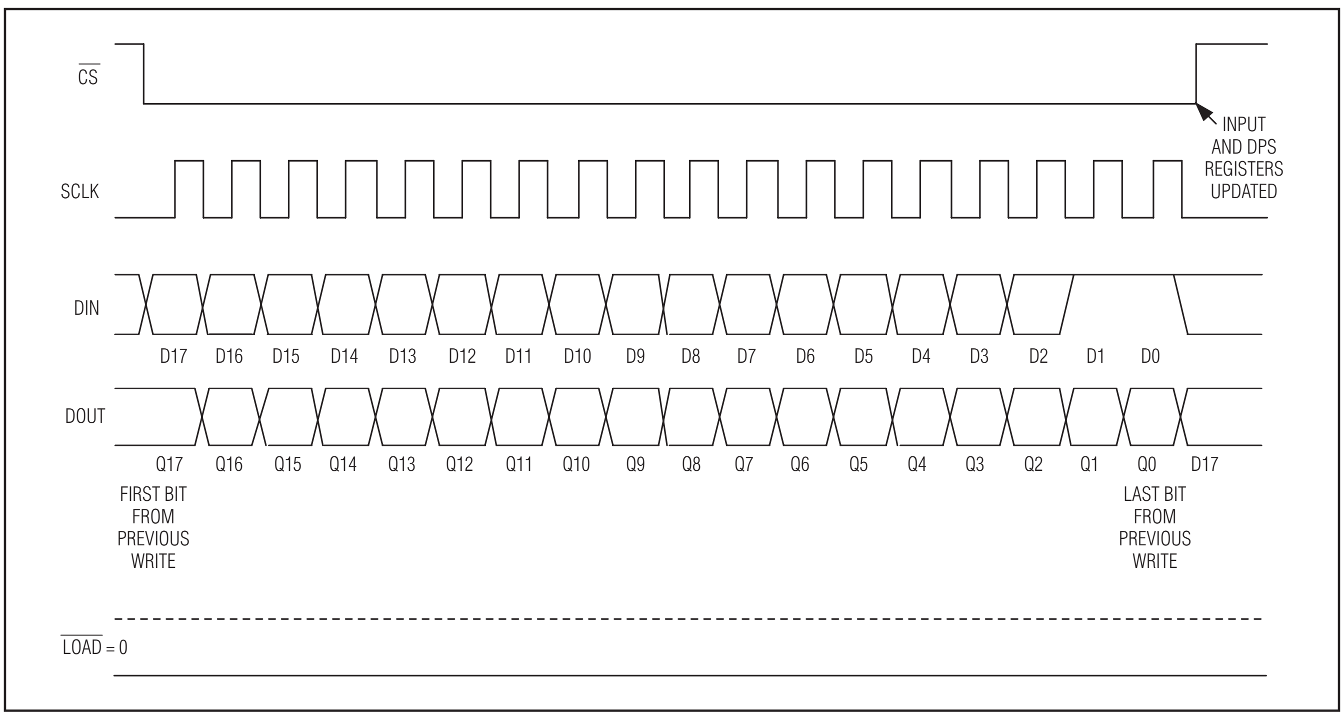


Figure 6. Serial Interface Timing with Synchronous Loading of the DPS Register

Applications Information

Exposed Pad

Leave EP unconnected or connect to V_{EE}. Do not connect EP to ground.

Lead Compensation Capacitor Selection

The MAX9959 can drive widely varying load capacitances. As the load capacitance increases, the output of the DPS tends to overshoot. To counter this, lead compensation capacitor network connections are provided, each with dedicated internal switches controllable through the serial interface (Figure 1). The networks can be tailored to specific needs, such as settling time vs. overshoot, with combinations of capacitors. Control bits D5 and D4 (LCOMP1 and LCOMP0) configure compensation capacitor connections as shown in Table 6.

Table 6. Lead Compensation Capacitor Selection

DATA BITS		COMPENSATION CAPACITOR SELECT	MINIMUM CAPACITOR VALUE (pF)	MAXIMUM CAPACITOR VALUE (pF)
LCOMP1 (D5)	LCOMP0 (D4)			
0	0	None	—	—
0	1	CCOMP1	27	330
1	0	CCOMP2	27	330
1	1	CCOMP1 and CCOMP2	27 each	330 each

Bypass Compensation Capacitor Selection

In addition to lead compensation, the DPS also implements bypass compensation, which may be required under conditions of heavy capacitive loading. Depending on the mode selected, FV or FI, control bits D3 and D2 (BCOMP1 and BCOMP0) select different capacitors.

In the FV mode, one of three bypass capacitors (CB1, CB2, and CB3), or none is selected, as shown in Table 7. Table 8 presents the recommended CB1, CB2, and CB3 capacitor values for various load conditions.

Table 7. FV Mode Bypass Capacitor Selection

DATA BITS		BYPASS CAPACITOR SELECT
BCOMP1 (D3)	BCOMP0 (D2)	
0	0	None
0	1	CB1
1	0	CB2
1	1	CB3

Table 8. CB1, CB2, and CB3 Recommended Values

RANGE	LOAD						
	≥ 1nF	≥ 10nF	≥ 100nF	≥ 1µF	≥ 10µF	≥ 100µF	≤ 1000µF
A	—	—	CB1 = 2.7nF	CB1 = 2.7nF	CB2 = 10nF	CB3 = 22nF	CB3 = 22nF
B	—	—	CB1 = 2.7nF	CB1 = 2.7nF	CB2 = 10nF	CB3 = 22nF	—
C	—	CB1 = 2.7nF	CB1 = 2.7nF	CB2 = 10nF	CB3 = 22nF	—	—
D	CB1 = 2.7nF	CB1 = 2.7nF	CB2 = 10nF	CB3 = 22nF	—	—	—

In FI mode, the bypass capacitor combination (CCH/CCL), or none, is selected (Table 9). Table 10 presents the recommended CCH and CCL capacitor values for various load conditions. These compensation capacitors provide improved stability for the voltage clamp circuit when driving heavy loads.

Table 9. FI Mode Voltage Clamp Compensation Capacitor Selection

DATA BITS		FORCE-CURRENT MODE COMPENSATION CAPACITOR SELECT
BCOMP1 (D3)	BCOMP0 (D2)	
0	0	None
X	1	CCL/CCH
1	X	CCL/CCH

X = Don't care.

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Table 10. CCH and CCL Recommended Values (CCH = CCL)

RANGE	LOAD							
	≥ 100pF	≥ 1nF	≥ 10nF	≥ 100nF	≥ 1µF	≥ 10µF	≥ 100µF	≤ 1000µF
A	—	—	—	4.7nF	4.7nF	4.7nF	4.7nF	4.7nF
B	—	—	4.7nF	4.7nF	4.7nF	4.7nF	4.7nF	—
C	—	4.7nF	4.7nF	4.7nF	4.7nF	4.7nF	—	—
D	4.7nF	4.7nF	4.7nF	4.7nF	4.7nF	—	—	—

Measure Output High-Impedance Control

Place the measure output into a low-leakage, high-impedance state in either of two ways: with the $\overline{HIZMS}$ control bit (D7), or the digital input $\overline{HIZMP}$. The two controls are logically AND ed, as shown in Table 11. Digital input $\overline{HIZMP}$ allows multiplexing between several DPS measure outputs without using the serial interface.

Table 11. Measure Output High-Impedance Control

DATA BIT $\overline{HIZMS}$ (D7)	DIGITAL INPUT $\overline{HIZMP}$	MEASURE OUTPUT (VMEAS, IMEAS) MODE
1	1	Measure Output Enabled
1	0	High Impedance
0	1	High Impedance
0	0	High Impedance

Voltage (Current) Clamp Enable

Control word bit CLEN (D10) enables the output clamps when high and disables the clamps when low, as indicated in Table 12. In FV mode, current compliance is active. In FI mode, voltage compliance is active.

Table 12. Clamp Enable Control

CONTROL BIT CLEN (D10)	CLAMP MODE
1	Clamps Enabled
0	Clamps Disabled

IDDQ Test Mode

While in FV mode, asserting digital input IDDQSEL switches the DPS to the minimum current range (range D), engaging the IDDQ test mode as shown in Table 13. Switching to the minimum current range through external control allows low-current IDDQ measurements without reprogramming the DPS through the serial interface. When IDDQSEL is deasserted the current range switches back to its programmed value.

Table 13. IDDQ Test Select

DIGITAL INPUT IDDQSEL	MODE
1	IDDQ Test
0	Normal

Power-Up Configuration

At power-up all analog outputs except TEMP default to high impedance.

Applications Circuits

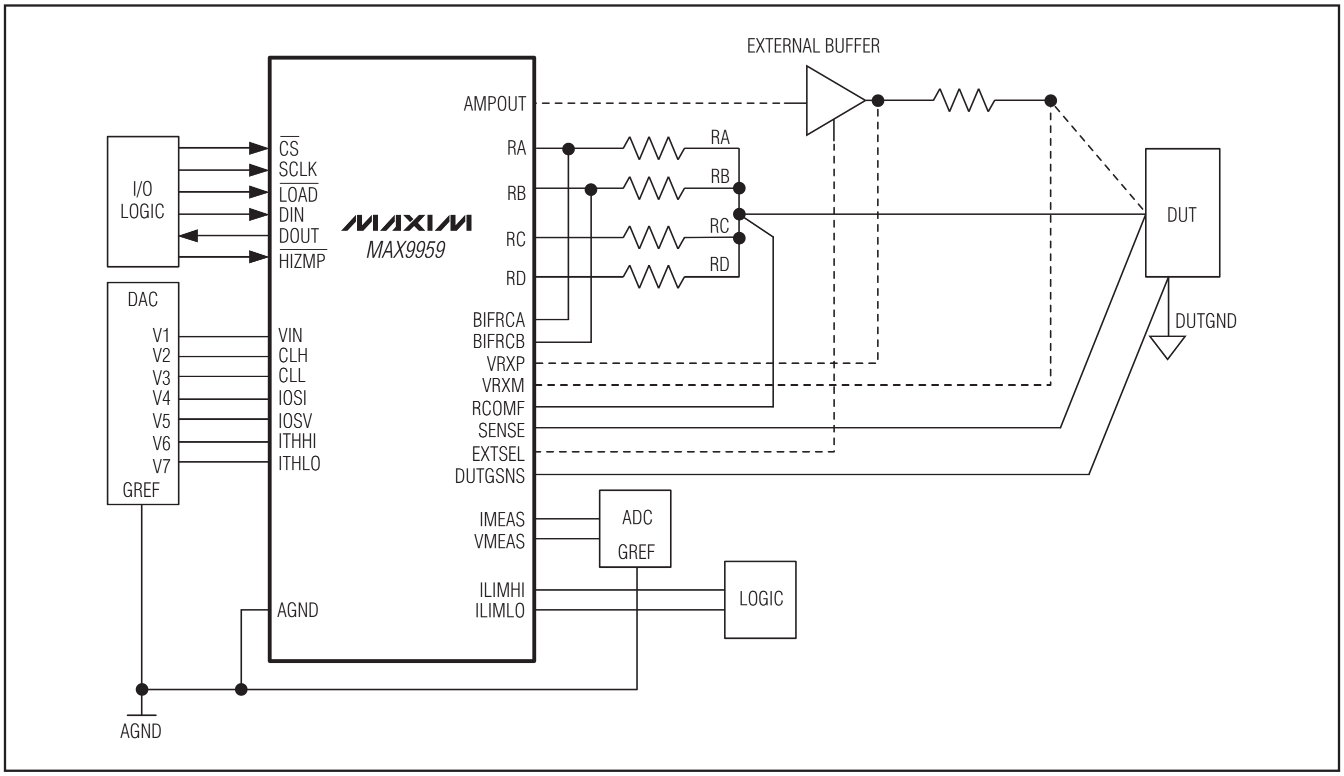

Figure 7. Single DPS Configuration

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Applications Circuits (continued)

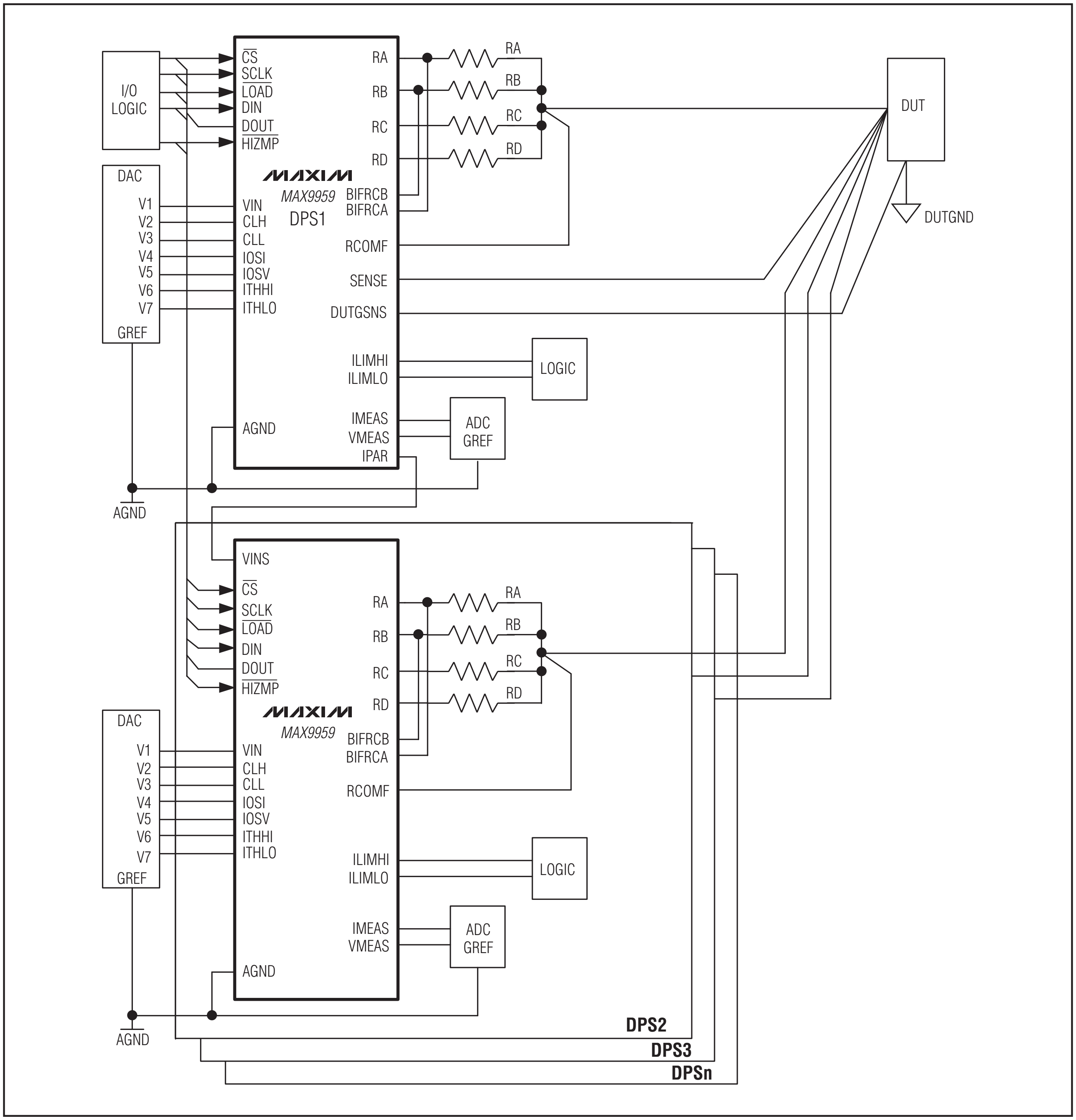
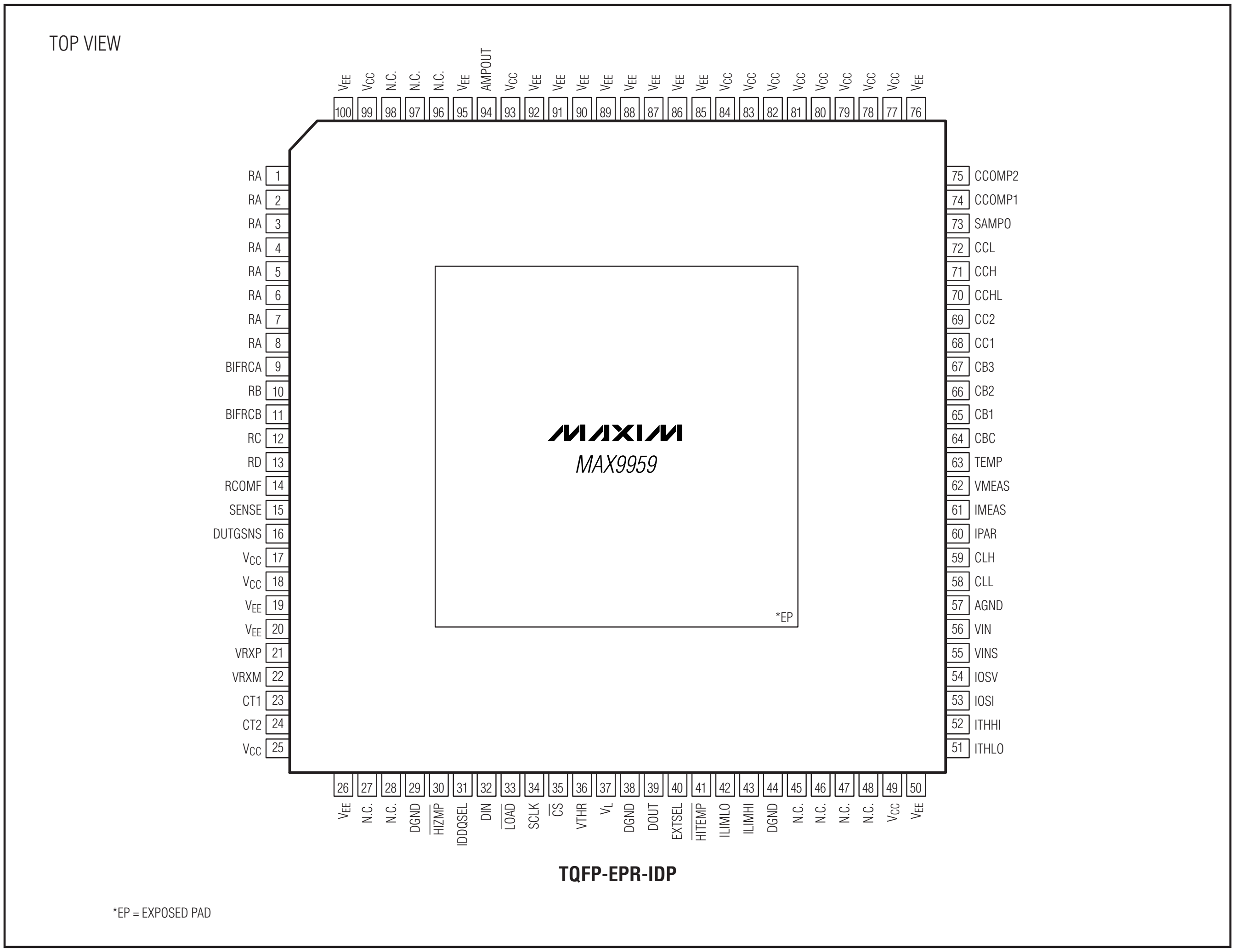


Figure 8. Parallel DPS Configuration Achieves Higher Output Current

Pin Configuration



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
100 TQFP-EPR-IDP	C100E-8R	21-0148	90-0159

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	3/07	—	1, 6, 23
3	3/09	Added exposed pad information	1, 11, 12, 19, 23
4	2/11	Updated *Absolute Maximum Ratings* and *DC Electrical Characteristics*, and corrected pins 42 and 43 in *Pin Description*	2, 4, 11