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# Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

## General Description

The MAX9972 four-channel, ultra-low-power, pin-electronics IC includes, for each channel, a three-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections. The driver features a -2.2V to +5.2V voltage range, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. The window comparator features 500MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Low-leakage, high-impedance, and terminate controls are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

This device is available in an 80-pin, 12mm x 12mm body, 0.50mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package for efficient heat removal. The MAX9972 is specified to operate over the 0°C to +70°C commercial temperature range, and features a die temperature monitor output.

## Applications

NAND Flash Testers  
 DRAM Probe Testers  
 Low-Cost Mixed-Signal/System-on-Chip (SoC) Testers  
 Active Burn-In Systems  
 Structural Testers

## Features

- ◆ Small Footprint—Four Channels in 0.3in<sup>2</sup>
- ◆ Low-Power Dissipation: 325mW/Channel (typ)
- ◆ High Speed: 300Mbps at 3V<sub>P-P</sub>
- ◆ -2.2V to +5.2V Operating Range
- ◆ Active Termination (3rd-Level Drive)
- ◆ Integrated PMU Switches
- ◆ Passive Load
- ◆ Low-Leak Mode: 20nA (max)
- ◆ Low Gain and Offset Error

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	HEAT EXTRACTION
MAX9972ACCS+	0°C to +70°C	80 TQFP-EP*	Bottom

+Denotes a lead(Pb)-free/RoHs-compliant package.

\*EP = Exposed pad.

*Pin Configuration appears at end of data sheet.*

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### ABSOLUTE MAXIMUM RATINGS

V <sub>DD</sub> to GND	-0.3V to +9.4V	CHV_, CLV_ to DUT_	V <sub>SS</sub> to V <sub>DD</sub>
V <sub>SS</sub> to GND	-6.25V to +0.3V	DOUT to GND	-0.3V to +5V
V <sub>DD</sub> to V <sub>SS</sub>	+15.7V	TEMP Short-Circuit Duration	Continuous
V <sub>L</sub> to GND	-0.3V to +5V	FORCE_ Path Switch Current	50mA
DHV_, DTV_, DLV_, LDV_, DUT_ to GND	V <sub>SS</sub> to V <sub>DD</sub>	SENSE_ Path Switch Current	1.5mA
DATA_, RCV_	-0.3V to +5V	Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
CHV_, CLV_, CMPH_, CMPL_, COMPHI, COMPLO to GND	V <sub>SS</sub> to V <sub>DD</sub>	80-Pin TQFP-EP (derate 35.7mW/°C above +70°C)	2857mW
FORCE_, SENSE_, PMU_ to GND	V <sub>SS</sub> to V <sub>DD</sub>	Storage Temperature Range	-65°C to +150°C
LD, DIN, SCLK, CS to GND	-0.3V to +5V	Junction Temperature	+150°C
DUT_, CMPH_, CMPL_ Short-Circuit Duration	Continuous	Lead Temperature (soldering, 10s)	+300°C
DHV_, DLV_, DTV_ to Each Other	V <sub>SS</sub> to V <sub>DD</sub>	Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS

(V<sub>DD</sub> = +8V, V<sub>SS</sub> = -5V, V<sub>L</sub> = +3V, V<sub>COMPHI</sub> = +1V, V<sub>COMPLO</sub> = 0V, V<sub>LDV\_</sub> = 0V, LOAD EN LOW = LOAD EN HIGH = 0, T<sub>J</sub> = +75°C. All temperature coefficients measured at T<sub>J</sub> = +50°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DRIVER (all specifications apply when DUT_ = DHV_, DUT_ = DTV_, or DUT_ = DLV_)</b>						
<b>DC CHARACTERISTICS</b>						
Voltage Range			-2.2		+5.2	V
Gain		Measured at 0V and 3V	0.995	1	1.005	V/V
Gain Temperature Coefficient				50		ppm/°C
Offset		V <sub>DHV_</sub> = 2V, V <sub>DLV_</sub> = 0V, V <sub>DTV_</sub> = 1V			±10	mV
Offset Temperature Coefficient				±250		µV/°C
Power-Supply Rejection Ratio	PSRR	V <sub>DD</sub> , V <sub>SS</sub> independently varied over full range			18	mV/V
Maximum DC Drive Current	I <sub>DUT_</sub>	All drive mode specs valid over this range	±40			mA
DC Output Resistance		I <sub>DUT_</sub> = ±10mA (Note 2)	48.5	49.5	50.5	Ω
DC Output Resistance Variation		I <sub>DUT_</sub> = -40mA to +40mA			2.5	Ω
DC Crosstalk		DHV_ to DLV_ and DTV_: V <sub>DLV_</sub> = V <sub>DTV_</sub> = +1.5V, V <sub>DHV_</sub> = -2.2V, +5.2V			5	mV
		DLV_ to DHV_ and DTV_: V <sub>DHV_</sub> = V <sub>DTV_</sub> = +1.5V, V <sub>DLV_</sub> = -2.2V, +5.2V			5	
		DTV_ to DHV_ and DLV_: V <sub>DHV_</sub> = V <sub>DLV_</sub> = +1.5V, V <sub>DTV_</sub> = -2.2V, +5.2V			5	
Linearity Error		0 to 3V (Note 3)			±5	mV
		Full range (Note 4)			±15	mV

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{COMP\ HI} = +1V$ ,  $V_{COMP\ LO} = 0V$ ,  $V_{LDV\_} = 0V$ , LOAD EN LOW = LOAD EN HIGH = 0,  $T_J = +75^\circ C$ . All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>AC CHARACTERISTICS (Note 5)</b>						
Dynamic Output Current		(Note 1)	40			mA
Drive-Mode Overshoot, Undershoot, and Preshoot		200mV to 4V <sub>p-p</sub> swing (Note 6)		5% +10		mV
Term-Mode Spike		$V_{D\ H\ V\_} = V_{D\ T\ V\_} = 1V$ , $V_{D\ L\ V\_} = 0V$		25		mV
		$V_{D\ L\ V\_} = V_{D\ T\ V\_} = 0V$ , $V_{D\ H\ V\_} = 1V$		25		
High-Impedance-Mode Spike		$V_{D\ L\ V\_} = -1V$ , $V_{D\ H\ V\_} = 0V$		25		mV
		$V_{D\ L\ V\_} = 0V$ , $V_{D\ H\ V\_} = 1V$		25		
Propagation Delay, Data to Output			1.6	2.6	4.2	ns
Prop-Delay Temperature Coefficient				10		ps/°C
Prop-Delay Match, $t_{LH}$ vs. $t_{HL}$				30		ps
Prop-Delay Skew, Drivers Within Package				150		ps
Prop-Delay Change vs. Pulse Width		Relative to 12.5ns pulse	3V <sub>p-p</sub> , 40MHz, PW = 4ns to 21ns	20		ps
			1V <sub>p-p</sub> , 40MHz, PW = 2.5ns to 23.5ns	90		
Prop-Delay Change vs. Common-Mode Voltage		1V <sub>p-p</sub> , $V_{D\ L\ V\_} = 0$ to 3V, relative to delay at $V_{D\ L\ V\_} = 1V$		80		ps
Prop Delay, Data to High Impedance		$V_{D\ H\ V\_} = +1.5V$ , $V_{D\ L\ V\_} = -1.5V$ , both directions		1.8		ns
Prop Delay, Data to Term		$V_{D\ H\ V\_} = +1.5V$ , $V_{D\ L\ V\_} = -1.5V$ , $V_{D\ T\ V\_} = 0V$ , both directions		1.6		ns
Minimum Voltage Swing		(Note 7)		25		mV
Rise/Fall Time		$V_{D\ H\ V\_} = 0.2V$ , $V_{D\ L\ V\_} = 0V$ , 20% to 80%		0.7		ns
		$V_{D\ H\ V\_} = 1V$ , $V_{D\ L\ V\_} = 0V$ , 20% to 80%		0.7		
		$V_{D\ H\ V\_} = 3V$ , $V_{D\ L\ V\_} = 0V$ , 10% to 90%	1.5	2.0	2.5	
		$V_{D\ H\ V\_} = 4V$ , $V_{D\ L\ V\_} = 0V$ , $R_L = 500_\Omega$ , 10% to 90%		2.6		
		$V_{D\ H\ V\_} = 5V$ , $V_{D\ L\ V\_} = 0V$ , $R_L = 500_\Omega$ , 10% to 90%		3.4		
Rise/Fall-Time Matching		$V_{D\ H\ V\_} = 1V$ to 5V		±5		%
Minimum Pulse Width (Note 8)		200mV, $V_{D\ H\ V\_} = 0.2V$ , $V_{D\ L\ V\_} = 0V$		1.8		ns
		1V, $V_{D\ H\ V\_} = 1V$ , $V_{D\ L\ V\_} = 0V$		2.4		
		3V, $V_{D\ H\ V\_} = 3V$ , $V_{D\ L\ V\_} = 0V$		3.3		

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{COMP1} = +1V$ ,  $V_{COMP0} = 0V$ ,  $V_{LDV} = 0V$ ,  $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$ ,  $T_J = +75^\circ C$ . All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>COMPARATOR (Note 9)</b>						
<b>DC CHARACTERISTICS (driver in high-impedance mode) (<math>V_{COMP1} = 0.8V</math>, <math>V_{COMP0} = 0.2V</math>)</b>						
Input Voltage Range			-2.2		+5.2	V
Differential Input Voltage		$V_{DUT\_} - V_{CHV\_}$ , $V_{DUT\_} - V_{CLV\_}$	-7.4		+7.4	V
Hysteresis		$V_{CHV\_} = V_{CLV\_} = 1.5V$		8		mV
Input Offset Voltage		$V_{DUT\_} = 1.5V$			$\pm 10$	mV
Input Offset Temperature Coefficient				25		$\mu V/^\circ C$
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_} = 0$ and $3V$	60			dB
Linearity Error (Note 10)		$V_{DUT\_} = 1.5V$			$\pm 5$	mV
		$V_{DUT\_} = -2.2V, +5.2V$			$\pm 10$	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_} = 1.5V$ , supplies independently varied over full range			5	mV/V
<b>AC CHARACTERISTICS (Note 11)</b>						
Equivalent Input Bandwidth		Terminated (Note 12)		500		MHz
		High impedance (Note 13)		300		
Propagation Delay			0.9	2.2	3.1	ns
Prop-Delay Temperature Coefficient				4		ps/ $^\circ C$
Prop-Delay Match, $t_{LH}$ to $t_{HL}$				120		ps
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL)		200		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 14)		0 to 4.9V		20		ps
		-1.9V to +4.9V		30		
Prop-Delay Dispersions vs. Overdrive		$V_{CHV\_} = V_{CLV\_} = 0.1V$ to $0.9V$ , $V_{DUT\_} = 1VP-P$ , $t_R = t_F = 500ps$ , 10% to 90% relative to timing at 50% point		220		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width		$\pm 60$		ps
Prop-Delay Dispersions vs. Slew Rate		0.5V/ns to 2V/ns		50		ps

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{COMP\ HI} = +1V$ ,  $V_{COMP\ LO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$ ,  $T_J = +75^\circ C$ . All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LOGIC OUTPUTS</b>						
Reference Voltages COMPHI and COMPLO		(Note 15)	0		+3.6	V
Output High Voltage Offset		$I_{OUT} = 0mA$ , relative to COMPHI at $V_{COMP\ HI} = 1V$			$\pm 50$	mV
Output Low Voltage Offset		$I_{OUT} = 0mA$ , relative to COMPLO at $V_{COMP\ LO} = 0V$			$\pm 50$	mV
Output Resistance		$I_{CHV\_} = I_{CLV\_} = \pm 10mA$	40	50	60	$\Omega$
Current Limit				25		mA
Rise/Fall Time		20% to 80%, $V_{CHV\_} = 1VP-P$ , load = T-line, $50\Omega$ , $> 1ns$		0.7		ns
<b>PASSIVE LOAD</b>						
<b>DC CHARACTERISTICS (<math>R_{DUT\_} \geq 10M\Omega</math>)</b>						
LDV_ Voltage Range			-2.2		+5.2	V
Gain			0.99		1.01	V/V
Gain Temperature Coefficient				0.02		%/ $^\circ C$
Offset					$\pm 100$	mV
Offset Temperature Coefficient				0.02		mV/ $^\circ C$
Power-Supply Rejection Ratio	PSRR			10		mV/V
Output Resistance Tolerance—High Value		$I_{DUT\_} = \pm 0.2mA$ , $V_{LDV\_} = 1.5V$	7.125	7.5	7.875	k $\Omega$
Output Resistance Tolerance—Low Value		$I_{DUT\_} = \pm 0.1mA$ , $V_{LDV\_} = 1.5V$	1.90	2.0	2.10	k $\Omega$
Switch Resistance Variation		Relative to 1.5V	0 to 3V	$\pm 10$		%
			Full range	$\pm 30$		
Maximum Output Current (Note 16)		$V_{LDV\_} = -2V$ , $V_{DUT\_} = +5V$	$\pm 4$		mA	
		$V_{LDV\_} = +5V$ , $V_{DUT\_} = -2V$	$\pm 4$			
Linearity Error, Full Range		Measured at -2.2V, +1.5V, and +5.2V (Note 16)			$\pm 25$	mV
<b>AC CHARACTERISTICS</b>						
Settling Time, LDV_ to Output		$V_{LDV\_} = -2V$ to $+5V$ step, $R_{DUT\_} = 100k\Omega$ (Note 17)		0.5		$\mu s$
Output Transient Response		$V_{LDV\_} = +1.5V$ , $V_{DUT\_} = -2V$ to $+5V$ square wave at 1MHz, $R_{DUT\_} = 50\Omega$		20		ns

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{COMP HI} = +1V$ ,  $V_{COMP LO} = 0V$ ,  $V_{LDV} = 0V$ ,  $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$ ,  $T_J = +75^\circ C$ . All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>PMU SWITCHES (FORCE_, SENSE_, PMU_)</b>						
Voltage Range			-2.2		+5.2	V
Force Switch Resistance		$V_{FORCE\_} = 1.5V$ , $I_{PMU\_} = \pm 10mA$			40	$\Omega$
Force Switch Compliance		$V_{PMU\_} = 6.2V$ , $V_{FORCE\_}$ set to make $I_{FORCE\_} = 30mA$	25			mA
		$V_{PMU\_} = -3.2V$ , $V_{FORCE\_}$ set to make $I_{FORCE\_} = -30mA$	25			
Force Switch Resistance Variation (Note 18)		0 to 3V		$\pm 10$		%
		Full range		$\pm 30$		
Sense Switch Resistance			700	1000	1300	$\Omega$
Sense Switch Resistance Variation		Relative to 1.3V, full range		$\pm 30$		%
PMU_ Capacitance		Force-and-sense switches open		5		pF
FORCE_ Capacitance				5		pF
SENSE_ Capacitance				0.2		pF
FORCE_ External Capacitance		Allowable external capacitance		2		nF
SENSE_ External Capacitance		Allowable external capacitance		1		nF
FORCE_ and SENSE_ Switching Speed		Connect or disconnect		10		$\mu s$
PMU_ Leakage		$FORCE\ EN\_ = SENSE\ EN\_ = 0$ , $V_{FORCE\_} = V_{SENSE\_} = -2.2V$ to $+5.2V$		$\pm 0.5$	$\pm 5$	nA
<b>TOTAL FUNCTION</b>						
<b>DUT_</b>						
Leakage, High-Impedance Mode		Load switches open, $V_{DUT\_} = +5.2V$ , $V_{CLV\_} = V_{CHV\_} = -2.2V$ , $V_{DUT\_} = -2.2V$ , $V_{CLV\_} = V_{CHV\_} = +5.2V$ , full range			2	$\mu A$
Leakage, Low-Leakage Mode		Full range		$\pm 1$	$\pm 20$	nA
Low-Leakage Recovery Time		(Note 19)		10		$\mu s$
Combined Capacitance		Term mode		2		pF
		High-impedance mode		5		
Load Resistance		(Note 20)		1		G $\Omega$
Load Capacitance		(Note 20)		12		nF

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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{COMPHI} = +1V$ ,  $V_{COMPL0} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$ ,  $T_J = +75^\circ C$ . All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>VOLTAGE REFERENCE INPUTS (DHV_, DTV_, DLV_, DATA_, RCV_, CHV_, CLV_, LDV_, COMPHI, COMPL0)</b>						
Input Bias Current					$\pm 100$	$\mu A$
Input Bias Current Temperature Coefficient				$\pm 200$		$nA/^\circ C$
Settling to Output		0.1% of full-scale step		10		$\mu s$
<b>DIGITAL INPUTS (DATA_, RCV_, <math>\overline{LD}</math>, DIN, SCLK, <math>\overline{CS}</math>)</b>						
Input High Voltage		(Note 21)	$V_L/2 + 0.2$		+3.6	V
Input Low Voltage		(Note 21)	0		$V_L/2 - 0.2$	V
Input Bias Current	DATA_				100	$\mu A$
	$\overline{LD}$ , DIN, SCLK, $\overline{CS}$				1	
<b>SERIAL DATA OUTPUT (DOUT)</b>						
Output High Voltage		$I_{OH} = -1mA$	$V_L - 0.4$		$V_L$	V
Output Low Voltage		$I_{OL} = 1mA$	0		+0.4	V
Output Rise and Fall Time		$C_L = 10pF$		1.1		ns
<b>SERIAL-INTERFACE TIMING (Note 22)</b>						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	$t_{CH}$		10			ns
SCLK Pulse-Width Low	$t_{CL}$		10			ns
$\overline{CS}$ Low to SCLK High Setup	$t_{CSS0}$		3.5			ns
SCLK High to $\overline{CS}$ Low Hold	$t_{CSH0}$		3.5			ns
$\overline{CS}$ High to SCLK High Setup	$t_{CSS1}$		3.5			ns
SCLK High to $\overline{CS}$ High Hold	$t_{CSH1}$		15			ns
DIN to SCLK High Setup	$t_{DS}$		7.5			ns
DIN to SCLK High Hold	$t_{DH}$		3.5			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Hold	$t_{CSHLD}$		6			ns
$\overline{CS}$ High Pulse Width	$t_{CSWH}$		20			ns
$\overline{LD}$ Low Pulse Width	$t_{LDW}$		20			ns
$\overline{LD}$ High to Any Activity			0			ns
SCLK Low to DOUT Delay	$t_{DO}$	$C_L = 10pF$	5		40	ns
$V_L$ Rising to $\overline{CS}$ Low		Power-on delay		2		$\mu s$
<b>TEMP SENSOR</b>						
Nominal Voltage		$T_J = +27^\circ C$		3.20		V
Temperature Coefficient				+10		$mV/^\circ C$
Output Resistance				500		$\Omega$



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### ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD} = +8V$ ,  $V_{SS} = -5V$ ,  $V_L = +3V$ ,  $V_{COMP\ HI} = +1V$ ,  $V_{COMP\ LO} = 0V$ ,  $V_{LDV\_} = 0V$ ,  $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 0$ ,  $T_J = +75^\circ C$ . All temperature coefficients measured at  $T_J = +50^\circ C$  to  $+100^\circ C$ , unless otherwise noted.) (Note 1)

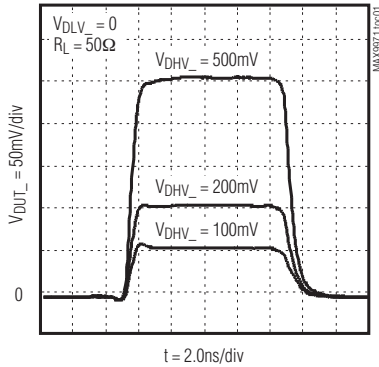
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLIES</b>						
Positive Supply Voltage	$V_{DD}$	(Note 23)	7.6	8	8.4	V
Negative Supply Voltage	$V_{SS}$	(Note 23)	-5.25	-5	-4.75	V
Logic Supply Voltage	$V_L$		2.3		3.6	V
Positive Supply Current	$I_{DD}$	$f_{OUT} = 0MHz$		97	120	mA
Negative Supply Current	$I_{SS}$	$f_{OUT} = 0MHz$		99	120	mA
Logic Supply Current	$I_L$			0.15	0.30	mA
Static Power Dissipation		$f_{OUT} = 0MHz$		1.3	1.5	W
Operating Power Dissipation		$f_{OUT} = 100Mbps$ (Note 24)		1.4		W

- Note 1:** All minimum and maximum specifications are 100% production tested except driver dynamic output current and driver/comparator propagation delays, which are guaranteed by design. All specifications are with  $DUT\_$  and  $PMU\_$  electrically isolated, unless otherwise noted.
- Note 2:** Nominal target value is  $49.5\Omega$ . Contact factory for alternate trim selections within the  $45\Omega$  to  $55\Omega$  range.
- Note 3:** Measured at 1.5V, relative to a straight line through 0 and 3V.
- Note 4:** Measured at end points, relative to a straight line through 0 and 3V.
- Note 5:**  $DUT\_$  is terminated with  $50\Omega$  to ground,  $V_{DHV\_} = 3V$ ,  $V_{DLV\_} = 0$ ,  $V_{DTV\_} = 1.5V$ , unless otherwise specified.  $DATA\_$  and  $RCV\_$  logic levels are  $V_{HIGH} = 2V$ ,  $V_{LOW} = 1V$ .
- Note 6:** Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.
- Note 7:** At the minimum voltage swing, undershoot is less than 20%.  $DHV\_$  and  $DLV\_$  references are adjusted to result in the specified swing.
- Note 8:** At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at  $DATA\_$ .
- Note 9:** With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.
- Note 10:** Relative to a straight line through 0 and 3V.
- Note 11:** Unless otherwise noted, all propagation delays are measured at 40MHz,  $V_{DUT\_} = 0$  to 1V,  $V_{CHV\_} = V_{CLV\_} = +0.5V$ ,  $t_R = t_F = 500ps$ ,  $Z_S = 50\Omega$ , driver in term mode with  $V_{DTV\_} = +0.5V$ . Comparator outputs are terminated with  $50\Omega$  to GND. Measured from  $V_{DUT\_}$  crossing calibrated  $CHV\_/CLV\_$  threshold to midpoint of nominal comparator output swing.
- Note 12:** Terminated is defined as driver in drive mode and set to zero volts.
- Note 13:** High impedance is defined as driver in high-impedance mode.
- Note 14:**  $V_{DUT\_} = 200mV_{P-P}$ . Propagation delay is compared to a reference time at 1.5V.
- Note 15:** The comparator meets all its timing specifications with the specified output conditions when the output current is less than 10mA,  $V_{COMP\ HI} > V_{COMP\ LO}$ , and  $V_{COMP\ HI} - V_{COMP\ LO} \leq 1V$ . Higher voltage swings are valid but AC performance may degrade. The maximum comparator output swing is  $(COMP\ HI - COMP\ LO) \leq 1V$  when the output is terminated with a  $50\Omega$  resistor to termination voltage  $V_{TERM}$ , where  $COMP\ HI \geq V_{TERM} \geq COMP\ LO$ .
- Note 16:**  $LOAD\ EN\ LOW = LOAD\ EN\ HIGH = 1$ .
- Note 17:** Waveform settles to within 5% of final value into load  $100k\Omega$ .
- Note 18:**  $IPMU\_ = \pm 2mA$  at  $V_{FORCE\_} = -2.2V$ ,  $+1.5V$ , and  $+5.2V$ . Percent variation relative to value calculated at  $V_{FORCE\_} = +1.5V$ .
- Note 19:** Time to return to the specified maximum leakage after a 3V, 4V/ns step at  $DUT\_$ .
- Note 20:** Load at end of 2ns transmission line; for stability only, AC performance may be degraded.
- Note 21:** The driver meets all of its timing specifications over the specified digital input voltage range.
- Note 22:** Timing characteristics with  $V_L = 3V$ .
- Note 23:** Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.
- Note 24:** All channels driven at  $3V_{P-P}$ , load = 2ns,  $50\Omega$  transmission line terminated with 3pF.

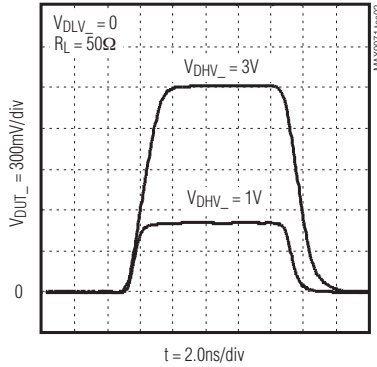
# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

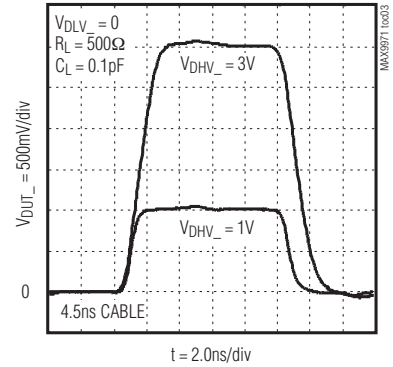
**DRIVER SMALL-SIGNAL RESPONSE**



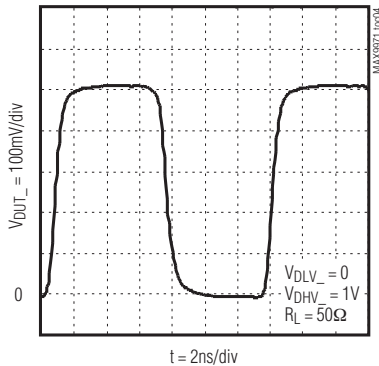
**DRIVER LARGE-SIGNAL RESPONSE**



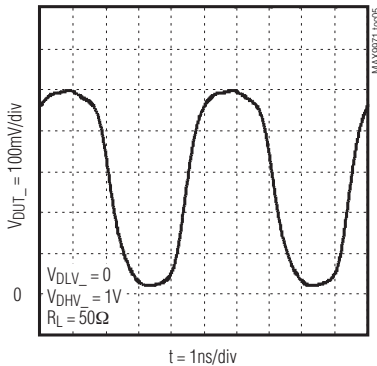
**DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω**



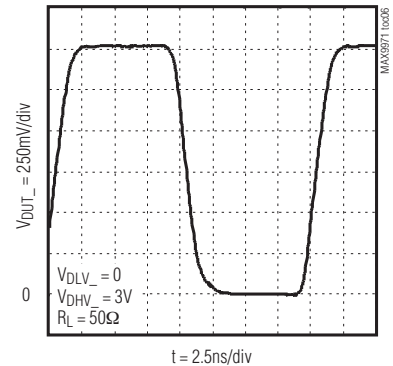
**DRIVER 1Vp-p, 150Mbps SIGNAL RESPONSE**



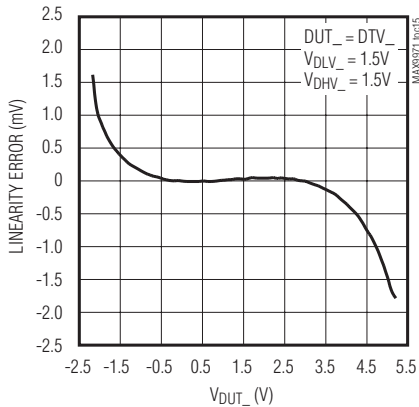
**DRIVER 1Vp-p, 400Mbps SIGNAL RESPONSE**



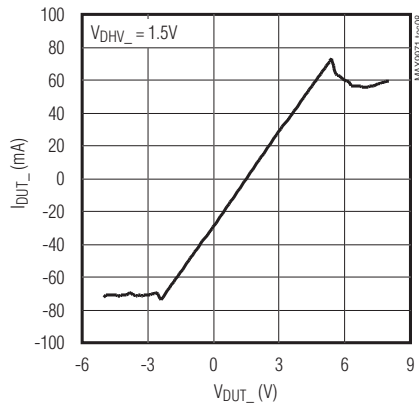
**DRIVER 3Vp-p, 100Mbps SIGNAL RESPONSE**



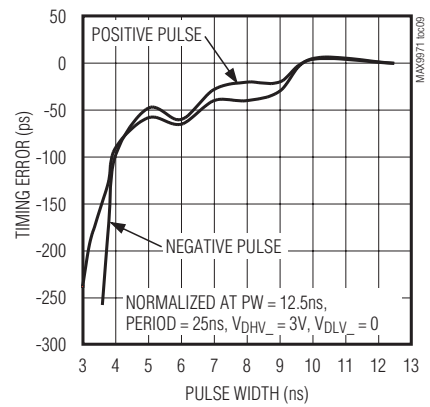
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



**DRIVER DC CURRENT-LIMIT AND OVERVOLTAGE RESPONSE**



**DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH**



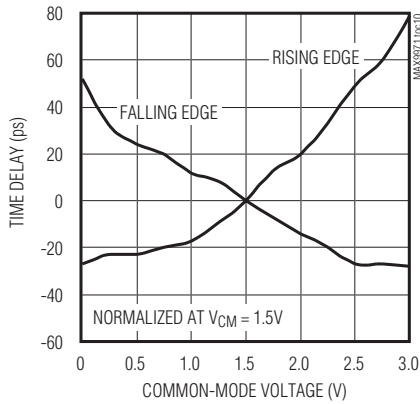
# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

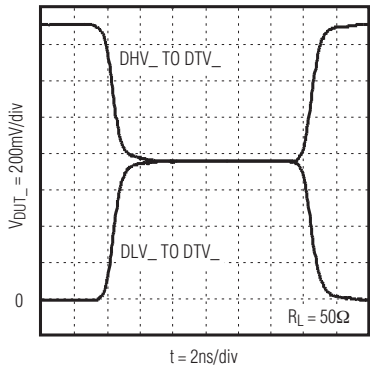
### Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

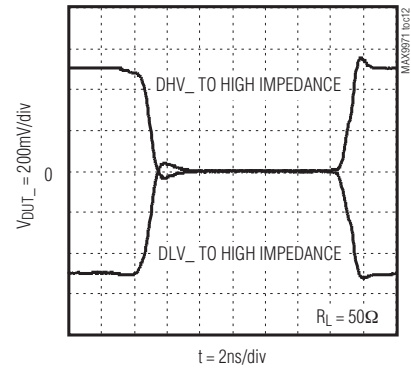
**DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE**



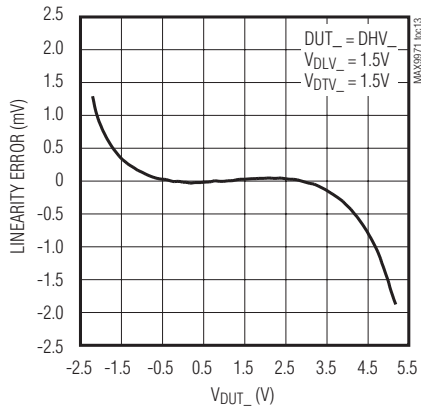
**DRIVE-TO-TERM TRANSITION**



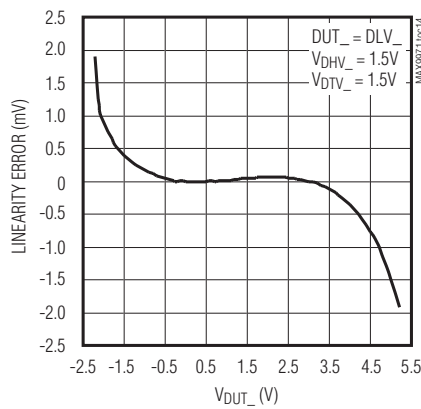
**DRIVE-TO-HIGH-IMPEDANCE TRANSITION**



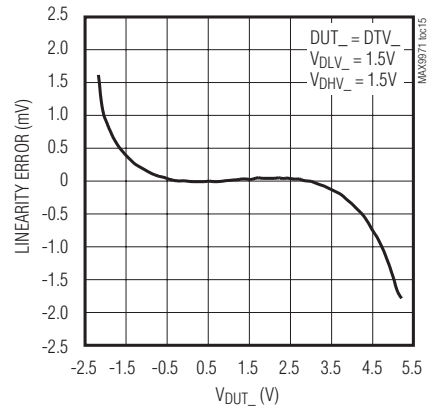
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



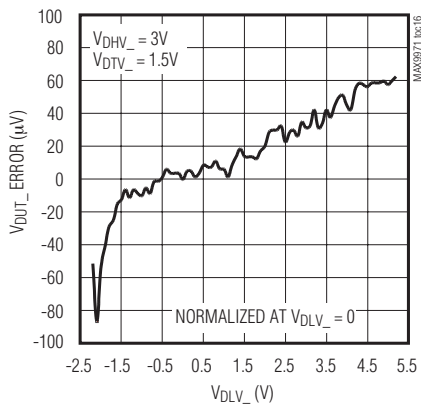
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



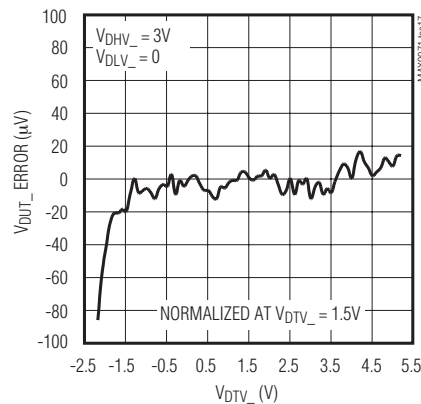
**DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE**



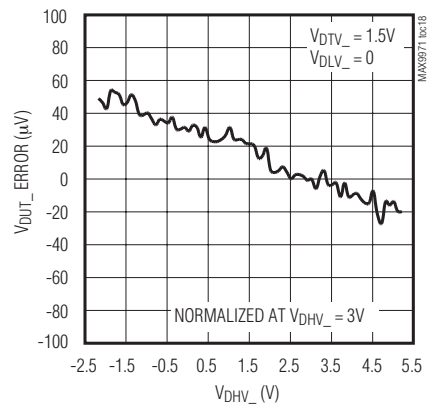
**CROSSTALK, DUT\_DRIVEN BY DHV WITH DLV VARIED**



**CROSSTALK, DUT\_DRIVEN BY DHV WITH DTV VARIED**



**CROSSTALK, DUT\_DRIVEN BY DLV WITH DHV VARIED**



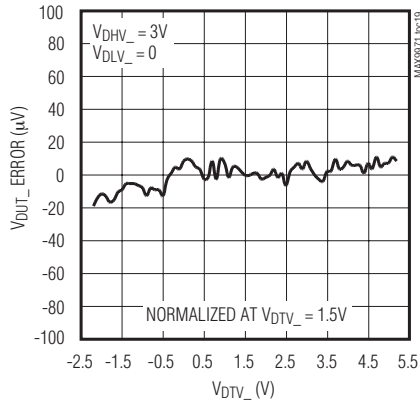
# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

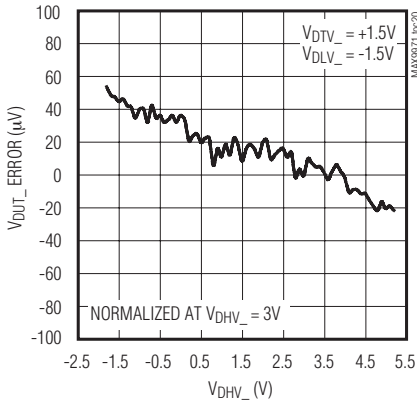
### Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

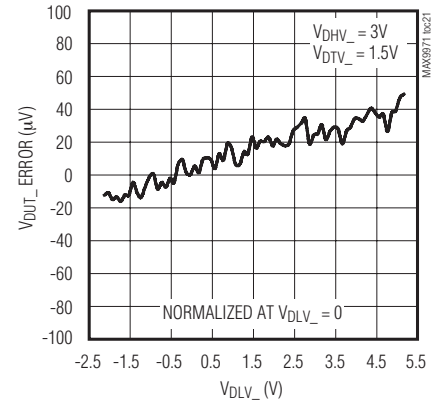
**CROSSTALK, DUT\_DRIVEN BY DLV\_WITH DTV\_VARIED**



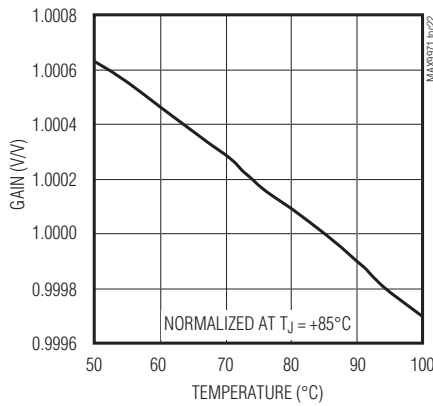
**CROSSTALK, DUT\_DRIVEN BY DTV\_WITH DHV\_VARIED**



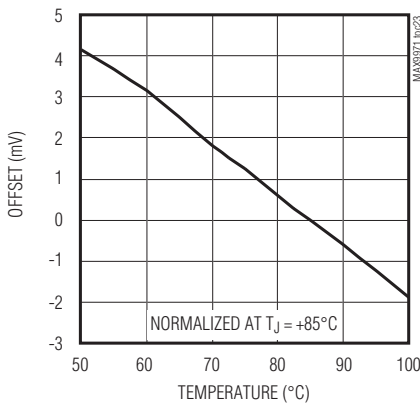
**CROSSTALK, DUT\_DRIVEN BY DTV\_WITH DLV\_VARIED**



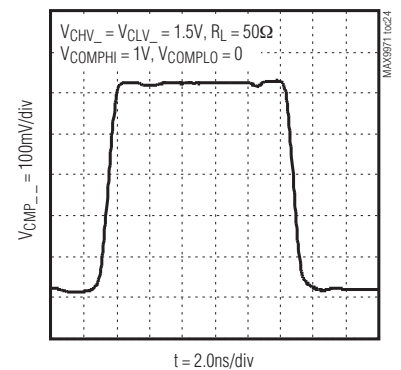
**DRIVER GAIN vs. TEMPERATURE**



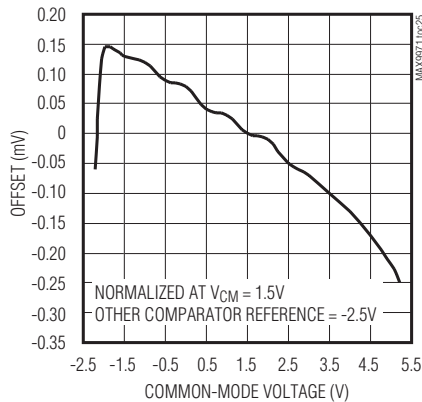
**DRIVER OFFSET vs. TEMPERATURE**



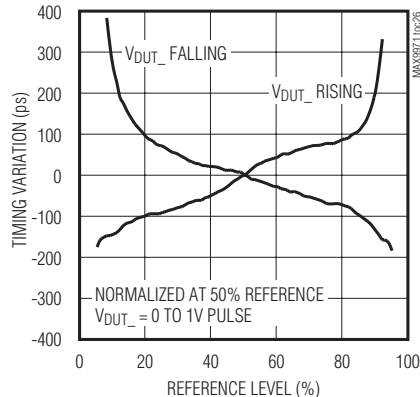
**COMPARATOR RESPONSE TO 0 TO 3V SIGNAL**



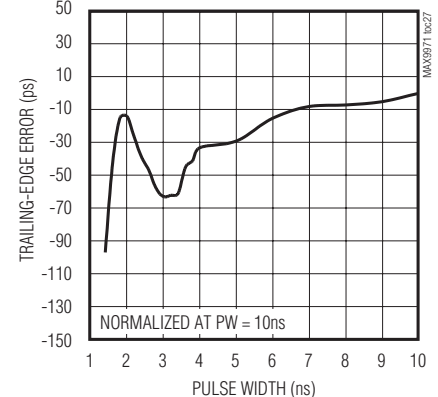
**COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE**



**COMPARATOR WAVEFORM TRACKING**



**COMPARATOR TIMING VARIATION vs. PULSE WIDTH**



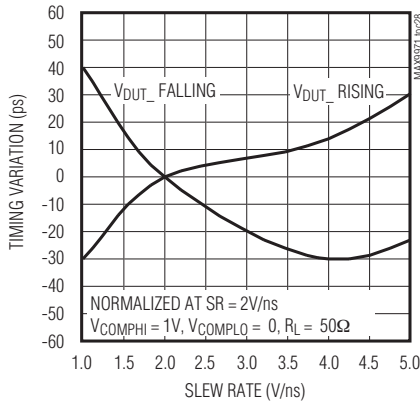
# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

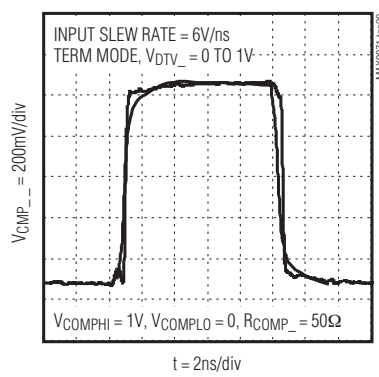
### Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

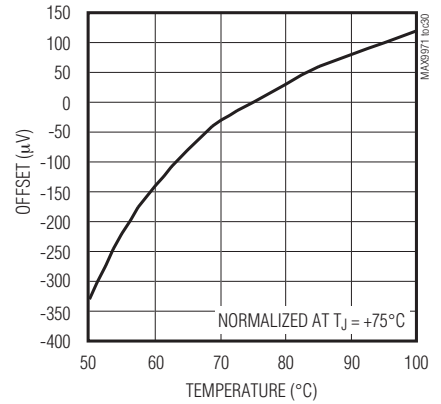
**COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE**



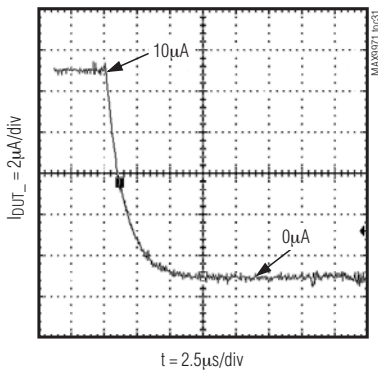
**COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE**



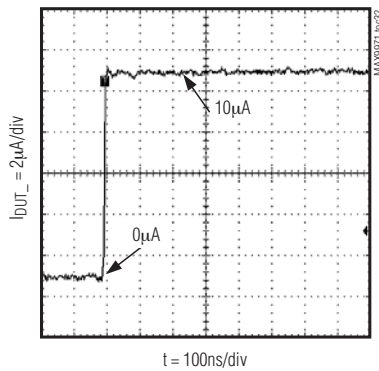
**COMPARATOR OFFSET vs. TEMPERATURE**



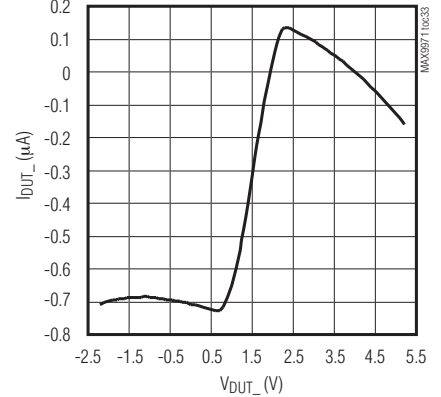
**DRIVE 1V TO LOW-LEAKAGE TRANSITION**



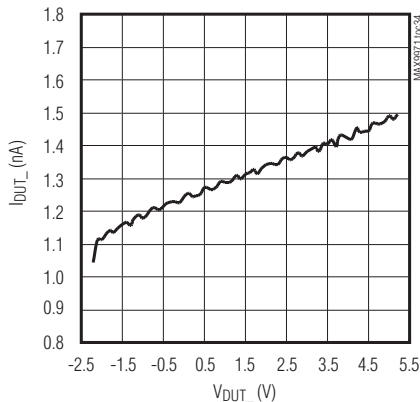
**LOW LEAKAGE TO DRIVE 1V TRANSITION**



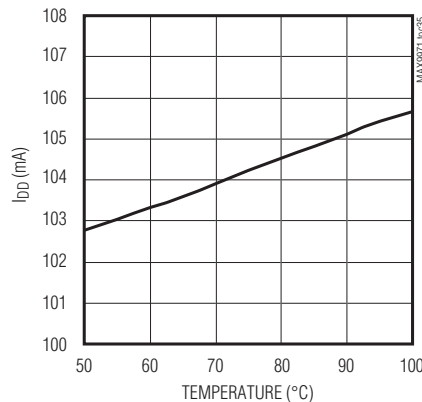
**HIGH-IMPEDANCE LEAKAGE AT DUT\_ vs. DUT\_ VOLTAGE**



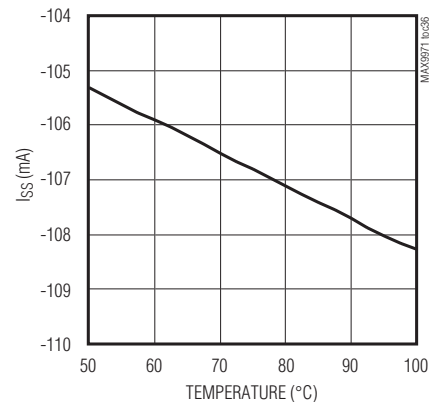
**LOW-LEAKAGE CURRENT vs. DUT\_ VOLTAGE**



**IDD SUPPLY CURRENT vs. TEMPERATURE**



**ISS SUPPLY CURRENT vs. TEMPERATURE**



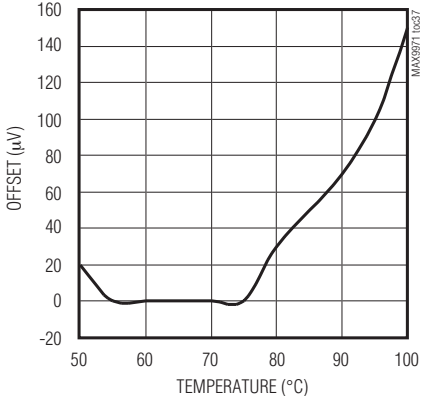
# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

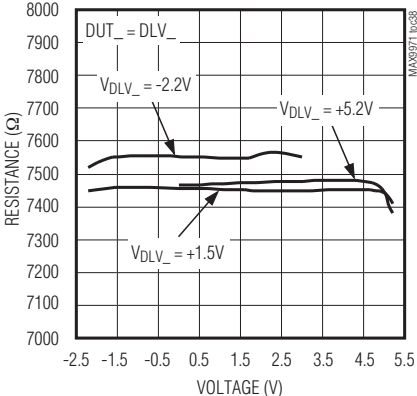
### Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

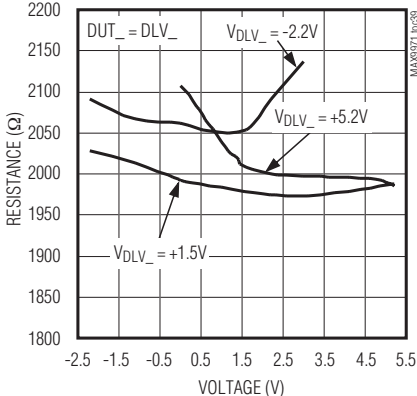
**PASSIVE LOAD OFFSET vs. TEMPERATURE**



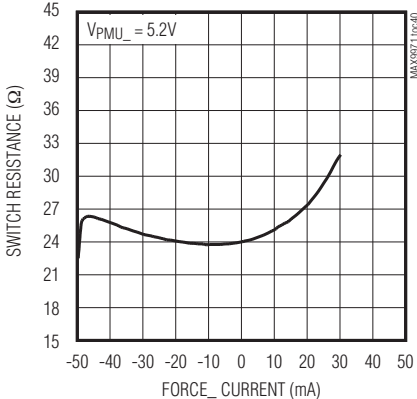
**PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE**



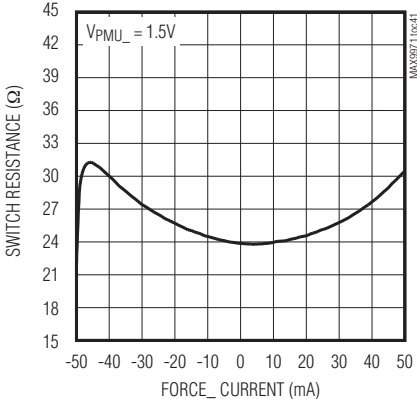
**PASSIVE LOAD LOW RESISTOR vs. VOLTAGE**



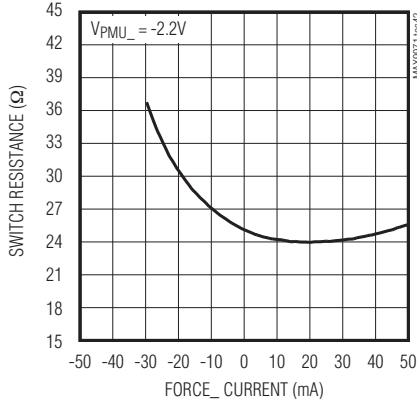
**PMU\_FORCE\_SWITCH RESISTANCE vs. FORCE\_CURRENT**



**PMU\_FORCE\_SWITCH RESISTANCE vs. FORCE\_CURRENT**



**PMU\_FORCE\_SWITCH RESISTANCE vs. FORCE\_CURRENT**



# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

### Pin Description

PIN	NAME	FUNCTION
1	DATA1	Channel 1 Multiplexer Control Input. Selects driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	RCV1	Channel 1 Multiplexer Control Input. Sets channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 8, 13, 18, 51	GND	Analog Ground
4	CMPH1	Channel 1 High-Side Comparator Output
5	CMPL1	Channel 1 Low-Side Comparator Output
6	DATA2	Channel 2 Multiplexer Control Input. Selects driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	RCV2	Channel 2 Multiplexer Control Input. Sets channel 2 mode to drive or receive. See Table 1 and Figure 2.
9	CMPH2	Channel 2 High-Side Comparator Output
10	CMPL2	Channel 2 Low-Side Comparator Output
11	CMPL3	Channel 3 Low-Side Comparator Output
12	CMPH3	Channel 3 High-Side Comparator Output
14	RCV3	Channel 3 Multiplexer Control Input. Sets channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	DATA3	Channel 3 Multiplexer Control Input. Selects driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	CMPL4	Channel 4 Low-Side Comparator Output
17	CMPH4	Channel 4 High-Side Comparator Output
19	RCV4	Channel 4 Multiplexer Control Input. Sets channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	DHV4	Channel 4 Driver High Voltage Input
22	DLV4	Channel 4 Driver Low Voltage Input
23	DTV4	Channel 4 Driver Termination Voltage Input
24	CHV4	Channel 4 Threshold Voltage Input for High-Side Comparator
25	CLV4	Channel 4 Threshold Voltage Input for Low-Side Comparator
26	DHV3	Channel 3 Driver High Voltage Input
27	DLV3	Channel 3 Driver Low Voltage Input
28	DTV3	Channel 3 Driver Termination Voltage Input
29	CHV3	Channel 3 Threshold Voltage Input for High-Side Comparator
30	CLV3	Channel 3 Threshold Voltage Input for Low-Side Comparator
31	DGND	Digital Ground Connection
32	DOUT	Serial-Interface Data Output
33	$\overline{\text{LD}}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.
34	DIN	Serial-Interface Data Input
35	SCLK	Serial Clock
36	$\overline{\text{CS}}$	Chip Select
37	SENSE4	Channel 4 PMU Sense Connection
38	FORCE4	Channel 4 PMU Force Connection

# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

### Pin Description (continued)

PIN	NAME	FUNCTION
39	SENSE3	Channel 3 PMU Sense Connection
40	FORCE3	Channel 3 PMU Force Connection
41	TEMP	Temperature Sensor Output
42, 47, 52, 56, 60	V <sub>DD</sub>	Positive Power-Supply Input
43	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	PMU4	Channel 4 Parametric Measurement Connection. PMU switch I/O node for channel 4.
45, 50, 53, 57	V <sub>SS</sub>	Negative Power-Supply Input
46	V <sub>L</sub>	Logic Power-Supply Input
48	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	PMU3	Channel 3 Parametric Measurement Connection. PMU switch I/O node for channel 3.
54	PMU2	Channel 2 Parametric Measurement Connection. PMU switch I/O node for channel 2.
55	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	PMU1	Channel 1 Parametric Measurement Connection. PMU switch I/O node for channel 1.
59	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61	FORCE2	Channel 2 PMU Force Connection
62	SENSE2	Channel 2 PMU Sense Connection
63	FORCE1	Channel 1 PMU Force Connection
64	SENSE1	Channel 1 PMU Sense Connection
65	COMPLO	Comparator Output-Low Voltage Reference Input
66	COMPHI	Comparator Output-High Voltage Reference Input
67	LDV4	Channel 4 Load Voltage Input
68	LDV3	Channel 3 Load Voltage Input
69	LDV2	Channel 2 Load Voltage Input
70	LDV1	Channel 1 Load Voltage Input
71	CLV2	Channel 2 Threshold Voltage Input for Low-Side Comparator
72	CHV2	Channel 2 Threshold Voltage Input for High-Side Comparator
73	DTV2	Channel 2 Driver Termination Voltage Input
74	DLV2	Channel 2 Driver Low Voltage Input
75	DHV2	Channel 2 Driver High Voltage Input
76	CLV1	Channel 1 Threshold Voltage Input for Low-Side Comparator
77	CHV1	Channel 1 Threshold Voltage Input for High-Side Comparator
78	DTV1	Channel 1 Driver Termination Voltage Input
79	DLV1	Channel 1 Driver Low Voltage Input
80	DHV1	Channel 1 Driver High Voltage Input
—	EP	Exposed Pad. Leave unconnected or connect to ground.



# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

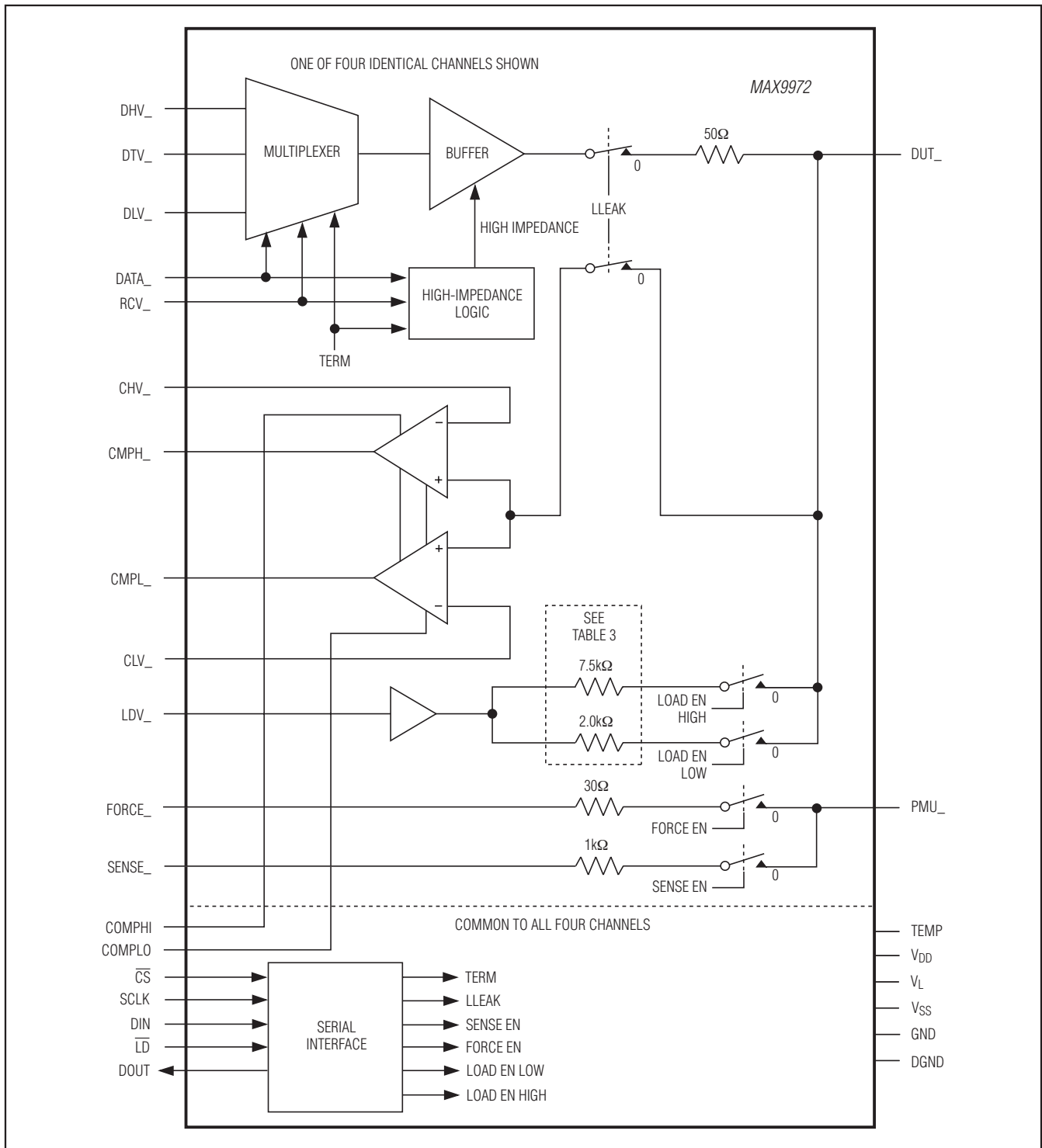


Figure 1. Block Diagram

# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

### Detailed Description

The MAX9972 is a four-channel, pin-electronics IC for automated test equipment that includes, for each channel, a three-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 1). All functions feature a -2.2V to +5.2V operating range and the drivers include both high-impedance and active-termination (3rd-level drive) modes. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT current loading. The Kelvin paths allow accurate connection of an instrument with  $\pm 25\text{mA}$  source/sink capability. Additionally, the MAX9972 offers a low-leakage mode that reduces DUT\_ leakage current to less than 20nA.

Each of the four channels feature single-ended CMOS-compatible inputs, DATA\_ and RCV\_, for control of the driver signal path (Figure 2). The MAX9972 modal operation is programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

### Output Driver

The driver input is a high-speed multiplexer that selects one of three voltage inputs: DHV\_, DLV\_, or DTV\_. This switching is controlled by high-speed inputs DATA\_ and RCV\_, and mode-control bit TERM (Table 1). DATA\_ and RCV\_ are single-ended inputs with threshold levels equal to  $V_I/2$ . Each channel's threshold levels are independently generated to minimize crosstalk.

DUT\_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 2, Table 1). High-speed input RCV\_ and mode-control bits TERM and LLEAK control these modes. In high-impedance mode, the bias current at DUT\_ is less than  $2\mu\text{A}$  over the -2.2V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT\_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is  $50\Omega$ . Custom resistance values from  $45\Omega$  to  $51\Omega$  are possible; consult factory for further information.

Table 1. Driver Channel Control Signals

EXTERNAL CONNECTIONS		INTERNAL CONTROL BITS		DRIVER OUTPUT	DRIVER MODE
RCV_	DATA_	TERM	LLEAK		
0	0	X	0	DUT_ = DLV_	Drive
0	1	X	0	DUT_ = DHV_	Drive
1	X	0	0	High Impedance	Receive
1	X	1	0	DUT_ = DTV_	Receive
X	X	X	1	Low Leak	Low Leakage

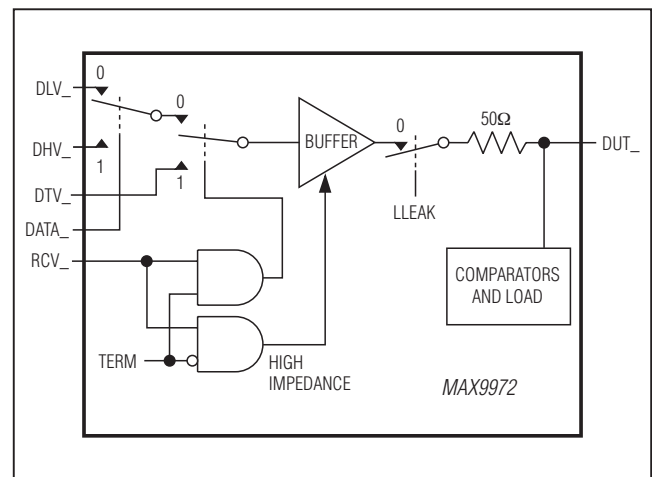


Figure 2. Multiplexer and Driver Channel

# MAX9972

## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

### Comparators

The MAX9972 provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT\_ and the other input connected to either CHV\_ or CLV\_ (see Figure 1). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPL0 to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPL0. The comparator 50Ω output impedance provides source termination (Figure 3).

### Passive Load

The MAX9972 channels each feature a passive load consisting of a buffered input voltage, LDV\_, connected to DUT\_ through two resistive paths (Figure 1). Each path connects to DUT\_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT\_ outputs.

### Parametric Switches

Each of the four MAX9972 channels provides force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 1). Each force-and-sense switch is independently controlled through the serial interface providing maximum application flexibility. PMU\_ and DUT\_ are provided on separate pins allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU\_. It also allows PMU\_ to connect to DUT\_ either directly or with an impedance-matching network.

### Low-Leakage Mode, LLEAK

Asserting LLEAK through the serial port places the MAX9972 into a very-low-leakage state (see the *Electrical Characteristics* table). This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK control is independent for each channel.

When DUT\_ is driven with a high-speed signal while LLEAK is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* table indicates device behavior under this condition.

Table 2. Comparator Logic

DUT_ > CHV_	DUT_ > CLV_	CMPH_	CMPL_
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

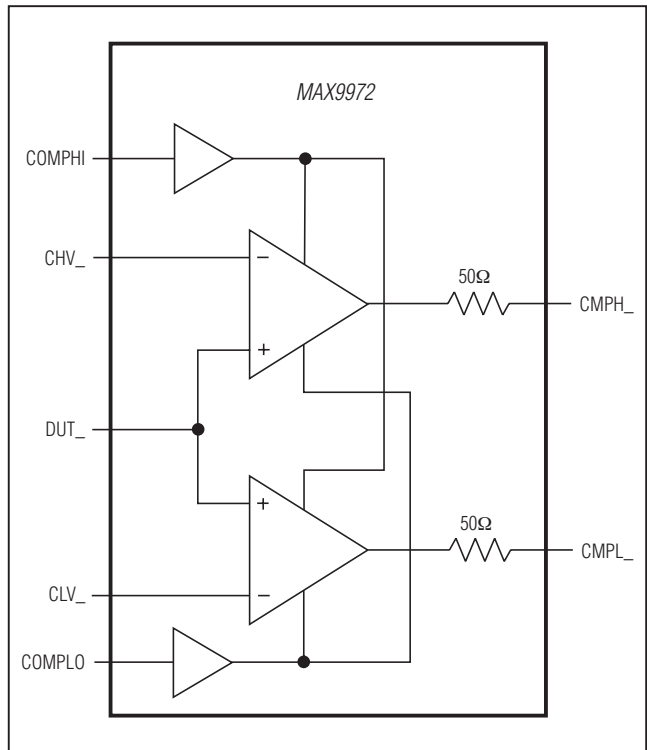


Figure 3. Complementary 50Ω Comparator Outputs

Table 3. Passive Load Resistance Values

HIGH RESISTOR (kΩ)	LOW RESISTOR (kΩ)
7.5	2

### Temperature Monitor

Each device supplies a single temperature output signal, TEMP, that asserts a nominal 3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 500Ω, typical.

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## Quad, Ultra-Low-Power, 300Mbps ATE Drivers/Comparators

### Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9972 modes (Figure 4). Control data flow into a 12-bit shift register (LSB first) and are latched when  $\overline{CS}$  is taken high. Data from the shift register are then loaded to the per-channel control latches as determined by bits D8–D11, and indicated in Figure 4 and Table 4.

The latches contain the six mode bits for each channel of the device. The mode bits, in conjunction with external inputs  $DATA_$  and  $RCV_$ , manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing  $\overline{LD}$  low. With  $\overline{LD}$  always low, data transfer on the rising edge of  $\overline{CS}$ .

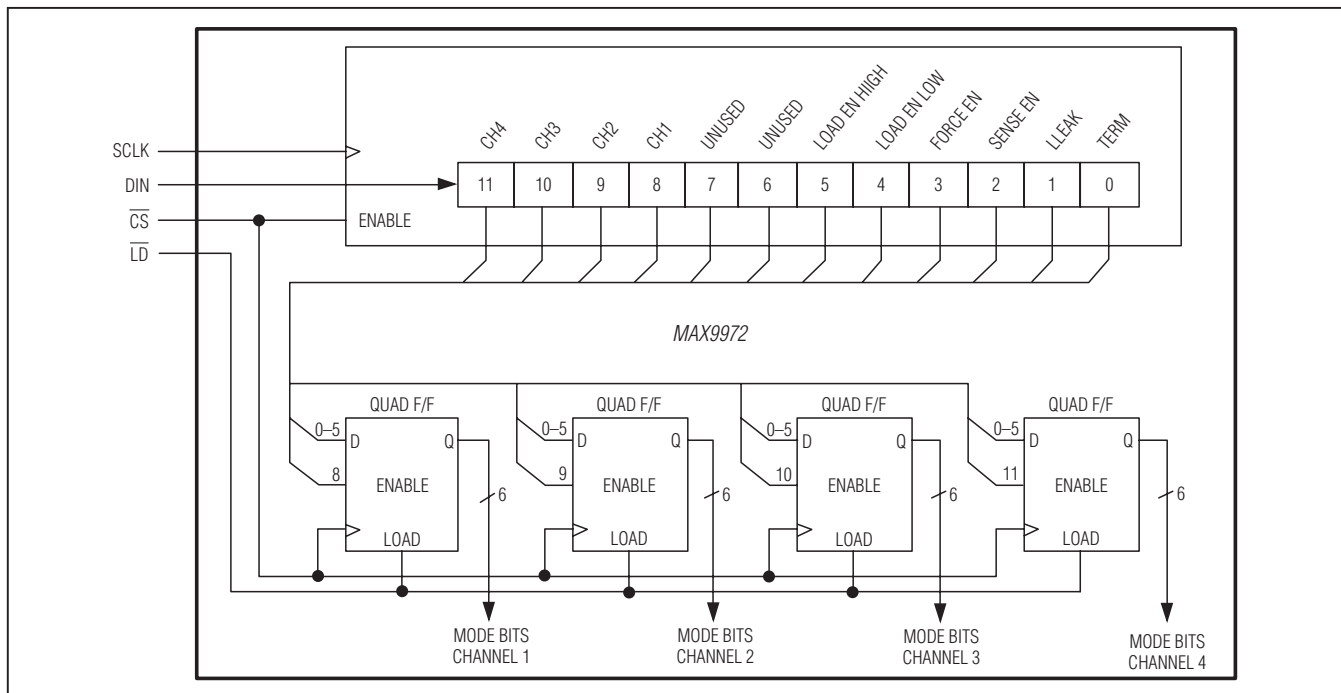


Figure 4. Serial Interface

Table 4. Control Register Bit Functions

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
0	TERM	Term Mode Control	High Impedance	Term Mode	0
1	LLEAK	Assert Low-Leakage Mode	Term Mode	Low Leakage	0
2	SENSE EN	Enable Sense Switch	Disabled	Enabled	0
3	FORCE EN	Enable Force Switch	Disabled	Enabled	0
4	LOAD EN LOW	Enable Low Load Resistor	Disabled	Enabled	0
5	LOAD EN HIGH	Enable High Load Resistor	Disabled	Enabled	0
6	—	Unused	X	X	0
7	—	Unused	X	X	0
8	CH1	Update Channel 1 Control Register	Disabled	Enabled	1
9	CH2	Update Channel 2 Control Register	Disabled	Enabled	1
10	CH3	Update Channel 3 Control Register	Disabled	Enabled	1
11	CH4	Update Channel 4 Control Register	Disabled	Enabled	1

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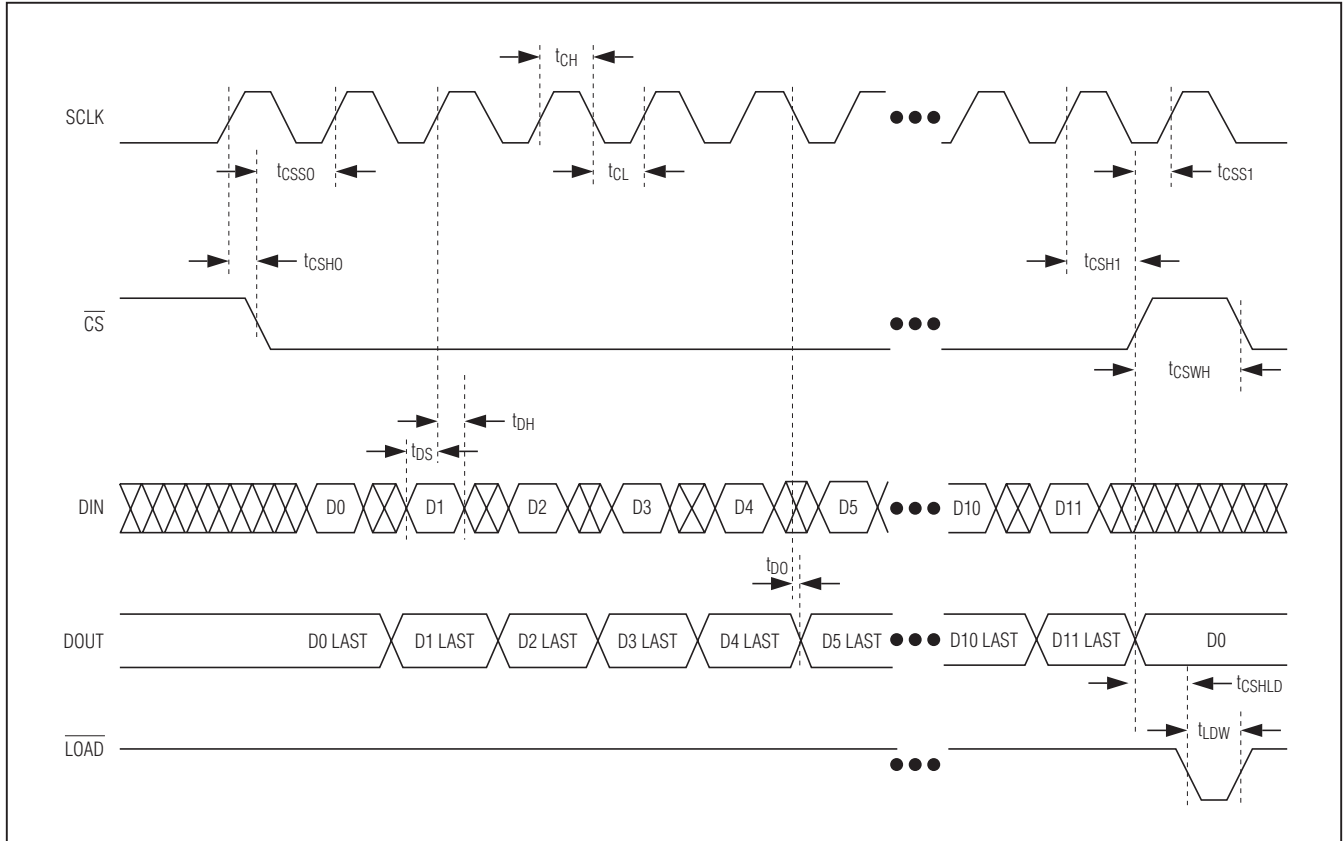


Figure 5. Serial-Interface Timing

### Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed pad, solder it to circuit board copper. The exposed pad must be either left unconnected, isolated, or connected to ground.

### Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

### Chip Information

PROCESS: BiCMOS

### Package Information

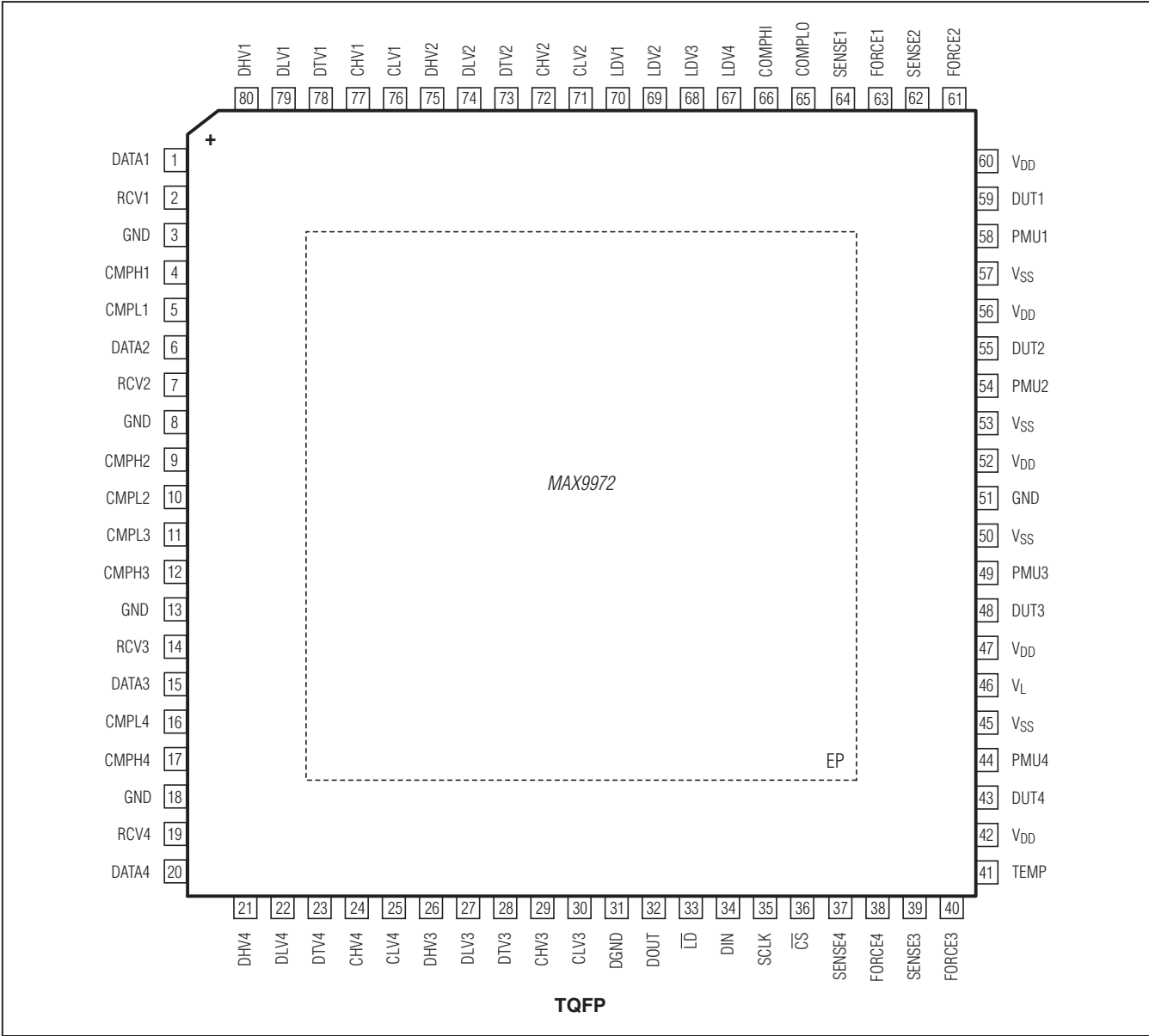
For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
80 TQFP-EP	C80E+4	<a href="#">21-0115</a>	<a href="#">90-0152</a>

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### Pin Configuration



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### Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/06	Initial release	—
1	7/09	Changed driver offset max value in <i>Electrical Characteristics</i> table and removed all references to MAX9971	1–22
2	4/10	Added soldering temperature to <i>Absolute Maximum Ratings</i> , updated SCLK to DOUT specification in <i>Electrical Characteristics</i> table, and replaced Figure 5	2, 7, 20
3	9/10	Updated <i>Absolute Maximum Ratings</i> and Figure 1	2, 16
4	12/10	Updated <i>Electrical Characteristics</i> table and notes	3, 4, 7, 8
5	1/11	Changed maximum DC drive current in <i>Electrical Characteristics</i> table to reflect actual circuit operation	2
6	3/11	Narrowed down product offerings and modified exposed die pad connection description; added CS high pulse width to <i>Electrical Characteristics</i> table	1, 2, 4, 5, 7, 15, 17, 18, 20
7	6/11	Corrected/changed SPI timing parameters to improve yield and changed global levels for V <sub>COMPHI</sub> and V <sub>COMPL0</sub>	2–8
8	6/11	Restored original global levels changed in Rev 7	2–8
9	10/11	Corrected value for Temp Sensor nominal voltage	7
10	7/14	Corrected <i>General Description</i>	1



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