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MAXM17761

4.5V to 76V,1A High-Efficiency DC-DC Step-Down Power Module with Integrated Inductor

General Description

The *Himalaya* series of voltage regulator ICs and Power Modules enable cooler, smaller, and simpler power supply solutions. The MAXM17761 is an easy-to-use power module that combines a synchronous step down DC-DC converter with integrated FETs, a fully shielded inductor, and the compensation components into a low-profile, thermally-efficient, system-in-package (SiP). The device operates over a wide input voltage range of 4.5V to 76V and delivers up to 1A continuous output current with excellent line and load regulation over an output voltage range of 0.8V to 5V. The device only requires five external components to complete the total power solution. The high level of integration significantly reduces design complexity, manufacturing risks, and offers a true plug-and-play power supply solution, reducing time-to-market.

The device offers resistor programmable switching frequency, $\overline{\text{RESET}}$ output voltage monitoring, adjustable input undervoltage lockout and programmable soft-start. The device also features robust overload protection and a thermal shutdown function.

The MAXM17761 is available in a low-profile, highly thermal-emissive, compact, 28-pin 6.5mm x 10mm x 2.92mm SiP package that reduces power dissipation in the package and enhances efficiency. The package is easily soldered onto a printed circuit board and is suitable for automated circuit board assembly. The device can operate over the full industrial temperature range from -40°C to $+125^{\circ}\text{C}$.

Applications

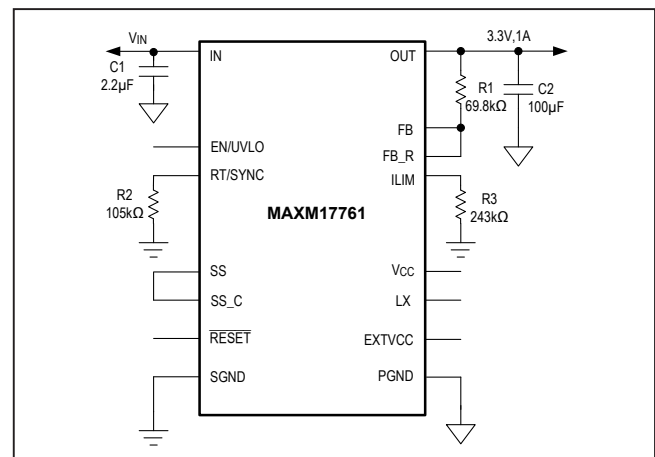
- Industrial Power Supplies
- Distributed Supply Regulation
- FPGA and DSP Point-of-Load Regulator
- Base Station Point-of-Load Regulator
- HVAC and Building Control

[Ordering Information](#) appears at end of data sheet.

Benefits and Features

- Reduces Design Complexity, Manufacturing Risks, and Time-to-Market
 - Synchronous Step-Down DC-DC Converter With Integrated FETs
 - Integrated Inductor
 - Integrated Compensation Components
- Saves Board Space in Space-Constrained Applications
 - Complete Integrated Step-Down Power Supply in a Single Package
 - Small Profile 6.5mm x 10mm x 2.92mm SiP Package
 - Simplified PCB Design with Minimal External BOM Components
- Offers Flexibility for Power-Design Optimization
 - Wide Input Voltage Range from 4.5V to 76V
 - Output-Voltage Adjustable Range from 0.8V to 5V
 - Adjustable Frequency with External Synchronization (180kHz to 537kHz)
 - Soft-Start Programmable
 - Optional Programmable EN/UVLO
- Operates Reliably in Adverse Industrial Environments
 - Integrated Thermal Fault Protection
 - Robust Overcurrent Protection
 - $\overline{\text{RESET}}$ Output Voltage Monitoring
 - High Industrial -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature Range/ -40°C to $+150^{\circ}\text{C}$ Junction Temperature Range

Typical Application Circuit



Absolute Maximum Ratings (Note 1)

IN to SGND	-0.3V to +80V	PGND to SGND.....	-0.3V to +0.3V
LX to PGND.....	-0.3V to $V_{IN} + 0.3V$	Operating Temperature Range.....	-40°C to +125°C
OUT to PGND ($V_{IN} < 6.3V$).....	-0.3V to $V_{IN} + 0.3V$	Junction Temperature.....	+150°C
OUT to PGND ($V_{IN} > 6.3V$).....	-0.3V to +6.3V	Storage Temperature Range	-55°C to +125°C
EN/UVLO, EXT \overline{VCC} to SGND	-0.3V to +26V	Lead Temperature (soldering, 10s)	+250°C
FB, FB \overline{R} , \overline{RESET} , SS, SS \overline{C} , V_{CC} , RT, ILIM to SGND.....	-0.3V to +6V	Soldering Temperature (reflow).....	+250°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 28PIN-SiP	
Package Code	L286510#8
Outline Number	<u>21-100181</u>
Land Pattern Number	<u>90-100059</u>
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction-to-Ambient Thermal Resistance (θ_{JA})	22.5°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

- Note 1:** Junction temperature greater than +125°C degrades operating lifetimes.
- Note 2:** Package thermal resistance is measured on evaluation board with natural convection.

Electrical Characteristics

($V_{IN} = 24V$, $V_{EN/UVLO} =$ unconnected, $R_{RT} = 69.8\text{ k}\Omega$ ($f_{SW} = 537\text{kHz}$). V_{PGND} , $V_{SGND} = 0V$, V_{CC} , LX, SS, \overline{RESET} , OUT = open. $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{IN}		4.5		76	V
Input Shut-down Current	I_{IN-SH}	$V_{EN/UVLO} = 0V$ (shutdown mode)	2.5	5	10	μA
Input Quiescent Current	I_{Q-PWM}	$R_{ILIM} = 243\text{k}\Omega$	3	4	5	mA
EN/UVLO						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.09	1.115	1.14	
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, true shutdown		0.7		
Enable Pullup Current	I_{EN}	$V_{EN/UVLO} = 1.215V$	2.2	2.5	2.8	μA

Electrical Characteristics (continued)

($V_{IN} = 24V$, $V_{EN/UVLO} = \text{unconnected}$, $R_{RT} = 69.8\text{ k}\Omega$ ($f_{SW} = 537\text{kHz}$). V_{PGND} , $V_{SGND} = 0V$, V_{CC} , LX, SS, $\overline{\text{RESET}}$, OUT = open. $T_A = -40^\circ\text{C}$ to 125°C , unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$. All voltages are referenced to SGND, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO						
V_{CC} Output Voltage Range	V_{CC}	$6V < V_{IN} < 76V$, $0\text{mA} < I_{VCC} < 5\text{mA}$	4.75	5	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	$V_{CC} = 4.3V$, $V_{IN} = 12V$	13	26	52	mA
V_{CC} Dropout	V_{CC-DO}	$V_{IN} = 4.5V$, $I_{VCC} = 5\text{mA}$			0.25	V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} Rising	4.05	4.2	4.35	V
	V_{CC-UVF}	V_{CC} Falling	3.65	3.8	3.95	
EXT LDO						
EXTVCC Switchover Threshold		EXTVCC rising	4.65	4.744	4.85	V
		Hysteresis		0.3		V
EXTVCC Dropout	EXTVCC-DO	EXTVCC = 4.75V, $I_{VCC} = 5\text{mA}$			0.1	V
EXTVCC Current Limit	$E_{VCC-MAX}$	$V_{CC} = 4.3V$, EXTVCC = 5V	15	21	60	mA
SOFT-START						
Charging Current	I_{SS}		4.7	5	5.3	μA
Soft-start capacitor	SS_C-internal			6800		pF
OUTPUT SPECIFICATIONS						
Line Regulation Accuracy		$V_{IN} = 10V$ to 76V, $V_{OUT} = 5V$		0.1		mV/V
Load Regulation Accuracy		Tested with $I_{OUT} = 0A$ and 1A		1		mV/A
FB Regulation Voltage	V_{FB-REG}	$R_{ILIM} = 243\text{k}\Omega$	0.788	0.8	0.812	V
FB Input Leakage Current	I_{FB}	$V_{FB} = 1V$, $T_A = 25^\circ\text{C}$	-100		+100	nA
Feedback Resistor	FB_R			22.1		k Ω
CURRENT LIMIT						
Average Current Limit Threshold	$I_{AVG-LIMIT}$	Source, $V_{OUT} = 5V$, $R_{ILIM} = 243\text{k}\Omega$		1.4		A
		Sink, $V_{FB} > V_{FB-REG}$, $R_{ILIM} = 243\text{k}\Omega$		0.49		
OSCILLATOR						
Switching Frequency	f_{SW}	$R_{RT} = 210\text{k}\Omega$	160	180	200	kHz
		$R_{RT} = 140\text{k}\Omega$	247	271	303	
		$R_{RT} = 105\text{k}\Omega$	324	360	396	
		$R_{RT} = 69.8\text{k}\Omega$	495	537	605	
Switching Frequency Adjustable Range			180		550	kHz
SYNC Input Frequency			1.15x			kHz
SYNC Pulse Minimum Off time			40			ns
SYNC High Threshold	V_{SYNC-H}		1	1.22	1.44	V
Hysteresis	$V_{SYNC-HYS}$			0.18		V
Number of SYNC Pulses to Enable Synchronization				1		Cycle

Electrical Characteristics (continued)

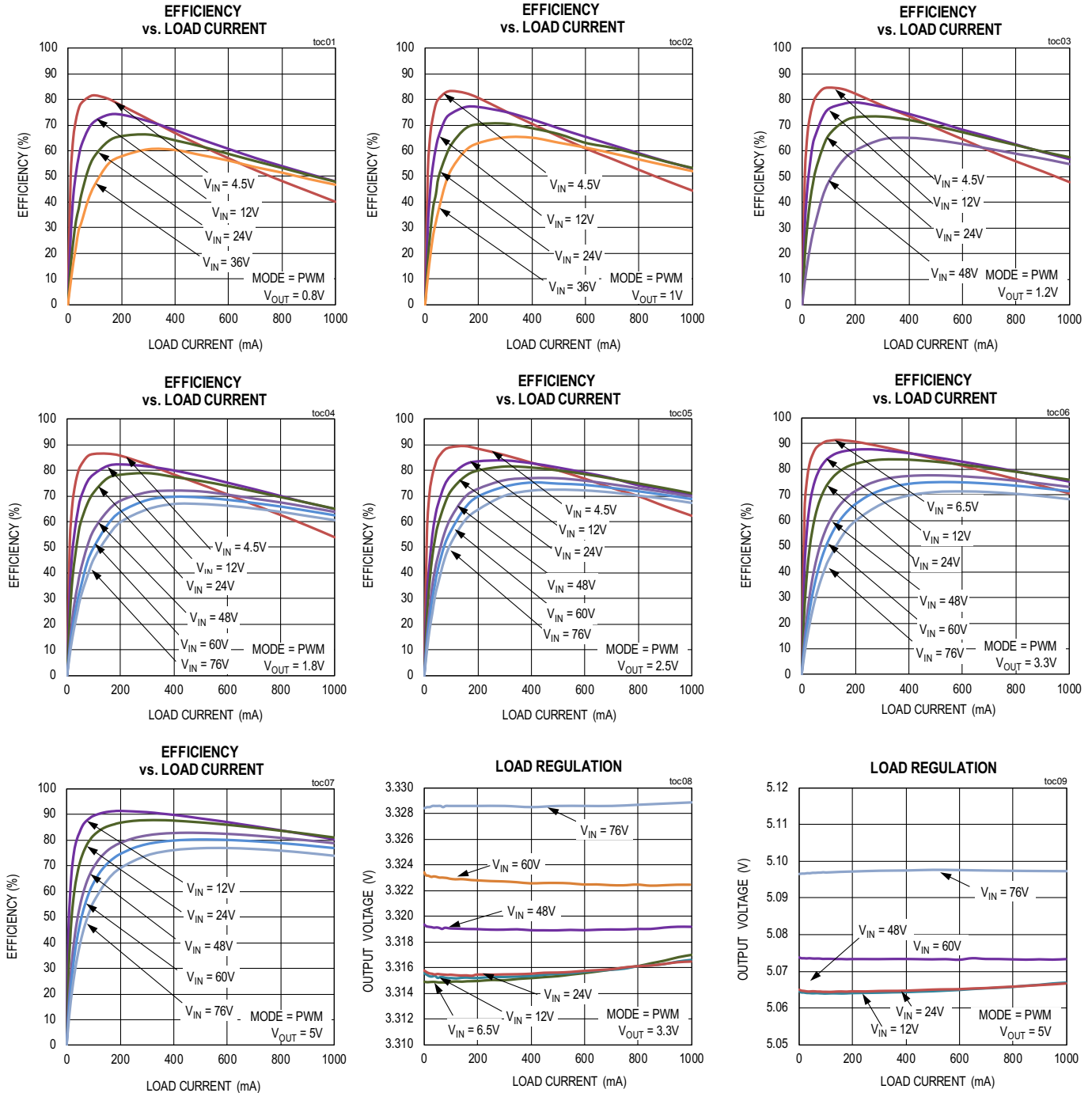
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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RESET						
$\overline{\text{RESET}}$ Output Level Low		$I_{\overline{\text{RESET}}} = 1\text{mA}$			0.07	V
$\overline{\text{RESET}}$ Output leakage Current		$V_{FB} = 1.01 \times V_{FB-REG}$, $T_A = +25^\circ\text{C}$			1	μA
FB Threshold for $\overline{\text{RESET}}$ Rising	V_{FB-OKR}	V_{FB} rising		95		%
FB Threshold for $\overline{\text{RESET}}$ Falling	V_{FB-OKF}	V_{FB} falling		92		%
$\overline{\text{RESET}}$ Delay After FB Reaches 95% Regulation				2.1		ms
TIMINGS						
Minimum On-Time	t_{ON-MIN}		45	70	115	ns
Maximum Duty Cycle	D_{MAX}		90	93	97	%
THERMAL SHUTDOWN						
Thermal Shutdown Threshold		Temperature rising		160		$^\circ\text{C}$
Thermal Shutdown Hysteresis				20		$^\circ\text{C}$

Note 3: Electrical specifications are production tested at $T_A = +25^\circ\text{C}$. Specifications over the entire operating temperature range are guaranteed by design and characterization.

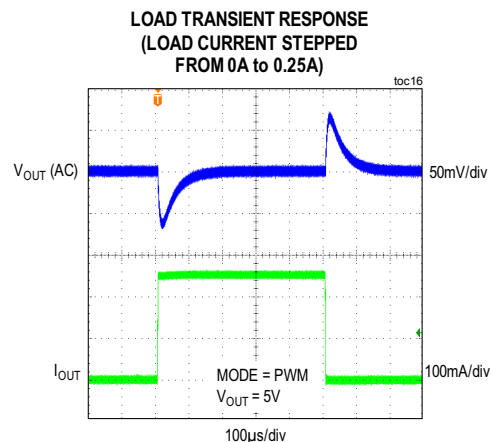
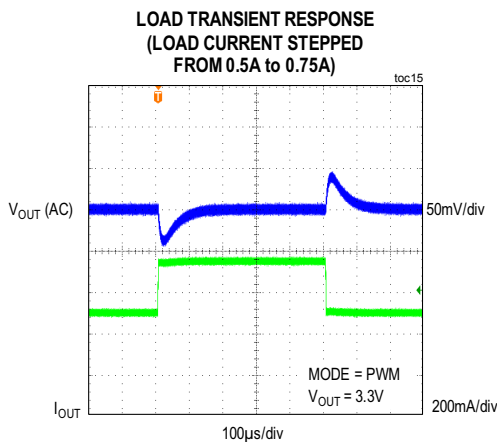
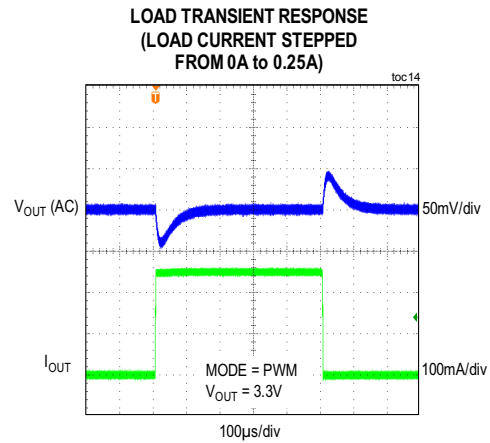
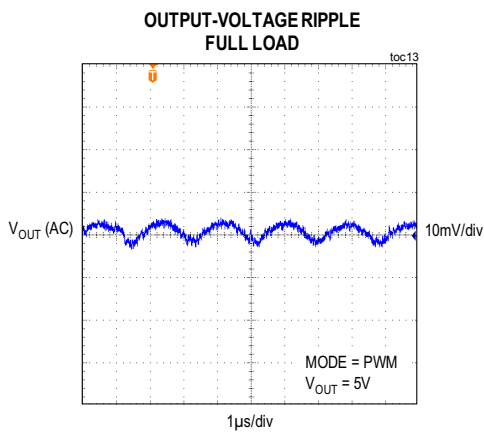
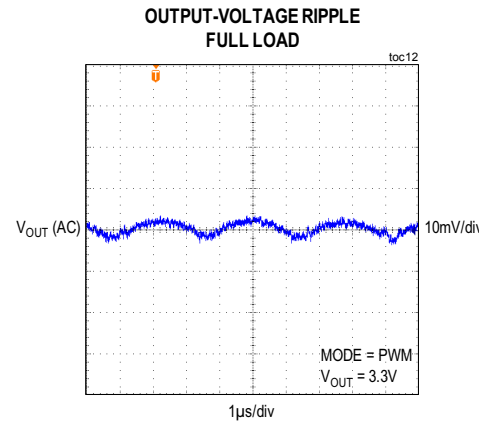
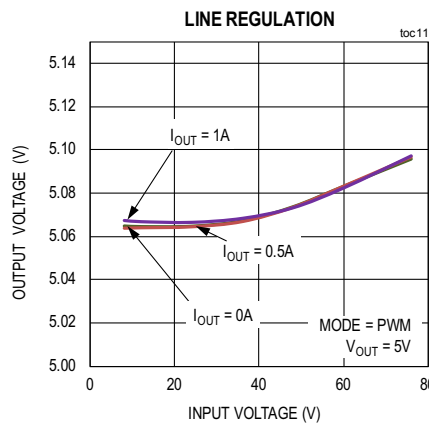
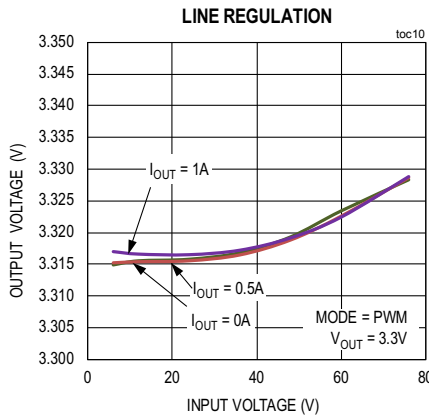
Typical Operating Characteristics

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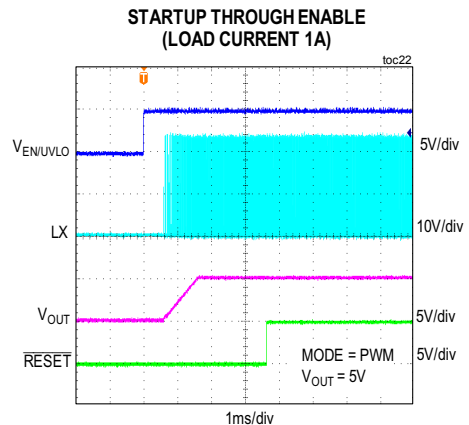
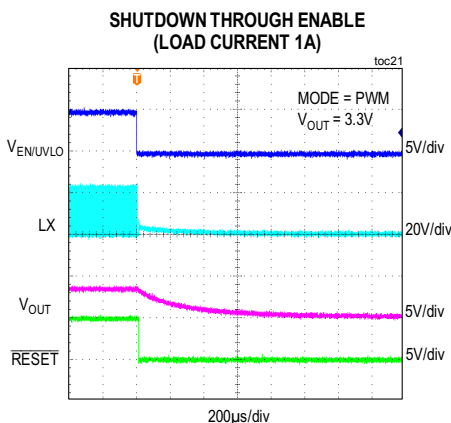
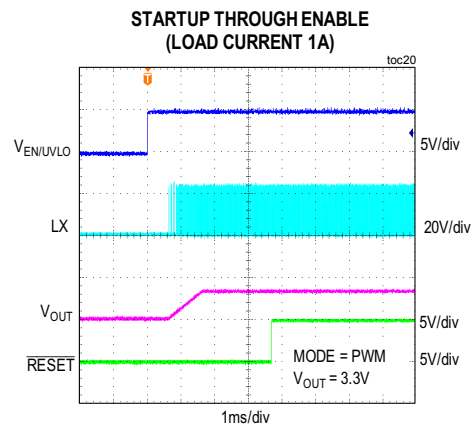
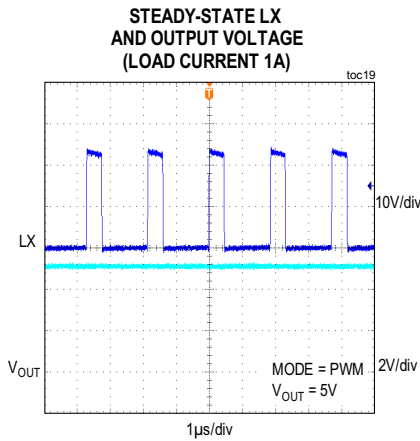
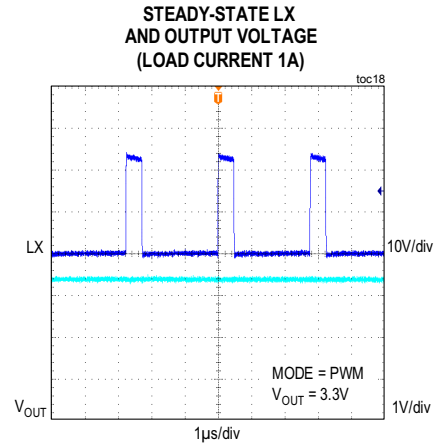
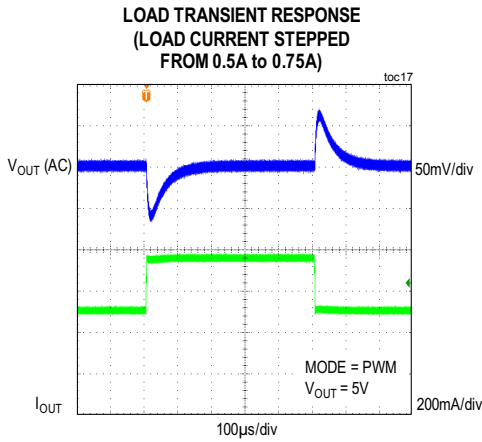
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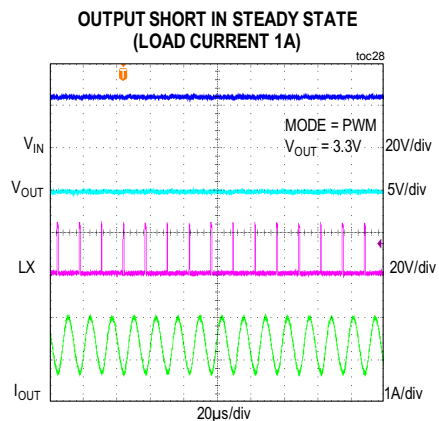
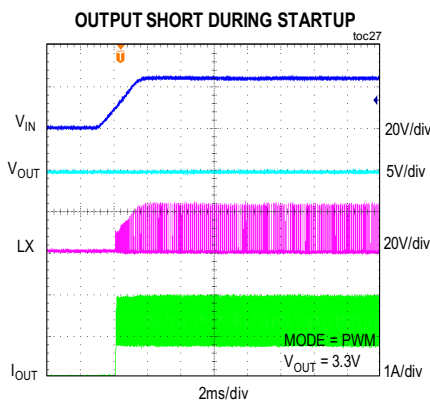
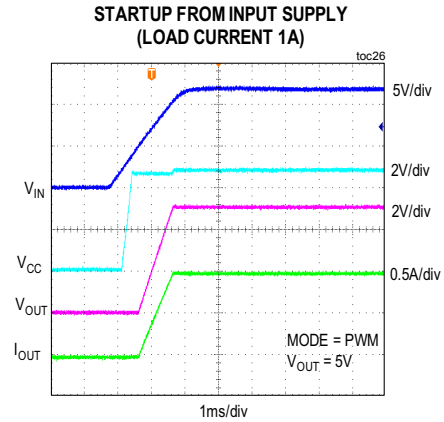
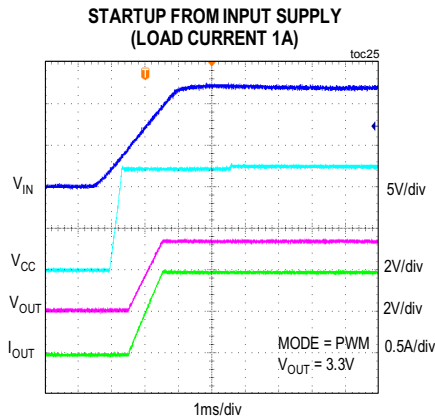
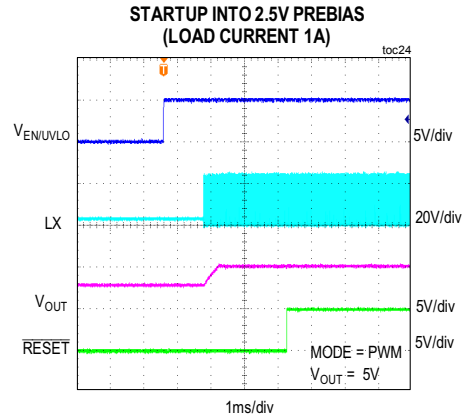
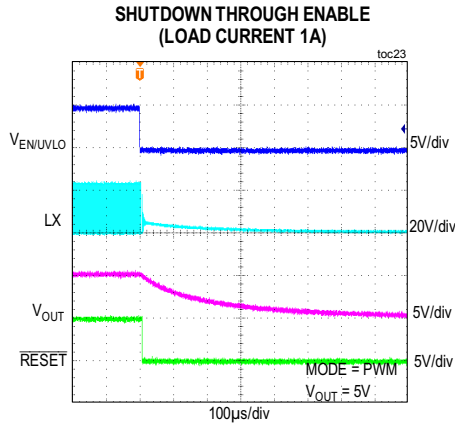
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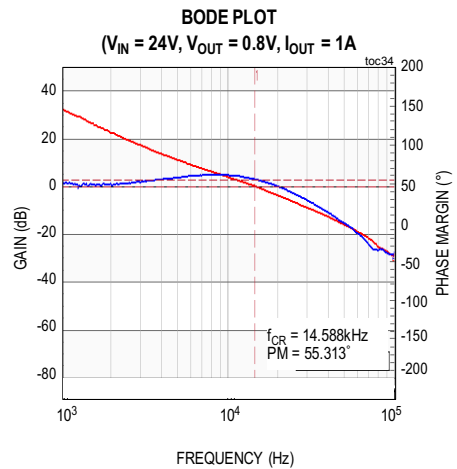
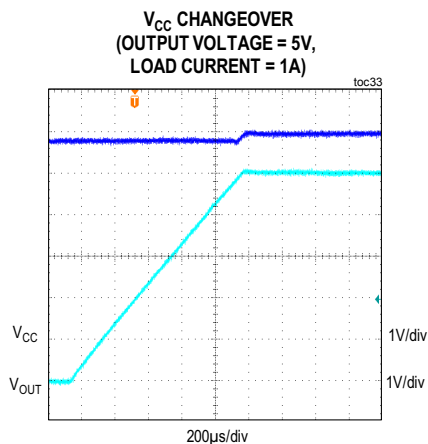
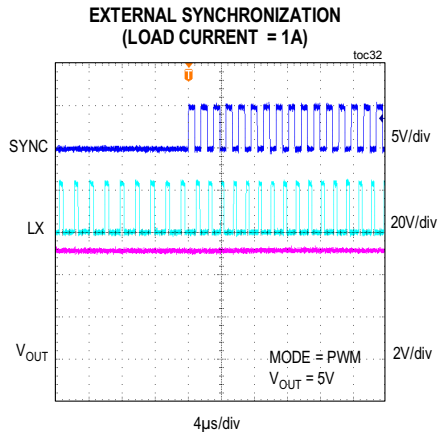
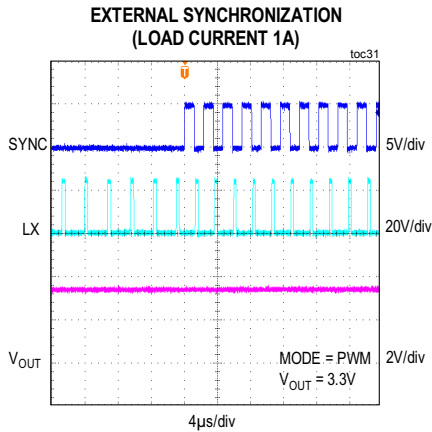
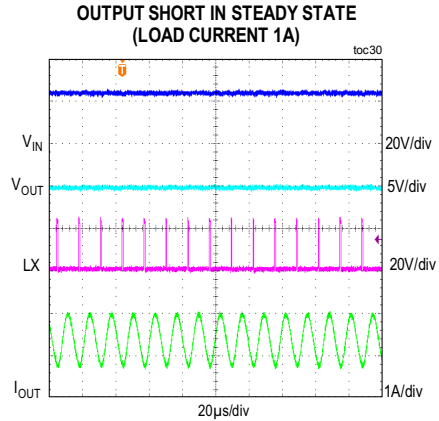
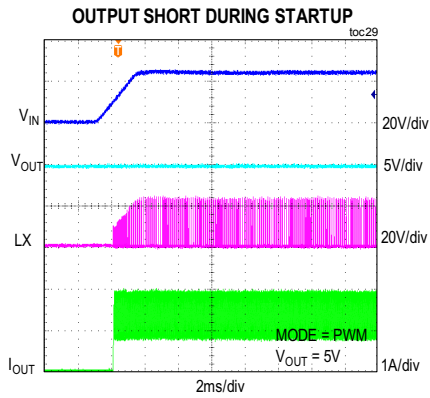
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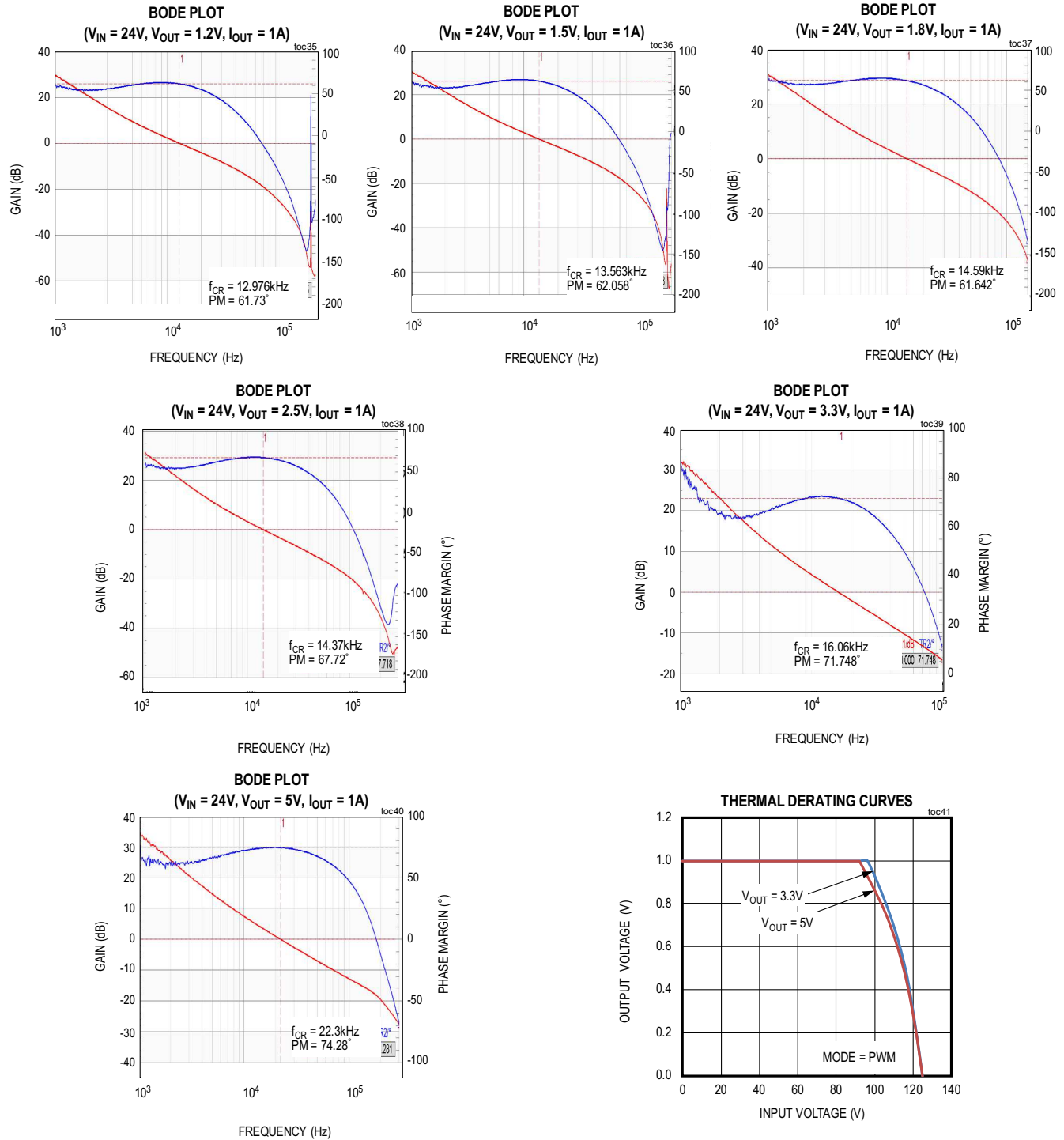
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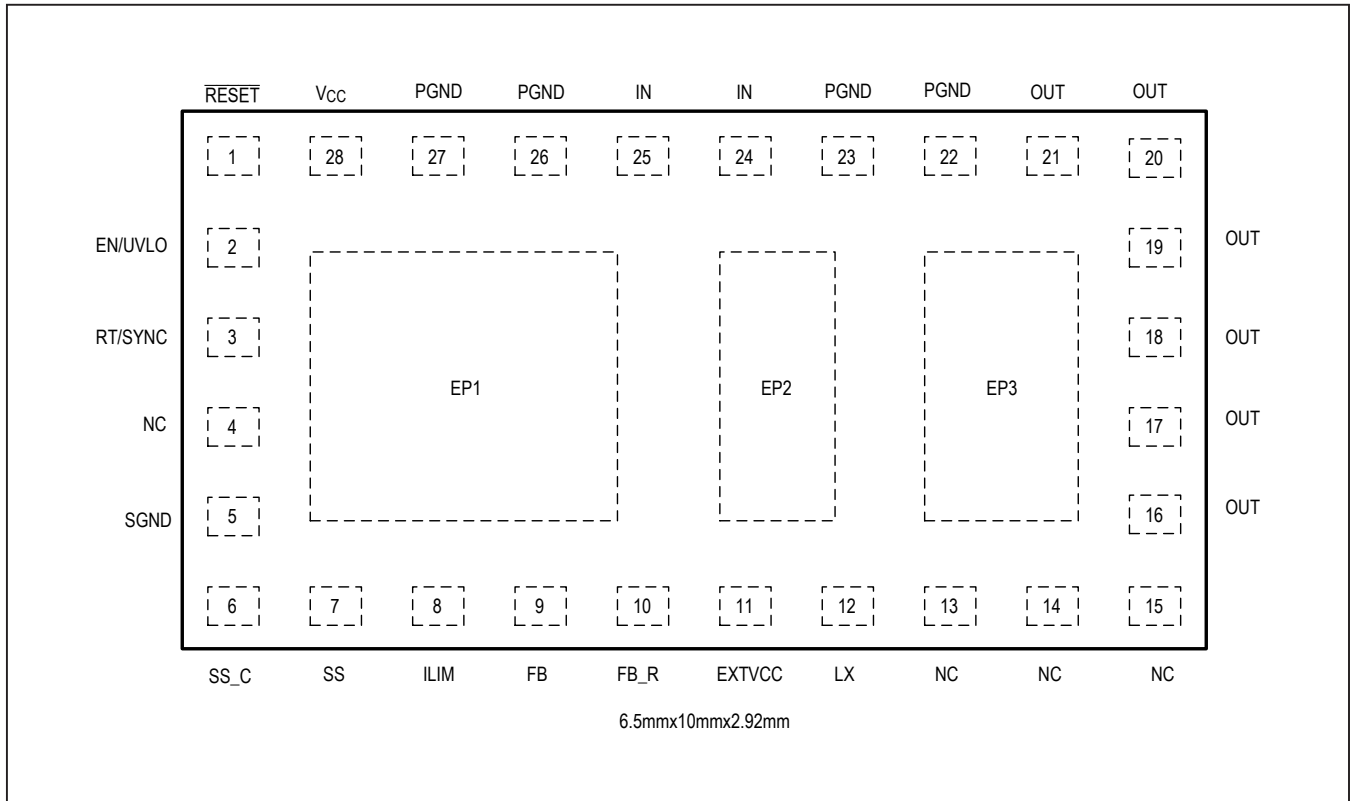


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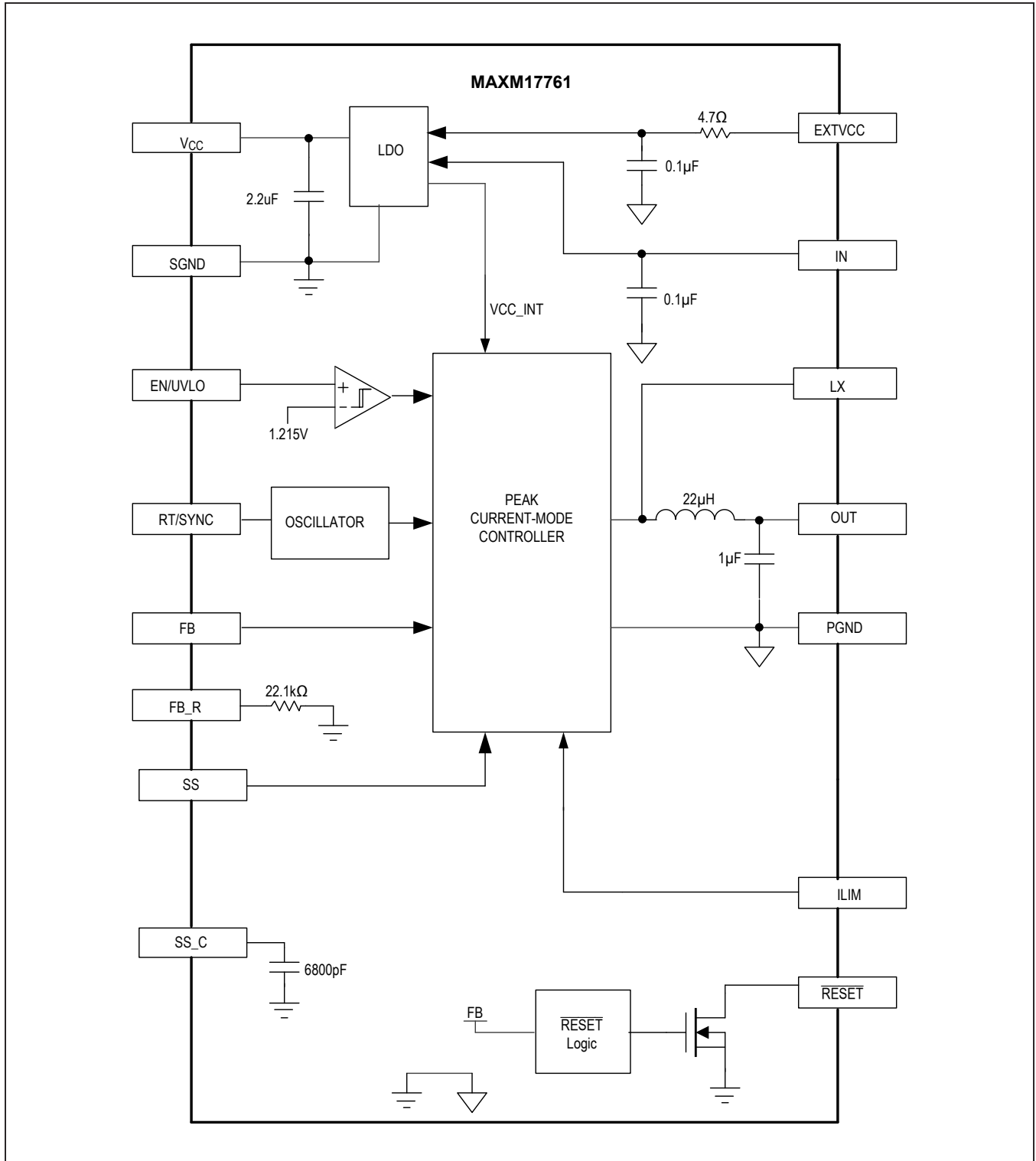
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	RESET	Open-Drain RESET Output. The RESET output is driven low if FB drops below 92% of its set value. RESET goes high 2.1ms after FB rises above 95% of its set value.
2	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between VIN and SGND to set the input voltage at which the part turns on. Leave the pin floating for always on operation.
3	RT/SYNC	Connect a resistor from RT to SGND to set the switching frequency of the part between 180kHz and 537kHz. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency. See the <i>External Synchronization</i> section for details.
4,13-15, EP2	NC	No Connection
5	SGND	Analog Ground Pin
6	SS_C	Soft-Start Capacitor. Internally, a 6800pF is connected from SS_C to SGND. Connect this pin to SS to use the internal cap for the soft-start function.
7	SS	Soft-Start Input. This module has one internal 6800pF capacitor from the SS_C pin to SGND, which programs a default soft-start time of 1ms when the SS pin is connected to SS_C. If soft-start time needs to be increased, connect an external capacitor from the SS pin to SGND.
8	ILIM	Connect a 243kΩ resistor from ILIM to SGND.
9	FB	Feedback Input. Internally, a 22.1k is connected between FB_R and SGND. Connect FB pin to FB_R to use the default internal component as a bottom resistor of the feedback resistive divider network. To set the programmable output, connect a resistor from OUT pin to FB.
10	FB_R	Feedback Resistive Node. Internally, a 22.1k is connected between FB_R and SGND. Connect this pin to FB to use the resistor as a default bottom resistor in the feedback resistive network.
11	EXTVCC	External Input for Powering Control Circuitry From the Output Side. Applying a voltage between 4.84V and 24V at the EXTVCC pin will bypass the internal LDO and improve efficiency.
12	LX	Switching Node. Do not connect external components to LX pin.
16-21	OUT	Regulator Output. Connect a capacitor from OUT to PGND. See <i>PCB Layout Guidelines</i> for more connection details.
22,23,26,27	PGND	Power Ground. Connect the PGND pins externally to the power ground plane
24,25	IN	Power-Supply Input. Connect the VIN pins together. Decouple to PGND with a capacitor, place the capacitor close to the VIN and PGND pins.
28	VCC	5V LDO Output. The VCC is bypassed to PGND internally through a 2.2μF capacitor. Do not connect external components to VCC pin
EP1	SGND	Exposed Pad. Connect to the SGND of the Module. Connect a large copper plane below the module to improve the heat dissipation capability.
EP3	OUT	Exposed Pad. Connect to the OUT pins of the Module. Connect a large copper plane below the module to improve the heat dissipation capability.

Functional Block Diagram



Detailed Description

The MAXM17761 is a high-efficiency, high voltage step-down power module with dual integrated MOSFETs that operate over a 4.5V to 76V input supports a programmable output voltage from 0.8V to 5V, delivering up to 1A current. The module integrates all the necessary components required for switching converter. The feedback voltage regulation accuracy meets $\pm 1.5\%$ over load, line, and temperature. The device uses a peak-current-mode control scheme. An internal transconductance error amplifier generates an error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator.

At each rising-edge of the clock, the high-side pMOSFET turns on, and remains on, until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side nMOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current limit is detected. The inductor releases the stored energy as its current ramps down, and provides current to the $R_{DS(ON)}$ pMOS/nMOS switches ensure high efficiency at full load. This device also integrates a switching frequency selector pin, current limit pin, enable/undervoltage lockout (EN/UVLO) pin, programmable soft-start pin, and open-drain RESET signal.

Mode of Operation

The MAXM17761 operates in PWM Mode. In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to variable switching frequency.

Switching Frequency Selection and External Frequency Synchronization

The RT/SYNC pin programs the switching frequency of the converter. Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part at any one of four discrete frequencies—180kHz, 271kHz, 360kHz, and 537kHz. [Table 1](#) provides resistor values.

The device can be synchronized by an external clock signal on the RT/SYNC pin. The external clock should

be coupled to the RT/SYNC pin through a 47pF capacitor, as shown in [Figure 1](#). The external synchronization clock frequency must be between $1.15 \times f_{SW}$ and $1.4 \times f_{SW}$, where f_{SW} is the frequency programmed by the RT resistor. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to external clock frequency from original frequency base on RT settings. The minimum external clock pulse-width low should be greater than 40ns. See the Oscillator section of the [Electrical Characteristics](#) table for details. Connect the SYNC pin to SGND if it is not used.

Linear Regulator

The MAXM17761 has two internal LDO (Low Dropout) regulators which powers V_{CC} . One LDO is powered from VIN (INLDO) and the other LDO is powered from EXT VCC (EXTVCC LDO). During power-up, when Enable pin voltage is above the true shutdown voltage, then the V_{CC} is powered from INLDO. When V_{CC} voltage is above the V_{CC} UVLO threshold and the EXT VCC voltage is greater than 4.74V(typ), then the V_{CC} is powered from EXTVCC LDO. Only one of the two LDOs is in operation at a time, depending on the voltage levels present at EXTVCC. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. EXTVCC voltage should not exceed 26V.

Table 1. Setting the Switching Frequency

SWITCHING FREQUENCY (KHZ)	RT/SYNC RESISTOR (KΩ)
180	210
271	140
360	105
537	69.8

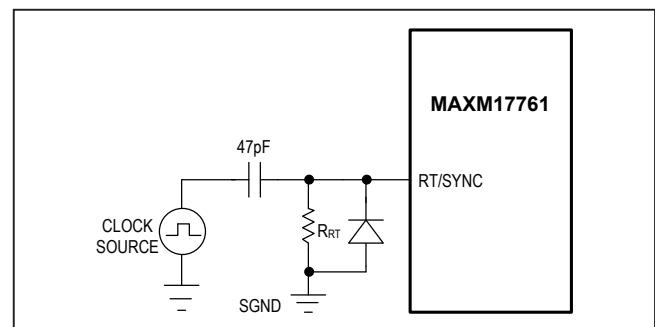


Figure 1. External Frequency Synchronization

Operating Input Voltage Range

The maximum input voltage is determined by the minimum controllable on-time, while the minimum input voltage is determined by the maximum duty cycle and the circuit-voltage drops. The minimum and maximum operating input voltages for a given output voltage should satisfy the following conditions:

$$V_{IN(MIN)} \geq \frac{V_{OUT} + (I_{OUT(MAX)} \times 0.913)}{D_{MAX}} + (I_{OUT(MAX)} \times 1.25)$$

$$\text{For Duty Cycle, } D > 0.3: V_{IN(MIN)} \geq 4.25 \times V_{OUT} - \frac{f_{SW}}{46.5}$$

$$V_{IN(MAX)} \leq \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where:

V_{OUT} = Steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

D_{MAX} = Maximum allowable duty ratio

$f_{SW(MAX)}$ = Maximum switching frequency

$t_{ON(MIN)}$ = Worst-case minimum switch on-time (115ns)

[Table 2](#) provides operating input-voltage ranges and the optimum switching frequency for different selected output voltages.

RESET Output

The device includes a $\overline{\text{RESET}}$ pin to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 2.1ms after the output voltage increases above 95% of the nominal voltage. $\overline{\text{RESET}}$ goes low when the output voltage drops to below 92% of the nominal voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Overcurrent Protection

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. When the overcurrent occurs, the module enters into hysteretic mode and limits the average output current delivered. Also, the module limits the average sink current by turning off the low-side switch in the event of negative over current.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +160°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 20°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation to avoid unwanted triggering of the thermal shutdown protection in normal operation.

Table 2. Selection Of Component Values

V_{INMIN} (V)	V_{INMAX} (V)	V_{OUT} (V)	C_{IN} (μF)	C_{OUT} (μF) (Note 2)	R_U (KΩ)	f_{SW} (KHZ)	R_T (KΩ)
4.5	36	0.8	4x2.2 100V 1206	3x100 6.3V 1210	0	180	210
4.5	40	1	4x2.2 100V 1206	2x100 6.3V 1210 +1x47 6.3V 1210	5.62	180	210
4.5	60	1.2	4x2.2 100V 1206	2x100 6.3V 1210 +1x22 6.3V 1210	11	180	210
4.5	60	1.5	3x2.2 100V 1206	2x100 6.3V 1210	19.6	180	210
4.5	76	1.8	3x2.2 100V 1206	1x100 6.3V 1210 +1x47 6.3V 1210	28	180	210
5	76	2.5	2x2.2 100V 1206	1x100 6.3V 1210 +1x22 6.3V 1210	47	271	140
6.5	76	3.3	1x2.2 100V 1206	1x100 6.3V 1210	69.8	360	105
10	76	5	1x2.2 100V 1206	1x47 10V 1210	118	537	69.8

Note: The X5R capacitors are selected as output capacitors in this table for different applications. In applications where the X7R capacitor is needed, follow the procedure given in the [Output Capacitor Selection](#) section to select the suitable capacitor.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) for a single output is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT}$), so $I_{RMS(MAX)} = I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long term reliability. Use low-ESR ceramic capacitors with high ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where $D = V_{OUT}/V_{IN}$ is the duty ratio of the controller, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency. In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Output Capacitor Selection

Ceramic output capacitors are preferred due to their stability over temperature in industrial applications. In [Table 2](#), the output capacitor is sized to support a step load of 25%

of the maximum output current in the application, such that the output-voltage deviation is contained to 3% of the output voltage. The minimum value of output capacitance required can be calculated using the following equations:

$$C_{OUT} = \frac{200}{V_{OUT}} \mu\text{F}; \text{ if } f_{SW} = 180\text{kHz}$$

and

$$C_{OUT} = \frac{150}{V_{OUT}} \mu\text{F}; \text{ if } f_{SW} \text{ is other than } 180\text{kHz}$$

Derating of ceramic capacitors with DC voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

Soft-Start Capacitor Selection

The device implements an adjustable soft-start operation to reduce inrush current during startup. Internally, a 6800pF is connected from SS_C to SGND. Connect this pin to SS to use the internal capacitor for the soft-start programming. An additional (C_{SS}) connected from the SS pin to SGND can be used to program the different soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum value of C_{SS} , as shown by the following equation.

$$C_{SS} \geq 30 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation.

$$t_{SS} = \frac{C_{SS}}{6.25 \times 10^{-6}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to SGND.

Input Undervoltage-Lockout Level

Drive EN/UVLO high to enable the output. Leave the pin floating for always on operation. Set the voltage at which the converter turns on with a resistive voltage-divider connected from V_{IN} to SGND (see [Figure 2](#)). Connect the center node of the divider to EN/UVLO pin.

Choose R1 as follows:

$$R1 \leq (110000 \times V_{INU})$$

where V_{INU} is the is the input voltage at which the MAXM17761 is required to turn on and R1 is in Ω . Calculate the value of R2 as follows:

$$R2 = \frac{1.215 \times R1}{(V_{INU} - 1.215 + (2.5\mu A \times R1))}$$

Setting the Output Voltage

The MAXM17761 supports a programmable output voltage from 0.8V to 5V.

Internally, a 22.1k Ω resistor is connected between FB_R pin to SGND of the module. Short the FB_R and FB pins of the module, to use this resistor as the bottom resistor of the feedback divider network. In this case, the top resistor (R_U) connected between OUT and the FB pin, as shown [Figure 3](#), can be calculated using the below equation,

$$R_U = \frac{22.1 \times (V_{OUT} - 0.8)}{0.8}$$

Where, V_{OUT} is the desired output voltage in Volts and the R_U is the top resistor of the feedback divider in k Ω .

The two resistors of the feedback divider network can be selected and placed external to the module as well. In this case, leave the FB_R pin unconnected. Use the following equations to select the R_U and R_B resistors of the [Figure 4](#).

$$R_U = \frac{15 \times V_{OUT}}{0.8}; R_B = \frac{0.8 \times R_U}{(V_{OUT} - 0.8)}$$

Where, V_{OUT} is the desired output voltage in Volts, R_U and R_B are the feedback divider resistors in k Ω .

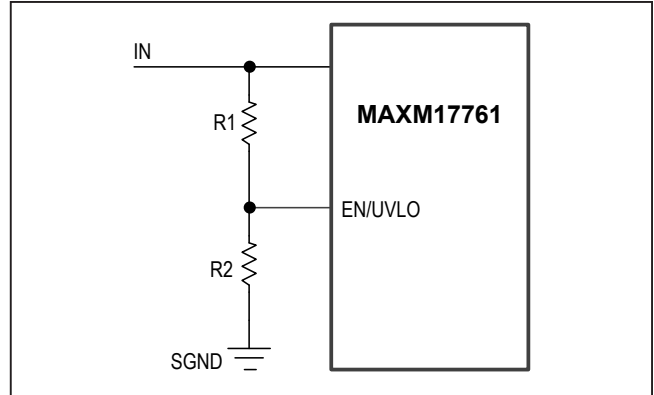


Figure 2. Setting the Undervoltage Lockout Level

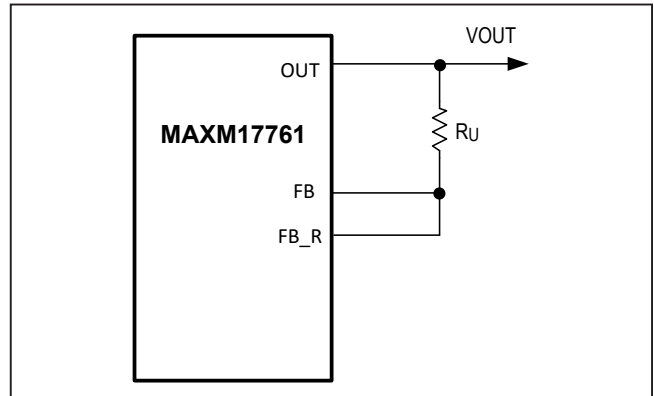


Figure 3. Setting the Output Voltage with One External Feedback Resistor

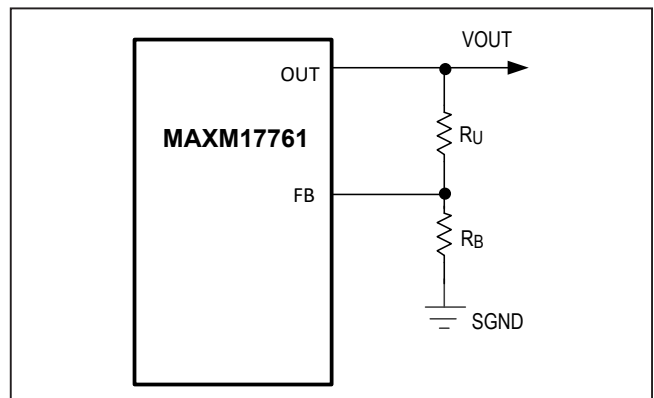


Figure 4. Setting the Output Voltage with External Feedback Resistors

Power Dissipation and Output-Current Derating

The MAXM17761 output current needs to be derated if the device needs to be operated in a high ambient-temperature environment. The amount of current-derating depends upon the input voltage, output voltage, and ambient temperature. The derating curves in TOC 41 from the *Typical Operating Characteristics* section can be used as guidelines for different output voltages generated from 24V input. The curves are based on the actual power loss measurements on bench to limit the maximum junction temperature (T_{JMAX}) to +125°C. The maximum allowable power losses can be calculated using the following equation:

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

where:

P_{DMAX} is the maximum allowed power losses with maximum allowed junction temperature. T_{JMAX} is the maximum allowed junction temperature. T_A is operating ambient temperature. θ_{JA} is the junction to ambient thermal resistance.

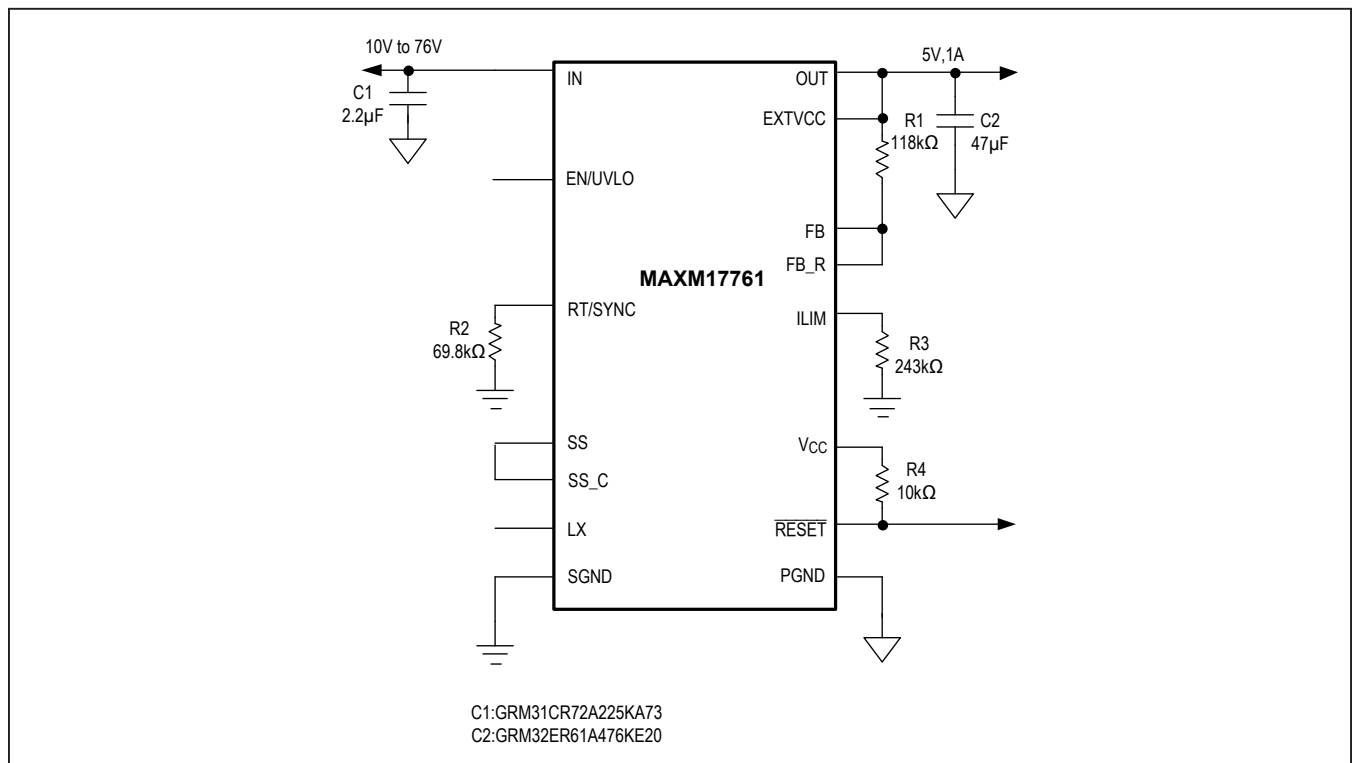
PCB Layout Guidelines

Careful PCB layout is critical to achieve clean, stable operation and to minimize EMI.

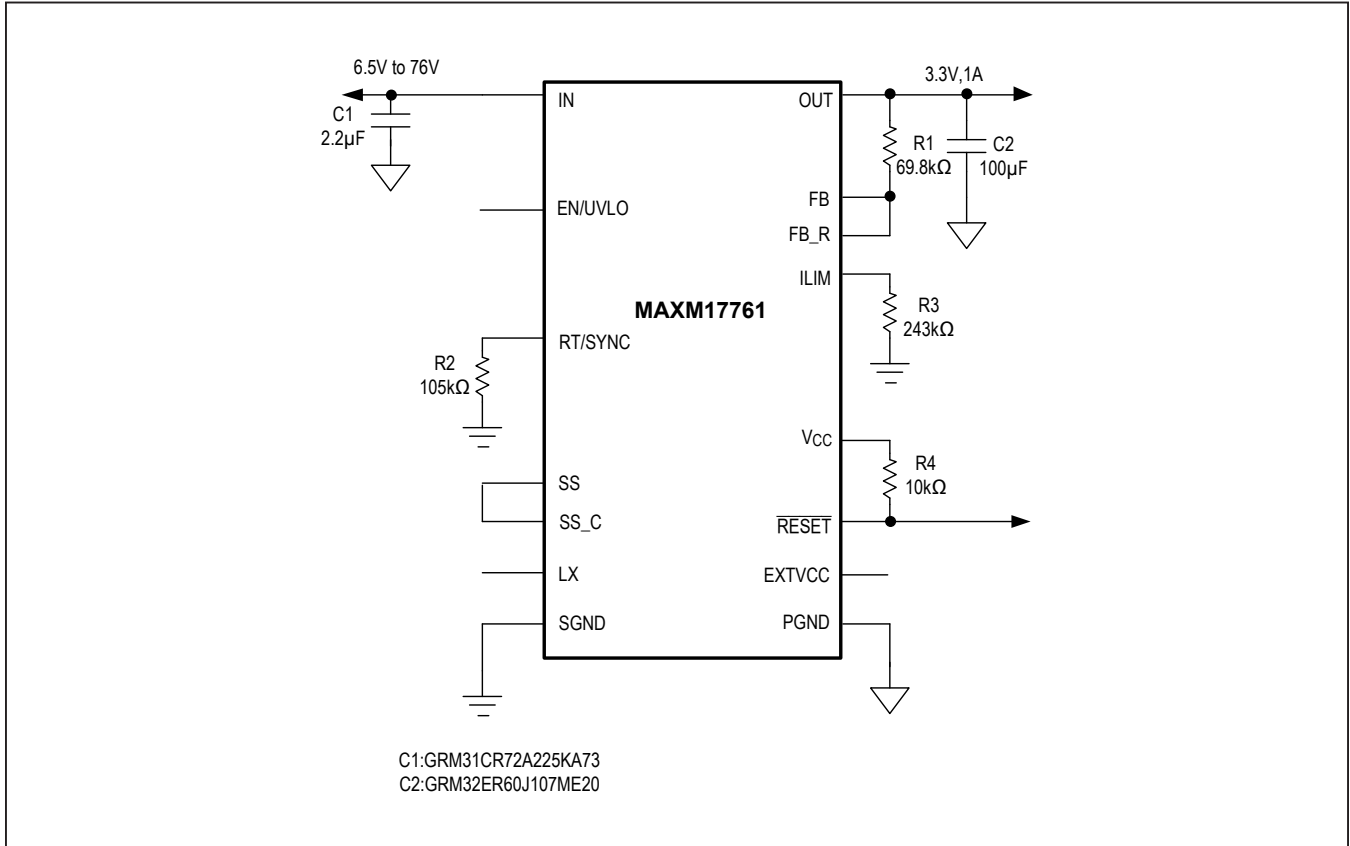
Use the following guidelines for good PCB layout. Refer to the MAXM17761 EV kit data sheet for a good sample layout.

- Keep the input capacitors as close as possible to the IN and PGND pins.
- Keep the output capacitors as close as possible to the OUT and PGND pins.
- Keep the feedback resistors as close as possible to the FB pin.
- Connect all of the PGND connections to as large as copper plane area as possible on the bottom layer.
- Connect EP1 to SGND plane on bottom layer.
- Do not keep any solder mask on EP1 and EP3 on bottom layer. Keeping solder mask on exposed pads decreases the heat dissipating capability.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency.

5.0V Output Typical Application Circuit



3.3V Output Typical Application Circuit



Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAXM17761ALI#	-40°C to +125°C	28-pin SiP 6.5mm × 10mm × 2.92mm

#Denotes a RoHS-compliant device that may include lead(Pb) that is exempt under the RoHS requirements.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	9/17	Updated <i>Package Information</i> table, <i>Typical Operating Characteristics</i> global characteristics, and TOC 08-11 and TOC 24. Merged and updated <i>Switching Frequency Selection</i> and <i>External Frequency Synchronization</i> sections, and added captions to Figures 1, 3 and 4, and updated the caption for Figure 2. Updated the <i>Power Dissipation</i> and <i>Output-Current Derating</i> TOC reference to TOC 41, and updated the part number in the <i>Ordering Information</i> table. Replaced the <i>Output Capacitor Selection</i> and <i>Operating Input-Voltage Range</i> sections.	2, 5–10, 14–19

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